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Multilevel In-Memory-Searching in 3D NAND-Flash Memory

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Abstract

We propose a novel method of multilevel in-memory-searching (IMS) using 3D NAND-flash memory. The approach provides ultra-high parallel searching capability with the database stored in high-density 3D NAND-flash IMS chip(s), with the power similar to a typical NAND flash read operation. Fail bit issues caused from retention loss, program/read disturbance are evaluated and solutions are provided. An example on applying the MLC NAND-IMS accelerator in deoxyribonucleic acid (DNA) read mapping is described. The multilevel IMS is promising for data-intensive applications including big data searching and future memory-centric computing systems.

Introduction

As the to-be-process data size increases, transferring data between the processor (CPU/GPU) and the memory (DRAM) becomes a bottleneck for the system performance [1]. Non- von Neumann based computing architectures thus provide new directions to alter the situation. In addition to the discussed in-memory-computing (IMC) architectures [1], in-memory-searching (IMS) is another topic that especially good for matching/allocating a target within the memory that stores the database. The NAND-flash-based IMS system [2] can provide tera-bit-level nonvolatile memory to store the database, and the search operations can be executed with ultra-high parallelism. We proposed a novel encoding methodology to enable multilevel IMS system based on the mature multi-bit-per-cell 3D-NAND technologies. This novel multilevel IMS system is a good candidate for read-intensive database-oriented applications.

Multilevel IMS Cell Design and Operations

A 48-layer 3D-NAND flash charge-trapping memory chip is used in the demonstration for the multilevel in-memory-search (IMS) system, where the IMS unit cell is composed of two serially-connected flash memory cells (**Figure 1)**. The "search" function is carried out by comparing the search target (search bit) to the stored data (IMS bit) through the to-be-discussed encoding scheme, and the conduction current can flow through the IMS bit only when both flash cells are turned on. **Figure 2** shows the example for the setup on a MLC (4-level VT) flash chip. The two-bit data can be stored in one IMS unit cell by assigning the Vt combination of the two memory cells. The search target is encoded into the word-line (WL) biases and applied to the gates of the two memory cells. The "Don't Care" data bit (Data XX), "Invalid" data bit (Data --), and the "Wildcard" search bit (Search XX) are also provided in the encoding scheme to provide flexibility in the IMS system (**Figure 2(b)**). **Figure 3** shows the extended table describing all matching combinations of the MLC-NAND IMS bit. The encoding scheme can be generalized and applied to higher-multilevel IMS systems, such as TLC IMS, QLC IMS, or even a general case for n-level IMS, with the same two-memory-cell structure (**Figure 4**). The general rule is that, as the multilevel IMS bit value increases, the first flash memory cell stores the data from low VT to high VT, and the second cell stores the data from high VT to low VT. Similarly, the search bit is encoded by biasing the first WL from low bias to high bias, and the second WL from high bias to low bias. Multiple IMS cells can be connected in series to form an IMS word, and be stored in a NAND string (**Figure 5(a)**) to perform the wired-AND function. The sense amplifier can detect the string current only when the content of the search word matches with the IMS word in the NAND string. The NAND flash array can store multiple IMS words (each in its NAND string) (**Figure 5(a)**), which can then be searched *in parallel* with only one search operation. **Figure 5(b)** shows the multilevel IMS system can accommodate long search word without the otherwise time-consuming search word partitioning process [2], thus significantly improve the searching speed.

Reliability Concerns and Solutions

VT distribution overlap will be the major reliability concern for the multilevel IMS system. **Figure 6** shows the TLC VT distribution after programming. VT of a memory cell may cross the read bias boundary when it is at the distribution head or tail, and results in IMS match error. Such error will resulting in two kinds of incorrect searching results: "escape" with not-preferred string current due to decreased VT (e.g. from retention loss), or "overkill" from cutting off the string current due to increased VT (e.g. from read disturb). For the example shown in **Figure 7**, when VT decrease occurs, search "001" (VS2 and VS7 at the gate for the first and the second cell, respectively) may not only match with data "001" (at VT2 and VT7 for the first and second cell, respectively) but also data "000" (at VT1 and VT8) and data "010" (at VT3 and VT6) when the memory VT cross the search bias boundary.

To reduce the searching error problem, two approaches are proposed: (1) Adopt advanced NAND flash programming algorithm [3]. (2) Skip some VT states from the multilevel NAND flash in the encoding table. For example, use TLC NAND programming technique for MLC NAND-IMS by skipping PV1, PV2, PV4, PV6 to gain the VT window for reliability requirements (**Figure 8)**. Eliminating the use of PV1 and PV2 states in NAND-IMS can prevent "overkill" problem from the low VT cells after data retention and read disturbance. **Figure 9** shows the VT distribution of the MLC-IMS before and after baking at 125°C for 5 hours. Plenty read window between EV and PV3 allows further optimization of the VT states. Read disturb immunity was evaluated by read at VS4 (Vpass for TLC NAND) for 100M read cycles for all VT levels. No significant VT increase was found on PV3, PV5, and PV7 states. The read disturb on EV state exists but is acceptable, even after overdriving the read bias to VS4+1.2V (**Figure 10**).

Application Example on DNA matching

We propose MLC 3D-NAND IMS system (**Figure 11**) as the genome read mapping accelerator, which can execute the seed-and-vote algorithm [4] to find the location of the extracted "reads" in the reference genome. The base encoding scheme transfers the nitrogenous base of the DNA (A, T, C, G) into digital forms (00, 01, 10, 11) suitable to be represented by one MLC IMS bit. The reference genome is stored in the 3D NAND array with sliding reference scheme, which creates multiple copies of the reference with shifted location in consecutive WLs. The sliding reference can allow seeds (sub-reads) starting from different locations without the concern of shifted read and reduce the number of seed inputs. The long "read" could be partitioned into several seeds with the length equal to or shorter than the IMS data string. "Wildcard (XX)" can be appended to the last seed when it cannot fulfill the search word after partitioning. "Don't Care" bits can be inserted to the end of the data string if the data length is shorter than the IMS string. Additional "Invalid" bits (always "off") can be inserted to the not-in-use IMS strings to prevent faulty votes. The IMS strings in the array are grouped into different "localities" to accumulate "the votes" from matching cases. The locality receiving highest vote indicates that the group of the IMS string of that locality are most similar to the seeds from the read. In other words, the location of the read in the reference genome is found. The compression skill can be applied here. For example, multiple search words of AAA, AAC, AAG, AAT can be grouped into AAX and further reduce the searching sessions.

Conclusion

We proposed a novel encoding method for multilevel IMS system based on mature 3D-NAND flash technology. This approach enables ultra-high parallelism on data matching tasks and is suitable for database searching and big-data/AI processing.

References:

[1] H.T. Lue, et al., pp. 38.1.1-38.1.4, IEDM, Dec. 2019. [2] P. H. Tseng. et al, pp. 36.1.1-36.1.4, IEDM, Dec. 2020. [3] S. Lee. et al, pp. 340-341, ISSCC, Feb.2018. [4] S. Liu. Et al, BMC Bioinformatics **17,** 466 (2016).

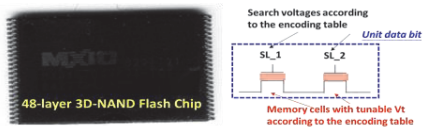


Fig.1. The 48-layer multilevel 3D-NAND flash chip for in-memory-search (IMS) system demonstration. The IMS unit bit is composed of two flash cells with tunable VT.

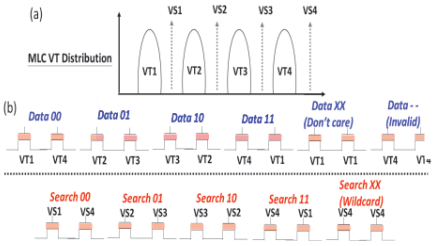


Fig.2. (a) Schematic MLC Vt distributions. (b) One IMS data bit is stored in two flash cells with different VT combinations. Search bit input from word line with different bias combinations.

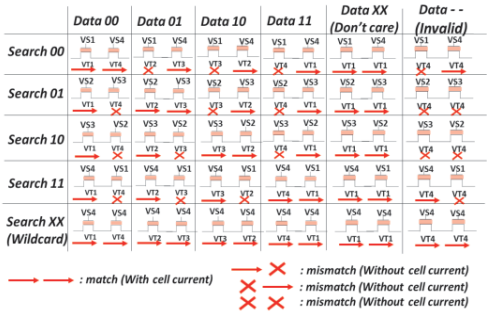


Fig.3. Operations in the multilevel IMS unit cell. The cell current pass through both flash cells only among the cases of Search00–Data00, Search01-Data01, Search10-Data10, Search11-Data11, Search "XX", and Data "XX". The Data "--" (Invalid) disabled the conduction current except for the case with Search "XX".

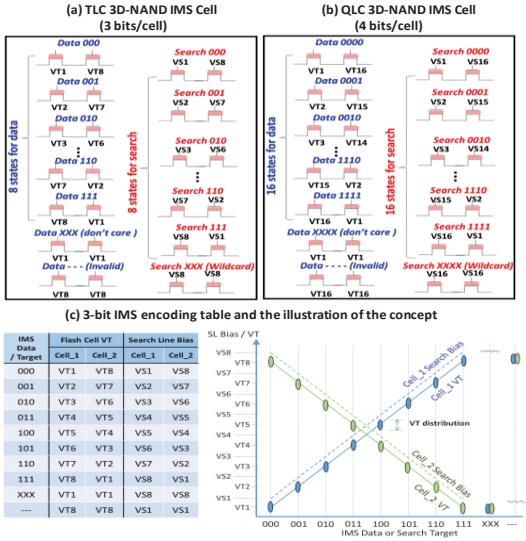


Fig.4. (a) TLC IMS cell. (b) QLC IMS cell. (c) The table and the illustration of the encoding scheme. The oval indicates the VT distribution for that state in the array. The sensing current can flow through the IMS unit cell only when the Data and the Search Target match each other, that is, for both Cell_1 and Cell_2 the search biases (VS) are higher than the stored levels (VT). The approach can be extended to an n-bit system.

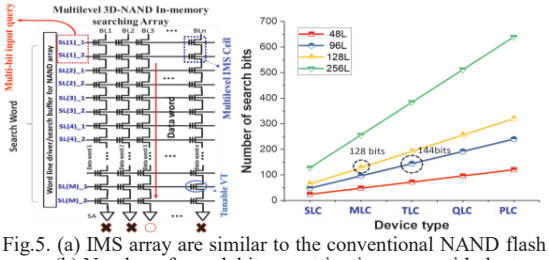


Fig.5. (a) IMS array are similar to the conventional NAND flash array. (b) Number of search bits per string increases with the type of the multilevel device and the layer number in 3D NAND.

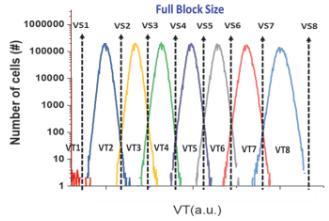


Fig.6. VT distributions for TLC 3D-NAND IMS array from one memory block. Overlaps are observed between neighboring VT states.

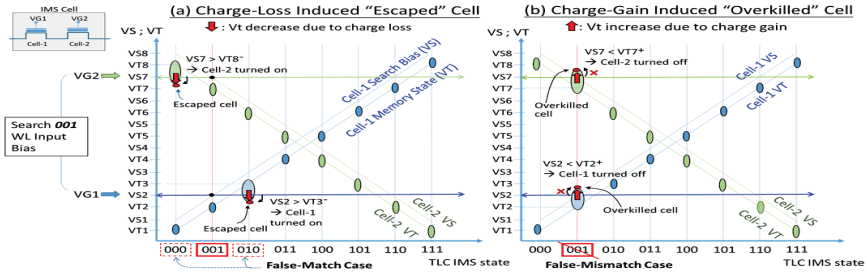


Fig.7 IMS failure modes caused by (a) charge-loss, or (b) charge-gain of the NAND flash cells.

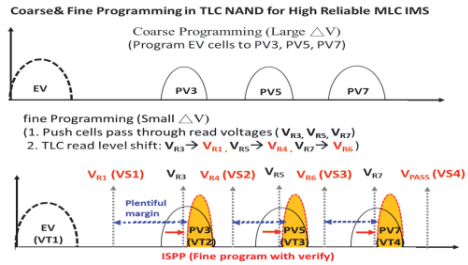


Fig.8. Applying TLC NAND programming techniques for MLC NAND-IMS. Read levels can be shifted accordingly to reserve sufficient sensing margin.

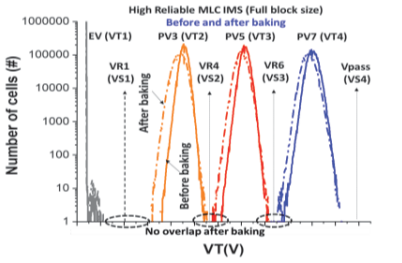


Fig.9. MLC IMS Vt distributions before and after baking. Only four states (EV, PV3, PV5, and PV7) are used, combining with optimized read level selection.

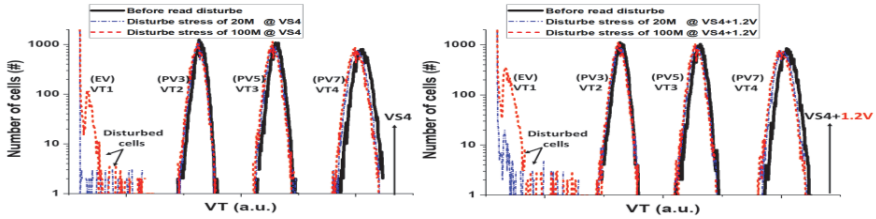
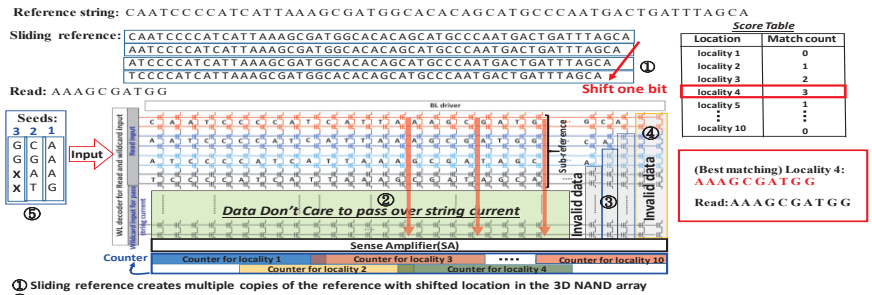


Fig.10. MLC IMS array before and after read stress with 100M read operations using the highest search voltage (VS4) and the overstress condition (VS4+1.2V). Read-intensive IMS system is demonstrated.



① Sliding reference creates multiple copies of the reference with shifted location in the 3D NAND array
② "Don't Care" can be inserted at the end of the string to pass over string current.
③ When the sub-reference length is shorter than the NAND string, "Invalid" data can be inserted at the end of the string to disable the comparison.
④ "Invalid" data can be inserted to the NAND string to prevent false "match" signal output.
⑤ When a seed is shorter than the input search word, the "wildcard (X)" should be inserted to the end of the search word.

Fig.11. Applying the Multi-level 3D-NAND IMS as the "Read mapping" accelerator in the Seed-and-Vote DNA matching tasks, with the following key steps: 1. Generate seeds (i.e. the search word) from the Read. Compress them if possible. 2. Compare the seeds to the reference genome stored in the MLC NAND-IMS system. 3. Count the votes by locality groups. 4. Report the locality with highest votes to the CPU. 5. Fine-search and pin-point the Read location in the locality by CPU/GPU.