Adder Tree / MAC

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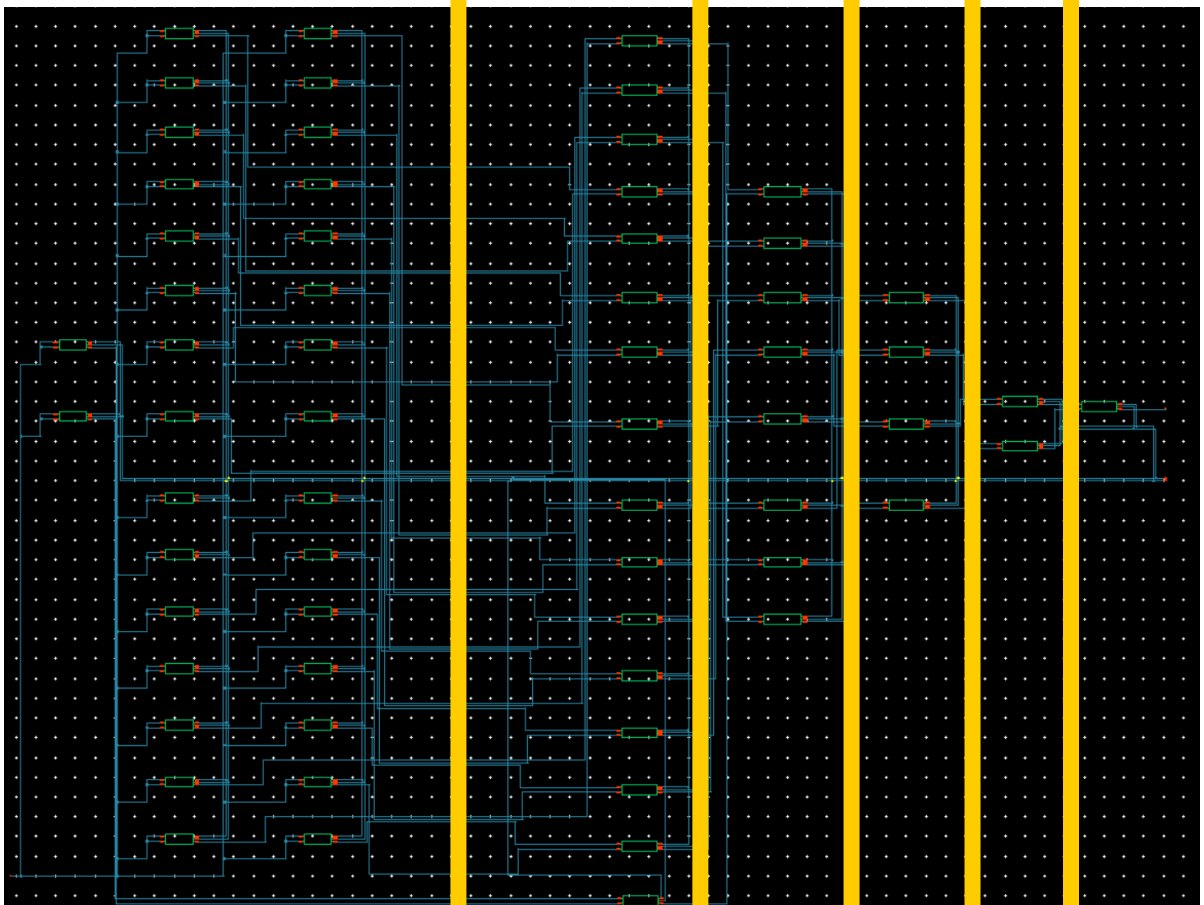
Adder Tree Implementation

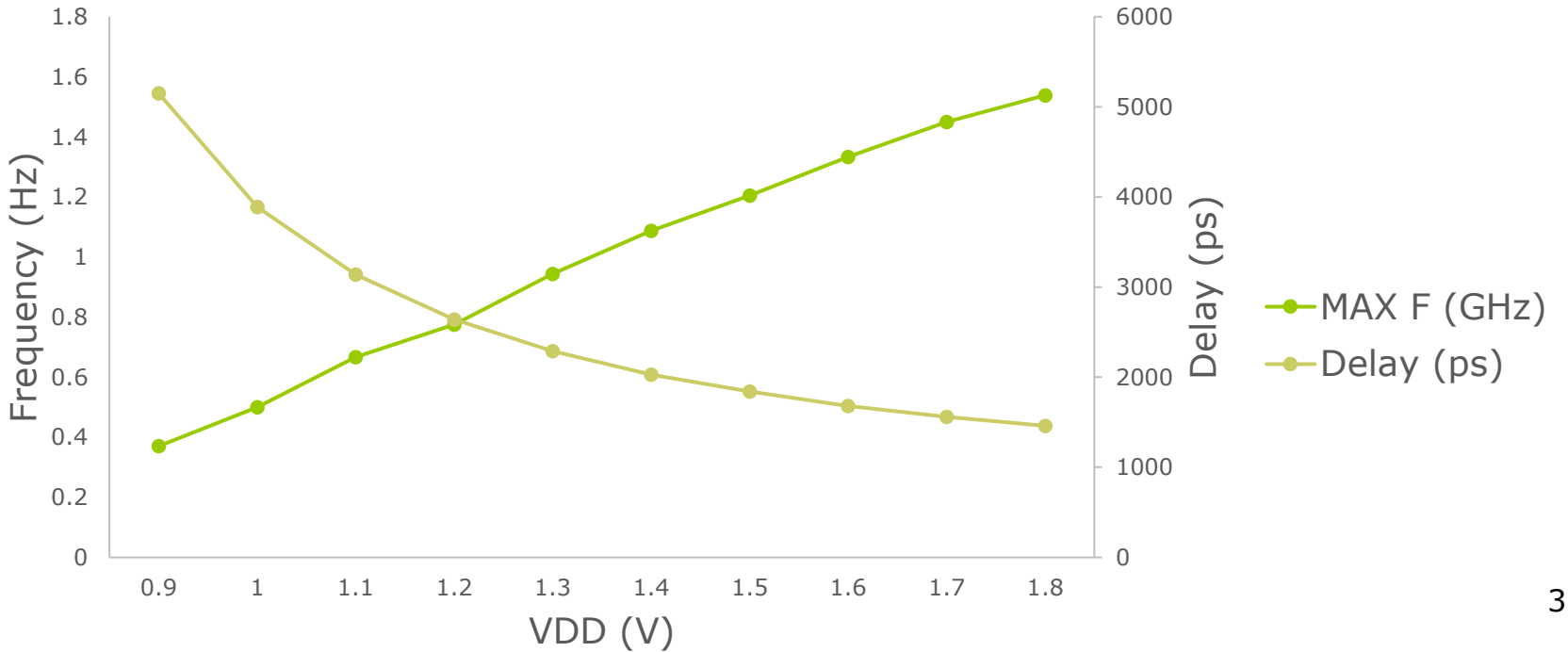
- 1st 2nd 3rd 4th 5th 6th



- 28T FA
  Wp 750n
  Wn 250n

Adder Tree Result

- Allowable clock rate grows with VDD
  - 0.37GHz at 0.9V, 1.54GHz at 1.8V
- Delay decreases with VDD growth
  - 5.15ns at 0.9V, 1.46ns at 1.8V

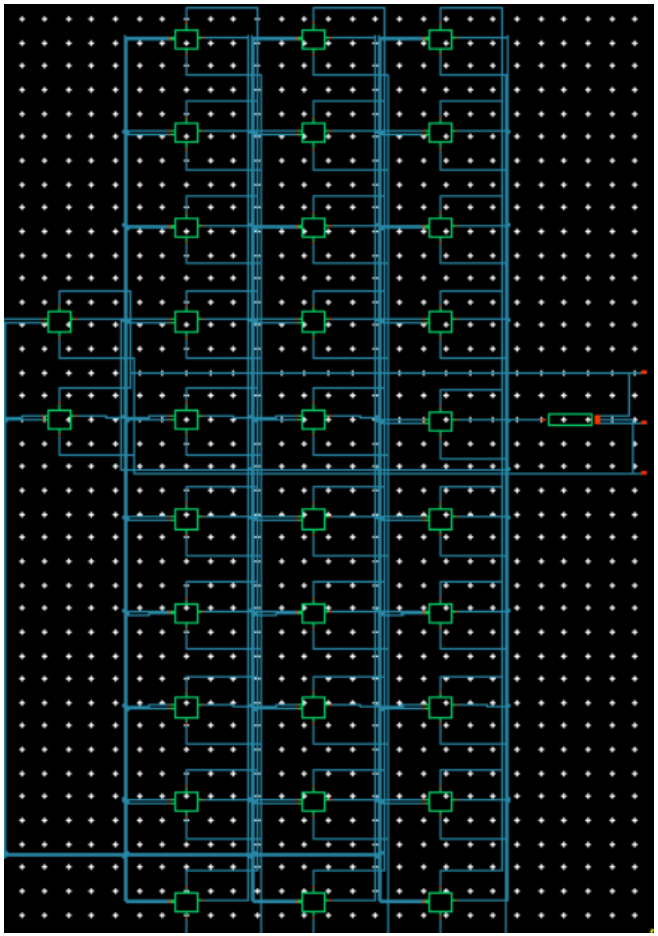


MAC Implementation

- N bit MAC has
  N AND gate and
  one adder tree

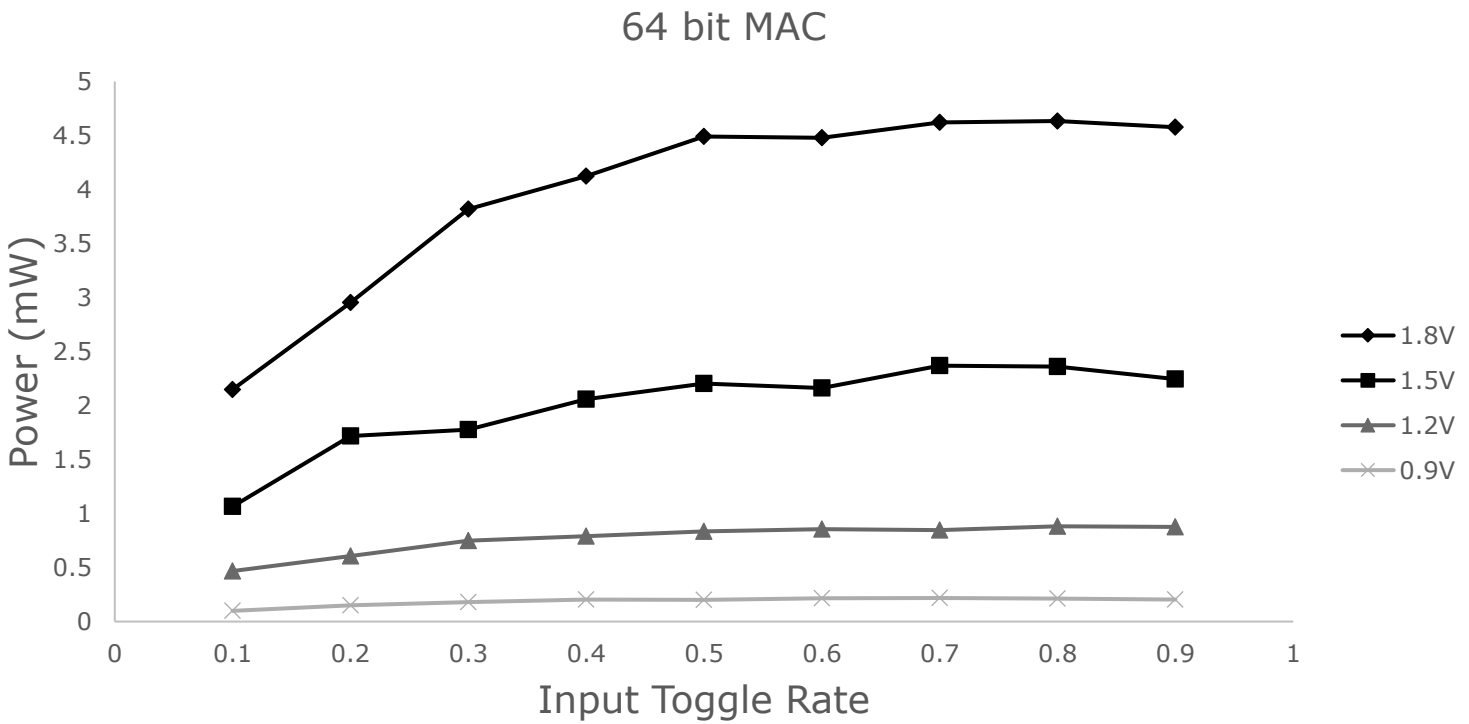
- 64 bit MAC composed of
  one 32 bit MAC ,
  two 16 bit MAC , and
  some additional FAs

32 bit MAC



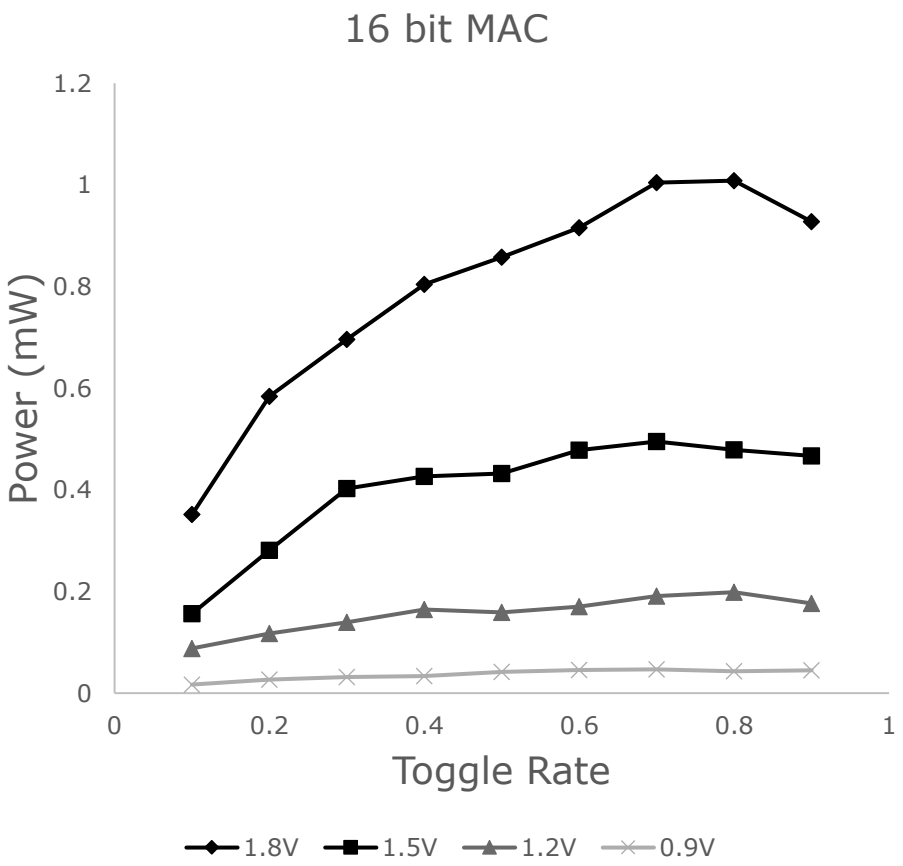
MAC Result

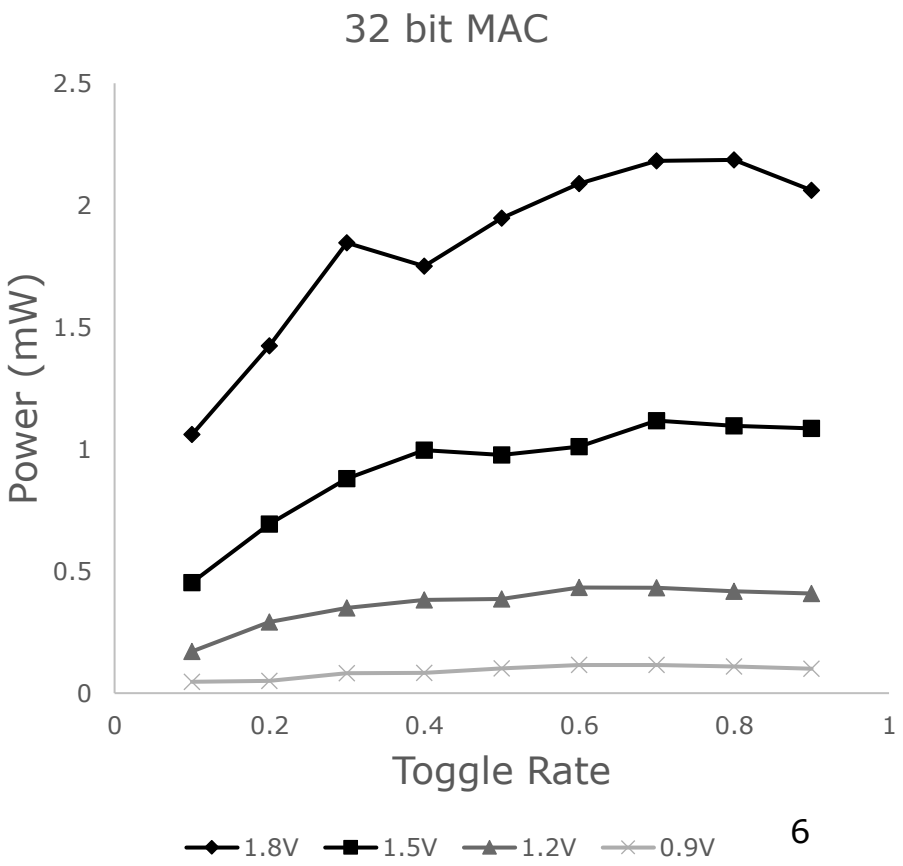
- Dynamic power grows with toggle rate
  - But decreases when toggle rate 0.8 -> 0.9
  - Due to 50% 1s and 0s in test data



MAC Result

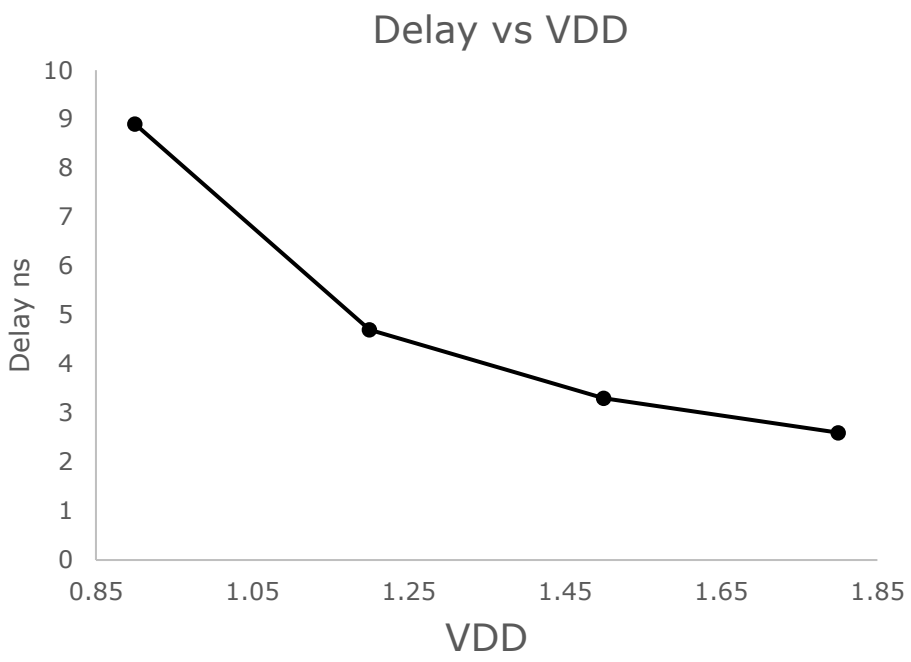
- Same situation occurs for 16 and 32 bit MAC

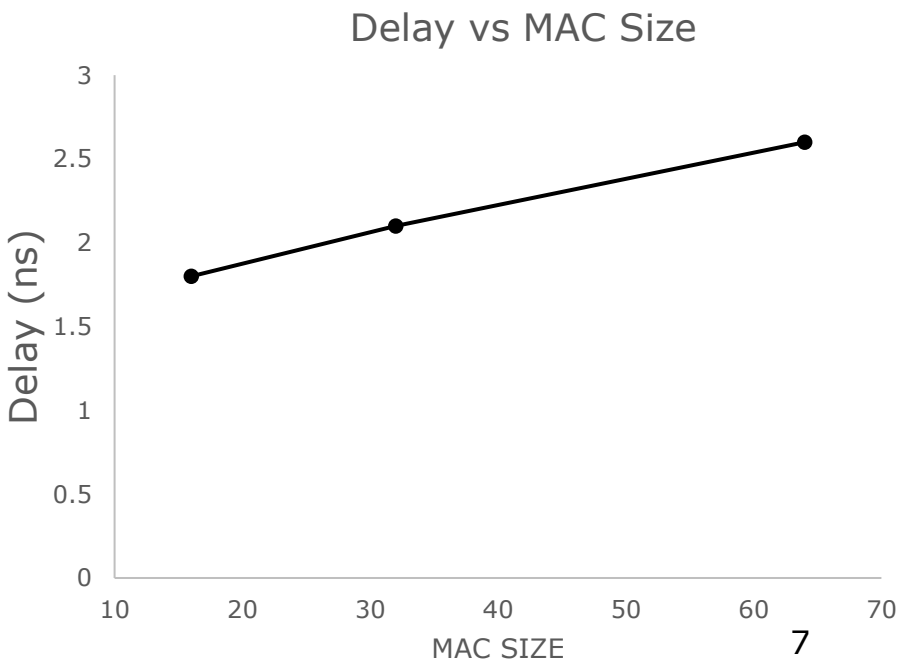




MAC Result

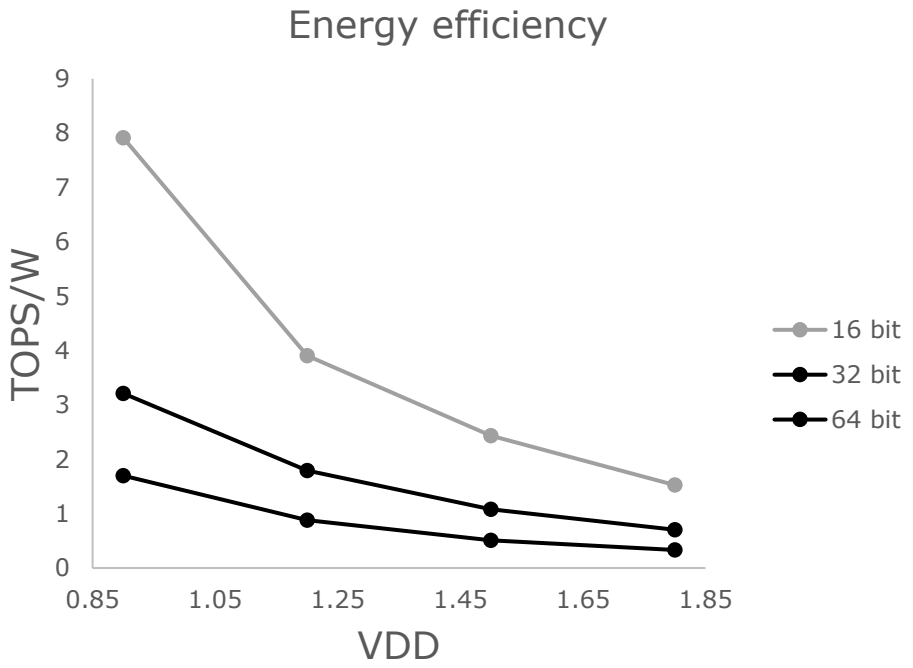
- Delay
  - 2.6 ns under 1.8 V, 8.9 ns under 0.9V supply

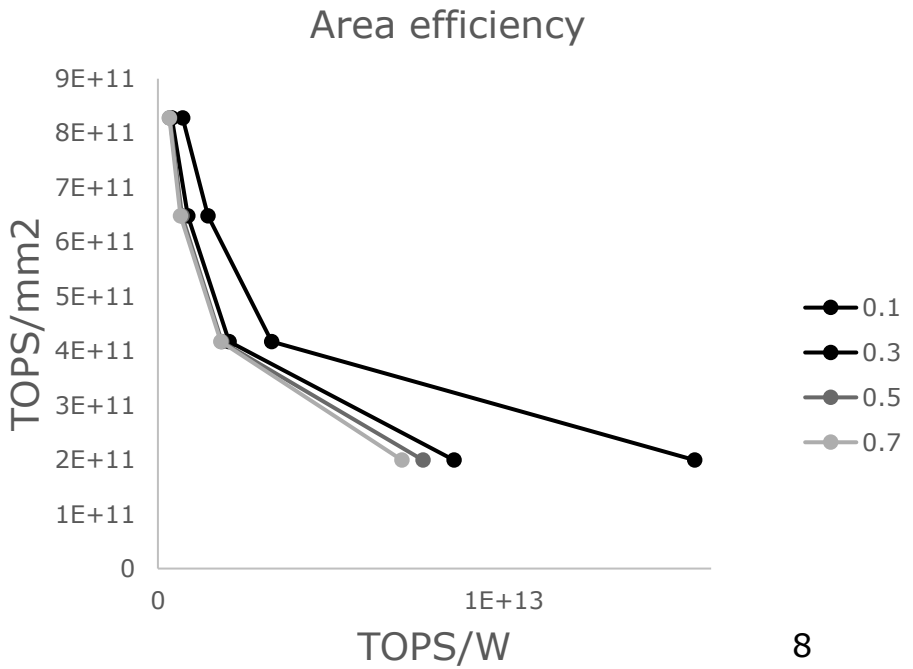




MAC Result

- Energy efficiency
  - 0.33 TOPS/W at 1.8V, 1.70 TOPS/W at 0.9V
- Area efficiency
  - 0.83 TOPS/mm2 at 1.8V, 0.20 TOPS/mm2 at 0.9V





MAC Result

- Energy efficiency
  - 4.38 TOPS/W for 16b, 0.72 TOPS/W for 64b
- Area efficiency
  - 3.76 TOPS/mm$_2$ for 16b, 0.83 TOPS/mm$_2$ for 64b