AND / FA

B11901027 王仁軒

NM with Wa Variation

☐ SNM:
   ■ Noise margin does not change with Wa

Wa = 0.36 um		Wa = 0.48 um		Wa = 0.60 um
0.794	=	0.794	=	0.794

☐ RNM:
   ■ Noise margin ↓ with Wa ↑

Wa = 0.36 um		Wa = 0.48 um		Wa = 0.60 um
0.373	>	0.291	>	0.222

☐ WNM
   ■ Noise margin ↑ with Wa ↑

Wa = 0.36 um		Wa = 0.48 um		Wa = 0.60 um
0.467	<	0.473	<	0.475

AND

□ Fastest at FF, slowest at SS

□ No Sizing -> rise time = 2x fall time

1.8V Performance

unit : ps

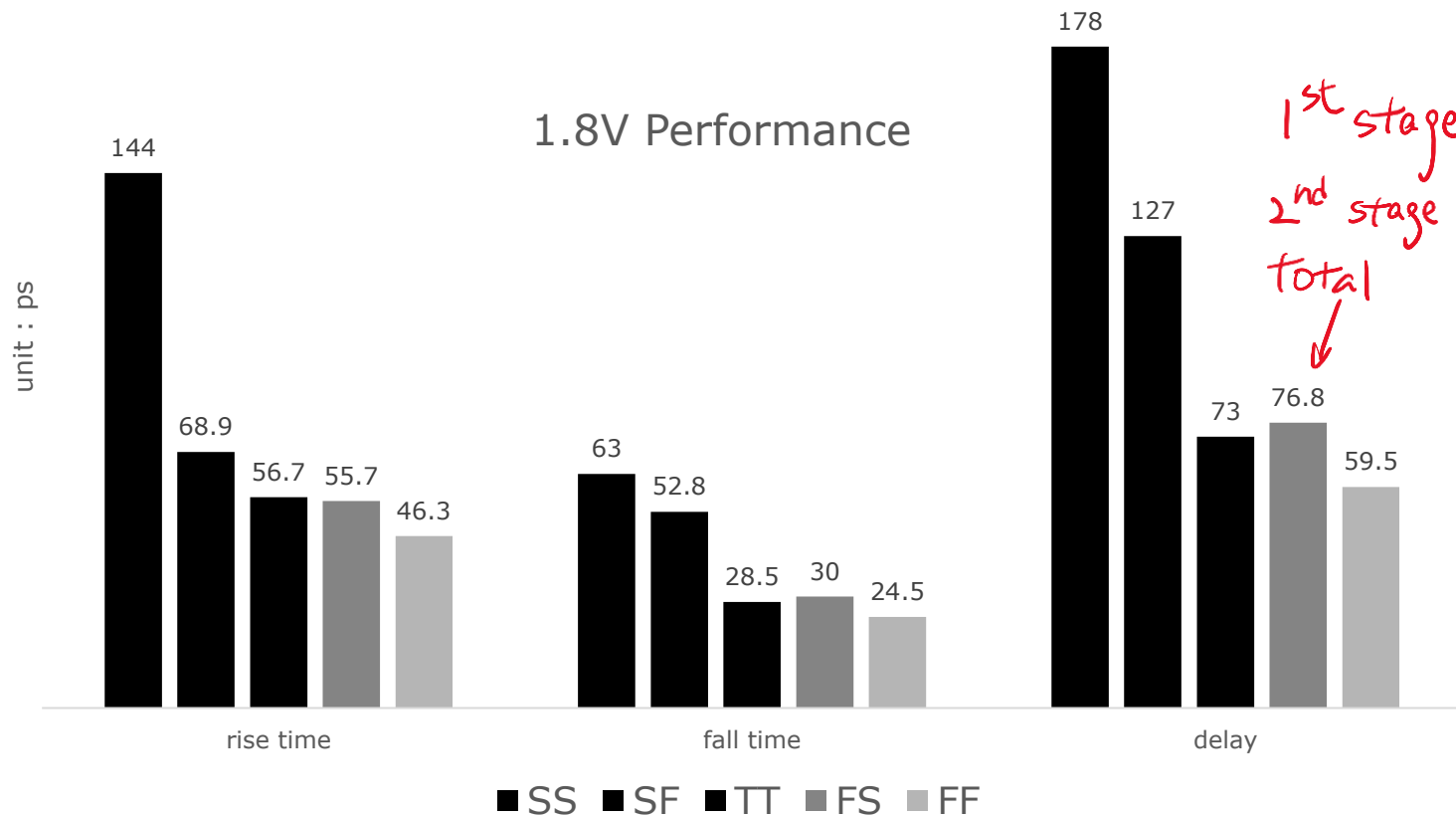|	rise time	fall time	delay
SS	144	63	178
SF	68.9	52.8	127
TT	56.7	28.5	73
FS	55.7	30	76.8
FF	46.3	24.5	59.5

■SS ■SF ■TT ■FS ■FF
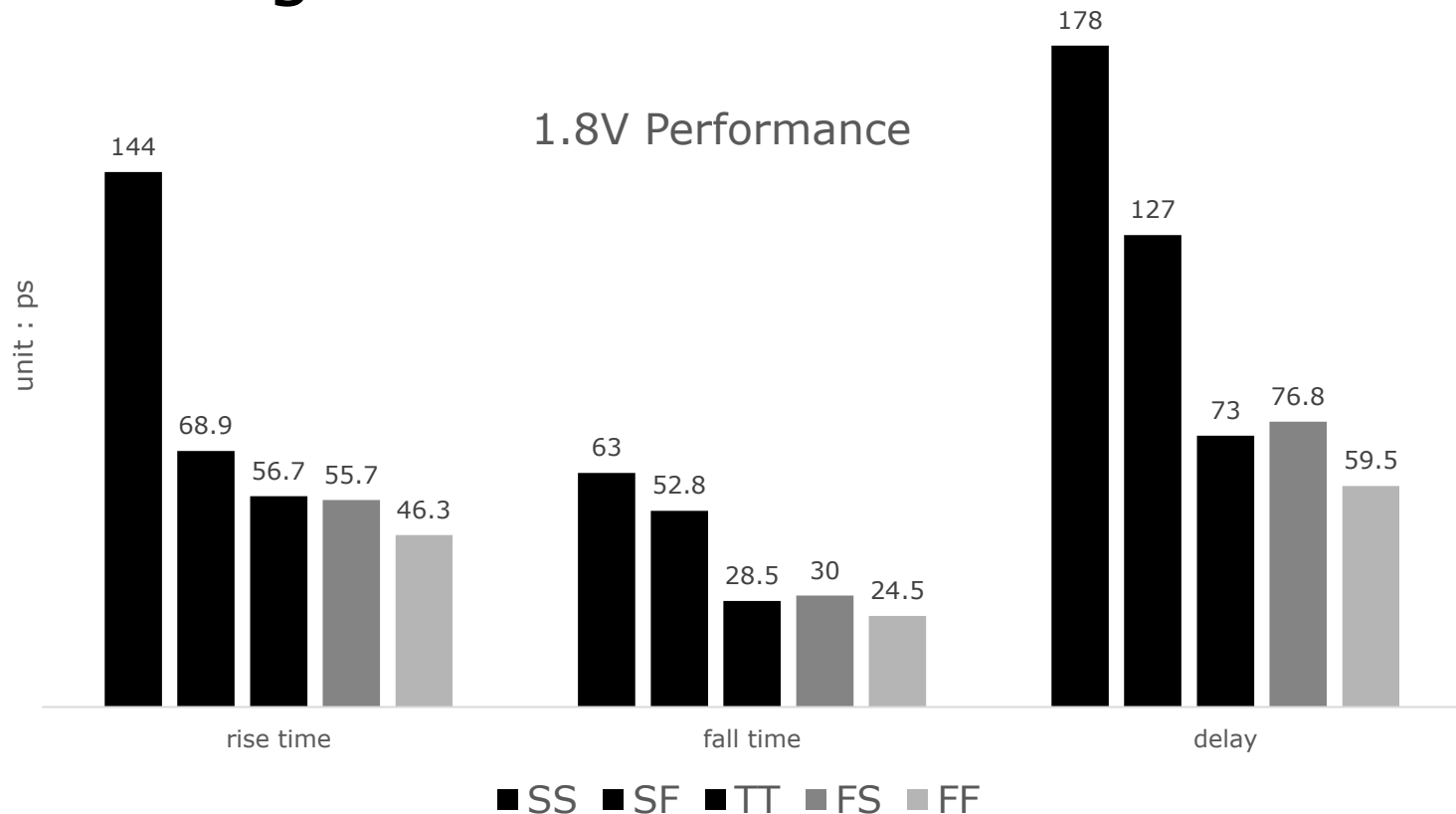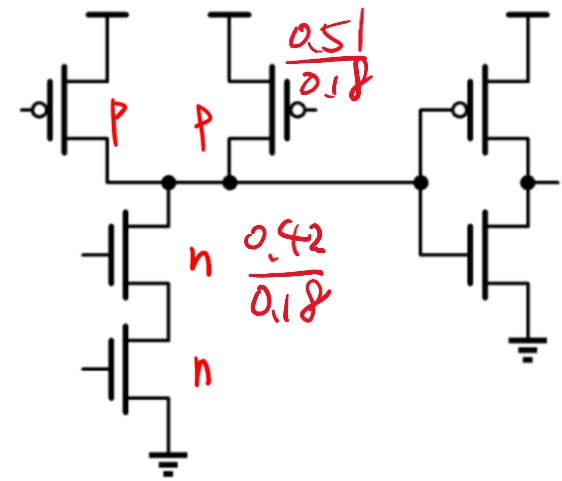
AND
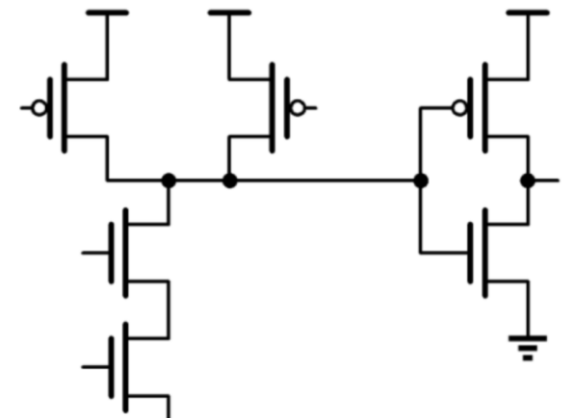
□ Delay: FS > SF

■ Unbalanced size -> maximum delay at falling

1.8V Performance

unit : ps

1st stage : faster
2nd stage : slower
total : ?

	rise time	fall time	delay
SS	144	63	178
SF	68.9	52.8	127
TT	56.7	28.5	73
FS	55.7	30	76.8
FF	46.3	24.5	59.5

■ SS ■ SF ■ TT ■ FS ■ FF

AND

□ High VDD -> Faster

Delay of VDD variation

SS: 178, 355, 785
SF: 127, 234, 482
TT: 73, 125, 220
FS: 76.8, 134, 234
FF: 59.5, 96.2, 155

■1.8V ■1.2V ■0.9V

AND (Adjust W by 40%)

☐ Adjust Wn,nand

	wn*1.4
	TT
	wn/1.4

rise time: 55.1, 56.7, 59.9
fall time: 29.7, 28.5, 27.3
delay: 64.9, 73, 84
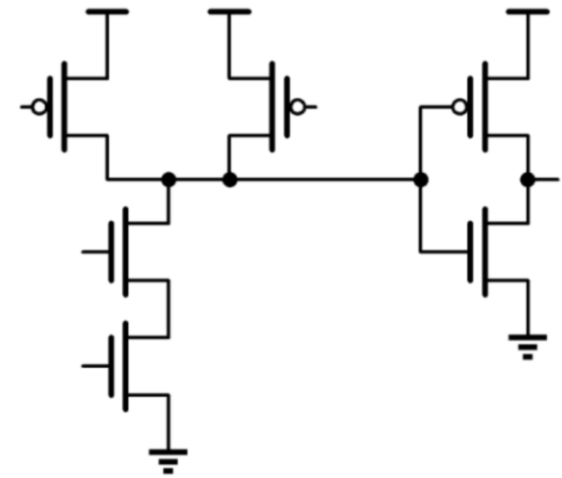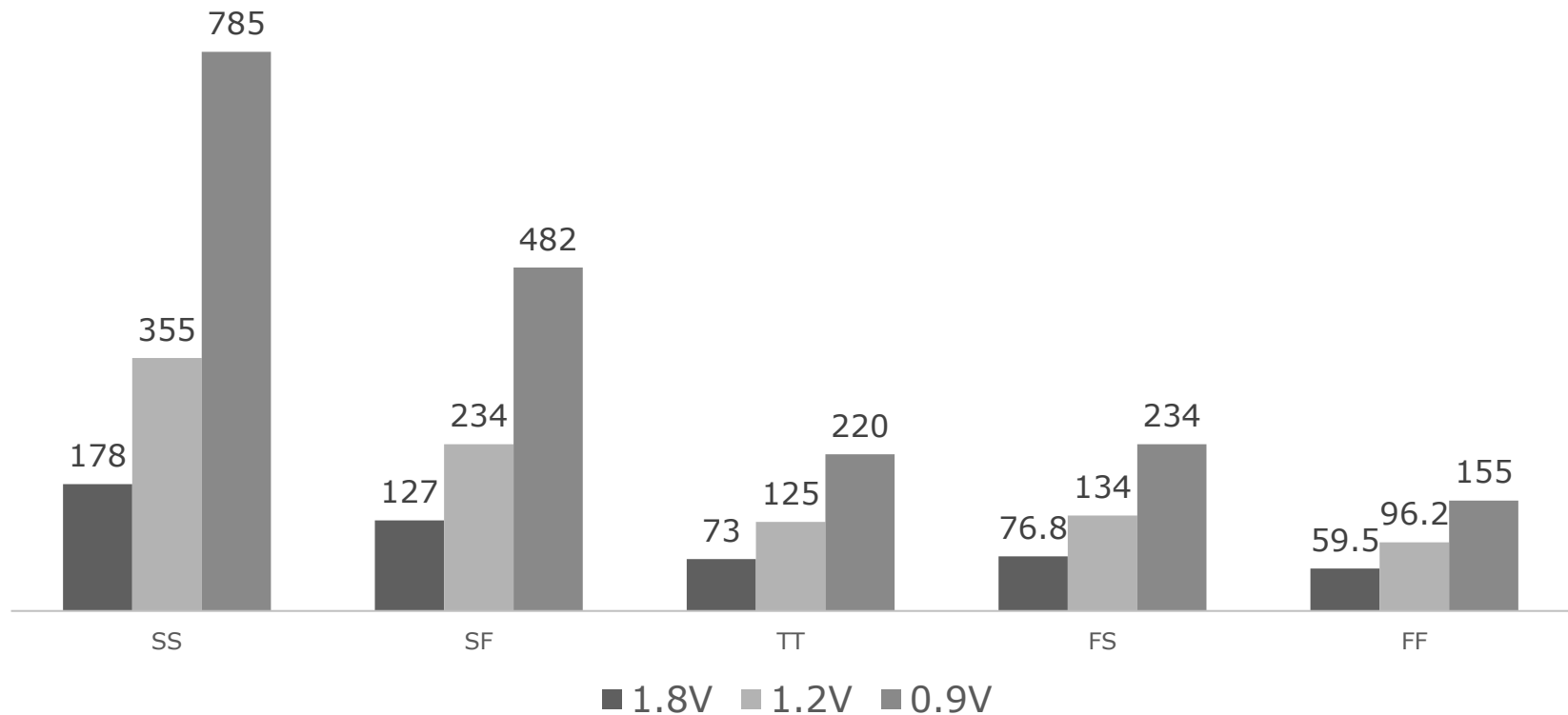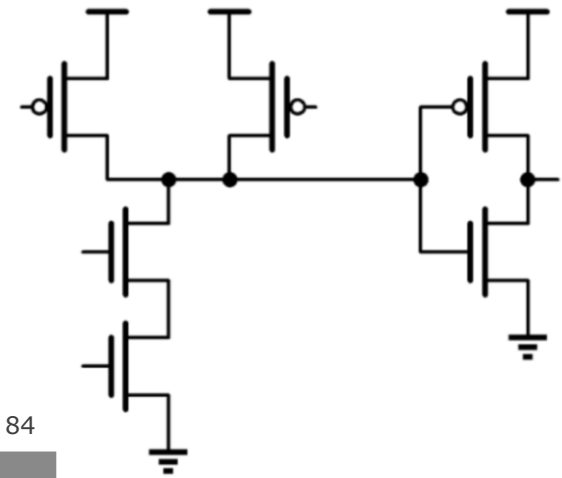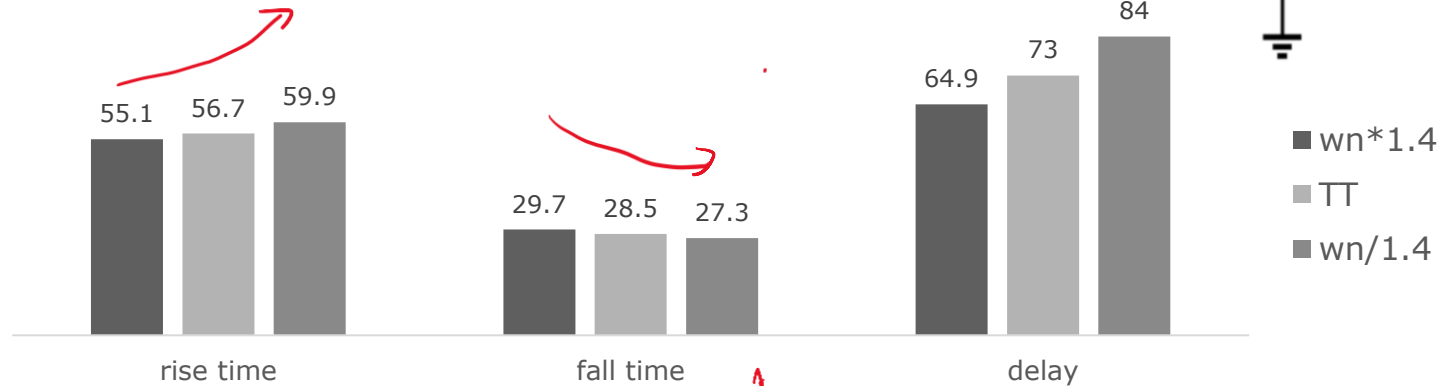
☐ Adjust Wp,nand

smaller caps

	wp*1.4
	TT
	wp/1.4

rise time: 58.9, 56.7, 57.1
fall time: 26.7, 28.5, 29.9
delay: 79, 73, 69

6

AND (Adjust W by 40%)

□ **Adjust Wn,inv**

rise time: 60.9, 56.7, 54.9
fall time: 27.2, 28.5, 32.3
delay: 79, 73, 68.7

Legend: wn*1.4, TT, wn/1.4

□ **Adjust Wp,inv**

rise time: 52.2, 56.7, 65.3
fall time: 29.8, 28.5, 27.9
delay: 70.8, 73, 77.3

Legend: wp*1.4, TT, wp/1.4
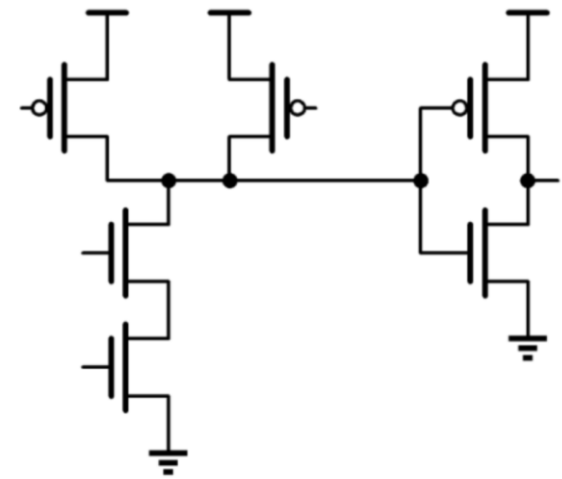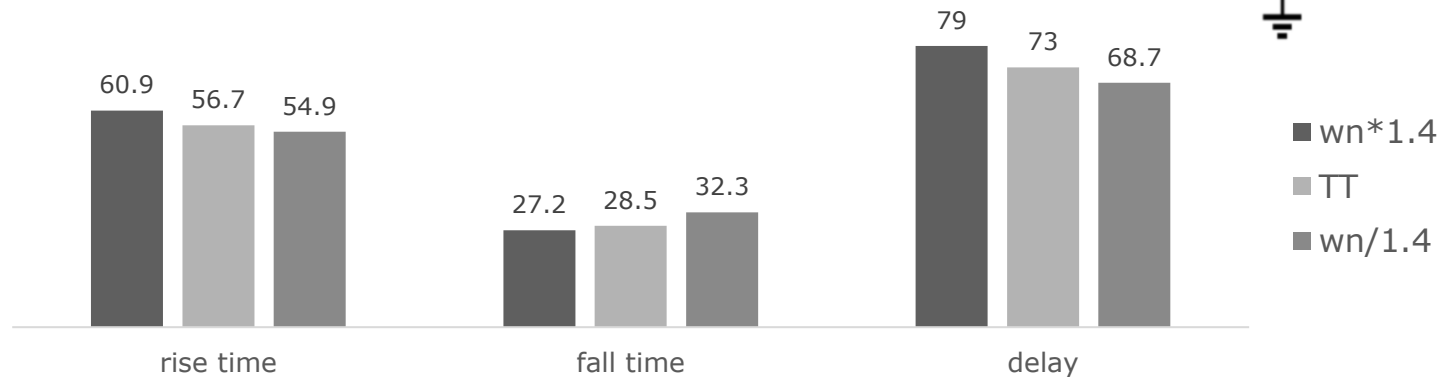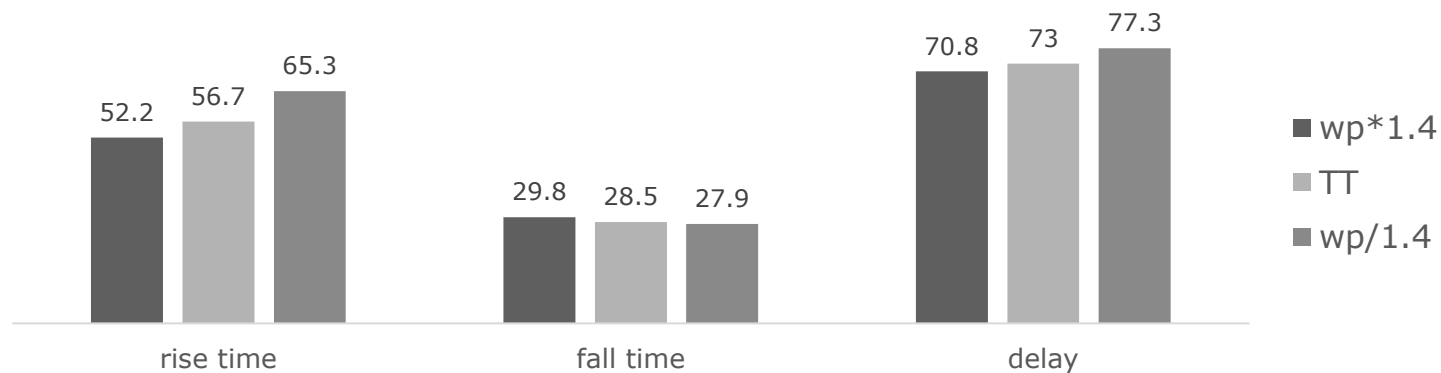
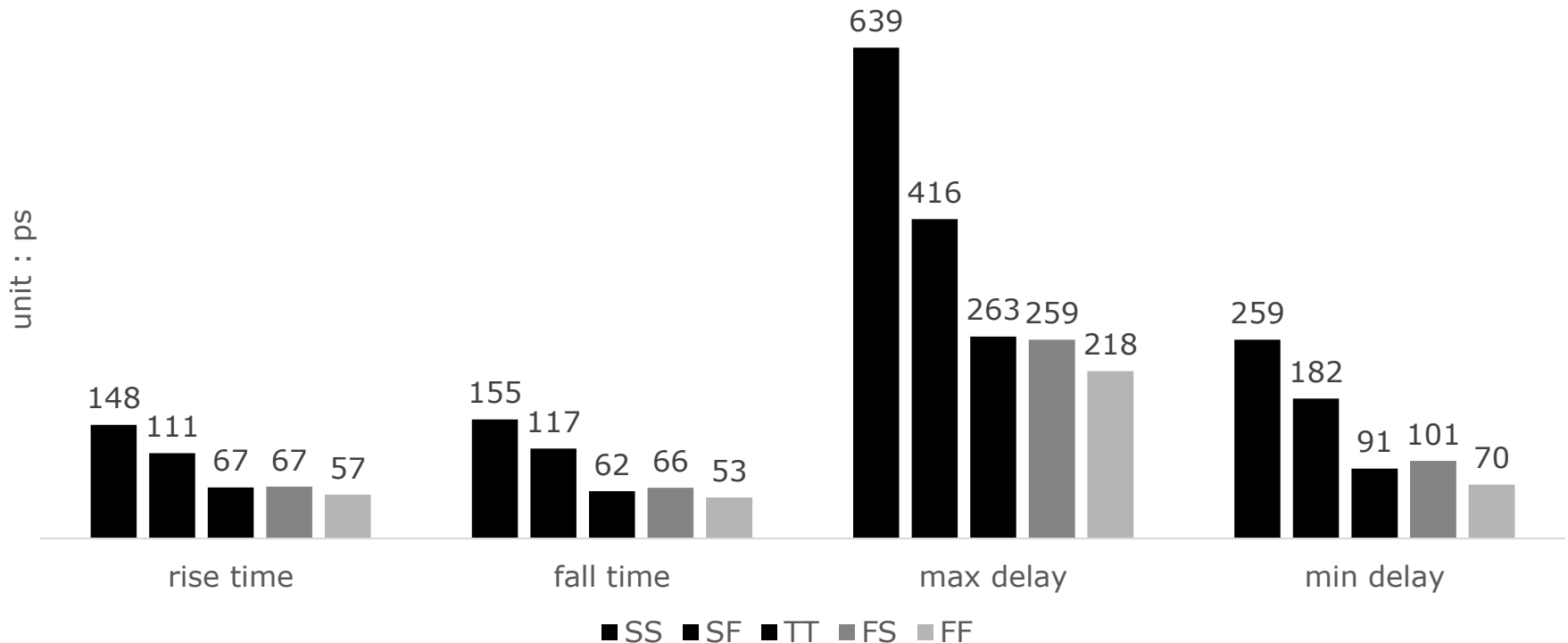# 28T Full Adder

□ Structure

■ Cout = MAJ(A , B , Cin)

■ Sum = ABC + (A + B + Cin)$\overline{\text{Cout}}$

■ Wp = 0.75u, Wn = 0.25u
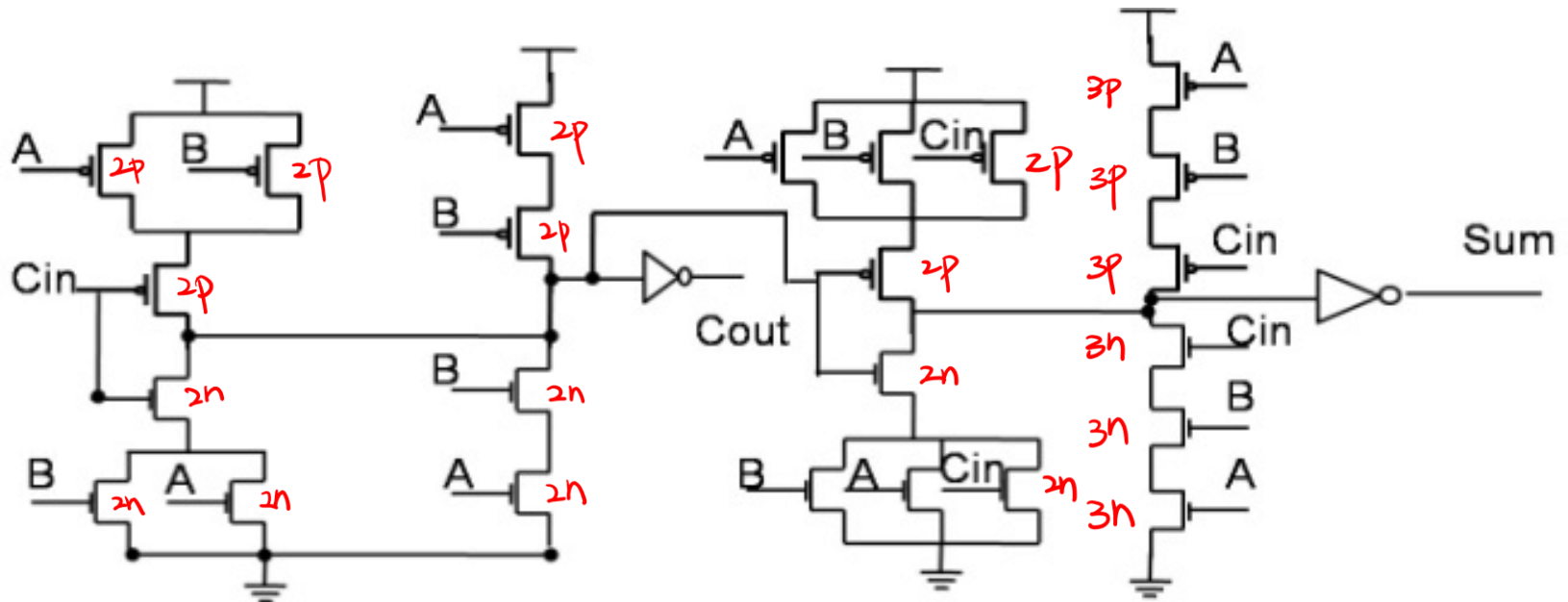
28T Full Adder

□ Fastest at FF, slowest at SS

1.8V Performance

unit : ps

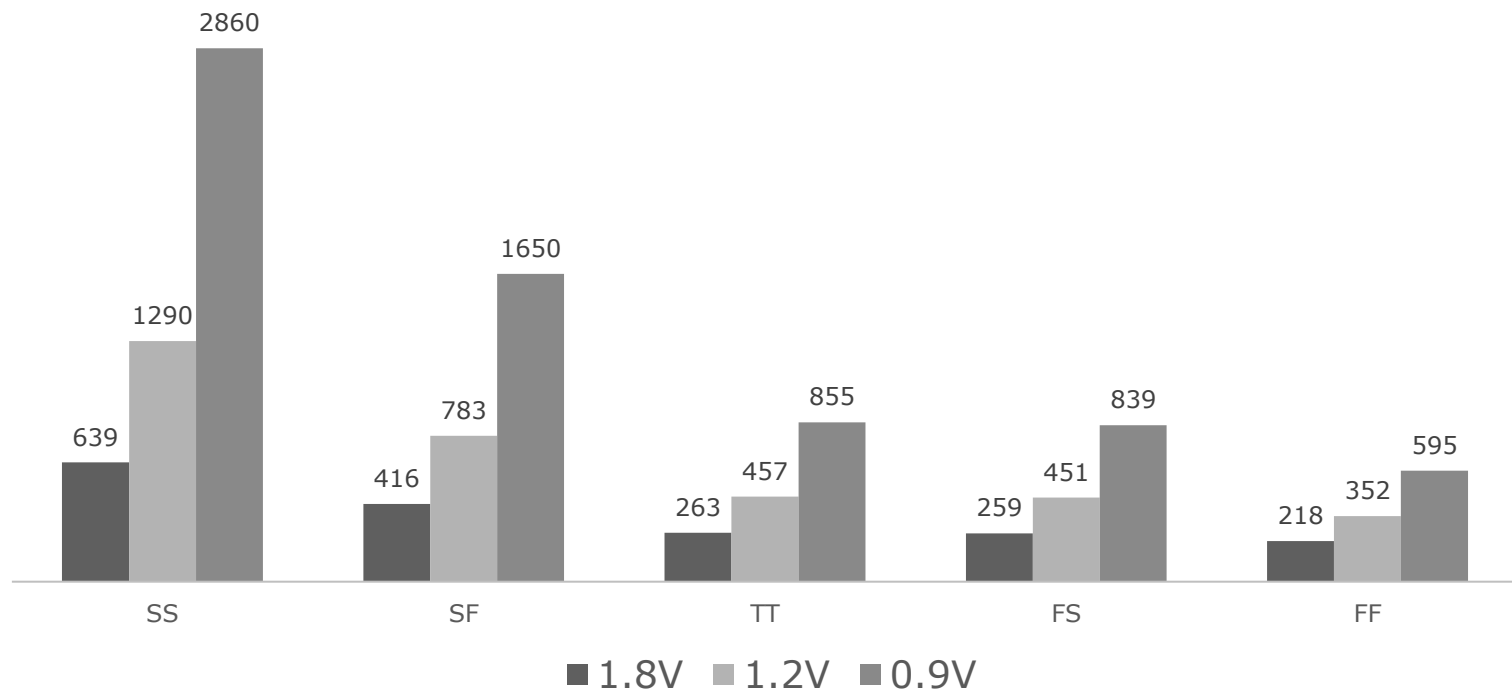|	rise time	fall time	max delay	min delay
SS	148	155	639	259
SF	111	117	416	182
TT	67	62	263	91
FS	67	66	259	101
FF	57	53	218	70

■ SS ■ SF ■ TT ■ FS ■ FF
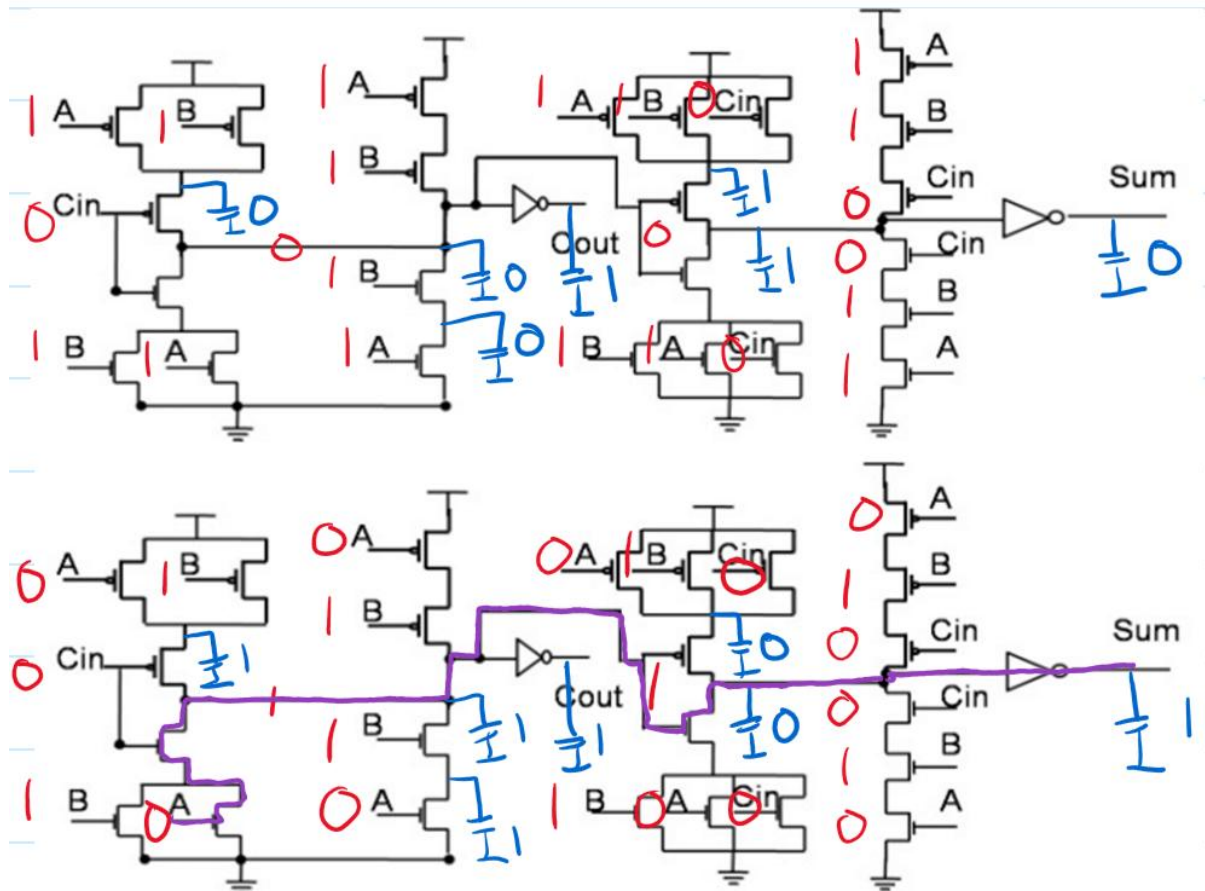
28T Full Adder

☐ High VDD -> Faster

Delay of VDD variation

28T Full Adder

□ Critical path

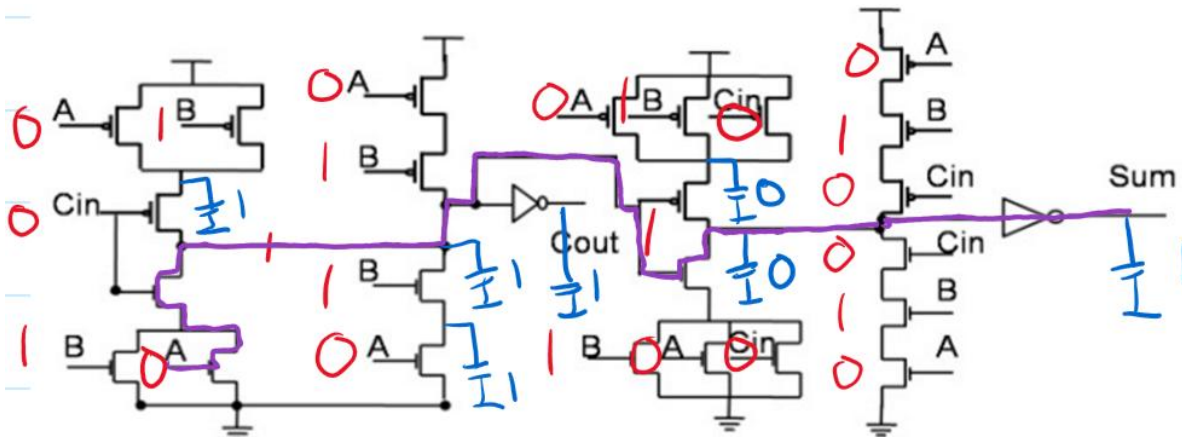■ A: 1->0 , B: 1 , Cin: 0, Cout: 1->0, Sum: 0->1
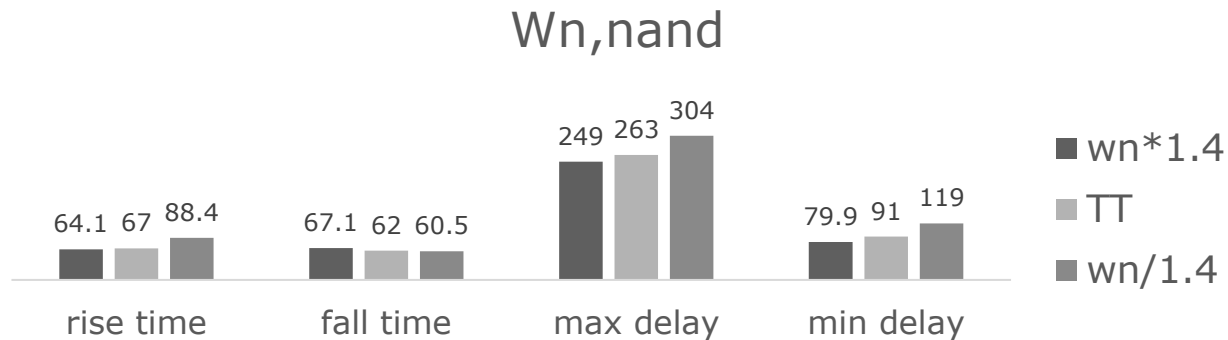
28T Full Adder

□ Critical path

  ■ A: 1->0 , B: 1 , Cin: 0, Cout: 1->0, Sum: 0->1
  ■ Delay can be estimated by Elmore RC model
  ■ Longer path -> larger effective capacitance

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + ... + (R_1 + R_2 + ... + R_N) C_N$$

28T Full Adder (Adjsut W by 40%)

☐ Adjust Wn (excluding inverters)

Wn,nand

	wn*1.4
	TT
	wn/1.4

- rise time: 64.1, 67, 88.4
- fall time: 67.1, 62, 60.5
- max delay: 249, 263, 304
- min delay: 79.9, 91, 119

☐ Adjust Wp (excluding inverters)

- ■ Shorter delay when reducing size of Wp
- ■ Max/Min delay happens at Sum : 0 -> 1

Wn,nand

	wp*1.4
	TT
	wp/1.4

- rise time: 78.1, 67, 64.9
- fall time: 62.1, 62, 69.2
- max delay: 278, 263, 261
- min delay: 107, 91, 77.5

13