AND / FA

B11901027 王仁軒

NM with Wa Variation

- SNM:
  - Noise margin does not change with Wa

Wa = 0.36 um **Wa = 0.48 um** **Wa = 0.60 um**

0.794 = **0.794** = **0.794**

- RNM:
  - Noise margin ↑ with Wa ↓

Wa = 0.36 um **Wa = 0.48 um** **Wa = 0.60 um**

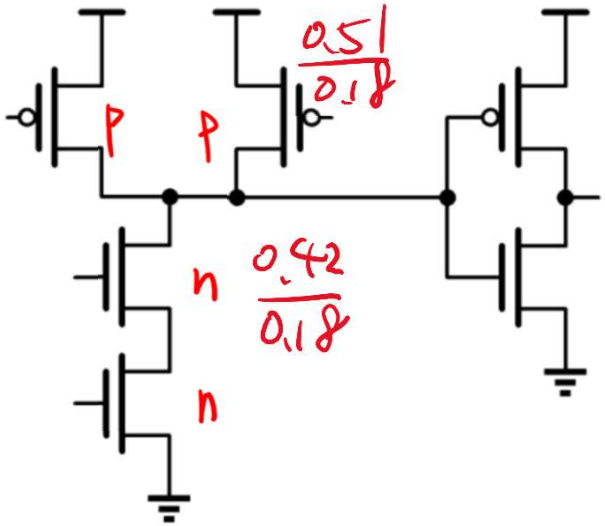
0.373 > **0.291** > **0.222**

- WNM
  - Noise margin ↑ with Wa ↑

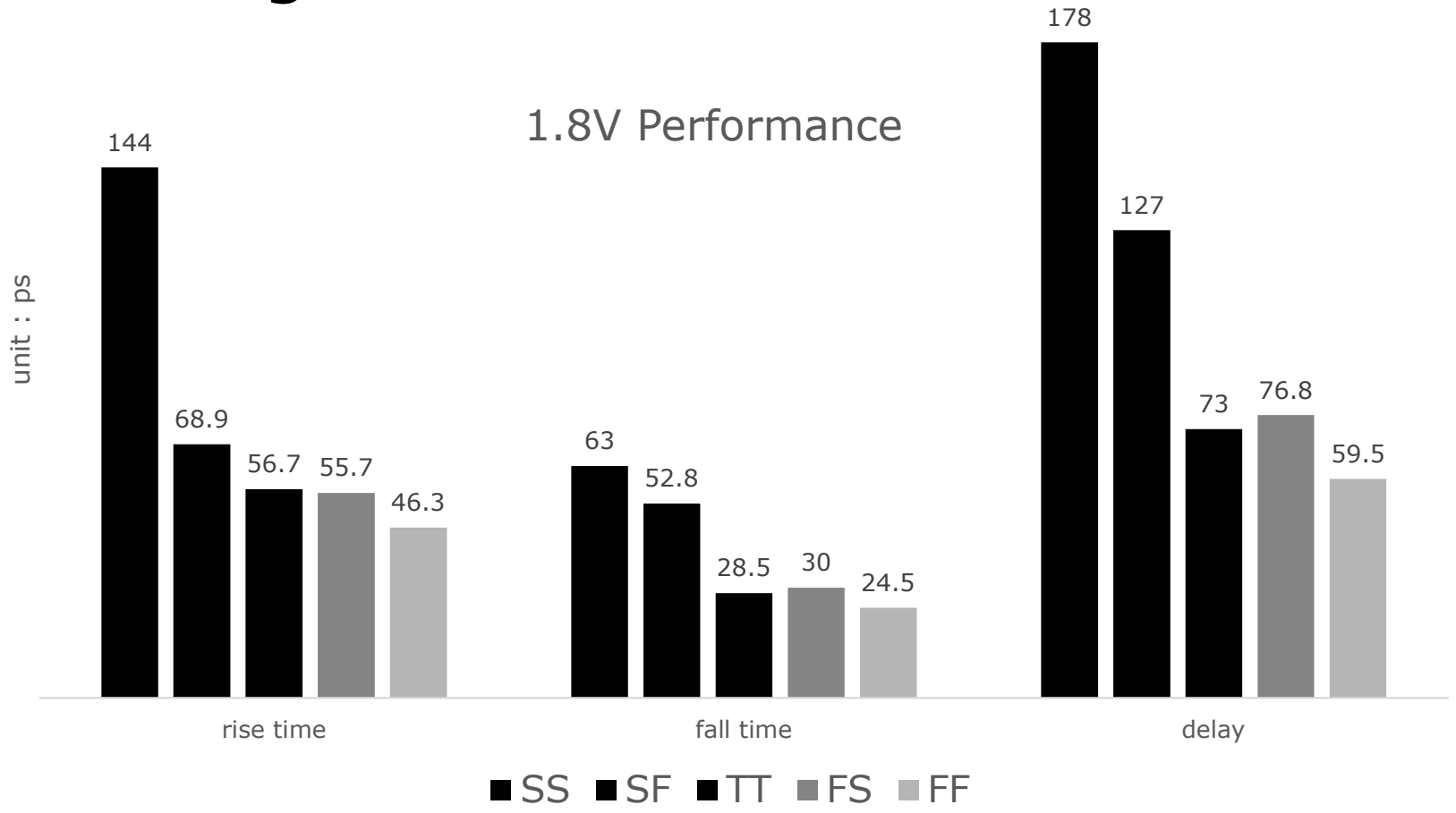
Wa = 0.36 um **Wa = 0.48 um** **Wa = 0.60 um**

0.467 < **0.473** < **0.475**

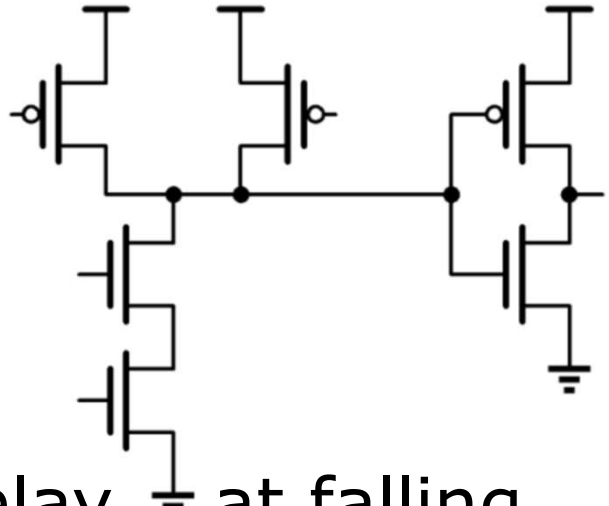
AND



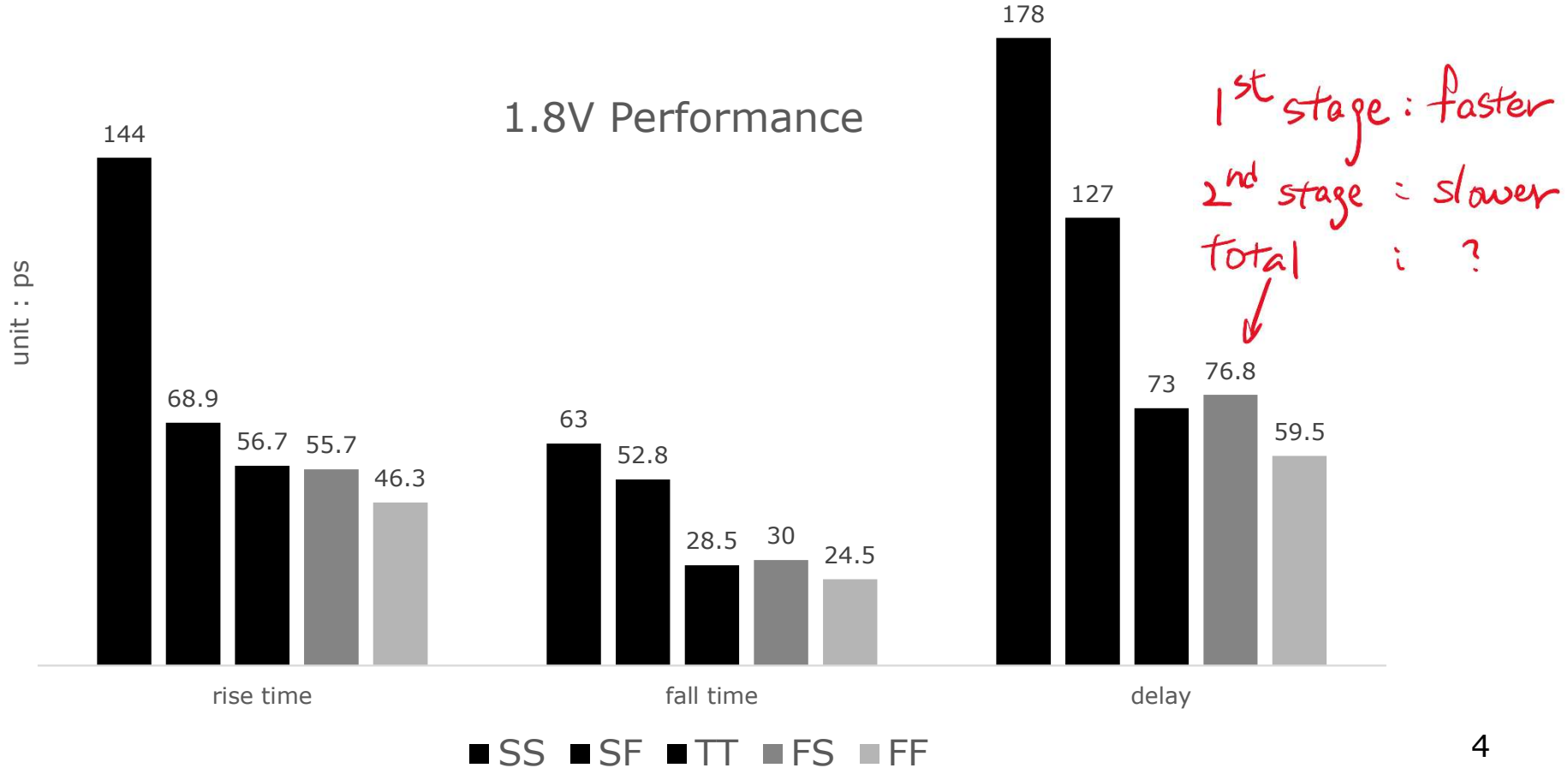
- Fastest at FF, slowest at SS
- No Sizing -> rise time = 2x fall time



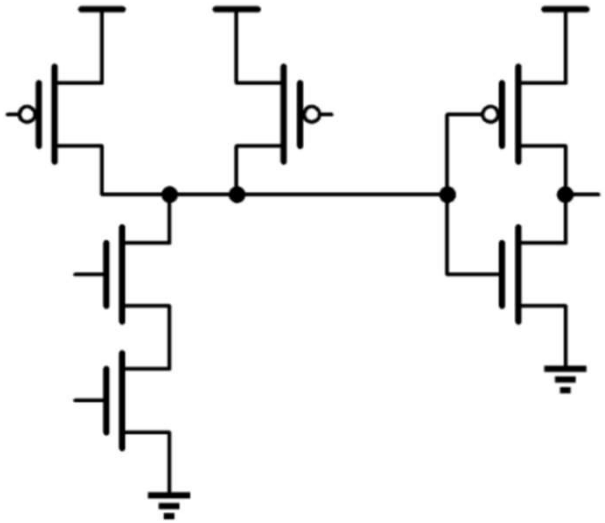
AND



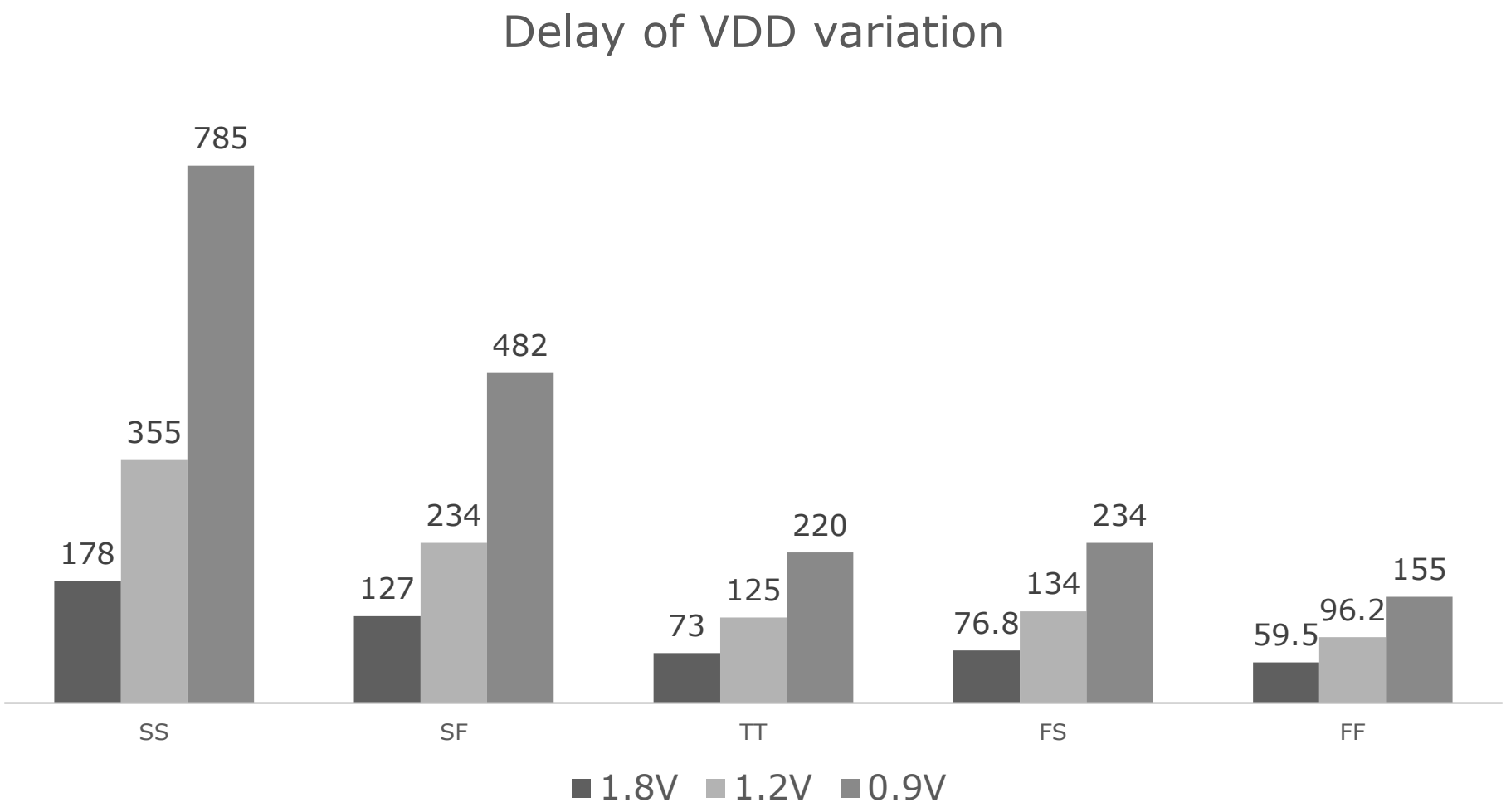
- Delay: FS > TT
  - Unbalanced size -> maximum delay at falling



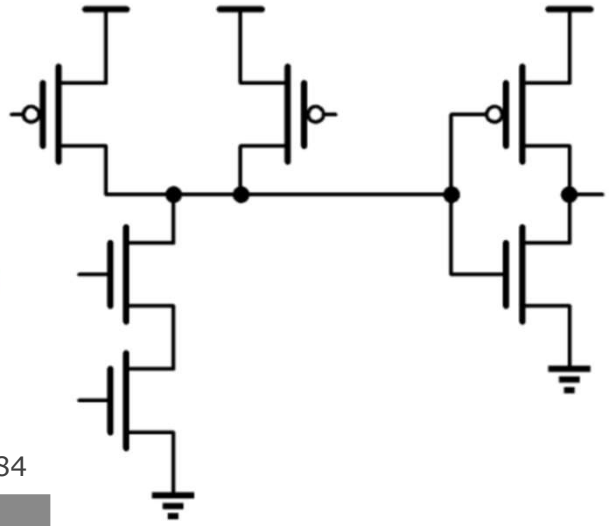
AND



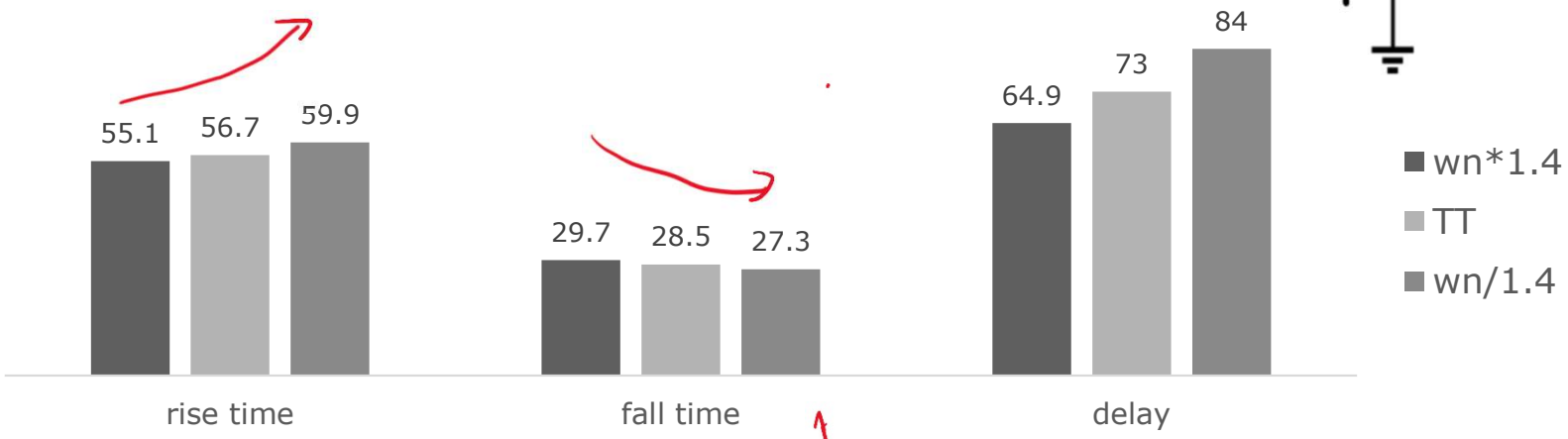
- High VDD -> Faster



AND (Adjust W by 40%)

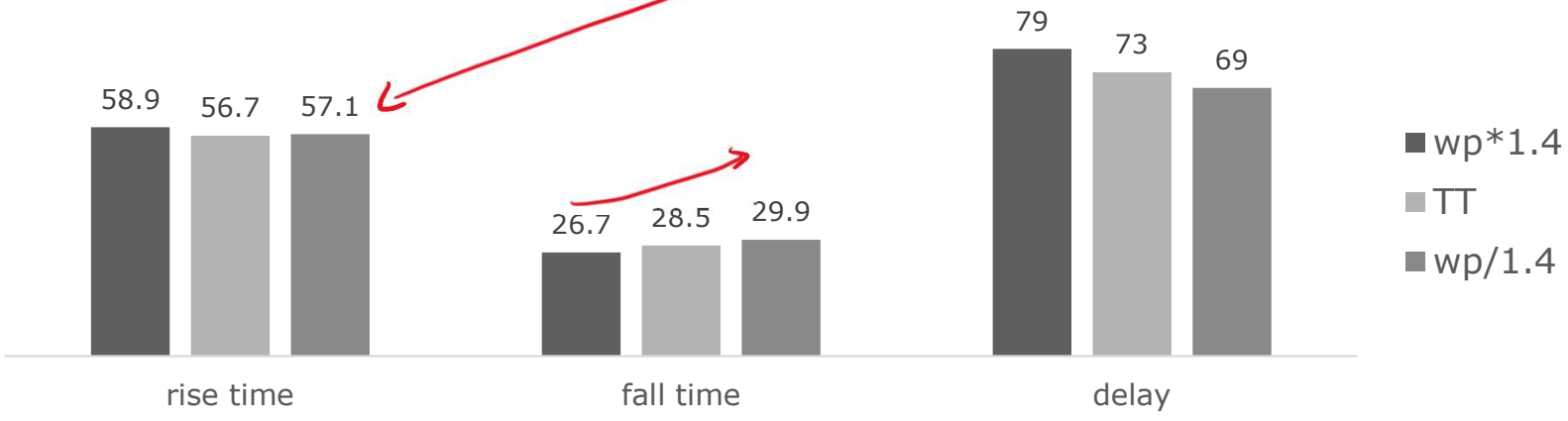


- Adjust Wn,nand

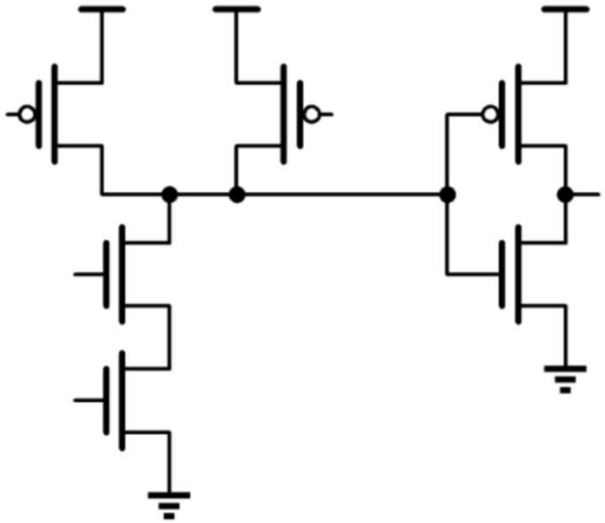


- Adjust Wp,nand

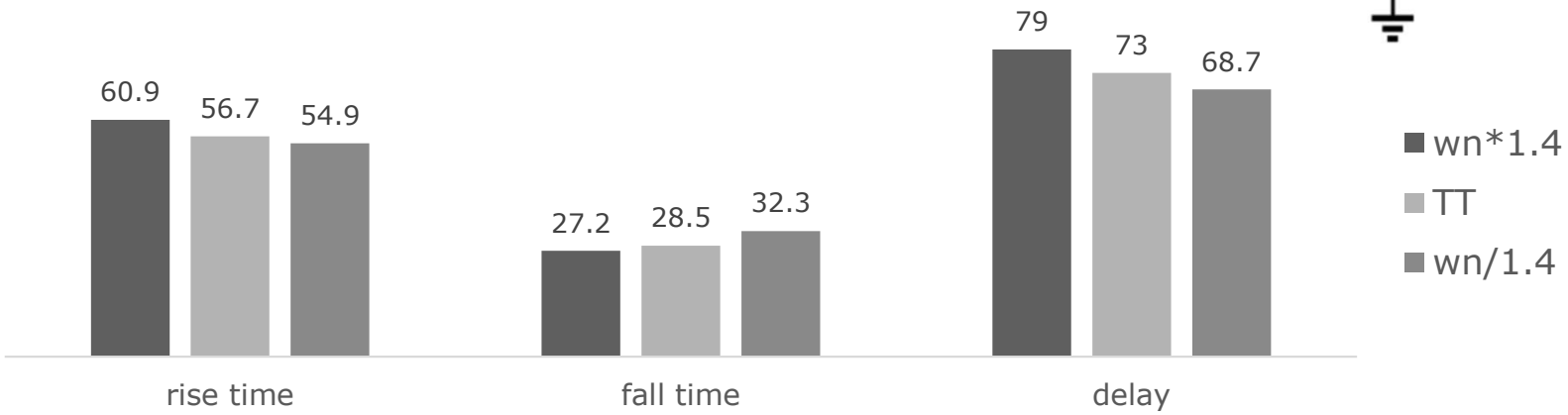
smaller caps



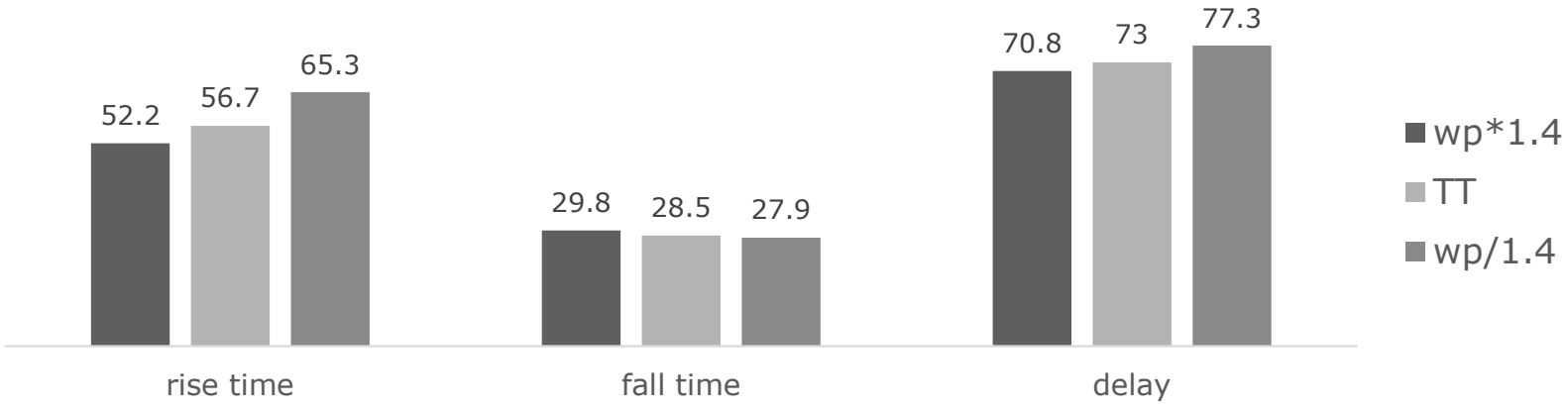
AND (Adjust W by 40%)



- Adjust Wn,inv

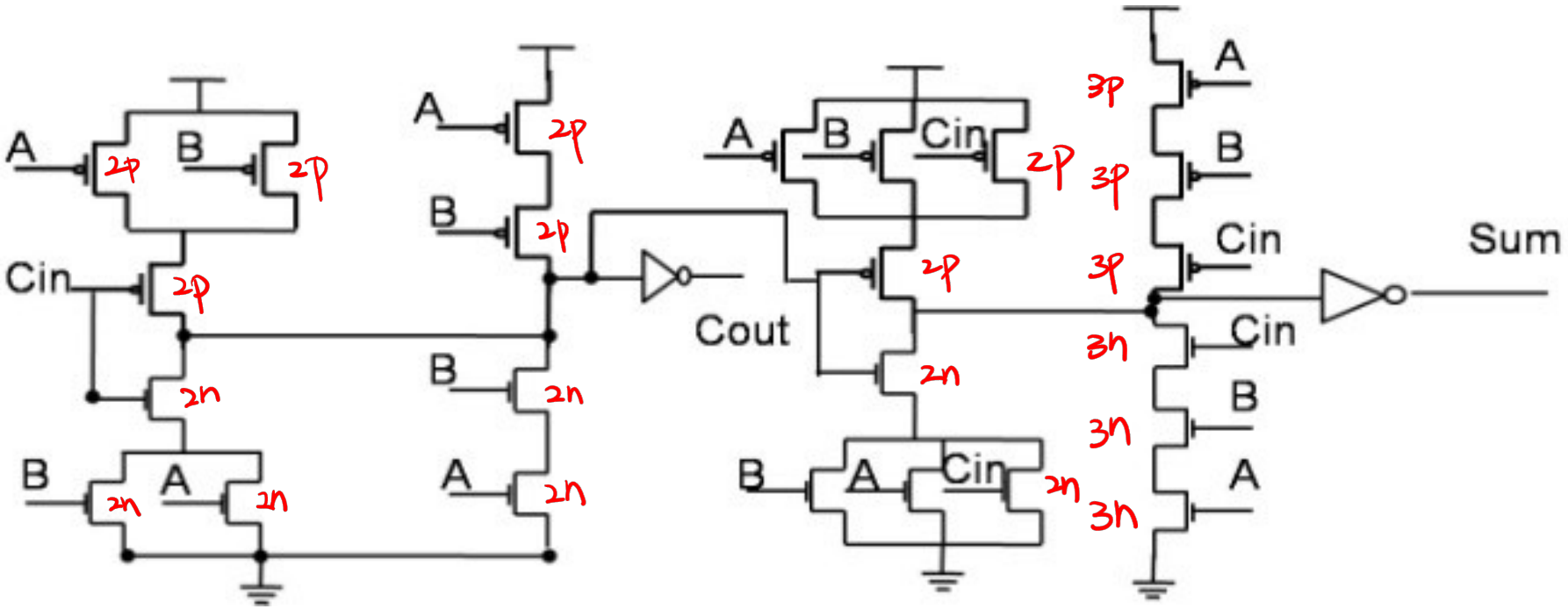


- Adjust Wp,inv



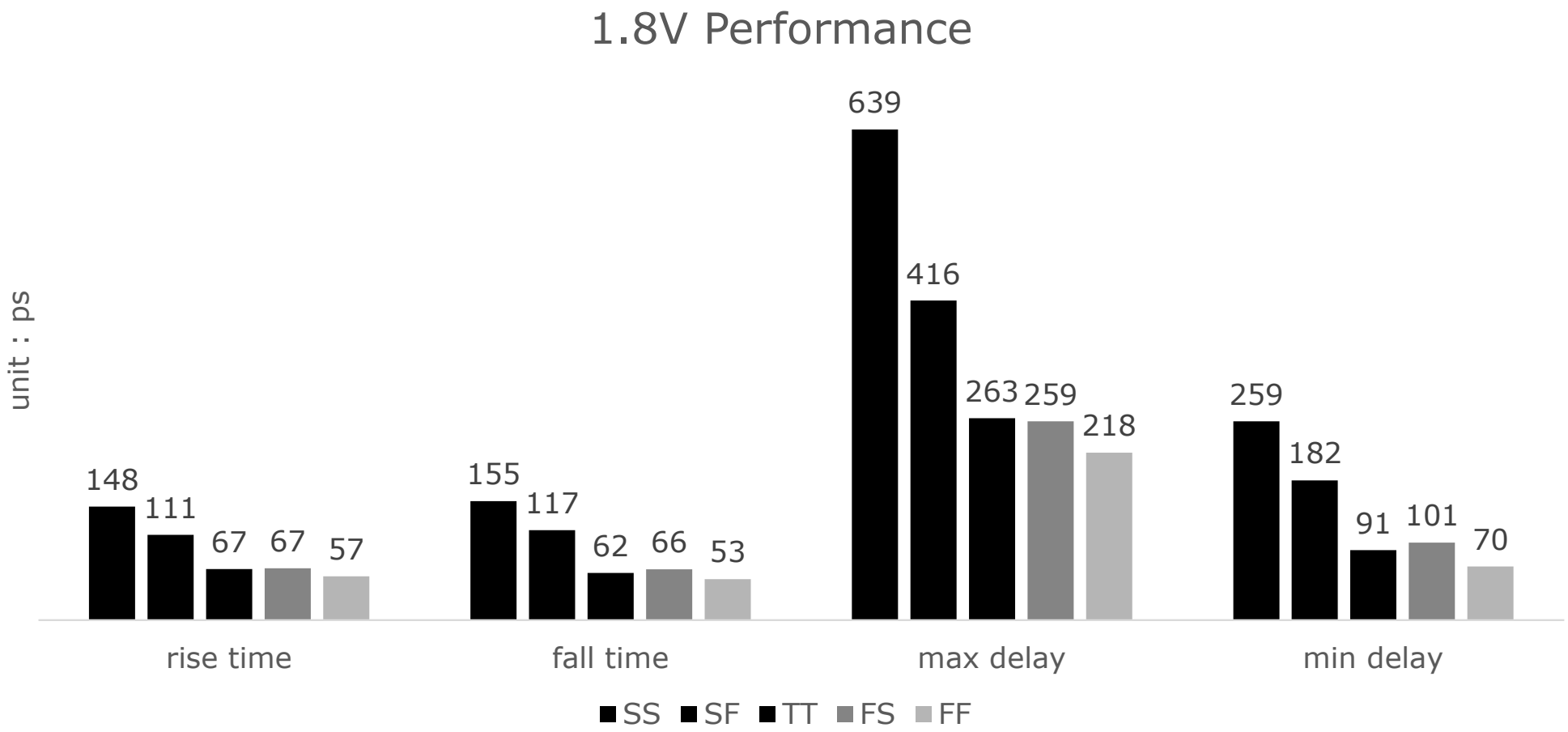
28T Full Adder

- Structure
  - Cout = MAJ(A , B , Cin)
  - Sum = ABC + (A + B + Cin)$\overline{\text{Cout}}$
  - Wp = 0.75u, Wn = 0.25u



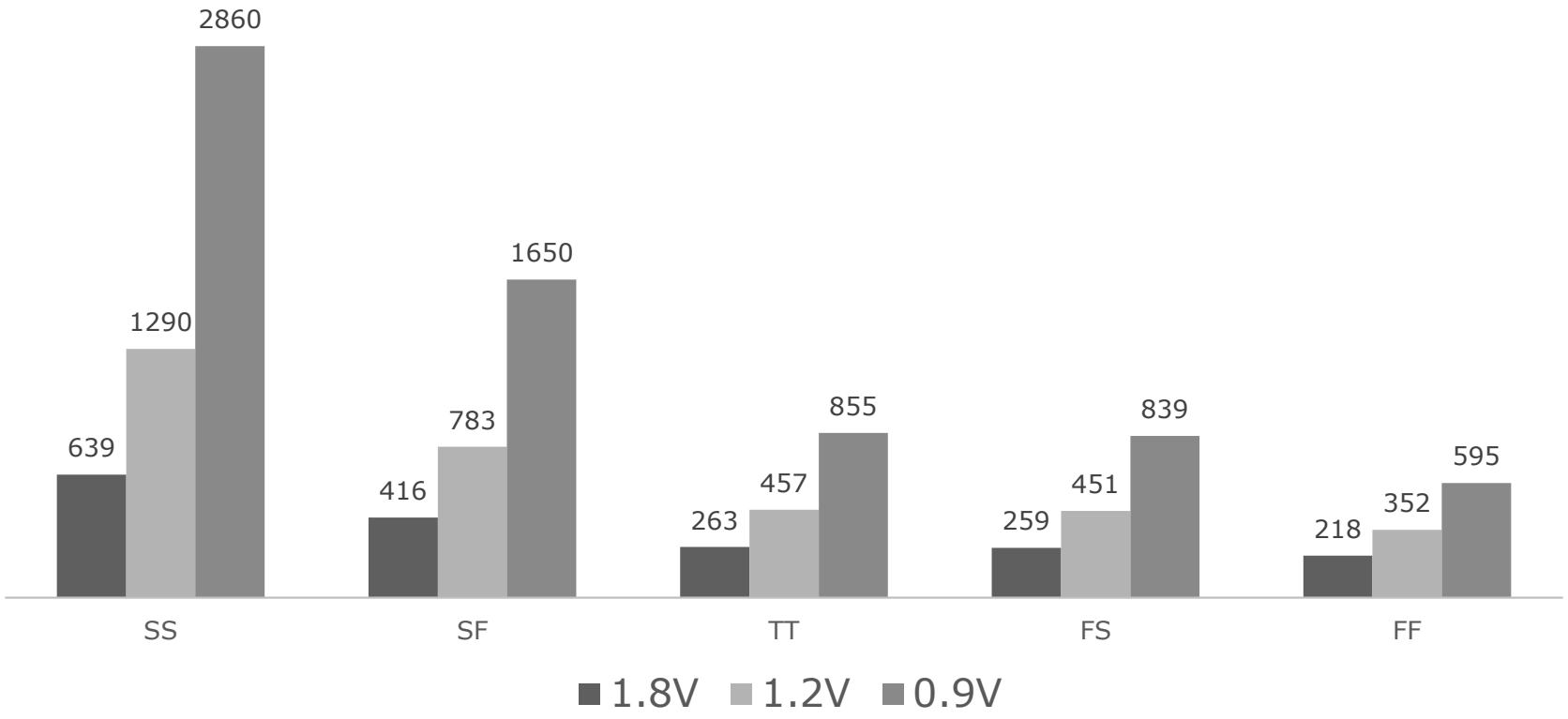
28T Full Adder

- Fastest at FF, slowest at SS



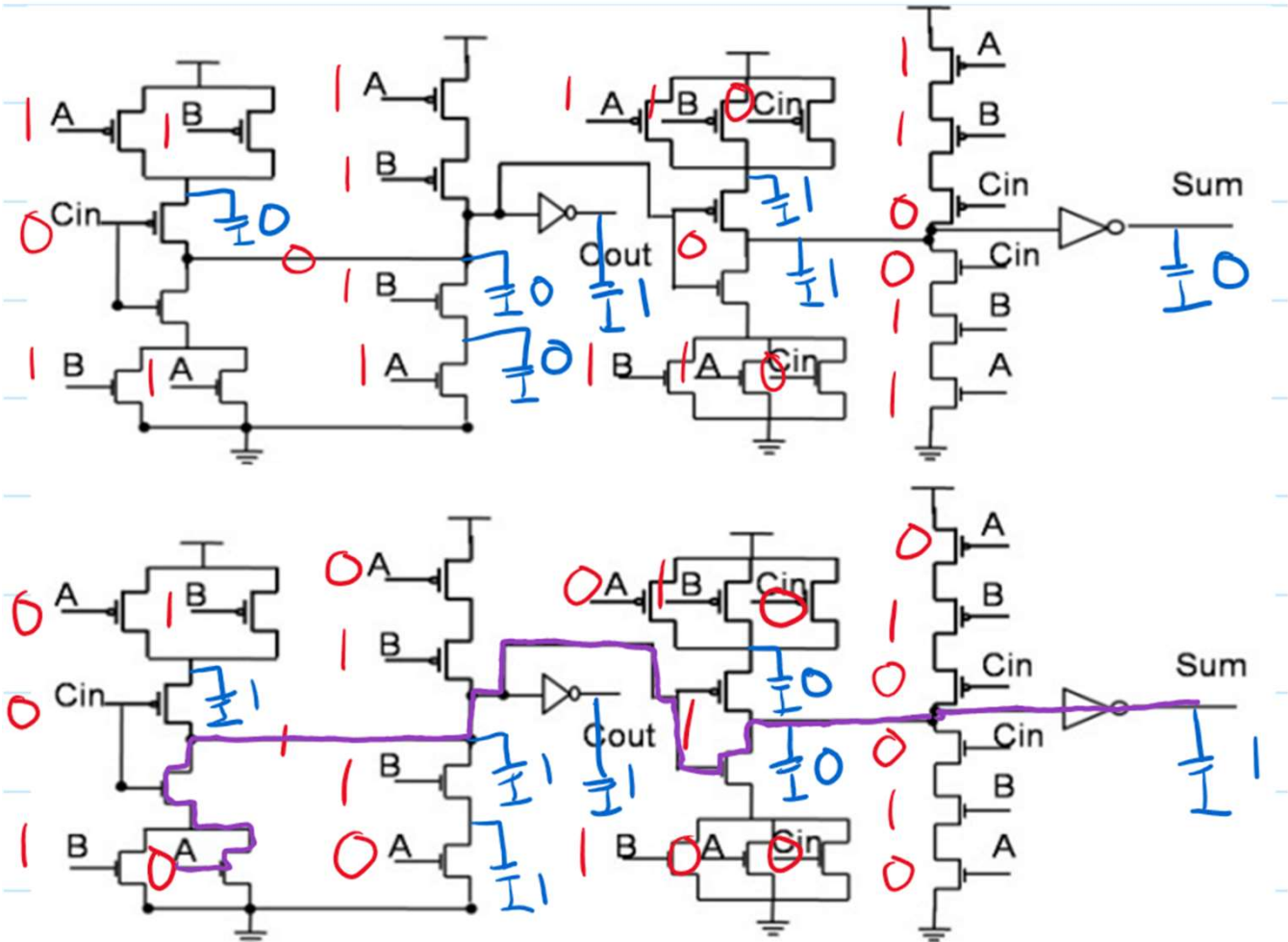
28T Full Adder

- High VDD -> Faster



28T Full Adder

- Critical path
  - A: 1->0 , B: 1 , Cin: 0, Cout: 1->0, Sum: 0->1

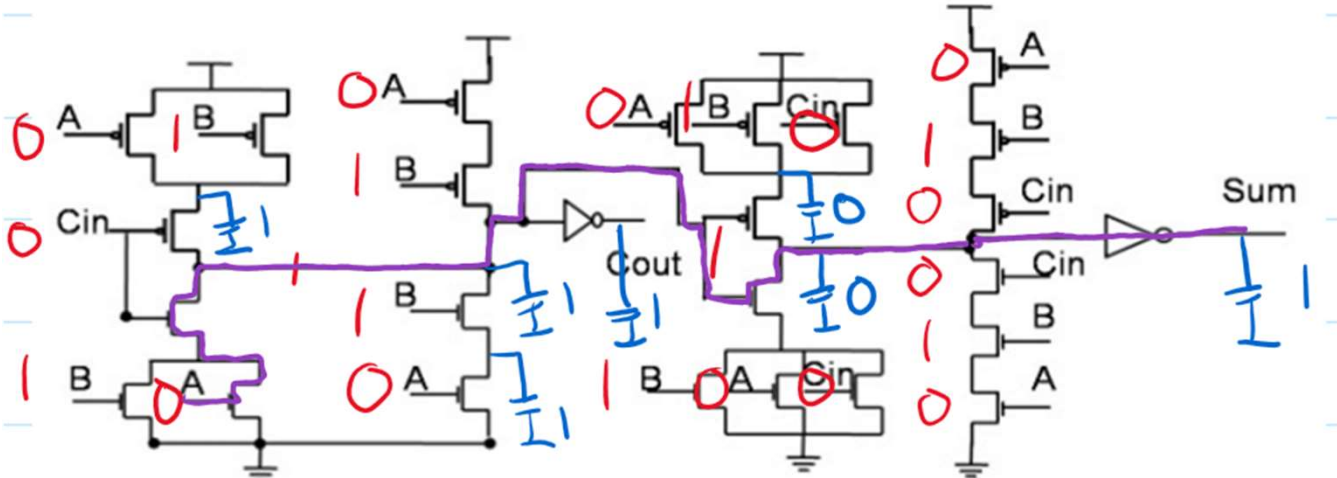


28T Full Adder

- Critical path
  - A: 1->0 , B: 1 , Cin: 0, Cout: 1->0, Sum: 0->1
  - Delay can be estimated by Elmore RC model
  - Longer path -> larger effective capacitance

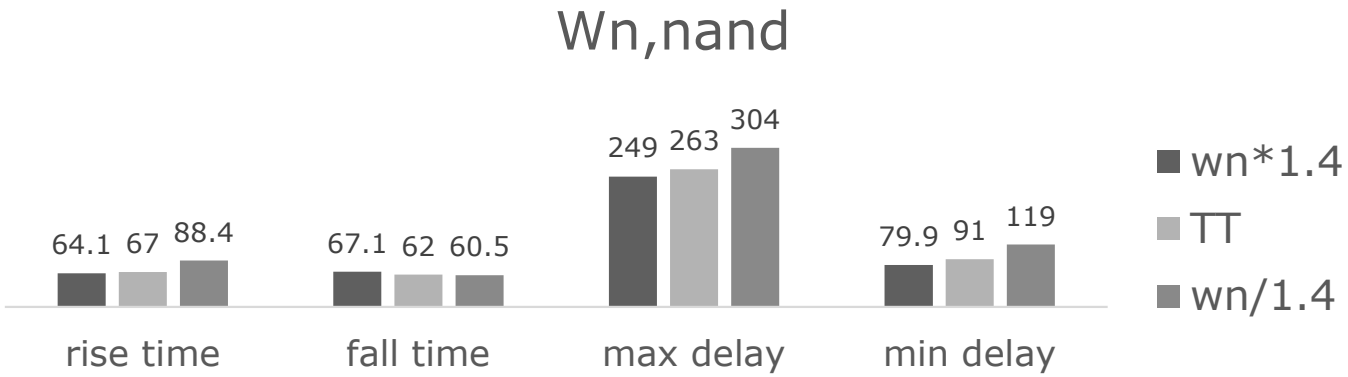
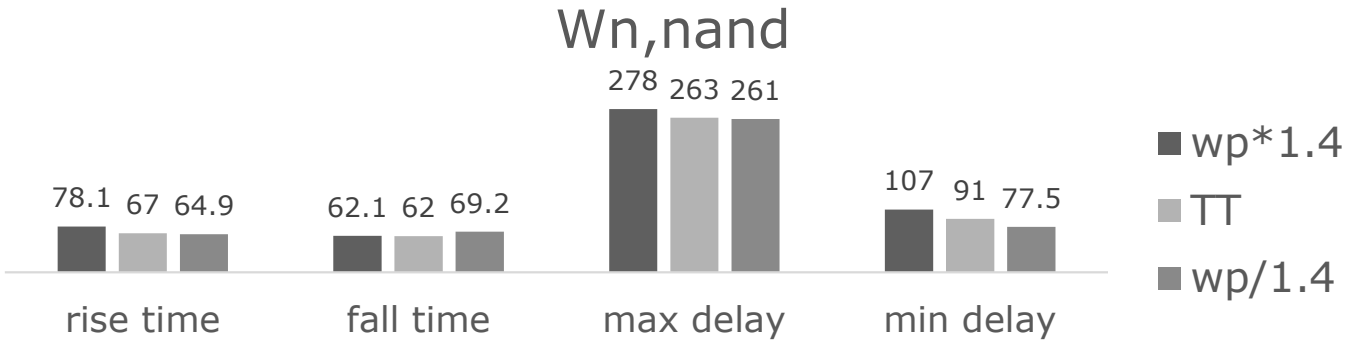
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



28T Full Adder (Adjsut W by 40%)

- Adjust Wn (excluding inverters)



- Adjust Wp (excluding inverters)
  - Shorter delay when reducing size of Wp
  - Max/Min delay happens at Sum : 0 -> 1