Static-Noise Margin Analysis of MOS SRAM Cells

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Abstract—**The stability of both resistor-load (R-load) and full-CMOS SRAM cells is investigated analytically as well as by simulation. Explicit analytic expressions for the static-noise margin (SNM) as a function of device parameters and supply voltage are derived. The expressions are useful in predicting the effect of parameter changes on the stability as well as in optimizing the design of SRAM cells. An easy-to-use SNM simulation method is presented, the results of which are in good agreement with the results predicted by the analytic SNM expressions. It is further concluded that full-CMOS cells are much more stable than R-load cells at a low supply voltage.**

I. Introduction

TWO aspects are important for SRAM cell design: the cell area and the stability of the cell. The cell area determines about two-thirds of the total chip area. The cell stability determines the soft-error rate and the sensitivity of the memory to process tolerances and operating conditions. The two aspects are interdependent since designing a cell for improved stability invariably requires a larger cell area.

There has been considerable effort over the past several years to understand and model the stability of flip-flop cells. The basic cross-coupled cell is deceptively simple in appearance, yet attempts to analytically model the cell stability have achieved only limited success [1]. Much of the published work has been concerned with the statistical and dynamic properties of flip-flop synchronizers in the metastable region [1]–[3]. The stability as expressed by the static-noise margin (SNM) [4] has also been investigated for both resistor-load [5], [6] and full-CMOS [7] SRAM cells. However, these studies have been limited to computer simulations; analytic work has not yet been reported. This paper is concerned with the SNM of SRAM cells both from an analytic as well as a simulation point of view, in the context of submicrometer MOS technology. The results are useful in optimizing the design of SRAM cells as well as in predicting the effect of parameter changes on the SNM.

Resistor-load (R-load) cells are widely used in NMOS- and CMOS- (mixed-MOS) SRAM's owing to their smaller cell area when compared to the six-transistor (6T) full-CMOS cell [8]. Cell-area reductions of 30–50 percent have been obtained, usually at the expense of a more complex process. However, this area advantage will be significantly reduced in future scaled-down memory processes requiring supply voltage reduction to avoid hot-carrier degradation. The reason is that the SNM for R-load cells becomes much lower than for 6T cells at low supply voltage. For sufficient noise margin the R-load cell must then be made larger. This means that 6T cells have greater potential. In order to explain these statements the SNM of SRAM cells is studied in this paper.

In Section II the cell stability is discussed with the aid of a graphical representation of the SNM. Analytical expressions for the SNM of both R-load and 6T cells are derived in Section III and Appendices A and B. An easy-to-use simulation method for SNM investigation is developed in Section IV. In Section V analytic and simulation results are compared. Good agreement is demonstrated, thus confirming the validity of the analytic results. The conclusions are presented in Section VI.

II. SRAM-Cell Stability

Fig. 1(a) and (b) shows the circuit diagrams of the R-load cell and the 6T full-CMOS cell, respectively, during a read access and with the bit lines precharged to the power supply voltage. This is in fact the most critical situation because the resistor or p-channel load elements are now shunted by the n-channel access transistors, which reduces the gain of the cell inverters.

Both cell types can be represented by a flip-flop comprised of two inverters as shown in Fig. 2. The voltage sources V_n are static-noise sources. Static noise is dc disturbance such as offsets and mismatches due to processing and variations in operating conditions. The SNM of the flip-flop is defined as the maximum value of V_n that can be tolerated by the flip-flop before changing states [4]. In this paper, only static-noise sources are taken into account. A SRAM cell should be designed such that under all conditions some SNM is reserved to cope with dynamic disturbances caused by α particles, crosstalk, voltage supply ripple, and thermal noise.

A basic understanding of the SNM is obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. This

Manuscript received April 2, 1987; revised June 4, 1987.
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IEEE Log Number 8716261.

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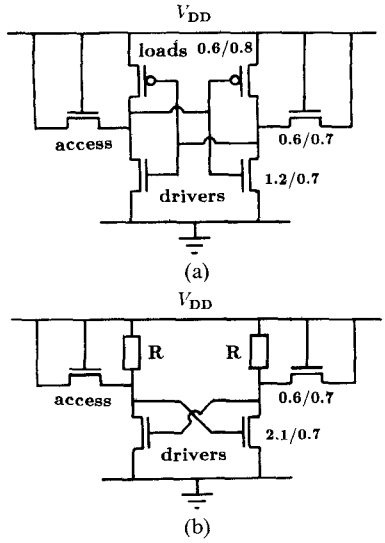

Fig. 1. SRAM cells during read access: (a) R-load, and (b) 6T full CMOS.

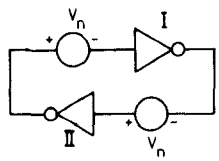

Fig. 2. A flip-flop comprised of two inverters. Static-noise voltage sources V_n are included.

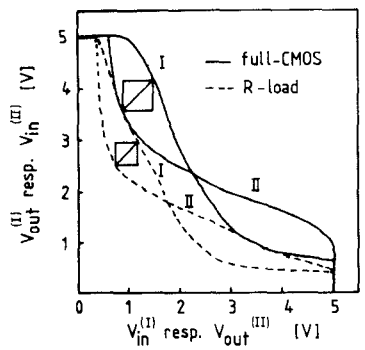

Fig. 3. Graphical representation of SNM. Curves II have been mirrored with respect to a line passing through the origin at 45° from the horizontal.

is a graphical technique of estimating the SNM [4], [5], [9]. It is illustrated in Fig. 3, using the most basic MOS model with constant threshold voltage and a simple exponential subthreshold current model. For the purpose of illustration, we assume $V_{DD} = 5$ V, $\beta_{\square n}/\beta_{\square p} = 2.3$ ($\beta_{\square}$ indicates the transconductance factor for a square transistor), all threshold voltages are 0.9 V, and transistor dimensions are as shown in Fig. 1. The ratio of β_{driver} to β_{access} is an important cell parameter called the "cell ratio" r. It determines the cell size as well as the cell stability. In this case, r is equal to 2 for the 6T cell and 3.5 for the R-load cell.

From Fig. 3 we see that the R-load inverter characteristic starts at V_{DD} when $V_{\text{in}} = 0$ V; it begins dropping sharply as soon as the subthreshold current is able to develop a noticeable voltage drop across the resistor (about 10 GΩ in our case). Subsequently the output voltage is clamped by the access transistor and drops further with reduced slope for $V_{\text{in}} > 1$ V when the driver transistor is turned on. Note that the cell noise margin in the R-load case is situated in the area where the load resistor and subthreshold current do not play any significant role. When comparing the maximum squares, it is clear that $\text{SNM}_{6T} > \text{SNM}_{R}$, in spite of the larger value of r for the R-load cell.

When V_{DD} is decreased, the SNM will likewise decrease for both cases; however, it is clear that the R-load cell will lose its data before the 6T cell does. In addition, the R-load cell can only be used with a V_{DD} somewhat larger than $2V_T$ (say 3 V in the case of $V_T = 1$ V) during access to avoid write-time problems.

III. Analytical Derivation of SNM

A. Assumptions and Analytic Expressions

The SNM can be found analytically by solving the Kirchhoff equations and applying one of the mathematically equivalent noise margin criteria [4]. For the cells of Fig. 1, we assume the right sides to be at level ZERO and the left sides at level ONE. This means that the cell circuit diagrams can be reduced to those shown in Fig. 4. The components shown dotted are assumed to be nonconducting, or at most to conduct only negligible currents. In Fig. 4(a), we assume Q_1, Q_3, and Q_4 operate in the saturation region and Q_2 in the linear region. In Fig. 4(b), Q_1 and Q_4 are assumed saturated while Q_2 and Q_5 are in the linear region. These assumptions were verified by simulation as well as by back substitution.

Explicit expressions for the SNM of the R-load cell and the 6T cell were obtained by using the basic MOS model equations with constant threshold voltages (equal for n- and p-channel) and neglecting second-order effects such as mobility reduction and velocity saturation. The detailed derivations are presented in Appendices A and B, of which the results are given below:

$$\text{SNM}_R = \frac{\sqrt{r}-1}{\sqrt{r}+1} V_T + \frac{r+1-\sqrt{2r^{3/2}+r+1}}{r(1+\sqrt{r})}(V_{DD}-V_T) \tag{1}$$

$$\text{SNM}_{6T} = V_T - \left(\frac{1}{k+1}\right)\left\{\frac{V_{DD}-\dfrac{2r+1}{r+1}V_T}{1+\dfrac{r}{k(r+1)}} - \frac{V_{DD}-2V_T}{1+k\dfrac{r}{q}+\sqrt{\dfrac{r}{q}\left(1+2k+\dfrac{r}{q}k^2\right)}}\right\} \tag{2}$$

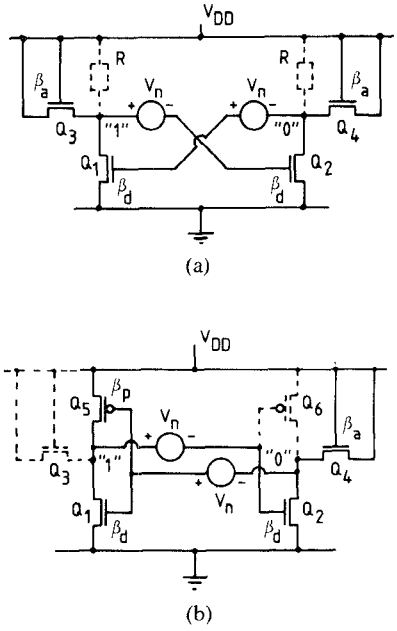

Fig. 4. (a), (b) Circuit diagrams of SRAM cells when accessed, with static-noise sources V_n inserted.

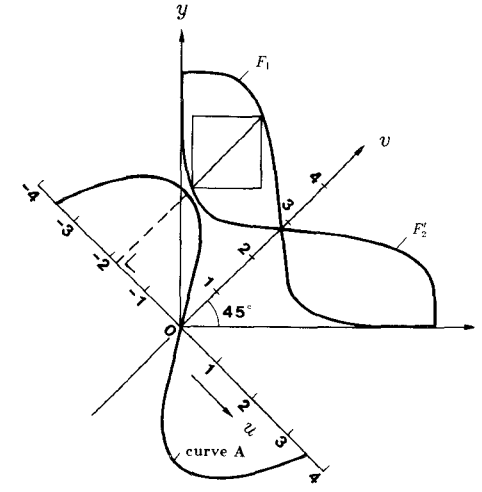

Fig. 5. SNM estimation based on "maximum squares" in a 45° rotated coordinate system.

where

$$r = \text{ratio} = \beta_d/\beta_a$$
$$q = \beta_p/\beta_a$$
$$V_T = \text{threshold voltage}$$
$$k = \left(\frac{r}{r+1}\right)\left\{\sqrt{\frac{r+1}{r+1-V_s^2/V_r^2}} - 1\right\}$$
$$V_s = V_{DD} - V_T$$
$$V_r = V_s - \left(\frac{r}{r+1}\right)V_T.$$

The derivation of (1) was exact; no simplifying approximations were needed. In the case of (2), only one approximation was required, i.e., assuming local linearity of the transfer curve of inverter Q_2/Q_4 around its operating point where Q_2 is in the linear region. See, for example, the full-CMOS curve I in Fig. 3. It is apparent that the bottom right-hand part is approximately linear.

B. Conclusions from Analytic Results

When studying the SNM expressions we can draw some interesting general conclusions. First, the SNM for both R-load and 6T cells depends only on threshold voltage, V_{DD}, and β ratios, and not on the absolute value of the β's. Therefore, the increased β values associated with submicrometer processes will not by themselves lead to improved cell stability.

Second, both SNM_R and $\text{SNM}_{6\text{T}}$ increase with r. $\text{SNM}_{6\text{T}}$ remains larger than zero for all values of $r > 0$; on the other hand, SNM_R already becomes zero for $r = 1$. To design the cells for maximum SNM, $r = \beta_d/\beta_a$ must be maximized and also (in the case of 6T cells) $q/r = \beta_p/\beta_d$ by appropriate choice of W/L ratios. This choice is, of course, constrained by the requirements of small cell area and proper cell-write operation.

Third, for particular values of r and q, $\text{SNM}_{6\text{T}}$ will be independent of V_{DD} variations. This is due to the coefficients of V_{DD} in (2) having opposite signs. Changing r or q will then result in either a positive or a negative dependence of $\text{SNM}_{6\text{T}}$ on V_{DD}. Thus, a particular required stability behavior with respect to varying V_{DD} can be obtained through proper choice of r and q. This is illustrated in Fig. 8 where two cases are shown with $r = 1$, $q = 3/8$ and $r = 2$, $q = 3/8$, respectively. On the other hand, for the R-load cell the SNM will always decrease with decreasing V_{DD}, as can be seen in Fig. 7.

Finally, both SNM_R and $\text{SNM}_{6\text{T}}$ will increase with increasing V_T. It follows that the SNM will decrease with increasing temperature since V_T decreases with temperature, and we have already concluded that the SNM is independent of the absolute value of the β's.

IV. SNM Simulation Method

A simulation method based on the graphical technique described in Section II is presented here. To estimate SNM values, a procedure is needed that finds values for the diagonals of the maximum squares as shown in Fig. 3. A method which is quick and easy to use was developed for use together with a standard dc circuit simulator [7].

Fig. 5 shows a stylized version of Fig. 3 in two coordinate systems which are rotated 45° relative to each other. In the (u, v) system, subtraction of the v values of normal and mirrored inverter characteristics at given u yields curve A, which is a measure of the diagonal's length. The maximum and minimum of curve A represent the required maximum squares.

Assume that the normal and mirrored inverter characteristics are defined by the functions $y = F_1(x)$ and $y = F_2'(x)$, where the latter is the mirrored version of $y = F_2(x)$. To find F_1 in terms of u and v, the (x, y) coordinates must first be transformed into the (u, v) system. The

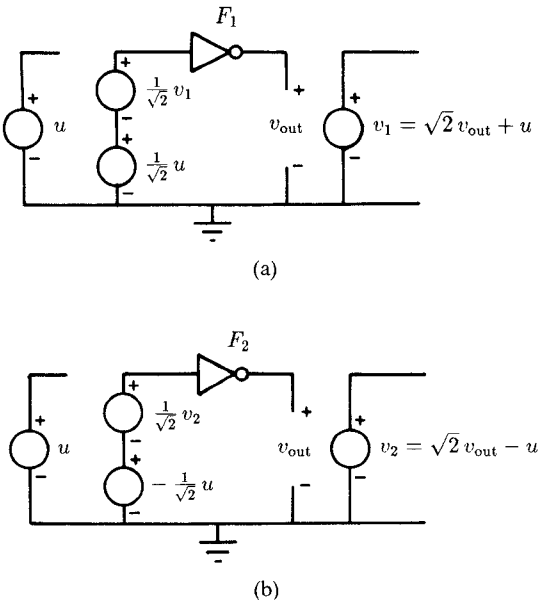

Fig. 6. Circuit implementations of (a) (4) and (b) (5).

required transformation is

$$x = \frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v \tag{3a}$$

$$y = -\frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v. \tag{3b}$$

Substitution of (3) in $y = F_1(x)$ gives

$$v = u + \sqrt{2}\,F_1\left(\frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v\right). \tag{4}$$

For F_2', first F_2 is mirrored in the (x, y) system with respect to the v axis, and then it is transformed to the (u, v) system. The required coordinate transformation is now the same as (3) but with x and y exchanged. Substituting in $y = F_2(x)$ gives

$$v = -u + \sqrt{2}\,F_2\left(-\frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v\right). \tag{5}$$

Equations (4) and (5) represent the inverters comprising the SRAM flip-flop cell. They give v as an implicit function of u. Solutions can be found with a standard dc circuit simulator by translating the equations into circuits, using voltage-dependent voltage sources in a feedback loop as shown in Fig. 6. The solutions of (4) and (5) are represented by v_1 and v_2 in Fig. 6(a) and (b), respectively. The difference between the two solutions, $v_1 - v_2$, is calculated by the simulator and is represented by curve A in Fig. 5.

The absolute values of the maximum and minimum are the values of the diagonals of the maximum squares. Multiplying the smaller of the two by $1/\sqrt{2}$ yields the SNM of the flip-flop.

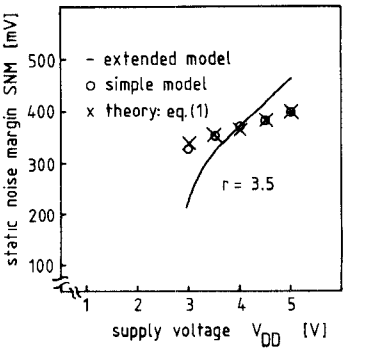

Fig. 7. SNM of R-load cell versus supply voltage.

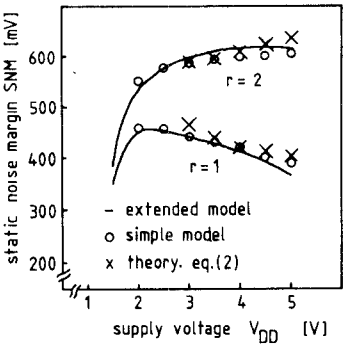

Fig. 8. SNM of full-CMOS cell versus supply voltage.

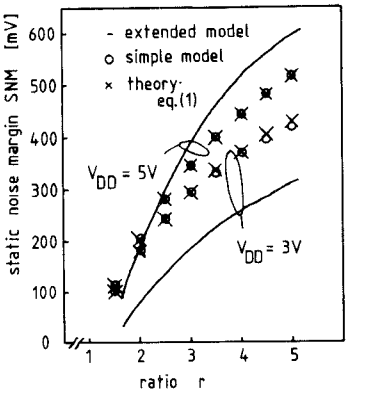

Fig. 9. SNM of R-load cell versus β_d/β_a ratio

V. Analytic and Simulation Results

In Figs. 7–10, the SNM's for the R-load and 6T cells, as predicted by (1) and (2), are plotted as a function of V_{DD} and r for $V_T = 0.9$ V and $q = 3/8$. The plots extend down to $V_{DD} = 3$ V which is the approximate limit of validity of the analytic models. In the figures the analytically predicted SNM is compared with simulations which were performed according to the method outlined in Section IV. For the simulations, both the most basic MOS model and a fully extended model with submicrometer transistor parameters (which includes subthreshold conduction, body effect, and mobility reduction) were used.

The curves obtained for the 6T cell (Figs. 8 and 10) show a good correspondence between (2) and the simulations for both transistor models. Note that the SNM is

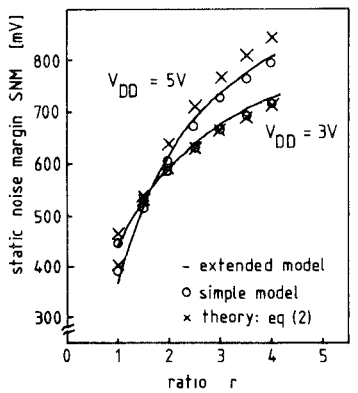

Fig. 10. SNM of full-CMOS cell versus β_d/β_a ratio.

approximately constant with V_{DD} for a ratio $r \simeq 1.7$. For smaller ratios the SNM increases with decreasing V_{DD} in contrast to the behavior with larger ratios. As discussed before, this behavior is predicted by (2).

The curves obtained for the R-load cell (Figs. 7 and 9) show a complete fit between (1) and simulations with the simple model. This is expected since the derivation of (1) was exact. However, a slope difference is observed for the simulation with the extended model. Further simulation has shown that this is caused by velocity saturation which was omitted from the simple model. This velocity saturation effect reduces the effective β of the access transistor Q_4 for large V_{DS} (see Fig. 4(a)). This reduces the influence of the high bit-line level on the low level in the cell, apparently increasing the SNM. In the case of the 6T cell of Fig. 4(b), this effect is compensated for by the mobility reduction of Q_5 and the drain feedback effects of Q_1 and Q_4.

As a general observation, we see that for decreasing V_{DD}, R-load cells need a significantly bigger ratio than 6T cells to achieve similar noise margins. Hence, for reduced supply voltage, the area advantage of R-load cells over full-CMOS cells begins disappearing.

So far the noise-margin comparison has been done for the read-access situation. When the SRAM is in the retention-mode (switched-off access transistors and $V_{DD} = 2$ V) the differences between SNM_R and SNM_{6T} are observed by simulation to be much less. For example, for the parameters shown in Fig. 1, SNM_R and SNM_{6T} are about 600 and 800 mV, respectively. These values are much better than the values obtained in the read-access case owing to the low-impedance access transistor loads being switched off. However, the impedances in the R-load case are much higher compared to the full-CMOS case. This makes the R-load cell much more sensitive to ac disturbances and α particles.

VI. Conclusions

Analytic expressions for the SNM of R-load and full-CMOS SRAM cells have been derived. The expressions are useful in predicting the effect of parameters and operating conditions on the SNM as well as in optimizing the design of SRAM cells. In addition, an SNM simulation method which is quick and easy to use has been developed. The simulation results are in good agreement with the analytic SNM predictions. For the R-load cell, velocity saturation in real transistors causes some deviation.

Further, it has been shown that full-CMOS cells have much better SNM values than R-load cells at low supply voltages. Therefore, in future memory processes, when the supply voltage has to be reduced to 3 V or less to avoid hot-carrier degradation, conventional R-load cells will suffer a significant disadvantage compared to full-CMOS cells. In order to maintain reasonable SNM values at a reduced supply voltage, the area required by R-load cells will be close to or equal to that of full-CMOS cells.

Appendix A
Derivation of SNM for R-Load Cell

We wish to analyze the circuit of Fig. 4(a). The MOS models we will use are

$$I_D = \frac{1}{2}\beta(V_{GS} - V_T)^2 \tag{A1}$$

$$I_D = \beta V_{DS}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right) \tag{A2}$$

in the "saturated" and "linear" regions, respectively. First we must know the operating conditions of the transistors (whether "saturated" or "linear"). Clearly, Q_1, Q_3, and Q_4 are saturated. Suppose Q_2 is also saturated. The voltage gain of each inverter is then $\sqrt{r}$, where $r = \beta_d/\beta_a$. The loop gain is therefore equal to r. It follows that for $r < 1$ the loop gain is insufficient for flip-flop operation [4]. For $r > 1$, the cell will be in a metastable condition independent of V_n and will unbalance until Q_2 enters the linear region. It follows that r must be larger than unity and we must take Q_2 in the linear region.

When equating the drain currents of Q_1 and Q_3 and those of Q_2 and Q_4, using the appropriate models, we find

$$V_{GS3} - V_T = \sqrt{r}\,(V_{GS1} - V_T) \tag{A3}$$

$$(V_{GS4} - V_T)^2 = 2rV_{DS2}\left(V_{GS2} - V_T - \frac{1}{2}V_{DS2}\right). \tag{A4}$$

Now we write the Kirchhoff voltage equations:

$$V_{GS1} = V_n + V_{DS2} \tag{A5}$$

$$V_{GS3} = V_{DD} - V_{GS2} - V_n \tag{A6}$$

$$V_{GS4} = V_{DD} - V_{DS2}. \tag{A7}$$

Substituting these into (A3) and (A4) yields

$$V_{DD} - V_{GS2} - V_n - V_T = \sqrt{r}\,(V_n + V_{DS2} - V_T) \tag{A8}$$

$$(V_{DD} - V_{DS2} - V_T)^2 = 2rV_{DS2}\left(V_{GS2} - V_T - \frac{1}{2}V_{DS2}\right). \tag{A9}$$

Eliminating V_{GS2} from (A8) and (A9) and simplifying results in a quadratic equation

$$aV_{DS2}^2 + bV_{DS2} + c = 0 \tag{A10}$$

with

$$\left.\begin{aligned} a &= 1 + r + 2r^{3/2} \\ b &= -2\{V_s(r+1) + r(\sqrt{r}-1)V_T - r(\sqrt{r}+1)V_n\} \\ c &= V_s^2 \end{aligned}\right\} \tag{A11}$$

where $V_s = V_{DD} - V_T$.

We now find the SNM by applying a condition for marginal stability to (A10) and (A11). We can choose from several equivalent stability criteria [4]. For this case it is easiest to use the condition of coinciding roots [4]. For (A10) this means a double root, which requires

$$b^2 = 4ac$$

or

$$b = -2\sqrt{ac} \tag{A12}$$

since $b < 0$. Substituting (A11) and solving for V_n yields the SNM:

$$\mathrm{SNM_R} = \frac{\sqrt{r}-1}{\sqrt{r}+1}V_T + \frac{r+1-\sqrt{2r^{3/2}+r+1}}{r(\sqrt{r}+1)}V_s. \tag{A13}$$

Next we determine the range of V_{DD} for which this analysis is valid. Q_1 and Q_3 have to operate in strong inversion, i.e., we require $V_{GS1} > V_T$. Together with (A5) this means

$$V_{DS2} > V_T - V_n. \tag{A14}$$

When solving for V_{DS2} from (A10) and (A11) under the condition (A12) and substituting (A13), we find

$$V_{DS2} = \frac{V_s}{\sqrt{2r^{3/2}+r+1}}. \tag{A15}$$

When next combining (A14) and (A15) and simplifying we find the minimum supply voltage for which this analysis is valid:

$$V_{DD\,\min} = \left\{1 + \frac{2r\sqrt{2r^{3/2}+r+1}}{(r+1)\sqrt{2r^{3/2}+r+1} - r^{3/2} - 1}\right\}V_T. \tag{A16}$$

For example, when $V_T = 0.9$ V this expression reduces to 3.2 V for $r = 3.5$ and 2.7 V for $r = 1$. It follows that (A13) is valid for V_{DD} down to about 3 V.

Appendix B
Derivation of SNM for Full-CMOS Cell

For the circuit of Fig. 4(b) we assume Q_1 and Q_4 to be saturated and Q_2 and Q_5 to operate in the linear region. These assumptions were checked by simulation and back substitution of the result. Equating the drain currents of Q_1 and Q_5 and those of Q_2 and Q_4, and using the models (A1) and (A2), results in

$$(V_{GS1} - V_T)^2 = \frac{2q}{r}V_{DS5}\left(V_{GS5} - V_T - \frac{1}{2}V_{DS5}\right) \tag{B1}$$

$$(V_{GS4} - V_T)^2 = 2rV_{DS2}\left(V_{GS2} - V_T - \frac{1}{2}V_{DS2}\right) \tag{B2}$$

where the threshold voltages of the p- and n-channel devices are assumed equal and $q = \beta_p/\beta_a$, $r = \beta_d/\beta_a$.

The required Kirchhoff voltage equations are

$$V_{GS1} = V_n + V_{DS2} \tag{B3}$$

$$V_{DS5} = V_{DD} - V_n - V_{GS2} \tag{B4}$$

$$V_{GS5} = V_{DD} - V_n - V_{DS2} \tag{B5}$$

and

$$V_{GS4} = V_{DD} - V_{DS2}. \tag{B6}$$

Substituting these into (B1) and (B2) yields

$$(V_{DS2} + V_n - V_T)^2 = \frac{q}{r}(V_{DD} - V_n - V_{GS2}) \cdot (V_s - V_T - V_n - 2V_{DS2} + V_{GS2}) \tag{B7}$$

$$(V_s - V_{DS2})^2 = 2rV_{DS2}\left(V_{GS2} - V_T - \frac{1}{2}V_{DS2}\right) \tag{B8}$$

with $V_s = V_{DD} - V_T$, as before.

Eliminating V_{GS2} or V_{DS2} from these two equations yields a fourth-degree equation which is too complex to be useful. A simplifying approximation leading to a lower degree is therefore needed.

In Section III-A we noted in connection with Fig. 3 that the transfer characteristic of the inverter which is ON has a fairly constant slope around its operating point. In Fig. 11 this part of the characteristic is shown, together with a straight-line approximation through point P at $V_{GS2} = V_s$ which is the approximate operating point when marginal noise is applied. The linear approximation is defined by the value of V_{DS2} and its slope at point P. V_{DS2} at point P is derived from (B8) by substituting $V_{GS2} = V_s$. The slope (denoted by $-k$) is determined by first differentiating (B8) with respect to V_{GS2} and then evaluating at $V_{GS2} = V_s$. The required linear approximation is then expressed as (see also Fig. 11)

$$V_{DS2} = V_0 - kV_{GS2} \tag{B9}$$

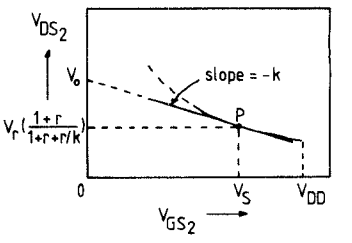

Fig. 11. Linearizing the transfer characteristic of the Q_2/Q_4 inverter around its operating point P.

with

$$V_r = V_s - \left(\frac{r}{r+1}\right)V_T \tag{B10}$$

$$k = \left(\frac{r}{r+1}\right)\left\{\sqrt{\frac{r+1}{r+1-V_s^2/V_r^2}} - 1\right\} \tag{B11}$$

and

$$V_0 = kV_s + \left(\frac{1+r}{1+r+r/k}\right)V_r. \tag{B12}$$

Next we eliminate V_{DS2} from (B7) and (B9). After simplifying, we obtain

$$X^2\left(1+2k+\frac{r}{q}k^2\right)+2X\left(\frac{r}{q}kA+A+V_T-V_s\right)+\frac{r}{q}A^2=0 \tag{B13}$$

where, for simplicity, we have defined

$$\left.\begin{aligned} X &= V_{DD}-V_n-V_{GS2} \\ A &= V_0+(k+1)V_n-kV_{DD}-V_T \end{aligned}\right\}. \tag{B14}$$

As in Appendix A, we now apply the double-root stability criterion to (B13). Next we substitute (B14), and finally solve for V_n to obtain the SNM:

$$\mathrm{SNM}_{6T} = V_T - \left(\frac{1}{k+1}\right)\left\{\frac{V_{DD}-\dfrac{2r+1}{r+1}V_T}{1+\dfrac{r}{k(r+1)}} - \frac{V_{DD}-2V_T}{1+k\dfrac{r}{q}+\sqrt{\dfrac{r}{q}\left(1+2k+\dfrac{r}{q}k^2\right)}}\right\}. \tag{B15}$$

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