

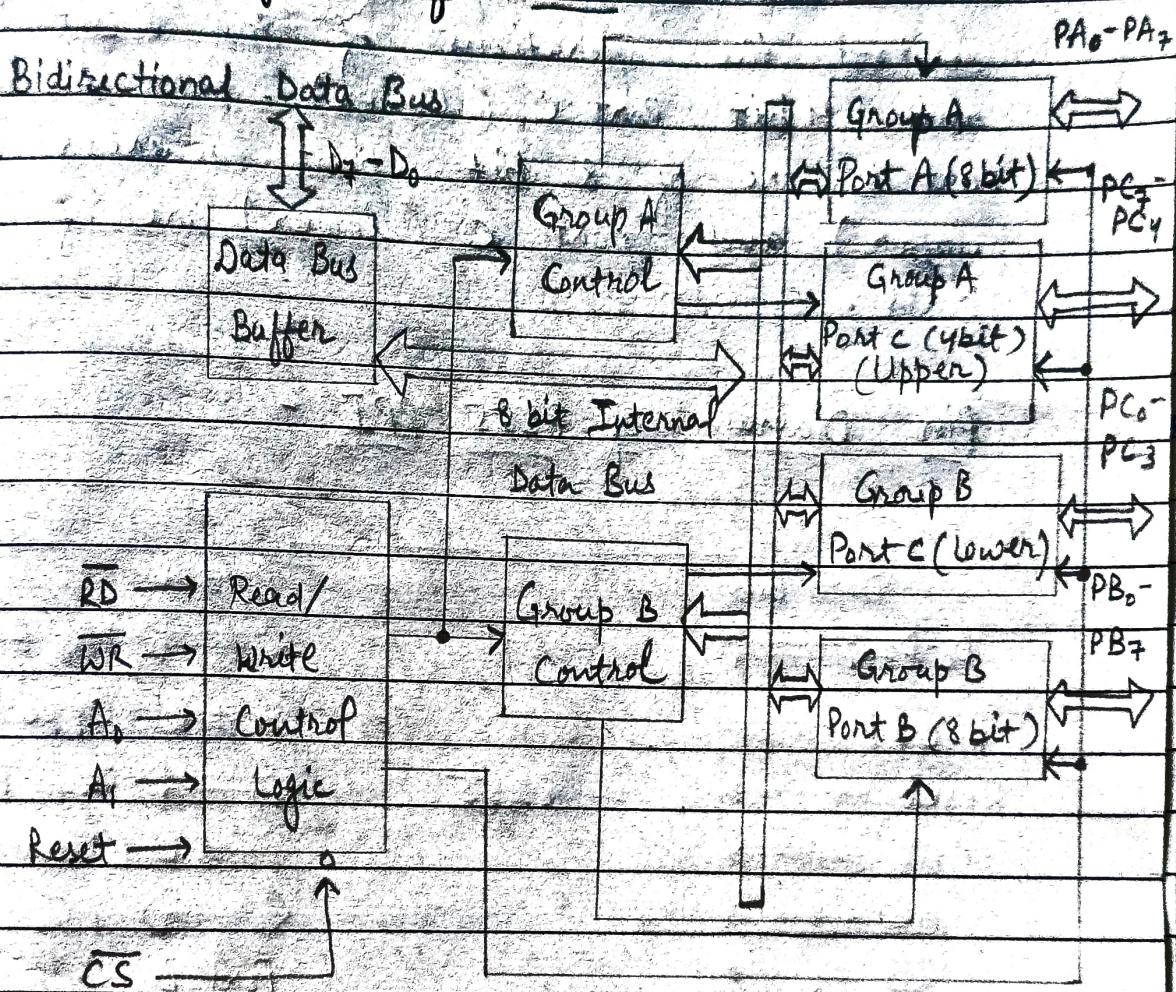
Assignment No. 8

Ques-1

Draw the Pin and block diagram of 8255 PPI and explain the same.

Ans -

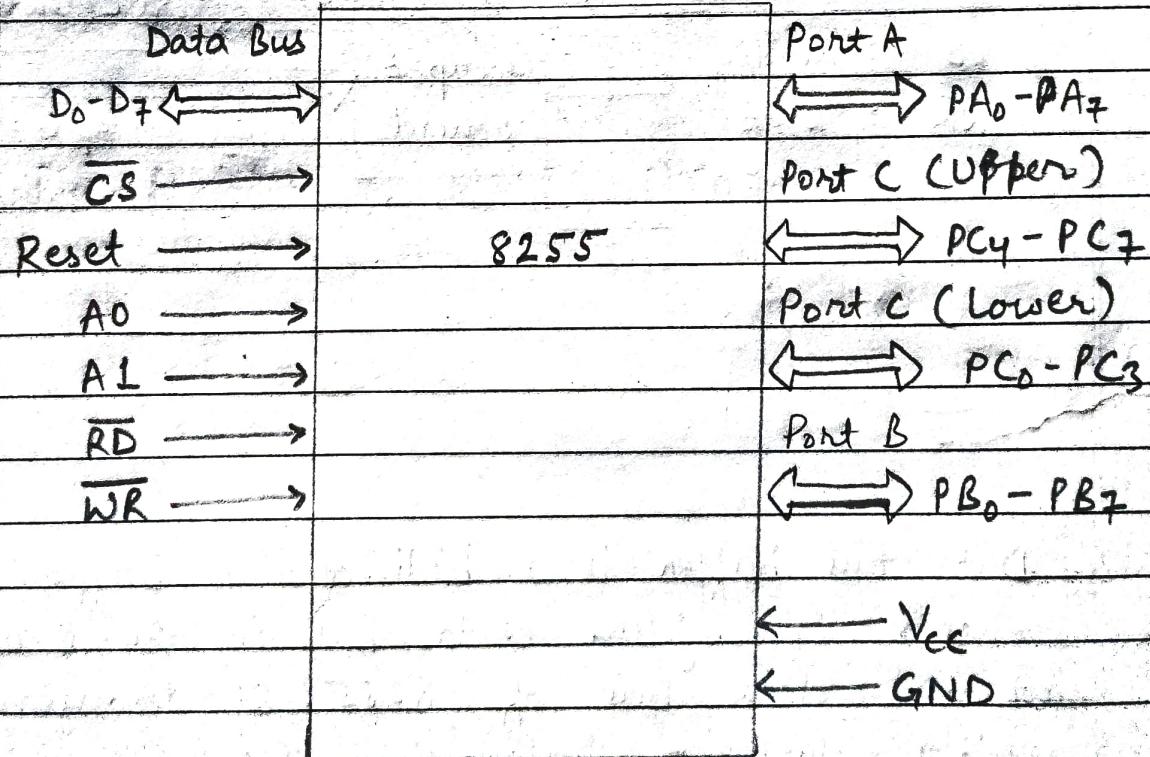
Block Diagram of 8255



Data bus buffer is a bidirectional buffer. It connects the system data bus to the 8 bit internal data bus of 8255. It transfers or receives data or instructions to or from the microprocessor. Read / Write control logic block controls the internal and external transfer.

of data. The signals RD, ADO, AD1, A0, A1, CS and reset are associated with this block. Group A control block receives commands from Read / Write control logic unit depending upon the control word. It controls the operation of Port A (8 bit) and Port C (upper) 4 bit. Group B control unit receives the commands from Read / write control logic and control the operations of the 8 bit port B and 4 bit Port C (lower). Port A and Port B are of 8 bit port whereas Port C (upper) and Port C (lower) are of 4 bits ports.

Pin Diagram of 8255 PPI -



Pin Names -

D ₇ -D ₀	→ Data Bus
CS	→ Chip Select
Reset	→ Reset Input
A ₀ , A ₁	→ Port Address
RD	→ Read input
WR	→ Write input
PA ₇ -PA ₀	→ 8 bit Port A
PC ₄ -PC ₇	→ 4 bit Port C (upper)
PC ₀ -PC ₃	→ 4 bit Port C (lower)
PB ₀ -PB ₇	→ 8 bit Port B
V _{cc}	→ +5V
GND	→ 0V

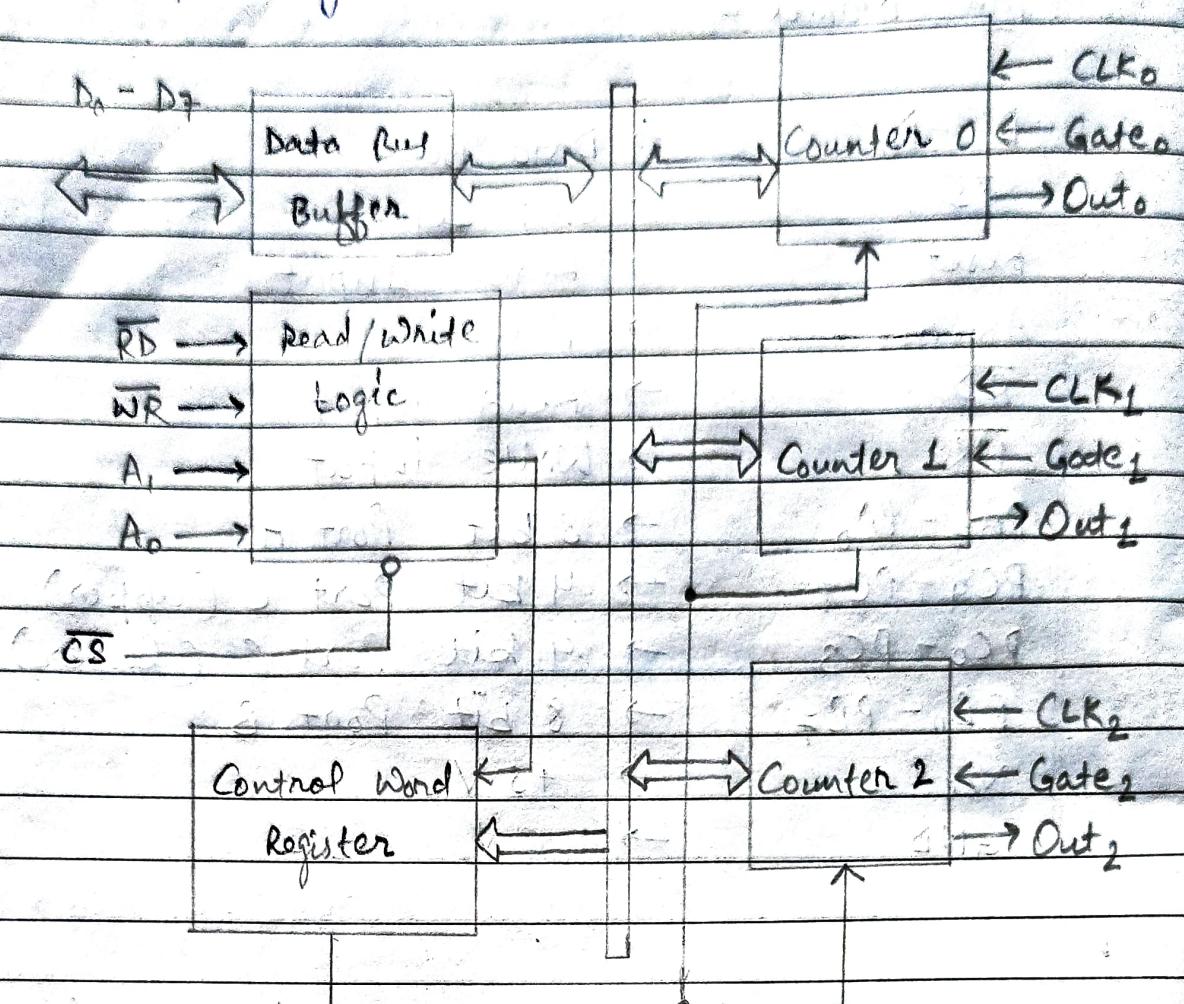
Ques-2 Draw the Pin and Block diagram of 8253 PIT and explain the same.

Ans -

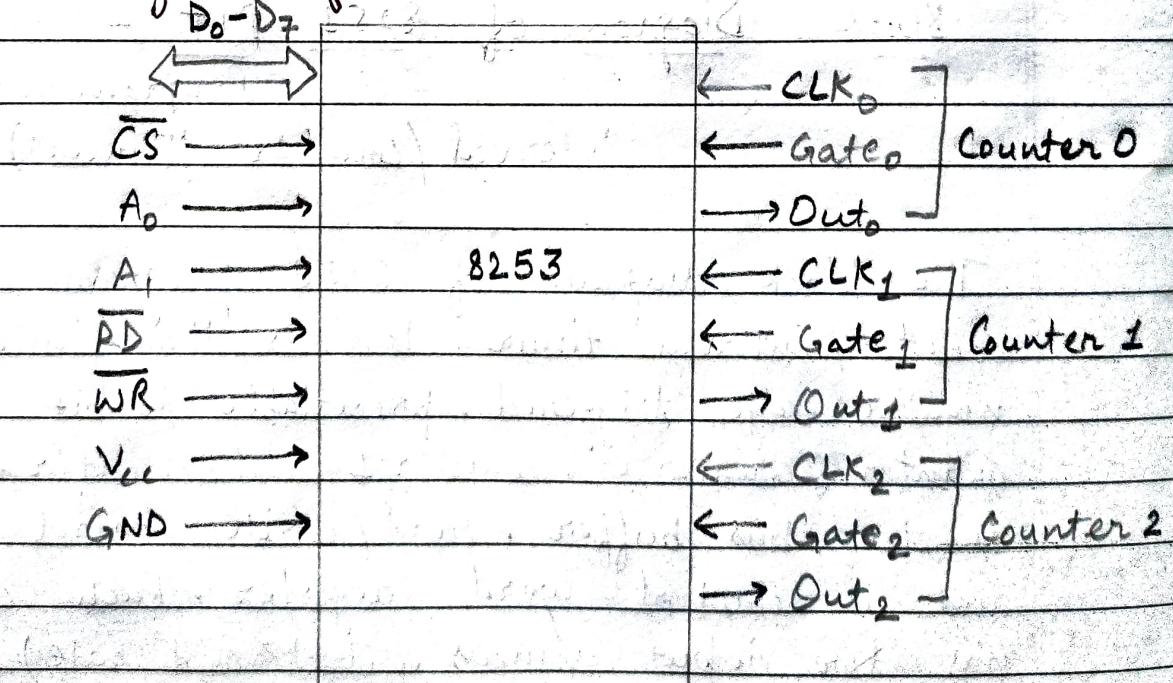
Block Diagram of 8253 PIT -
 (Programmable
 Interval Counter Timer)

The block diagram of 8253 programmable counter/interval timer. It has three independent negative edge triggered, presetable 16 bit down counters (counter 0, counter 1 and counter 2), a data bus buffer, read/write control logic and a control word register. Each counter has two input signals, (clock and gate) and

one output signal.



Pin Diagram of 8253 PIT -



$D_0 - D_7$

→ Bidirectional data bus

\overline{CS}

→ Chip Select

A_0, A_1

→ These pins are connected to the address bus. These are also used to address the control word register for mode selection.

\overline{RD}

→ When the signal on this pin is low, the CPU reads data.

\overline{WR}

→ When the signal on this pin is low, the CPU writes data or loads the counters.

CLK_0, CLK_1, CLK_2 → There are clock input for the counter 0, counter 1 and counter 2.

$Gate_0, Gate_1, Gate_2$ → These are the gate terminals of counter 0, counter 1 and counter 2.

Out_0, Out_1, Out_2 → These are the outputs of counter 0, counter 1 and counter 2.

8257

Ques-3 Draw the Pin and block diagram of ~~8255~~ DMA and explain the same.

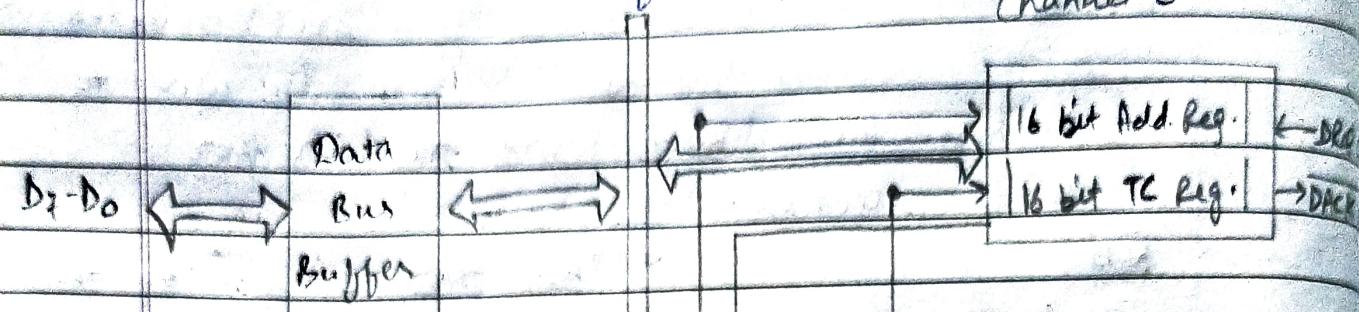
Ans -

Block Diagram of 8257 DMA Controller -

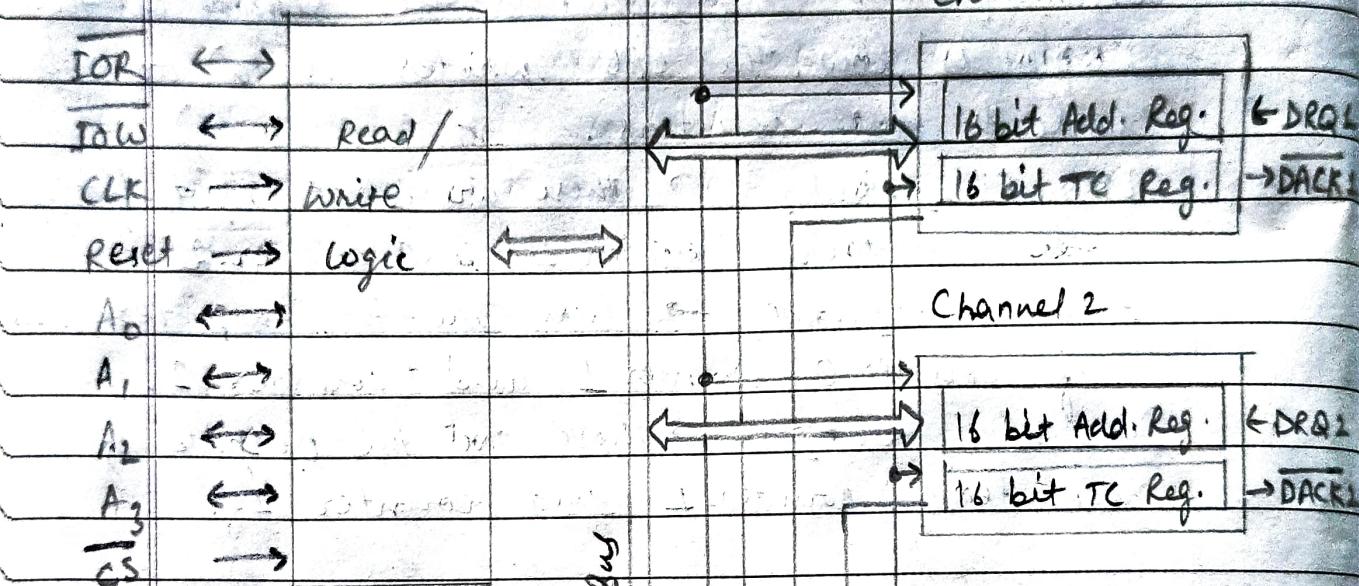
The 8257 is a programmable 4 channel DMA controller (Direct Memory Access) Controller which allows upto four I/O devices to access memory without involving the microprocessor. It is designed simply to

transfer the data at high speed for the microprocessor system. It can be interfaced with slow or fast peripherals.

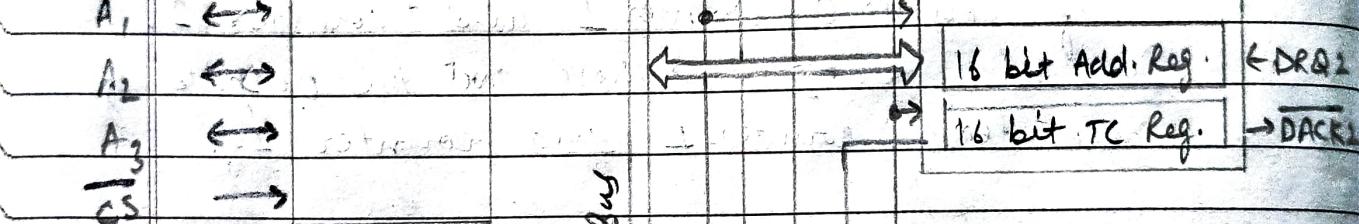
channel 0



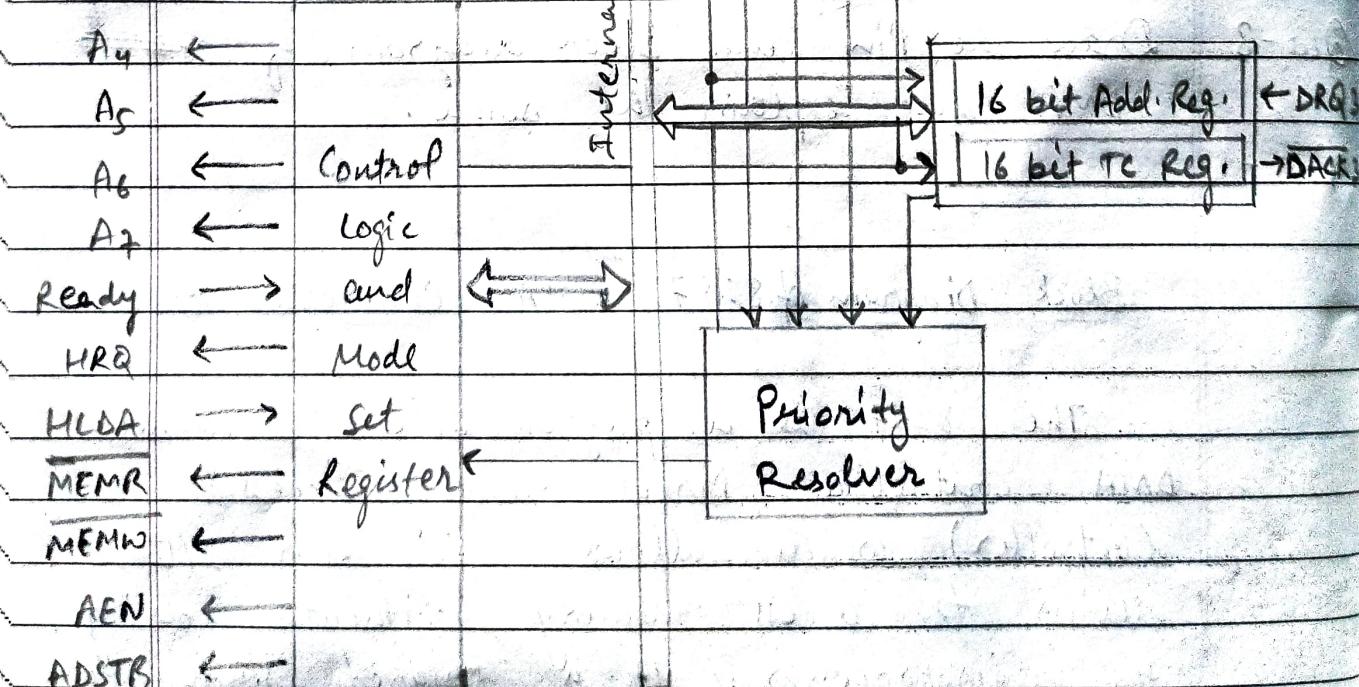
Channel 1



Channel 2



Channel 3



Pin Diagram of 8257 DMA Controller -

<u>IOR</u>	1	40	A ₇
<u>IOW</u>	2	39	A ₆
<u>MEMR</u>	3	38	A ₅
<u>MEMW</u>	4	37	A ₄
MARK	5	36	T _C
READY	6	35	A ₃
HLDA	7	34	A ₂
AD STB	8	33	A ₁
ACN	9	32	A ₀
HREQ	10	8257	Vcc
<u>CS</u>	11	31	D ₀
CLK	12	29	D ₁
Reset	13	28	D ₂
<u>DACK₂</u>	14	27	D ₃
<u>DACK₃</u>	15	26	D ₄
<u>DRQ₃</u>	16	25	<u>DACK₀</u>
<u>DRQ₂</u>	17	24	<u>DACK₁</u>
<u>DRQ₁</u>	18	23	D ₅
<u>DRQ₀</u>	19	22	D ₆
GND	20	21	D ₇

IOR → I/O Read

IOW → I/O Write

MEMR → Memory read

MEMW → Memory write

MARK → This output notifies the selected

peripheral that the current DMA cycle is the 28th cycle since the previous mark output.

READY → Ready signal

HLDA → Hold Acknowledge

AD STB → Address strobe

ACN → Address Enable

HRQ → Hold Request

CS → Chip Select

CLK → Clock input

Reset → Input signal which disables all DMA channels by clearing the mode register and tristates all control lines.

DACK₃ - DACK₀ → DMA Acknowledge

DRQ₃ DRQ₃ - DRQ₀ → DMA request input

D₇ - D₀ → Data bus

A₇ - A₀ → Address bus

TC → Terminal count.