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Assignment No. 6

Que-1 Explain maskable and non-maskable interrupts of 8085.

Ans-

Maskable Interrupt :-

In this type of interrupt, we can disable the interrupt by writing some instructions into the program. E.g. RST 7.5, RST 6.5, RST 5.5.

Non-Maskable Interrupt :-

In this type of interrupt, we cannot disable the interrupt by writing some instructions into the program. E.g. TRAP.

Que-2 Explain Software and hardware interrupts of 8085.

Ans-

Software Interrupt :-

Interrupts which can be initiated through programs are called software interrupts. RST stands for restart. External hardware is required to insert an RST instruction when INTR interrupt is requested.

There are 8 software interrupts, RST0 to RST 7. These are single byte instructions. When any of these instructions are executed, a ~~CALL~~ CALL to the specified address is executed.

Interrupts	Hex code	Vector Address
RST 0	C7	0000
RST 1	CF	0008
RST 2	D7	0010
RST 3	DF	0018
RST 4	E7	0020
RST 5	EF	0028
RST 6	F7	0030
RST 7	FF	0038

Hardware Interrupt :-

These interrupts are initiated by the hardware. In 8085, only external hardware initiated interrupts are there.

These 8085 microprocessor has 5 interrupts named as TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR. An interrupt vector is a pointer to the memory location where the Interrupt service Routine (ISR) is stored. All interrupts are bad mapped into a memory area called Interrupt vector table. The interrupt vectors of 8085 interrupt are -

Interrupt	Vector address in Hex
TRAP	0024
RST 5.5	002C
RST 6.5	0034

RST 7.5	003C
INTR	

Que-3 Explain vectored and non-vectored interrupts of 8085.

Ans -

Vectored Interrupts :-

The interrupts for which the address of the ISR is fixed are called vectored interrupts. The interrupting device need not to supply the address of the ISR.
E.g. TRAP, RST 6.5, RST 5.5.

Non-vectored Interrupts :-

The interrupts for which the address of the ISR is not fixed are called non-vectored interrupts. Address of the ISR is required to the supplied externally by the device. E.g. INTR.

Que-4 Explain edge triggered and level triggered interrupts.

Ans -

Edge Triggered Interrupts :-

If the interrupt is recognized by the microprocessor only when the interrupt input signal changes its level, then such interrupts are called

edge triggered interrupts. A positive edge triggered interrupt is recognized when the its input signal level changes from low level to high level. Similarly, a negative edge triggered interrupt is recognized when its input signal level changes from high to low level.

Level Triggered Interrupts :-

If the interrupt is recognized by the microprocessor when the interrupt signal input signal stay at logic high level for some particular time period, then such interrupts are called level triggered interrupts. e.g. INTR.

Que-5 Explain TRAP, RST 7.5, RST 6.5, RST 5.5, ~~RST 7.5~~, INTR in detail.

Ans -

TRAP :

The interrupt TRAP has the highest priority. It is non-maskable interrupt and need not be enabled. It can not be disabled. It is level and Edge sensitive. It means that the input should change from low level to high level and then stay high for one instruction time period (can to be acknowledged).

RST 7.5 :

RST 7.5 has the second highest priority. It is maskable and positive edge triggered interrupt. The RST 7.5 interrupt request is stored internally by D flip flop. Thus the interrupt signal is not required to remain high till acknowledged. The D flip-flop is reset by either R7.5 bit of SIM, RESET IN signal or internal RST 7.5 acknowledge signal.

RST 6.5 and RST 5.5 :

These are maskable interrupts. These interrupts has the lower priority than TRAP and RST 7.5. Both these interrupts are level sensitive. They can be enabled by SIM instruction. Vector address for RST 6.5 is 0034 H and RST 5.5 is 002C H.

INTR :

INTR interrupt is maskable and it has the lowest priority. During the execution of each instruction, the microprocessor checks INTR. If it is high then the microprocessor complete its current operation and sends an interrupt acknowledgement signal $\overline{INTA}$ active low.

* Priority of Interrupts -