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2nd Sessional

4th Semester / Computer Engg.

Subject: Microprocessor and Peripheral Devices

Sec-A

Ans-1

i) & ii) Explain the following instructions of 8085 as under -

Sr. No.	Syntax	Example	Length	Addressing Mode	Description
1.	LDAX B/D	LDA B	3 Bytes	Register Addressing Mode	Load from register pair to accumulator
2.	SHLD	SHLD 2050	3 Bytes	Direct Addressing Mode	Stores the contents of H-L register pair in the memory location specified by address.
3.	ADI 8 bit data	ADI 41H	2 Bytes	Immediate Addressing Mode	Add immediate to the accumulator.

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4.	SBB M	~~SBB M~~ SBB 2050	1 Byte	Indirect Addressing Mode	Subtracts memory with borrow from accumulator.
5.	RRC	RRC	1 Byte	Implied Addressing Mode	Rotate the accumulator to the right.
6.	JNC 16 Bit Address	JNC AHEAD	3 Bytes	Implied Addressing Mode	Jumps to the label if no carry is generated.

iii) Instruction format of 8085 :-

As we know that instructions are not of same that is why these are differentiated into three different parts -

a) One byte Instructions
b) Two byte Instructions
c) Three byte Instructions

a) One byte -

these have the opcode and operand of same byte. The length of machine codes in this is one byte.

e.g. MOV, ADD, etc.

b) Two Byte -

In this, the first byte consists of opcode and second byte is the operand.

e.g. MVI.

c) Three Byte -

In this, the first byte is the opcode and second and third are the 16 bit address.

e.g. JMP.

iv) Addressing Modes of 8085 are -

The various techniques that specifies the address of data in an instruction are known as addressing modes. There are five types of addressing modes -

- Immediate Addressing Mode
- Register Addressing Mode
- Direct Addressing Mode
- Indirect Addressing Mode
- Implied Addressing Mode

vi) Maskable and Non-maskable Interrupts of 8085 :-

• Maskable Interrupt :

Maskable interrupts are generally the interrupts which can be ignored it means that the processor can continue with the process it is working on without worrying about it.

E.g. INTR, ~~RST 5.5~~, etc.
RST 7.5

• Non-maskable Interrupt :

Non-maskable interrupts are the type of interrupts which cannot be ignored by the processor are Non-Maskable Interrupts.

These interrupts have to be taken in consideration by the processor and queue them or either work on it immediately depending upon its priority.

E.g. TRAP.

~~(TRAP has the~~
(TRAP is the most prioritied amongst all others).

Sec - B

Ans-3 Difference between Peripheral Mapped I/O and Memory Mapped I/O :-

	Peripheral Mapped I/O	Memory Mapped I/O
i)	These cannot be accessed like other memory locations.	i) These can be accessed like memory locations.
ii)	These are designed for 8-bit address values.	ii) these are designed for 16-bit address values.
iii)	IN and OUT are the instructions used in this.	iii) LDA and STA are the instructions used in this.
iv)	Cycles involved are- IO read and IO write.	iv) Cycles involved are- ~~IO read~~ Memory read and Memory write.
v)	Only the accumulator can communicate in this case.	v) Any register can communicate in this case.

vi) 256 IO ports are available in this.	vi) In this, 256 ports are available.
vii) IO/$\overline{M}$ = 1, during writing or read cycles.	vii) IO/$\overline{M}$=0, during writing or read cycles.
viii) Some special control signals are used in IO in Peripheral mapped.	viii) No special control signals required in Memory mapped IO.
ix) Arithmetic and Logical operations cannot be performed directly in the case of Peripheral Mapped IO.	ix) Arithmetic and Logical operations can be performed directly in case of Memory mapped IO.
x) In this, less data space is available.	x) In this, more data space is available.