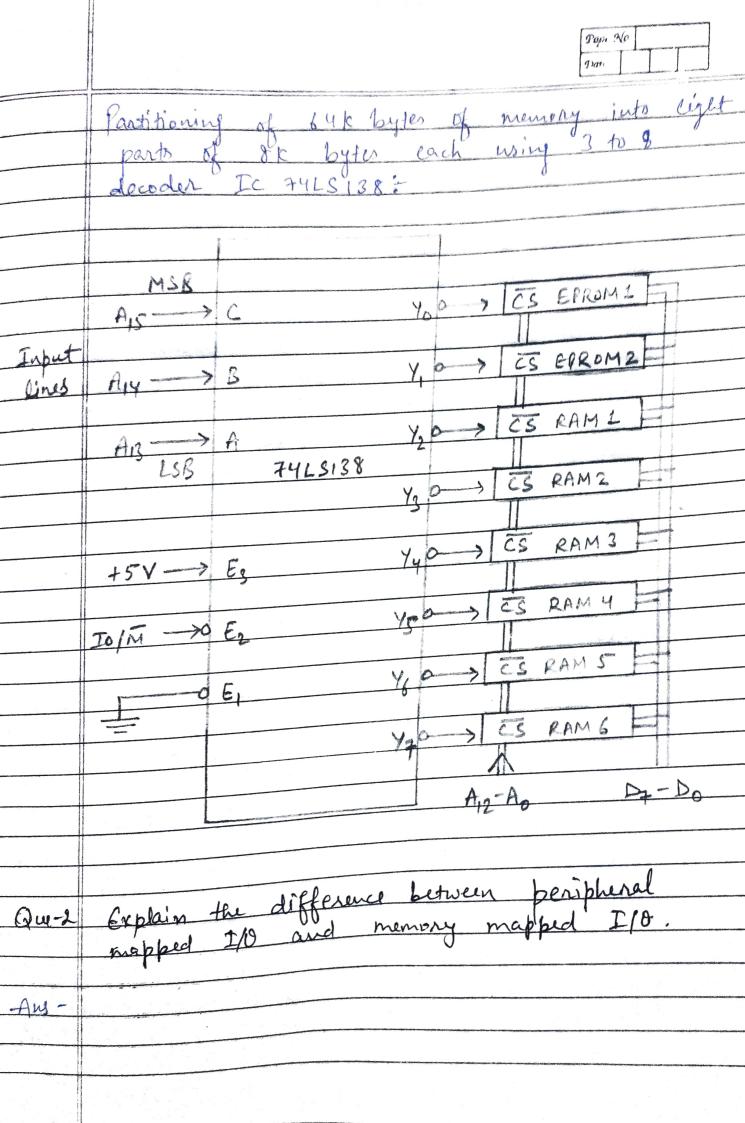
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	Assignment No. 5
Que-1	Explain the concept of memory mapping, partitionly of total memory space of 8085.
	Memory Mapping of 8085 - Memory interfacing is used
	to provide more memory space to accontemodate complex program for more complicated systems. Types of memories which are most commonly
	and ff PROM. 8085 can access 64kb of external memory. It can be explained as - total number
	it can access e'16 = 65535 locations j-e. 64 kg.
	where n = number of memory locations where n = number of address lines
	Partitioning of total memory space of 8085. The 8085 microprocessor has 16 address lines.
	So, it can address a total of 216 = 64 k memory locations, Since 8085 hows 8 bit data lines, so each memory location can be of 8 bit. Thus
	each memory location can be of 8 bit. Thus a total of 64k bytes of memory can be connected to the 8085 microprocessor. The
	is 0000H to FFFFH.



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	Peripheral Mapped I/O	Memory Mapped I/o
·	They are although with 8 lost	· They are designed with
	soldres values.	16-bit address values.
1	They cannot be accessed	· ID devices are accessed
	like any other numbry	like any other memory
Company of the Company	location.	location.
MARIN STREET,	The instruction used are	· The Instruction used are
Tites o resist resistant consequen	IN and DUT.	LDA and STA etc.
Para de la companya d	Cycles involved during	· Cycles involved during
	operation are ID read	operation are memory
Total Brokenson	and ID write in the	head and Memory white.
•	case of 10 Mapped 10.	
The same of the sa	Duly accumulator can	Any register con
	communicate with TO	communicate with the
	devices in case of 20 Mapped 20.	DO device in case of
	Only 256 to ports are	Memory Mapped 10. 216 Do ports are possible
	available for interfacing	to be well don't love by
	in case of ID Mapped	to be used for interfacing
	10.	mapped to.
•	During writing or read	· During withing or read
	Lyder (PAIM = 1)	cycles (10/M=0).
	Special control signals are	No separate si control
	used in this.	signal required in this.
6	Arethmetic and logical	Arithmetic and logical
	operations cannot be	pleastion are beaterned
the content of the latest self-self-self-self-self-self-self-self-	performed directly on the	directly on the data
	data in the case of	in the case of Memory
	Is Mapped Io.	Mapped Io.

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Qu-3	Explain interfacing of memory napped Io	
Ans -	Interfacing Memory Mapped I/O device:	
	An input/output device when connected of a nicroprocessor in memory mapped I/O scheme, it has 16 bet address, IO/M	0
	signal is low, MEMR/MEMW signal are used for head-write operations. Thigh-order Address Bus Device Device	10 / Officero - Seminario - Annie - An
8085	Aug-As row order Address Address	- Contract
_µР АД	ALE Bus Decoder Tri-state EN EN -ADo Tri Latches 8 Decoder Tri-state EN Buffer FD Lotel	1
10/M	RD WR	_
	Cinemit MEMW	
IOR	The logic circuit generates MEMR (memory Read)	
	and MEMN (memory white) signals from IO/M, RD and WR signals of the microprocessor. MEMR is activated when IO/M signals is low	

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- Acceptance	
	and RD is active. Similarly, MEMIN is activated. ALE signal is used to pensultiplex low-orders address and data bus. Address decoder circuit
-	ALE signal is used to pensagipus bow order circuit
	activates address line of the Input Coutput device for a particular 16-bit address.
-	device for a particular 16-bit address.
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