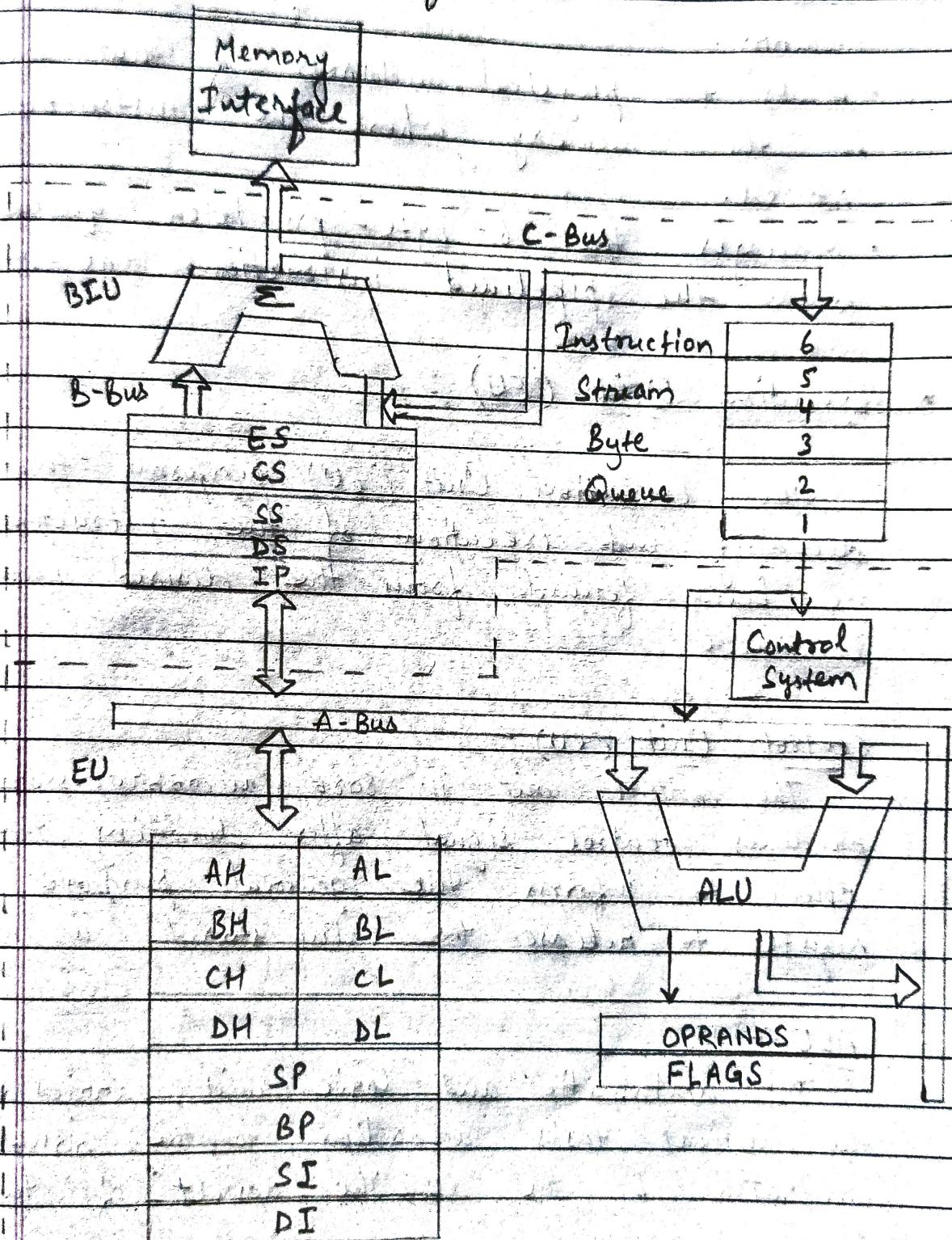


Assignment No. 9

Que - 1 Draw and explain the block diagram of 8086.

Ans -

Block Diagram of 8086 :-



* Bus Interface Unit : (BIU)

The Bus Interface Unit (BIU) manages the data, address and control buses.

- The BIU functions in such a way that it:
 - fetches the sequenced instruction from the memory.
 - finds the physical address of that location in the memory where the instruction is stored.
 - Manages the 6-byte-pre-fetch queue where the pipelined instructions are stored.

* Execution Unit (EU) :

The Execution Unit (EU) performs the decoding and execution of the instructions that are being fetched from the desired memory location.

Control Unit (CU) -

The control unit in 8086 microprocessor produces control signal after decoding the opcode to inform the general purpose register to release the value stored in it.

ALU -

The arithmetic and logic unit carries out the logical tasks according to the signal generated by the CU. The result of the

operation is stored in the desired register.

Flag Register -

Here the flag register holds the status of the result generated by the ALU. It has several flags that show the different conditions of the result.

Temporary Register -

It is a temporary register and is used by the processor to hold the temporary values at the time of operation.

Ques-2 Draw and explain the Pin diagram of 8086.

Ans -

PIN DIAGRAM of 8086 -

AD₀ - AD₁₅ → Multiplexed Address / Data Bus

A₁₆ - A₁₉ → Multiplexed Address / Status Bus

S₃ S₇

BHE / S₇ → Bus High Enable

RD → Read Operation

READY → Peripheral is ready to transfer data

RESET → System Reset

CLK → 5.8 or 10 MHz

INTR → Interrupt Request

NMI → Non-Maskable Interrupt

TEST → when low, ^{operation} continues execution
otherwise wait

V_{CC} → +5V , GND → Ground .

			40	→ Vcc +5V
N _S GND	—	1	39	↔ AD15
AD ₀ -AD ₁₄	↔	2-16	38	→ A ₁₆ /S ₃
			37	→ A ₁₇ /S ₄
			36	→ A ₁₈ /S ₅
		Intel	35	→ A ₁₉ /S ₆
		8086	34	↔ BHE/ST
			33	→ MN/MX
NMI	→	17	32	→ RD
			31	↔ HOLD RQ/GT ₀
			30	↔ HLDA RQ/GT ₁
INTR	→	18	29	→ WR LOCK
			28	→ M/IO S ₂
CLK	→	19	27	→ DT/R S ₁
			26	→ DEN S ₀
			25	→ ALE QS ₀
			24	→ INTA QS ₁
V _S GND	←	20	23	← TEST
			22	← READY
			21	← RESET

Que-3 Explain the Maximum and Minimum mode of 8086.

Ans -

Operating Modes of 8086 - Minimum Mode

Control Signals, Memory & I/O ← Microcomputer System

Maximum Mode \rightarrow Multiprocessor system
 (8298 Bus controller is used with 8086)

(Pin 33) $MV/MX \Rightarrow$ pins 24 to 31 have alternate functions

* Pin description for Minimum mode (24-31)

INTA (Output) - Interrupt Acknowledge

ALE (Output) - Address latch enable - latch Address

DEN (Output) - Data enable - Output Enable

DT/R (Output) - Data Transmit / Receive

M/I/O (Output) - Memory / I/O

WR (Output) - Write operation

HLD (Output) - Hold Acknowledgement

HOLD (Input) - Another device wants to use the address / data bus of microprocessor.
 (MP)

* Pin description of Maximum mode

(Output) Q_S, Q_{S0} (Instruction Queue Status)

0 0 - No operation

0 1 - 1st byte of opcode from queue

1 0 - Empty the queue

1 1 - Subsequent byte from queue.

(Output) S_2, S_1, S_0 (Connected to the 8288 bus controller)

Logic for Status Signal 3

0 0 0 - Interrupt Acknowledgement

0 0 1 - Read data from I/O Port

- 0 1 0 - write data on I/O port
- 0 1 1 - Halt
- 1 0 0 - opcode fetch
- 1 0 1 - memory fetch read
- 1 1 0 - memory read write
- 1 1 1 - memory passive state

LOCK (OpP) - All interrupts are masked & no HOLD requested ~~nor~~ granted.

RQ/GT₁ & RQ/GT₀ (bidirectional) - Local Bus Priority control.