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3rd Sessional
4th Semester / Comp. Engg.
170844
Subject: Microprocessor and Peripheral Devices

Sec - A

Ans - 1

i) Data Transfer:

Data transfer is basically the transfer of data between microprocessor during execution of a program.

⇒ Data transfer is needed in computers so that data can be transferred from memory to I/O device or microprocessor and vice versa.

Types of Data Transfer Schemes are:-

a) Programmed Data transfer Scheme.
- Synchronous Mode
- Asynchronous Mode
- Interrupt Mode

b) DMA (Direct Memory Access) mode of Data Transfer
- Burst mode of DMA
- Cycle mode of DMA

ii)

Parallel Data Transfer Schemes	Serial Data Transfer Schemes
• In this, data is	• In this, data is

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transferred parallely.	transferred serially.
• Transmission rates of data are higher.	• Data transmission rates are lower.
• It needs more number of microprocessors.	• It needs less number of microprocessors. (mostly 1)
• It is costly.	• It is cheaper.
• It is faster.	• It is comparatively slower.

iii) Serial Data Transfer Techniques -

Data transfer can be of two types either parallel or serial. In Serial Data Transfer mode, the data is transferred bit by bit over a single channel. Serial transmission has less chances of errors. It involves less microprocessors (mostly 1).
Serial Data transfer is convenient for data of less bits but for big byte data parallel data transfer is good.

⇒ Serial Data Transfer Techniques -

a) Serial Input Data (SID)
b) Serial Output Data (SOD)

iv) Interrupt Driven I/O Transfer Scheme -

In this type of data transfer, CPU doesn't sit doing nothing. At In this, whenever the I/O device have to read/write data and memory is not available at that moment then the CPU issues a command for I/O interrupt in the system and CPU goes to do other works. This is known as Interrupt driven I/O transfer scheme.
It consists of different schemes -

a) Several I/O devices connected to single interrupt level
b) One I/O device connected to each interrupt level
c) More than one I/O device connected to each interrupt level

v) Direct Memory Access (DMA) :-

In DMA, a DMA controller is used which out offs the involvement of CPU during data transfer during program execution.
In this the CPU tells some of the details (about what I/O device needs) and goes back to other works of it. After that DMA read/write the data from/into memory that is from I/O device respectively.

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a) The DMA is of two types -

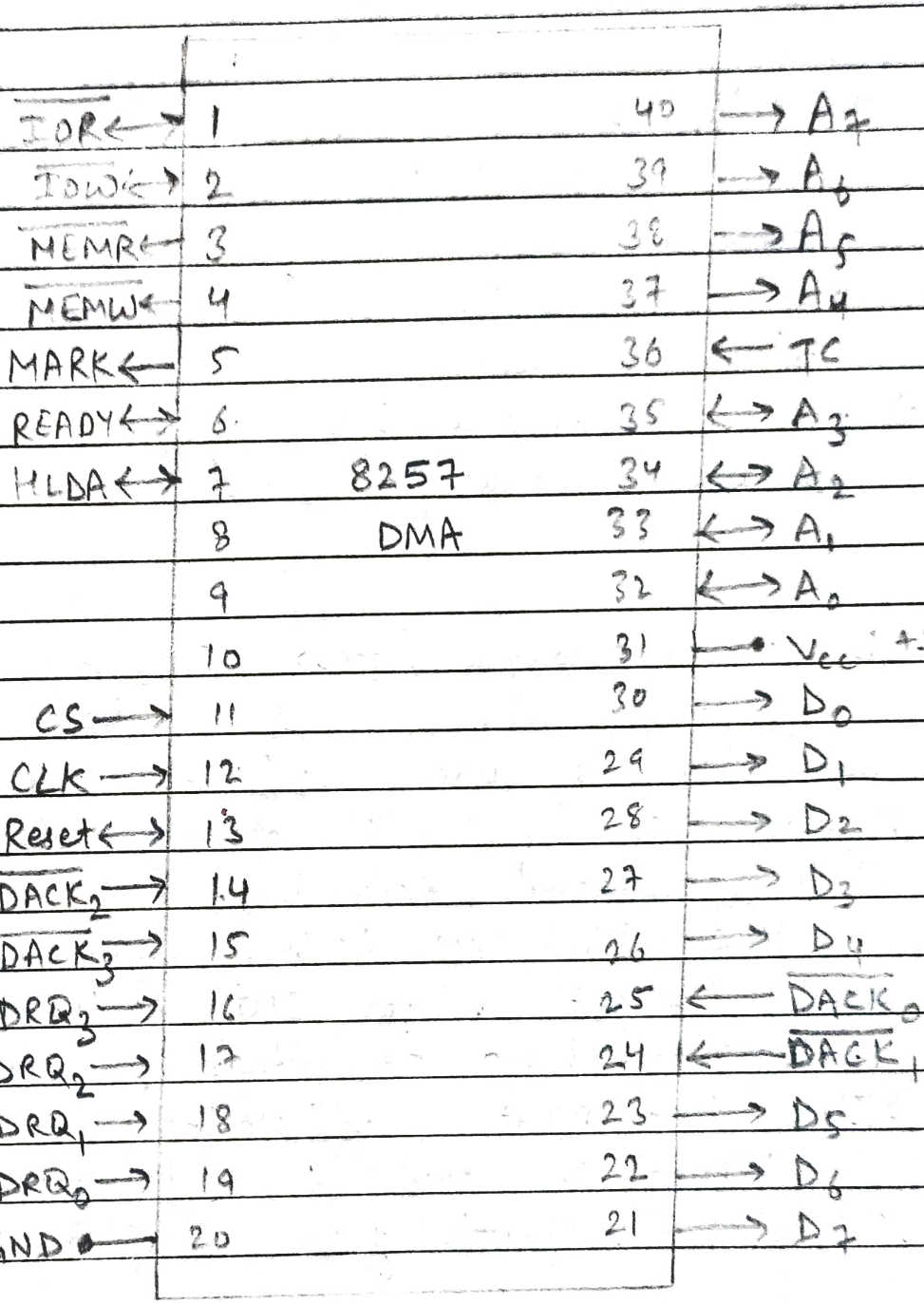
a) Burst mode DMA

b) Cycle mode DMA

Sec - B

Ans-2

PIN DIAGRAM of 8257 DMA :-



PINS :-

- $\overline{IOR}$ → I/O Read. Active low signal. (High when low/0).
- $\overline{IOW}$ → I/O write. Active low signal.
- $\overline{MEMR}$ → Memory read. Active low signal.
- $\overline{MEMW}$ → Memory write. Active low signal.
- READY → Ready signal. Turns on CPU.
- HLDA → Hold Acknowledgement.
- $\overline{CS}$ → chip select.
- CLK → clock signal.
- Reset → Resets DMA.
- V_{cc} → Power supply. +5V
- ~~V_{SS}~~ GND → Ground.
- ~~DREQ$_0$~~
- $\overline{DACK_3} - \overline{DACK_0}$ ⇒ DMA Acknowledgement.
- $DRQ_3 - DRQ_0$ ⇒ DMA Request.
- $D_7 - D_0$ ⇒ Data lines.
- $A_7 - A_0$ ⇒ Address lines.
- TC ⇒ Terminal Count.

* Block Diagram : (is on next page)

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* Block Diagram of 8257 DMA :-