Physics and Technology of Electronic Devices: LABORATORY REPORT

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1 Introduction

The laboratory experience aims to analyse the behaviour of different electronic devices, characterizing their main properties. Knowing the internal structure of each device, it is also possible to simulate their electrical properties, obtaining a reference behaviour with which we can compare the experimental results, verifying the presence of any agreement between the two. The devices analysed are the following:

- Zener Diode;
- *npn* BJT;
- *n*-channel MOSFET.

1.1 Experimental Measurements

All the devices tested are found on the H9T0AA Silicon wafer produced by STMicroelectronics. The zener Diode and the single emitter *npn* BJT are found inside the KC23AA technology module, which is dedicated to parametric testing structures. The Zener Diode is identified by the code TEG7_B0 and its two contacts are identified by the indices 8 and 10 on the column. The single emitter *npn* BJT is identified by the code TEG3_B2 and its Emitter, Base and Collector contacts are identified by the indices 5, 6 and 4 respectively. The *n*-channel MOSFET is found inside the KC23BA technology module, which is dedicated to CMOS modeling structures. It is identified by the code TEG2 (structure 1) and its Source, Drain, Gate and Body contacts are identified by the indices 1, 2, 3 and 21 respectively.
The experimental measurements are carried out via a manual probe station using a 4200 Keithley Semiconductor Characterization System (SCS). Once the device is found on the wafer surface through the use of a microscope, it is possible to create a contact between each device terminal and the conductive tip of the SMU (Source Measure Unit) related to that terminal, using appropriate

micro-manipulators that allow for microscopic movements of the tip itself. Once every necessary contact is created, each SMU is programmed, using the software Clarius, in order to force a certain voltage (or current) to its respective device terminal, while it measures the current passing through it (or its voltage). In this way it is possible to carry out I-V measurements, paying attention to turn off the lights in order to avoid any significant carrier photogeneration inside the tested device.

1.2 Electronic Simulations

The simulation of the electronic devices are carried out via the software TCAD (Technology Computer-Aided Design). Of paramount importance in the simulation process are the following aspects:

- Domain definition;
- Boundary conditions;
- Dopant distribution;
- Refinement criteria.

These information are used as input data for the first step of the device simulation, implemented through the software Sentaurus Structure Editor (SSE). Once the physical structure of the device has been generated, it undergoes a discretization and meshing process of each domain, via SNMESH. Then the device behaviour has been simulated through SDEVICE, and the results displayed via the software SVISUAL.
From the simulation process we obtain as outputs the electric characteristics of each device terminal (voltage and current), local temperature, electric potential and charge distribution.

2 Zener Diode

The diode is a two-terminal semiconductor device based on the physical working principle of the PN junction, which consists of an interface realized with two oppositely doped semiconductors. Inhomogeneity in the carrier concentration between the two regions causes carrier diffusion of majority carriers across the junction. Diffusion and bipolar recombination on both sides of the junction causes the formation of a depletion region, where no mobile carriers are found. For this reason an array of fixed ionized impurities is exposed in this region adjecent to the interface, with positively ionized donors on the N-side and negatively ionized acceptors on the P-side. The presence of a charge distribution in the depletion layer causes the establishment of an electric field that induces carrier drift in the opposite direction with respect to diffusion. At equilibrium no current flow is recorded and the Fermi level is constant throughout the junction. Due to the presence on the electric field in the depletion region we observe

the development of a Built-In voltage V_{bi} across the junction. This device finds an important place in several everyday applications, due to the very specific I-V trend that characterizes it.

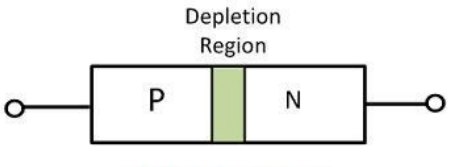

Figure 1: *PN* Junction Diode

It is possible to distinguish two different regions of operation:

- FORWARD BIAS: the p-doped region is held at a higher voltage than the n-region. The eternal field causes a decrease of the depletion layer width and potential barrier height, favouring diffusion of carriers across the junction.
- REVERSE BIAS: the p-doped region is held at a lower voltage than the n-region. The eternal field causes an increase of the depletion layer width and potential barrier height. This reduces the diffusion contribution to the current, leaving only the minority carrier drift current (which is limited by the small concentrations of minority carriers).

Depending on the sign of the applied voltage at the terminals of the diode, two different electrical behaviours can be observed.
The general ideal diode I-V characteristic is described by the Shockley Model

$$I = I_0(e^{\frac{qV_A}{nkT}} - 1), \tag{1}$$

where I_0 is the reverse saturation current, V_A is the applied woltage bias and n represents the ideality factor of the diode and define how close the behavior of the device is to the ideal one. In the ideal diode we assume that no carriers are found in the depletion region and no recombination processes happen in the depletion region. In a real diode lots of different phenomena enter in the functioning of the device, causing the I-V characteristic to deviate from the expected trend, such as recombination processes (important at low voltage bias), that translates into an ideality factor value close to 2. With higher voltage, close to the built-in tension V_{bi} one should also consider other effects, such as high-level injection and series resistance effect, which translates into a sub-linear behavior with respect to the ideal one. If used in a reverse bias configuration, an ideal diode tends to prevent current from flowing through the junction (the depletion region gets thicker), therefore showing a flat valued I-V characteristic at $-I_0$, due to minority carrier drift. Realistically this is not the case since the behavior will be influenced by the presence of carrier thermal generation and recombination phenomena that will cause the reverse low voltage bias current to increase with the reverse voltage bias. Another important parameter in

this configuration is the breakdown tension V_{br}, that represents a threshold value over which Avalanching (carrier production due to impact ionization of atoms with accelerated carriers in the depletion region) and Zener effect (carrier tunneling from one region to the other in heavily doped junctions under reverse bias conditions) take place, causing the current to quickly diverge. This last feature is commonly exploited in Zener diode applications which are usually used as voltage regulators in electronic circuits.

2.1 Results and analysis

The objective of the experimental investigation is to measure the I-V characteristics of the Zener diode and determining the breakdown voltage V_{br}, the inverse saturation current module I_0, the diode series resistance R_S and the ideality factor n.
We measure I as a function of V (which is increased from -6.5 to $1\,V$ in $50\,mV$ steps). hence showing the Zener diode behavior in both forward and reverse bias configurations. The detected I-V trend is represented in Fig.2, together with the results of the simulation in the same interval.

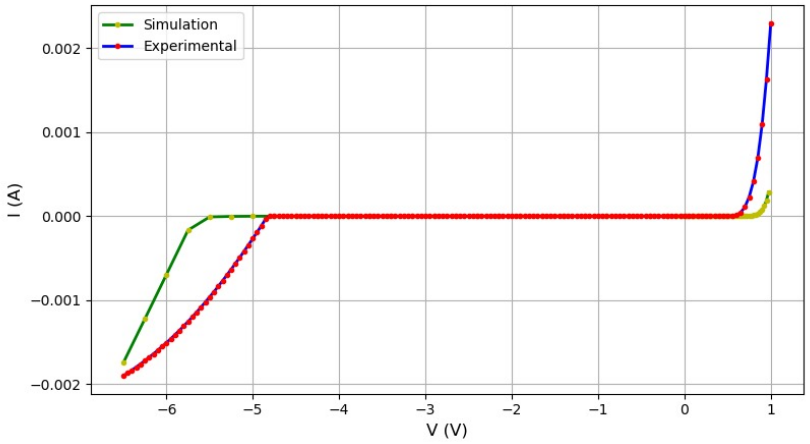

Figure 2: Comparison between the theoretical and experimental I-V characteristics observed for the tested Zener diode.

It should be noted that the experimental low bias regime behavior reflects very well the expected one, showing no significant increase in current up to certain values in both forward and reverse configurations. We observe that the current increases more rapidly in the experiment in the FB regime compared to the simulation. The measured breakdown voltage is $V_{br} = -4.825 \pm 0.025\,V$, which differs in a quite significant manner from the result of the simulation ($V_{br} \approx 5.7\,V$). Moreover we extracted from the experimental data the values of

I_0, R_S and n. This has been accomplished by inverting the FB characteristic (V as a function of I) and fitting the data with the reversed diode characteristic model, which takes into account non-idealities (series resistance and carrier recombination in the depletion layer):

$$V = R_S I + n\frac{k_B T}{q} ln(1 + \frac{I}{I_0}), \tag{2}$$

where we assume that the device is working at room temperature ($\frac{k_B T}{q} = 25\, mV$). The results of the fit are shown graphically in Fig.3 and are reported below:

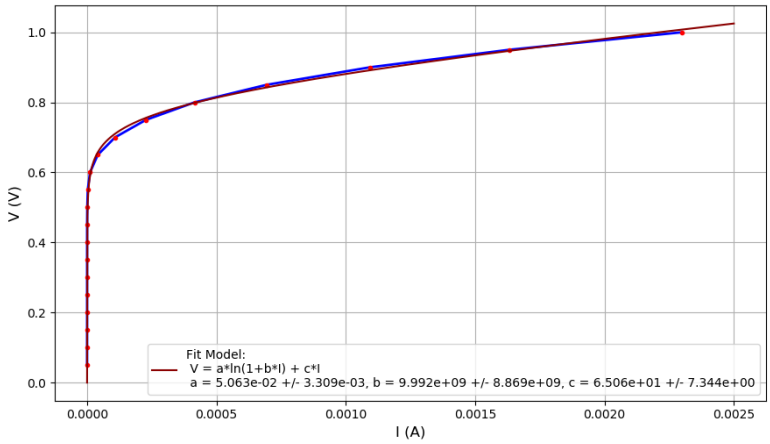

Figure 3: Fit of the FB characteristic of the diode.

- $I_0 = 90 \pm 47\, pA$
- $R_S = 61.7 \pm 4.5\, \Omega$
- $n = 1.932 \pm 0.075$

All the values extracted from the fit are in the order of magnitude we expect them to be. In particular, n is close to 2, as expected since we are dealing with a Si based diode.

3 *npn* BJT

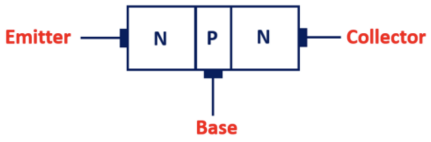

Figure 4: BJT npn

The bipolar junction transistor (BJT) is a three-terminal semiconductor device that, in certain configurations, acts as a voltage/current amplifier or as a switch. It has three doped regions (heavly doped *emitter*, moderatly doped *base* and lightly doped *collector*). The base region is found in between the emitter and collector regions and has a small width compared to the minority carrier diffusion length. It is possible to distinguish *npn* and *pnp* transistors based on the doping configurations of these three regions. It's often useful, in order to understand the structure of the BJT, to see it as two *pn* junctions, one between B and C and the other between B and E (Fig.5). It is important to underline that, since the base is thinner that the diffusion length of the minority carrier in it, electronically it doesn't actually work as two *pn* junctions in series.

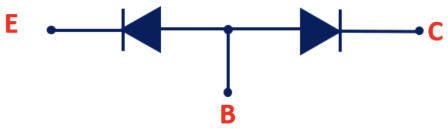

Figure 5: *npn*-BJT as *pn* junctions

The BJT can operate in four biasing modes:

- Saturation: both EB and CB junction are foward biased;
- Active: EB junction forward biased, CB junction reverse biased;
- Inverted: EB junction reverse biased, CB junction forward biased;
- Cut-off: both EB and CB junctions reverse biased;

We work in active biasing mode with grounded E (common emitter configuration: input in B and output in C). In active mode we have a forward biased EB junction and, since the emitter is highly doped with respect to the base, the current that flows through the EB junction will be mostly due to electron diffusion from E to B. Since the width of the base is smaller than the recombination length of the electrons, most of them are able to reach the depletion

region between B and C and then drift into the collector.

The BJT is decribed by some performance parameters:

- *Emitter efficency*: fraction of emitter current carried by the electrons $\gamma = \frac{I_{En}}{I_E}$
- *Base transport factor*: fraction of electrons captured by the collector $\alpha_T = \frac{I_C}{I_{En}}$
- *Common-base current gain*: $\alpha = \frac{I_C}{I_E} = \alpha_T \cdot \gamma$
- *Common-emitter current gain*: $\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$

3.1 Results and analysis

The objective of the experimental investigation is to measure the I-V characteristic of the *npn*-BJT device, experimentally determining the common-emitter current gain β, finding the linear region of operation of the device (interval of V_{be} values where β is constant).
The first investigation carried out involves the measurement of the *npn*-BJT I-V characteristic: we measure I_c as a function of V_{ce} (which is increased from $0\,V$ to $5\,V$ in $50\,mV$ steps) at different constant I_B. The base current is increased from $0.1\,\mu A$ to $0.45\,\mu A$ in steps of $87.5\,nA$. The results of these measurements are shown in Fig.6.

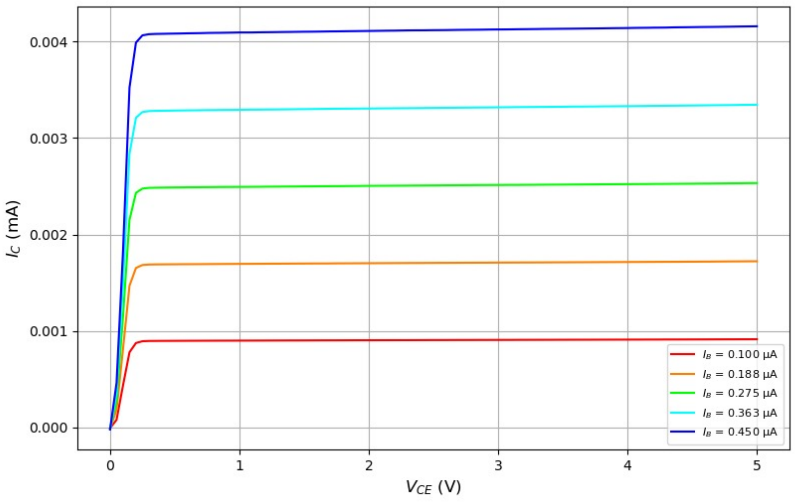

Figure 6: I_c vs V_{ce}

From the experimental results we notice that, as soon as V_{ce} reaches a certain value ($V_{ce} \approx 200\,mA$) and the proper biasing configuration of the device is obtained, the collector current becomes constant as a function of V_{ce}, keeping the input current at the base constant. These observations are consistent with theoretical considerations.

The second investigation carried out involves the measurement of the *npn*-BJT Gummel plots: we measure I_c and I_b as a function of V_{be} (which is increased from $0.2\,V$ to $1\,V$ in $50\,mV$ steps). The results of these measurements are shown in Fig.7. We also show the simulation results in this figure in order to compare them with our experimental data. We can see a good agreement between the simulation and the experimental results in the linear region (that we identify in a region $0.35\,V \leq V_{be} \leq 0.75\,V$). Outside this interval we observe expected deviation from the ideal model, since we enter regions where effects such as recombination (small V_{be}) and series resistance or high level injection (high V_{be}) become non negligible.
It's worth noting that, in terms of the collector current, the linear range is between $10^{-9}\,mA$ and $10^{-2}\,mA$.

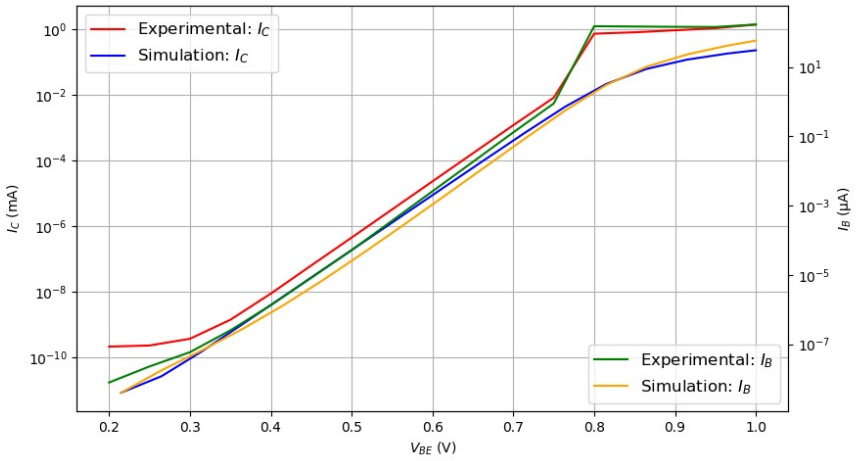

Figure 7: I_b, I_c vs V_{be}, logarithmic plot

Now we explicitly plot the common-emitter current gain $\beta = \frac{I_c}{I_b}$ as a function of the collector current I_C and we compare it with the results of the simulation in Fig.8.

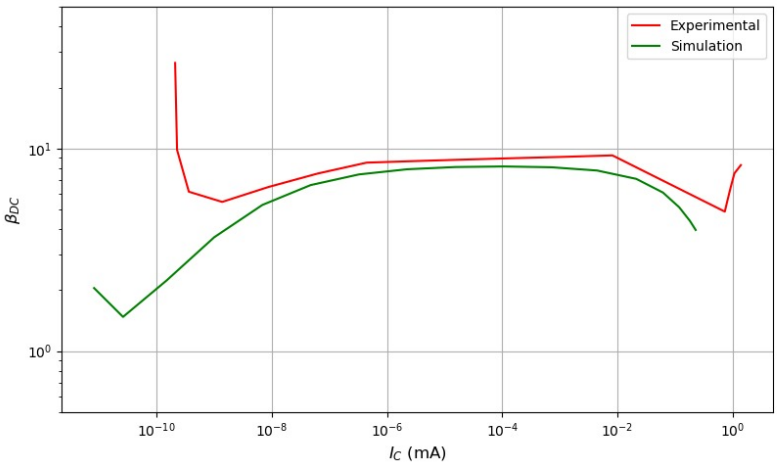

Figure 8: Gain vs I_c, double logarithmic plot

Once again the simulation and the experimental result are in good agreement in the linear zone ($10^{-9} \leq log(I_c) \leq 10^{-2}$), which is consistent with the one found before. In this region we find $\beta = 8.7$ wich is a reasonable value for a real BJT device.

4 *N*-channel MOSFET

MOS (Metal-Oxide-Semiconductor) is an important device used in microelectronic. MOSFET devices have three terminals: *Source*, *Drain* and *Gate*. A voltage bias applied to the *Gate* contact is used to control the current which flows between *Source* and *Drain*. A MOSFET device consists of a Si substrate in which we distinguish a lightly doped main body and two heavily doped terminals (S and D), physically separated from one another. The doping type of the S and D terminals is opposite to that of the main body. Upon the substrate, between the S and D terminals, an oxide layer (insulator) is first deposited, followed by a conductive layer, forming the G contact. The present work scope is to analyse and present the characteristics of the transistor MOS in Common Source configuration (the input voltage is V_{gs} and the output voltage is V_{ds}).

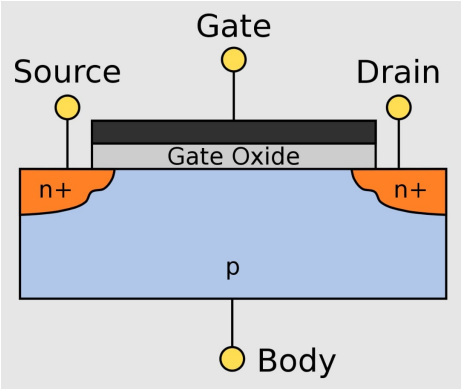

Figure 9: N-channel MOSFET

The device tested is an N-channel MOSFET: Source and Drain are made of heavily doped N-type Si, while the substrate is made of P-type Si. The G conductive contact is usually built using extremely doped poly-Silicon.

Starting with grounded S, D and body, we supply a voltage to the G. We observe different operation regions depending on the G voltage:

- Accumulation mode ($V_{gs} < 0$): holes in the substrate accumulate in a small region near the semiconductor/oxide interface, preventing any current flow between S and D (due to an increase of recombination phenomena);
- Delpetion mode ($0 < V_{gs} < V_{th}$): holes in the substrate are repelled from the semiconductor/oxide interface, producing a depletion region, still preventing any significant current flow between D and S (a small subthreshold diffusion current can be detected);
- Strong inversion ($V_{gs} > V_{th}$): electrons are attracted at the semiconductor/oxide interface, creating a conductive channel beneath the G oxide, thus giving rise to a significant current when a voltage V_{ds} is applied between S and D.

The threshold voltage V_{th} is the minimum Gate-Source voltage that produces the formation of the conductive channel at the semiconductor/oxide interface. When the threshold voltage is applied at the Gate, the concentration of electrons at the interface is exactly equal to the concentration of impurities (acceptors) in the bulk P-Type substrate.

4.1 Results and analysis

The objective of the experimental investigation is to measure the I-V characteristic of the N-channel MOSFET device, experimentally determining the threshold

voltage V_{th}, observing the difference between the OFF state (depletion mode, no conduction) and the ON state (strong inversion mode, conduction).
The first investigation carried out involves the measurement of the MOSFET I-V characteristic: we measure I_{ds} as a function of V_{ds} (which is increased from $0\,V$ to $5\,V$ in $200\,mV$ steps) at constant V_{gs}. The Gate voltage V_{gs} is increased in steps of $250\,mV$ from $0\,V$ to $2\,V$, then in steps of $500\,mV$ from $2\,V$ to $5\,V$. The results of these measurements are shown in Fig.10 (ON characteristic) and in Fig.11 (OFF characteristic). Substrate and *Source* were grounded during each measurement.
We observe that, when the MOSFET is in the ON state ($V_{gs} > V_{th}$) each I-V curve shows an initial increase of the I_{ds} current as a function of V_{ds} which then saturates to a value I_{ds-sat} when the D to S voltage reaches a certain value V_{ds-sat}. When the MOSFET is in the OFF state ($V_{gs} < V_{th}$) we almost observe the absence of any current. Only a small sub-threshold current contribution can be detected, which gives rise to a current of few tens of μA as V_{gs} approaches V_{th}.
When the MOSFET is in its ON state, then the I_{ds} current is caused by electron *drift* across the channel. The Shockley model is used to describe I_{ds} as a function of V_{ds} below the saturation condition, given a certain V_{gs} bias applied to the *Gate*:

$$I_{ds} = \frac{\mu_n C_{ox} W}{L}[V_{ds}(V_{gs} - V_{th}) - \frac{V_{ds}^2}{2}], \tag{3}$$

where μ_n is the electron mobility, C_{ox} is the Gate capacitance, W and L are the channel width and channel length respectively. In contrast with this, when the MOSFET is in the OFF state, the sub-threshold current is caused by *diffusion* of electrons and it can be shown that it varies exponentially as a function of V_{gs}.

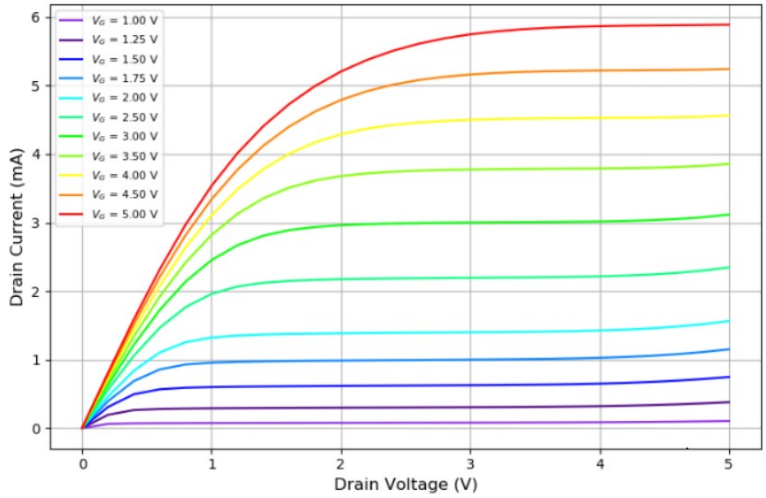

Figure 10: N-channel MOSFET ON I-V characteristic.

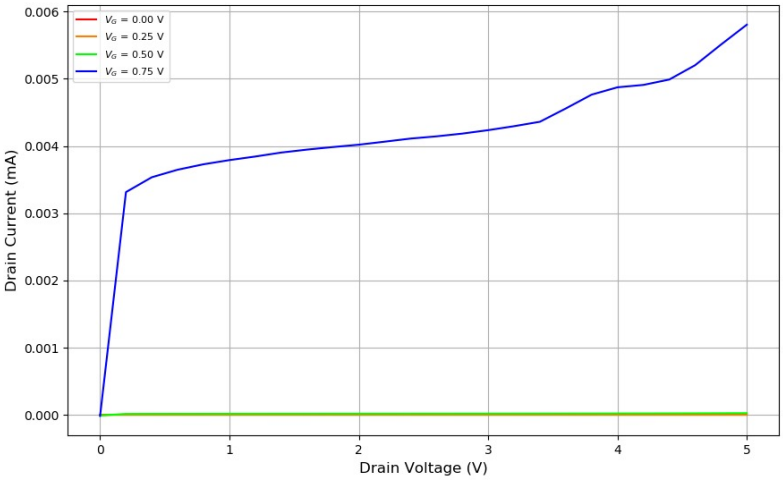

Figure 11: N-channel MOSFET OFF I-V characteristic.

The threshold voltage V_{th} is experimentally determined interpolating the *Drain* saturation current I_{ds-sat} as a function of the *Gate* voltage V_{gs} in the strong inversion regime. When Drain current saturation is caused by channel pinch-off,

we observe a regime in which I_{ds-sat} is given by

$$I_{ds-sat} = \frac{\mu_n C_{ox} W}{2L}(V_{gs} - V_{th})^2[1 + \lambda(V_{ds} - V_{ds-sat})], \tag{4}$$

where λ is the channel modulation coefficient (describes the increase of the saturation current for $V_{ds} > V_{ds-sat}$ due to the channel length reduction). However a linear increase of the *Drain* saturation current as a function of *Gate* voltage is observed from the experimental data instead of the parabolic trend described by the pinch-off model. It is also possible to observe that the *Drain* saturation current is essentially independent on the channel length L since it does not vary significantly once saturation is reached. This deviation in the electrical behaviour of the device can be explained by considering that current saturation is caused by the fact that electrons reach their saturation velocity v_{sat}, which happens when the electric field in the channel that gives rise to the electrons motion from S to D is grater than the saturation electric field ($V_{ds}/L > E_{sat}$). In this regime we observe that I_{ds-sat} varies linearly with V_{gs}:

$$I_{ds-sat} = WC_{ox}v_{sat}(V_{gs} - V_{th}). \tag{5}$$

From this linear interpolation (Fig.12), we are able to extract the coefficients of the linear fit, which can then be exploited to evaluate V_{th}. We obtain $V_{th} = (1.08 \pm 0.02)\,V$, which is consistent with typical values of threshold voltage for commercial MOSFET.

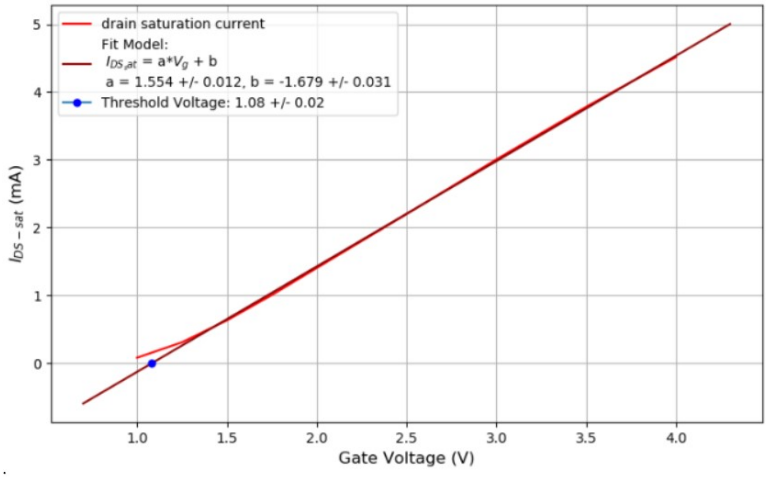

Figure 12: I_{ds-sat} as a function of V_{gs}. Data are interpolated with a linear function in order to find V_T.

It is possible to see that for $V_{gs} \approx V_{th}$ the Drain saturation current tends to deviate from the linear behavior. This is a consequence of the fact that in this

case we switch from strong inversion mode to depletion mode, and in this case the main contribution to I_{ds-sat} is the sub-threshold current.
We conclude the analysis of the MOSFET device showing the comparison between the results of the experimental I_{ds} vs V_{ds} characteristic with the results of the simulation (Fig.13). Both curves were taken with $V_{gs} = 3.0\,V$.

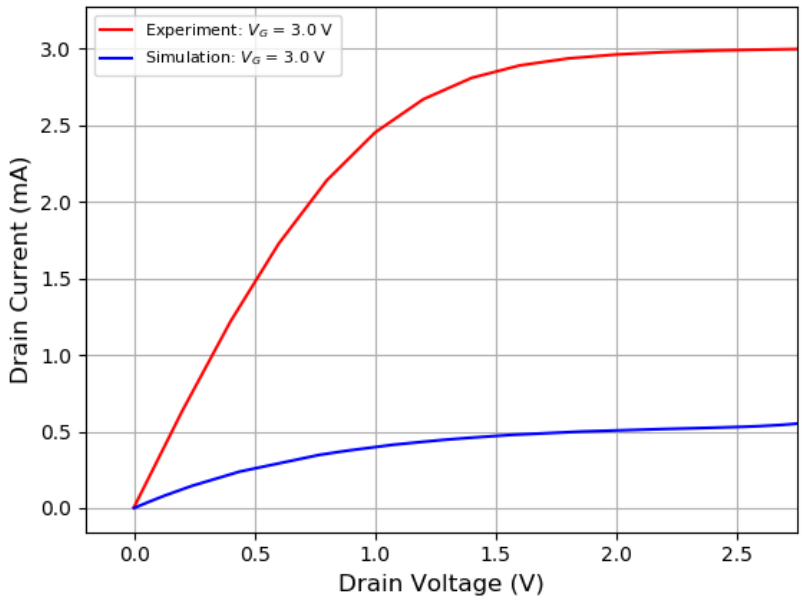

Figure 13: Comparison between experimental data and simulation results for the MOSFET ON regime.

As it is possible to see from the graph in Fig.13, the qualitative trend of both curves is very similar and both have a $V_{ds-sat} \approx 2.0\,V$. However, the quantitative information given by the simulation is misleading, in fact the current measured in the experiment is six times larger than the current output of the simulation.

5 Conclusions

In light of the collected information, we can conclude that the study conducted has provided experimental results that follow, in a general sense, the theoretical expectations. Naturally there is a large number of physical phenomena that usually enter in the evaluation of a device working principle, that can't be considered in the simulation process. This in some cases leads to significant

differences between the simulations and the experimental results, as we have observed in the study of the Zener diode and N-channel MOSFET behaviors. All things considered, we deem this study to represent very well the electrical and physical properties of the analyzed devices, yielding results whose values reflect the commonly spread quantities in the market.