Variation-Aware Analysis: Savior of the Nanometer Era?

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ABSTRACT
VLSI engineers have traditionally used a variety of CAD analysis tools (e.g. SPICE) to deal with variability. As we go into deep sub micron issues, the analysis is becoming harder due to many secondary effects becoming primary. Panelists will debate the variability trend and present the order of importance of many variability trends (Vdd, Vt, Interconnect, Leff, Gate Width) and their impact on design tools and methodologies.

What new design tools, new modeling methodologies, and new (or old) design styles will combine to address variability? Will conservative design to accommodate variability halt the progress of Moore's Law? Is life as we know it over, or are we facing an opportunity for innovation in tools and design that will move us forward over the barriers that technology has placed in our path?

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General Terms: Design, Verification, Performance.

Keywords: Variability, Yield, DFY

Position Statements:
Panelists have provided their position statements (see below) outlining their opinions. In the panel, each panelist will give no more than three specific takeaway points that designers must consider while analyzing their designs.

1. Sani R. Nassif:
In the olden days, simulating a transistor required knowing L and W, both of which could be extracted from very local geometry (the intersection of poly with diffusion and bingo!). As we pushed lithography to print features smaller than the illumination wavelength, the number of "features" required to accurately predict the size of a device has grown and it is now common to require knowledge of a broad region around the device in order to accurately predict its behavior. This trend is going to continue, and we are rapidly going to enter a regime where "composability" as we have known it -i.e. the ability to construct a circuit out of disparate components by fairly arbitrary combinations- will be gone. The corollary to the loss of composability is that we will no longer be able to simulate or predict the behavior of our designs without deep changes to the manner in which we model the interaction between layout and device behavior. Emerging phenomena such as channel stress will cause circuit extractors to require ever larger geometries in order to allow accurate prediction of circuit performance. This will drive new requirements for CAD, for technology modeling, for device modeling, and for technology characterization. The eco-system to support all of these activities is in its infancy and will require significant investment to thrive.

2. Dennis Sylvester:
The burden of suppressing variability is shifting from process to design (e.g., a relaxing of process tolerances to make new nodes achievable in the expected ~2 year timeframe). The design and CAD communities must therefore step up and assume more responsibility in creating highly manufacturable designs considering stressed underlying devices. Some open areas include:

Statistical static timing analysis (SSTA) remains unproven and not overly useful without optimization capabilities. Alternatives to mainstream SSTA should be explored that are more palatable to designers. One possibility is the use of well established and fast deterministic approaches combined with variation space sampling to yield an efficient and proven robust design strategy.

Systematic variability, such as those based on optical proximity effects, must be addressed in the near term. These are good examples of low-hanging fruit with low implementation costs and high payoffs (e.g., the systematic behavior of critical dimension linewidth with respect to lithographic defocus).

Highly regular design (beyond orientation restrictions or forbidden pitches) will be a significant help as early as 45nm. However, adaptive circuit techniques provide an alternative way of coping with large variability. There is currently no concept of automated adaptivity; there is a need for design flows that inherently consider adaptive circuit design techniques to improve parametric yield. A question is: is it more effective/cheaper to pursue regularity (extreme "correct by construction") or intelligent adaptivity ("sense and correct")?

3. Vijay Pitchumani:
Nuisance, Thy Name is Variation

The Bard once wrote, "Nuisance, thy name is variation". Well, if he didn't, he should have. For variation is vying with mother-in-law as a nuisance and a tyrant. Is its notoriety well-deserved? Will it derail Moore's Law? Objective minds, not to mention enquiring ones, want to know.

Yes, variability has become an increasing challenge. The light at the end of the tunnel has been 193 nm for too long. However, the news is not all bad. Deterministic process variations are amenable

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to layout restrictions, density fill, aggressive OPC, process recipe optimization, and when all else fails, modeling. Deterministic environmental variations can be conquered by modeling too. Systematic within-die variation has not been a worsening problem and is under control by process/product engineers. Random Vt variation has been increasing but we benefit from path delay averaging, though leakage does require some care. Die-to-die variation is manageable. Advanced process control, high volume manufacturing learning and "Copy Exactly!" between factories are helping to keep variation in check. Design methodologies and CAD tools have been getting smarter too, enriching our variation-fighting arsenal. On the research side, from regular layout fabric to a particularly sharp Razor, the academia has been prolific with ideas on variation avoidance and variation tolerance.

In short, variation has a formidable opponent, particularly in an IDM, due to a tight design-process coupling. With continued advances on process, design and EDA fronts, the show, a.k.a. Moore's Law, will go on.

4. Clive Bittlestone:

Increasing design parameter uncertainty has become intolerable from a process entitlement viewpoint, triggering a massive mitigation effort to understand, model, mitigate, reduce or live with these variations. Some effects were considered random, or computationally infeasible to model. However many are systematic and can be bounded/modeled as new tools come on line.

For transistors we have pattern fidelity/alignment, NBTI, etch and stress effects. For wires we have CMP thickness variations, pattern fidelity, etch and so forth. We also have very restrictive design rules to help keep silicon behavior in model bounds. Fabs are also delivering much more variation information to design, we (and eda tools) must be ready! We must have variation aware tools/methodology to handle these effects (checkers and optimizers). Even after systematic effects are comprehended, there are still significant truly random effects that have to be handled. Residual effects that remain computationally infeasible will continue to be components of design margin. In addition, circuit and system techniques will have to be deployed to support variation tolerant design and variation insensitive/corrective and adaptive design styles.

5. Norma Rodriguez:

Creativity in the DFM arena has manifested itself in the proliferation of acronyms (Design for Yield, Design for Variability, Design for Profitability, etc.) rather than with needed integrated flows and novel software tools offerings from CAD vendors.

Nevertheless, the development of process-aware design and verification flows (PAD and PAV) has continued, driven mostly by cross-functional teams within IDM's and possibly large foundries.

The most notable example is certainly represented by the family of Layout Printability Verification flows, which were originally built to perform Post-OPC verification, but which have now been generalized to validate physical designs before and not after tape-out, thus introducing the notion of "prevention" rather than "correction".

In the transition from 65 nm to 45 nm technologies, prevention by Design Rule Augmentation will become the predominant paradigm for physical verification. This means that process variability, both systematic and statistical, will be addressed by different classes of Design Rules (restricted DR, preferred DR, etc.), depending on the different circuit element, or type of library component (or even its placements within the larger system).

The reason for this conservative and somewhat limited approach (as compared with "true", i.e. simulation based DFM flows) resides in the inability of current design flows to deal with continuous type of check results, instead of the pass-fail mechanism built-in in DRC systems.

In the transition from 45 nm to 32 nm nodes, then, process variability information will have to be natively available, embedded, in most (if not all) CAD design tools, from circuit design, to library implementations, to synthesis, to routing, all the way into full-chip verification.

The grand challenge will be to create a series of mappings from the continuous yield functions, which describe intrinsic process variability, to the discrete, integral, optimization constraints at each step of the design flow.

It is incumbent upon the entire CAD industry to develop these novel functionalities, allowing variability and yield to be "understood" as primary inputs to any software tool (with suitable standards). It is also essential that design-closure be associated with a yield figure of merit, where a "manufacturability index" could also be used to optimize and control the fabrication process (implementing the complete feedback loop denoted as DEM or Design Enhanced Manufacturing).

6. Riko Radojcic:

It is clear that the traditional corner-based design methodologies need to evolve to address the variability challenges at 45 and below. What is not clear is (a) how big are those challenges, and (b) the predominant solutions.

Thus, firstly, if the industry ends up pursuing the highly restrictive design rules, some of the principal sources of variability that we worry about today, may be a mute point, and the corner-based methodology may be extendible – mostly - for at least one more node.

If on the other hand that is not the case, or is only partially so, then there seems to be two principal methodologies out there that people talk about. One focuses on addressing the systematic sources of variability through use of the new "DFM Simulators". Thus, Shape Simulators (for modeling fidelity in the x-y space – mostly driven by the litho effects) or Thickness Simulators (for modeling fidelity in the z-space – mostly driven by the CMP effects) could be used to bring these effects separately into the design flow, either at the IP level or at the chip level, or both, leaving the rest of the corner based methodology intact. The other methodology focuses on abandoning the corner based methodology entirely and evolving a true statistical design.

In reality, it is likely that the industry will in fact use some blend of these methodologies. We believe that the selection of the mix will in fact be driven by the process-end of the industry spectrum, through the process characterization infrastructure, rather than the EDA-end through definition of new tools or flows.