Tomorrow's Analog: Just Dead or Just Different?

Georges Gielen
Katholieke Universiteit Leuven
Kasteelpark Arenberg 10
3001 Leuven, Belgium
+32 16 321047
gielen@esat.kuleuven.be

Rob Rutenbar
Dept ECE, CMU
3105 Hamerschlag Hall
Pittsburgh, PA 15213, USA
+1 412 268 3334
rutenbar@ece.cmu.edu

Shekhar Borkar
Intel
2111 NE 25th Ave
Hilssboro, OR 97124, USA
+1 503 712 2871
y.borkar@intel.com

Robert Brodersen
Dept. EECS, UC Berkeley
Berkely, CA 94720, USA
+1 510 666 3110
bwb@bwrc.eecs.berkeley.edu

Jue-Hsien Chern
Mentor Graphics Corporation
USA
+1 503 685 4716
jue-hsien_chern@mentor.com

Eric Naviasky
Cadence Design Services
USA
+1 410 290 2800
enav@cadence.com

Daniel Saias
ST Microelectronics
850, rue Jean Monnet
38926 Crolles, France
+1 33 4 76 925166
daniel.saias@st.com

Charles Sodini
Dept EECS, MIT
60 Vassar Street
Cambridge, MA 02139, USA
+1 617 253 4938
sodini@mit.edu

ABSTRACT

This panel discusses the following topics. With the ongoing trend towards more and more digitization in applications ranging from multimedia to telecommunications, there is a big debate about whether there will remain a need for analog circuits in scaled technologies. Analog circuits do not seem to take advantage of nanometer CMOS; rather they suffer from it. So if the question is asked "Will analog scale?", you get conflicting opinions. One camp argues for an almost-all-digital future: analog/RF content should be limited, because it's difficult, expensive, risky, and can be done with DSP. The opposing camp counters that some critical circuits simply do not want (or need) to scale, and analog is only "risky" when you let digital designers do it. So, what is the future role of analog circuits in scaled CMOS, and can analog EDA tools help in this ?

Categories and Subject Descriptors

B.7.2 : Design Aids for Integrated Circuits

General Terms: Design, Algorithms

Keywords: Analog design; mixed-signal design; RF design; analog design methodologies; analog CAD tools

1. PROBLEM STATEMENT

With the evolution towards ultra-deep-submicron and nanometer CMOS technologies [1] the design of complex Systems on a Chip (SoC) is emerging in consumer-market applications such as telecom and multimedia. These integrated systems are increasingly mixed-signal designs, embedding high-performance analog or mixed-signal blocks and possibly sensitive RF frontends together with complex digital circuitry (multiple processors, some logic blocks, and several large memory blocks) on the same chip. In addition, the growth of wireless services and other telecom applications increases the need for low-cost highly-integrated solutions with very demanding performance specifications.

The use of nanometer CMOS technologies below 90nm however also brings along significant challenges for circuit design (both analog and digital) [2]. Some of these challenges were never encountered before, while others existed before but have become even stronger limitations today. For analog circuits in particular technology scaling does not bring large area reductions, because the active area (width times length) of key analog transistors in a circuit is determined by noise or mismatch constraints, both of which limit the dynamic range or accuracy levels that can be achieved. In addition, the use of nanometer technologies brings along lower supply voltages and more technology parameter variability. In addition, increased integration of entire systems causes more signal integrity problems for the analog circuits. So, analog circuits do not seem to take advantage of nanometer CMOS; rather they suffer from it.

Therefore, with the ongoing trend towards more and more digitization in applications ranging from multimedia to telecommunications, there is a big debate about whether there will remain a need for analog circuits in scaled technologies. If the question is asked "Will analog scale?", you get conflicting opinions. One camp argues for an almost-all-digital future: analog/RF content should be limited, because it's difficult, expensive, risky, and can be done with DSP. The opposing camp counters that some critical circuits simply do not want (or need) to

DAC 2006, July 24 28, 2006, San Francisco, California, USA.
ACM 1-59593-381-6/06/0007.

scale, and analog is only "risky" when you let digital designers do it. This panel vividly discusses these topics. In addition, there has been significant progress in analog CAD tools (both at academic and commercial level) to alleviate some of the above problems. So the panel members will debate the future role of analog circuits in scaled CMOS, and how analog EDA tools might help in this.

2. POSITION STATEMENTS

The following are the position statements of the different panel members.

Shekhar Borkar, Intel Fellow, believes that there will be analog tomorrow: analog will be there to prove the point that it did exist at some time, and it still does, but that's about it. Technology scaling does not help analog in power or performance--in fact it makes it difficult, and thus analog does not enjoy economic benefits from scaling. Therefore, more and more analog functions will be done digitally, providing higher performance, lower power, and lower cost. So, the only reason analog will exist tomorrow is to prove the point that it is not dead yet!

Charles Sodini, EECS professor at MIT, argues that analog and mixed-signal circuit design is far from dead. In fact, the availability of increased digital processing has lead to many innovative architectures, where digital processing is used to improve analog performance metrics. Along with digitally enhanced analog design we are seeing innovative techniques being investigated such as the replacement of opamps in switched capacitor circuits with comparators. We are also seeing predominantly digital architectures replacing analog functions such as the recently published all-digital PLL and transmitter. With that said, a big question is whether these techniques will be implemented in technologies at the 65nm node and beyond. Substantial gate leakage with silicon dioxide gate dielectrics and increased 1/f noise with alternative gate dielectrics continue to plague charge-based circuit design. The bottom line is that innovation is alive and well in the mixed-signal circuit design community. The integration of these innovations into state-of-the-art technology without the availability of less aggressively scaled I/O type devices is still an open question.

Daniel Saias from ST Microelectronics raises the question how analog circuits can be dead when what makes them analog is precisely their analogy to continuous physical phenomena in nature and life. Is nature dead? Is life dead? At a time when circuits need to interact more and more with their physical environment, how could they be purely digital? Digital circuits mainly exist because they provide efficient storage and easy/steady computing possibilities. They clearly rely on analog signal conditioning to interface with the real world. Why be reluctant to use neat analog circuits when they provide (and will continue to provide) performance and consumption advantages on their digital counterparts?

Eric Naviasky from Cadence Design Services states that the end of analog is not the question. As long as interfacing to the real world is part of the project goals, we will need analog. The presence of analog on the big SoC's of the future is a matter of techno-economics. When the price of including the analog on chip is less than the cost of putting it off chip (though maybe still in the same package), product marketing will seek that solution. Analog/mixed-signal designers being the masochists they are, will sign up for the challenge and do the hereto impossible. It is getting harder to incorporate the analog in the latest processes but I see no sign of a tailing off in demand for analog content.

Robert Brodersen, EECS professor at UC Berkeley, confirms that it is certainly obvious to all that digital circuit design is easier than analog, and that the digital circuits usually also scale better with technology and have better design automation tools. So why is there any discussion on why anyone would voluntarily choose to use an analog circuit solution? It has to do with the unfortunate fact that the world we live in is an analog one and that the conversion between the analog and digital domains typically limits the performance or quality of user applications. For example, if we could avoid the analog circuitry for wireless systems, we could easily have gigabit/second links, eliminate interference and have a robustness nearly equal to wired systems. Therefore the signal conditioning in preparation to the A/D conversion and vice versa will always be required and as we get more sophisticated in our digital processing, the analog circuits become ever more challenging and limiting of the system performance. On the other hand, to try to use analog to do algorithms or processing that can be done in the digital domain…forget it!

Jue-Hsien Chern, VP at Mentor Graphics, states that it is hard to imagine that analog designs will go away since analog is the undeniable interface to the real world. However, there are two significant trends in analog circuit design: larger-scale integration and conversion to digital design wherever possible. The consequence of these trends is that they create even more complicated mixed-signal designs. Because of this, two main challenges emerge: how to do system-level mixed-signal designs, and how to verify system-level functionality after chip assembly.

Come and see the panel and participate to the discussion to find out about the final answers to these questions.

3. REFERENCES

[1] "International Technology Roadmap for Semiconductors 2005," http://public.itrs.net.

[2] Georges Gielen, Wim Dehaene, "Analog and digital circuit design in 65 nm CMOS: end of the road?," proc. DATE conference, 2006.

[3] G. Gielen, R. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," Proceedings of the IEEE, Vol. 88, No. 12, pp. 1825-1854, December 2000.