CS224

Section No.: 3

Spring 2021

Lab No.: 6

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Q1

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits[1]	Byte Offset Size in bits[2]	Block Replacement Policy Needed (Yes/No)
1	8	1	8	8	2^{10}	16	10	3	0	No
2	8	2	16	8	2^{8}	17	8	3	1	Yes
3	8	4	16	4	2^{8}	18	8	2	1	Yes
4	8	Full	16	4	2^{0}	26	0	2	1	Yes
9	32	1	16	2	2^{13}	14	13	1	1	No
10	32	2	16	2	2^{12}	15	12	1	1	Yes
11	32	4	8	8	2^{10}	16	10	3	0	Yes
12	32	Full	8	8	2^{0}	26	0	3	0	Yes

Table 1: Various cache memory charactheristics to be represented for 0.5 GB main memory

Q2

Consider the following MIPS code segment. (Remember MIPS memory size is 4 GB.) Cache capacity is 8 words, Block size: 4 words, N= 1.

```
addi        $t0, $0, 5
loop:  beq      $t0,  $0,
                done
lw          $t1, 0xA4($0)
lw          $t2, 0xA8($0)
lw          $t3, 0xAC($0)
addi        $t0, $t0, -1
j           loop
done:
```

a)

Instruction	**Iteration No.** 1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory Miss	Hit	Hit	Hit	Hit
lw $t2, 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3, 0xAC($0)	Hit	Hit	Hit	Hit	Hit

Table 2: Hit and Miss rates for Cache memory with 8 words capacity, 4 words block size, N= 1

b. What is the memory size of one set in number of bits? What is the total cache memory (SRAM) size in number of bits? Note: Include the V bit in your calculations. Show the details of your calculation.

Size of memory: 4 GB = $2^2 2^{30} = 2^{32}$B

Physical address size: $\log_2(2^{32})$ = 32 bits required for address

The specific cache is direct associative since N = 1

(#ofBlocks) B = Capacity / Block size = 8 / 4 = 2

(#ofSets) S = B / N = 2 / 1 = 2

Set size = $\log_2$(#ofSets) = $\log_2(2)$ = 1 bits

Word block offset size = $\log_2$(#ofWordsInBlock) = $\log_2(4)$ = 2 bits

Byte offset size = $\log_2$(#ofBytesInWord) = $\log_2$(#ofBytesInWord) = $\log_2(2^2)$ = 2 bits

Tag = 32 – 1 – 2 – 2 = 27 bits

Size of one set: 1 (valid bit) + 27 (Tag bits) + 32 (Data00) + 32 (Data01) + 32 (Data10) + 32 (Data11) = 156 bits

Cache size: 156 * 2 = 312 bits

Memory address:

Tag (27 bits)	Set Size (1 bit)	Block Offset (2 bits)	Byte Offset (2 bits)

Cache architecture:

V (1 bit)	Tag(27 bits)	Data (32 bits)	Data (32 bits)	Data (32 bits)	Data (32 bits)
V (1 bit)	Tag(27 bits)	Data (32 bits)	Data (32 bits)	Data (32 bits)	Data (32 bits)

c. State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory. No drawing is needed.

To supply this particular design additional hardware is requried:

1 X Equality Comparator (Compares tag)

1 X AND Gate (Decides hit or miss)

1 X 4:1 MUX (32 bits) (Selects correct data within the set)

3. Consider the above MIPS code segment. The cache capacity is 2 words, block size is 1 word. N= 2. The block replacement policy is LRU.

a. In the following table indicate the type of miss, if any: Compulsory, Conflict, Capacity.

Instruction	**Iteration No.** **1**	**2**	**3**	**4**	**5**
lw $t1, 0xA4($0)	Compulsory Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss
lw $t2, 0xA8($0)	Compulsory Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss
lw $t3, 0xAC($0)	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss

Table 3: Hit and Miss rates for Cache memory with 2 words capacity, 1 words block size, N= 2

b. How many bits are needed for the implementation of LRU policy: for a set, for the entire cache memory? What is the total cache memory size in number of bits? Include the V bit and the bit(s) used for LRU in your calculations. Show the details of your calculation.

Size of memory: 4 GB = $2^2 2^{30} = 2^{32}$B

Physical address size: $\log_2(2^{32})$ = 32 bits required for address

The specific cache is 2 way set associative since N = 2

(#ofBlocks) B = Capacity / Block size = 2 / 1 = 2 words

(#ofSets) S = B / N = 2 / 2 = 1

Set size = $\log_2$(#ofSets) = $\log_2(1)$ = 0 bits

Word block offset size = $\log_2$(#ofWordsInBlock) = $\log_2(1)$ = 0 bits

Byte offset size = $\log_2$(#ofBytesInWord) = $\log_2$(#ofBytesInWord) = $\log_2(2^2)$ = 2 bits

Tag = 32 – 2 = 30 bits

Size of one set: 1 (valid bit) + 1 (LRU check bit) + 30 (Tag1) + 32 (Data1) + 1 (valid bit) + 30 (Tag0) + 32 (Data0) = 127 bits

Cache size: 127 * 1 = 127 bits

Memory address:

Tag (30 bits)	Set Size (0 bits)	Block Offset (0 bits)	Byte Offset (2 bits)

Cache architecture:

V (1 bit)	LRU (1 bit)	Tag(30 bits)	Data (32 bits)	V (1 bit)	Tag(30 bits)	Data (32 bits)

c. State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory. No drawing is needed.

To supply this particular design additional hardware is requried:

2 X Equality Comparator (30 bits) (Compares if tag is EQUAL)

2 X AND Gate (Decides hit or miss by checking both tag is EQUAL and it is VALID)

1 X OR Gate (gets Hit0 and Hit1 and decides Hit condition: Only one can be 1!)

1 X 2:1 MUX (32 bits) (Selects correct data within the set)