CSE 436/536

INTEGRATED CIRCUIT DESIGN

CMOS Design and Simulation Report

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1. Layout Design Methodology

The layouts for the inverter, 2-input NAND, and 2-input NOR gates were designed following standard CMOS design rules and lecture guidelines. Key design considerations included:

- Maintained cell height of 100λ as per specifications
- Used specified transistor dimensions:
    - NMOS: W/L = 4λ/2λ
    - PMOS: W/L = 8λ/2λ
- Carefully monitored and addressed DRC (Design Rule Check) warnings in Magic VLSI tool (drc why, drc find)
- Implemented proper layer connections using metal1 for power rails and signal routing

2. Netlist Extraction and Simulation Setup

The simulation environment was prepared using the following steps:

1. Extracted the layout to SPICE format using Magic's extraction commands
2. Modified the SPICE netlist to include:
    - TSMC 0.25µm technology model inclusion
    - Power supply (VDD = 2.5V)
    - Input signal definitions with appropriate pulse parameters
    - Load capacitance (1fF)
    - Transient analysis parameters

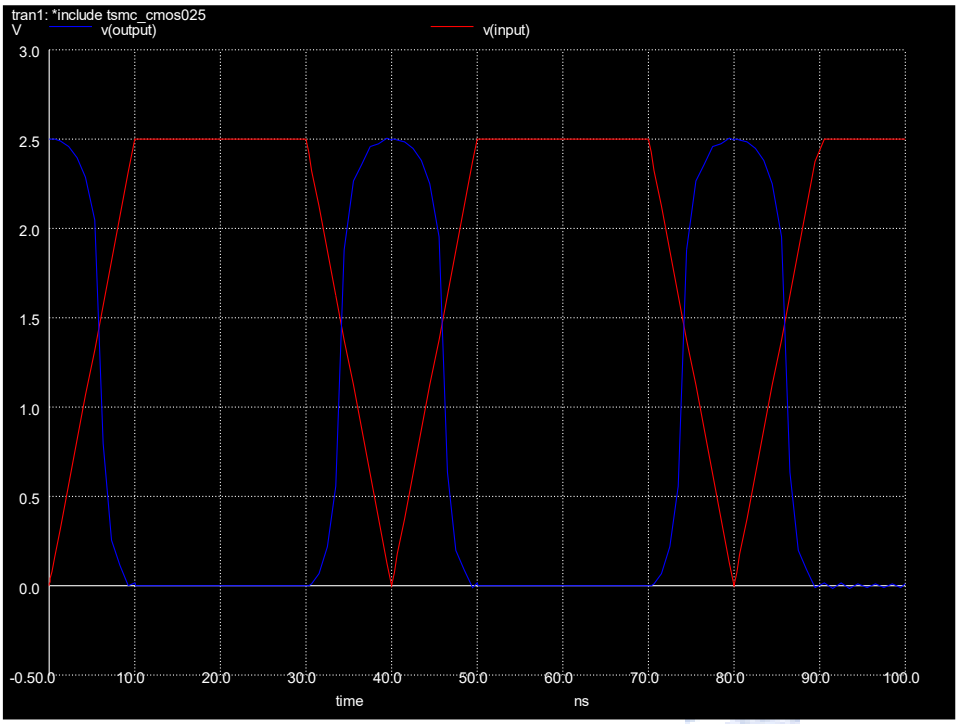
3. Simulation Results Analysis

The simulation results demonstrate proper functionality of all three circuits:

Inverter Analysis

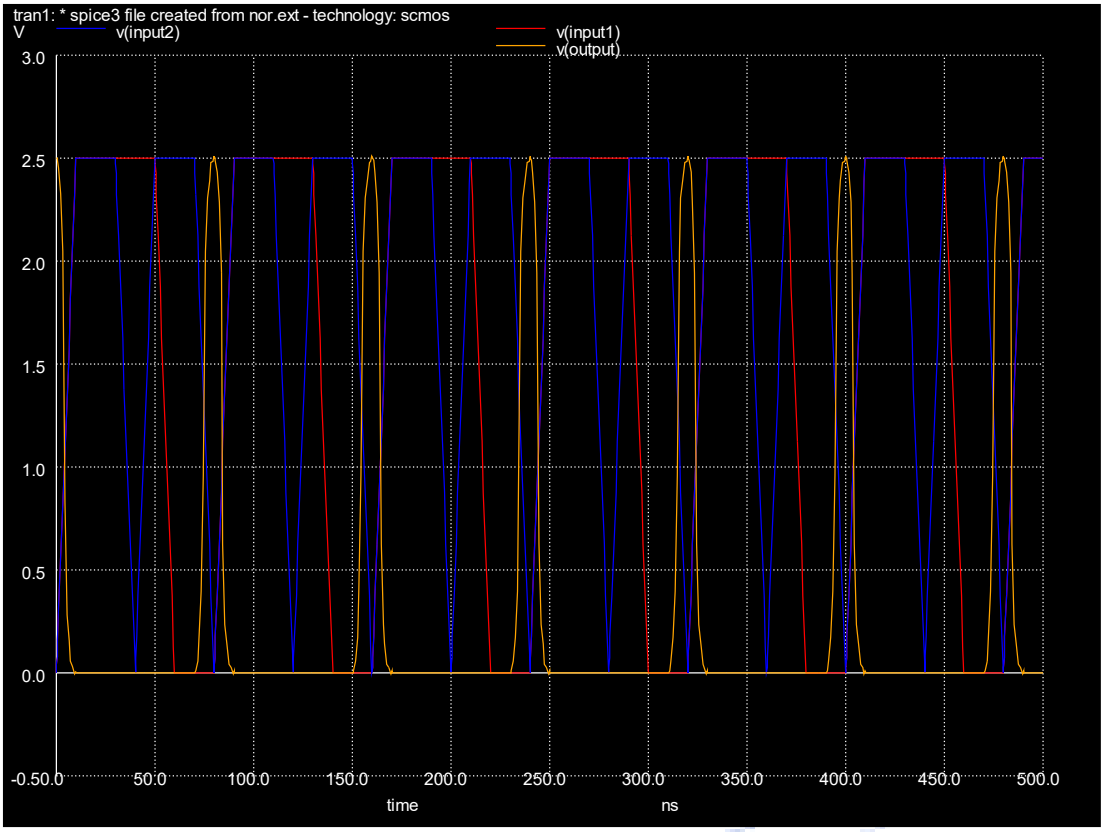
- The output shows correct logical inversion of the input signal
- Clean transitions between logic levels (0V and 2.5V)
- Acceptable rise and fall times with minimal delay
- The inverter showed fast switching with sharp transitions between high and low states. Propagation delay was very small, highlighting the efficiency of the inverter design.

- The W/L ratios (PMOS: 8λ/2λ, NMOS: 4λ/2λ) ensured strong pull-up and pull-down capabilities, allowing the output to transition quickly and efficiently.



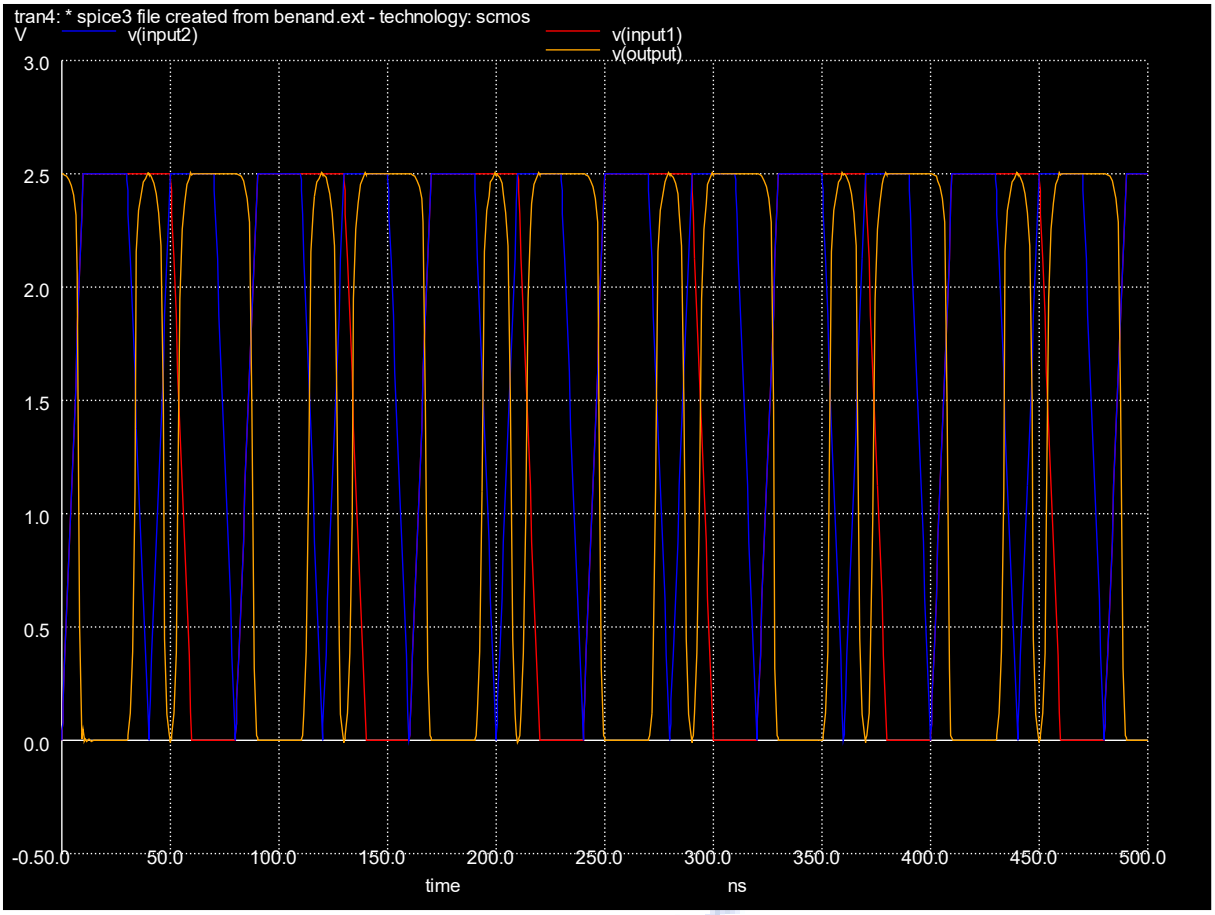
NOR Gate Analysis

- Output correctly implements NOR logic function
- Output is high (2.5V) only when both inputs are low
- Shows proper switching behavior with varying input combinations
- Maintains stable output levels during steady-state conditions
- The rise and fall times were within expected ranges, and the propagation delay was consistent with typical NOR gate performance. The PMOS transistors efficiently pulled the output high, while the NMOS transistors provided strong pull-down action.
- Similar to the NAND gate, the chosen W/L ratios (PMOS: 8λ/2λ, NMOS: 4λ/2λ) ensured efficient operation and proper logic levels at the output.



NAND Gate Analysis

- Demonstrates correct NAND functionality
- Output goes low only when both inputs are high
- Exhibits expected switching characteristics
- Shows good noise margins at both logic levels
- The output transitions were smooth with appropriate rise and fall times. Propagation delay was minimal and consistent with expected performance for the technology used.
- The W/L ratios (PMOS: 8λ/2λ, NMOS: 4λ/2λ) provided balanced performance, ensuring proper output charging and discharging.



All three circuits demonstrate successful implementation of their respective logic functions using TSMC 0.25µm technology, with proper voltage levels and switching behavior.