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VERSION 01

<DRAFT>

OSSAT OBC Dev Board Manual

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# Document History

Please see the following record of revisions:

|  |  |  |  |
| --- | --- | --- | --- |
| Document Revision | Document  Status | Change  Description | <SharePoint  Version> - |
| PA | DRAFT | First Version |  |
|  |  |  |  |

# Applicable Documents

The following references are applicable to this document.

|  |  |  |  |
| --- | --- | --- | --- |
| Document Reference | Document Title | Date | Notes |
| KS-SCH-01466  (.PDF) | OSSAT OBC Development Board Schematic |  | Schematic diagram |
| KS-SCH-01466  (.sch) | OSSAT OBC Development Board Schematic |  | Fusion 360 schematic source file, in ‘Eagle’ format |
| KS-SCH-01466  (.lbr) | OSSAT OBC Dev board library |  | Fusion 360 Library file in ‘Eagle’ format. Contains library definitions for parts used in the design. |
| KS-SCH-01466  (.xlsx) | OSSAT OBC Dev Board BOM with manufacturer data |  | Bill of materials for the board assembly |
| KS-BRD-01467  (.brd) | OSSAT OBC Development Board PCB |  | Fusion 360 PCB source file in ‘Eagle’ format |
| KS-BRD-01467  (.zip) | OSSAT OBC Dev Board PCB Manufacturing files |  | Gerber file set and PnP file |
| KS-BRD-01467  (.docx) | OSSAT OBC Dev Board Layer Stack-up |  | Defines the layer stack and pcb materials / thicknesses for the board |
| KS-DOC-01526  (.docx) | OSSAT OBC Dev Board Verification Procedure |  | Board Verification Test procedure, used to confirm board function after build. |
| KS-DOC-01529  (.docx) | OSSAT OBC Dev Board Build Document |  | Build process control document |
| KS-SOF-01541  (software) | Software to support h/w test of the OSSAT OBC dev board |  | Test Software |

# References

The following references are applicable to this document.

|  |  |  |  |
| --- | --- | --- | --- |
| Document Reference | Document Title | Date | Reference in this Document |
| KS-DOC-01073-01 | OSSAT Baseline document revision reference |  | [OSSAT Baseline] |

# Introduction

## Overview

The OSSAT OBC Development board provides a convenient hardware platform that collaborators can use, to develop satellite firmware.

The board is based upon the STM32 microcontroller and includes various interfaces for connection to other satellite sub-systems.

The board includes an STLink programmer/debugger interface to facilitate firmware development and debugging activities.

The design shares several attributes with a sister board that is being developed for a space application.

Figure 1 shows a view of the board.

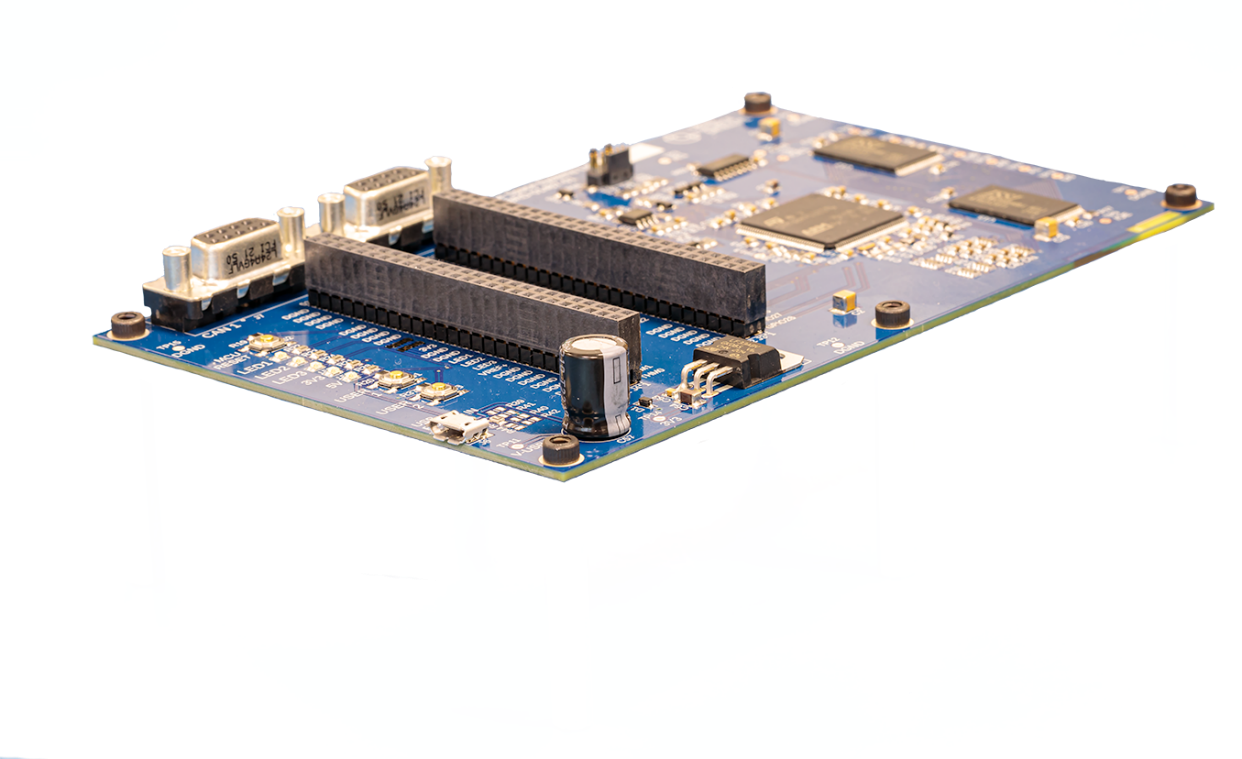


Figure View of Board

## Features

* STM32 Microcontroller (STM32H753ZIT)
* SRAM 4Mx16bit (8Mx8bit) CMOS Static RAM
* STLink Programming and Debug interface (with UART)
* 2x CAN Bus channels (with local 120R termination), with D-Sub (9 way sockets)
* 2x UART interface
* 8x Thermistor interface (10K Negative Temperature Coefficient)
* 31x General Purpose I/O lines
* Local 3V3 regulator, operating from USB supply, via Micro-USB connector
* MCU Reset Button
* 2x push-buttons for test use
* 3x status LEDs for test use
* 2x power status LEDs
* Real-time clock

Form Factor

The board is based upon a PC104 form factor (88.1mm x 94.5mm), with added area for additional items, to aide development activities. Hence it is Eurocard size: (160 x 100mm). Refer to Figure 2, below.

The red box within the figure demonstrates an approximate PC104 profile, and it can be seen that the core board functionality lies within that area.

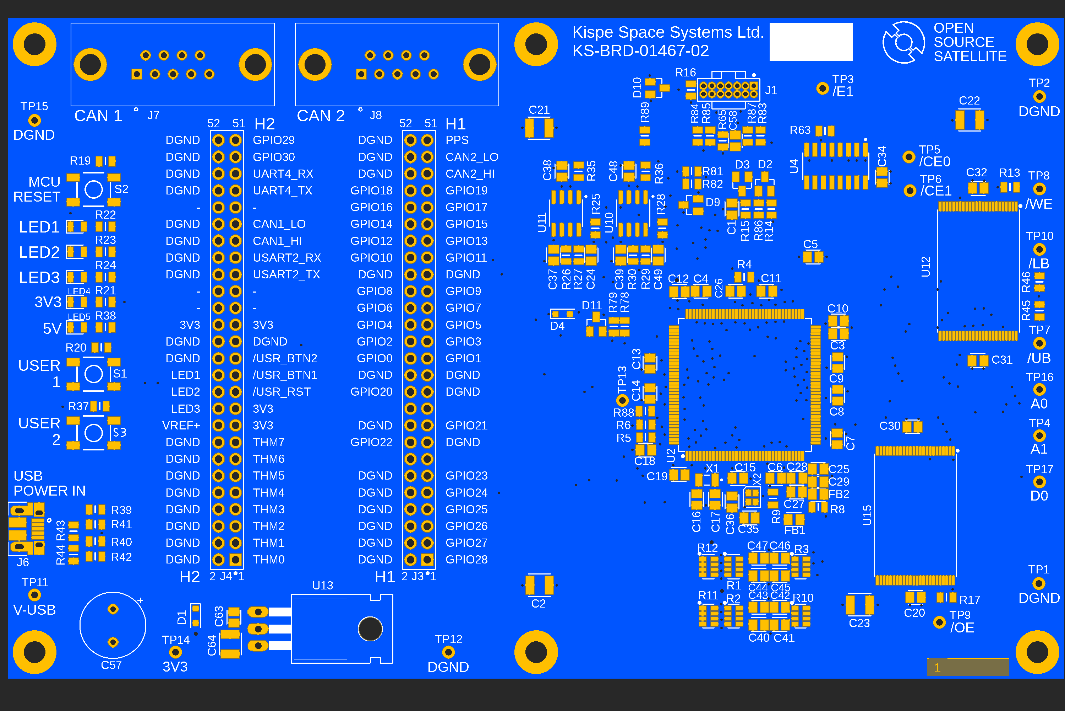


Figure PCB Form Factor

The normal PC104 connector has been split into two parts to enable adding descriptions of the pin functions, to the board silk screen.

## Design Documentation

The list of related design documentation is given in section 2.

It refers to several types of document as denoted by the file extension.

# Technical Details

## Board Overview

Figure 3 below shows a view of the fully assembled board. There are no components on the reverse side.

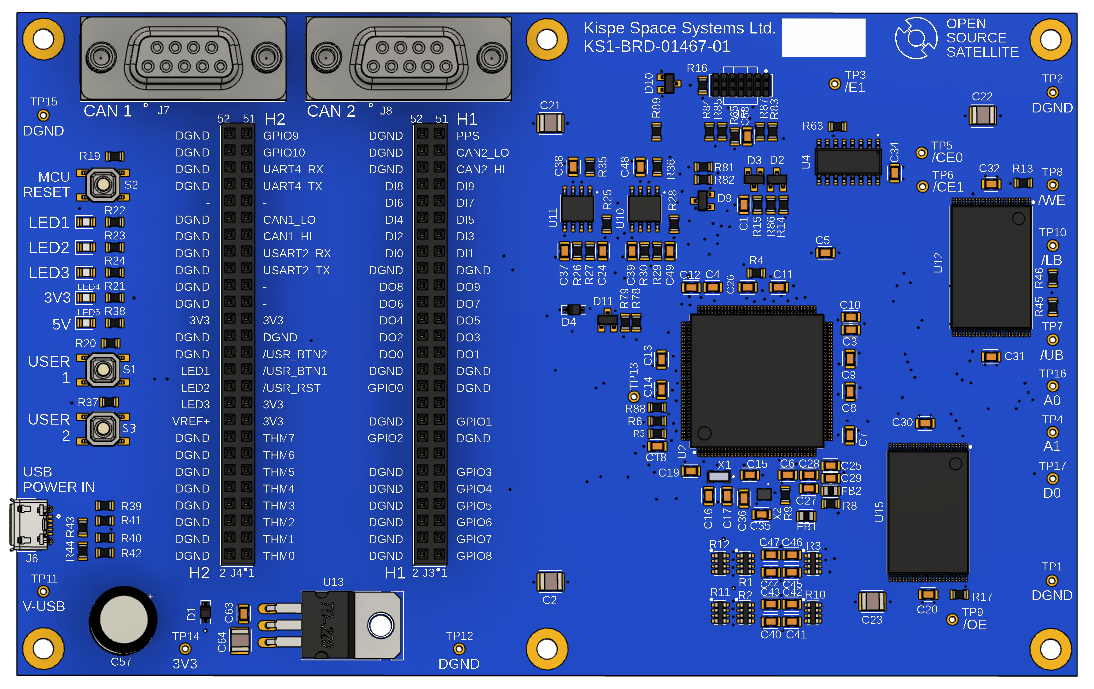


Figure View of Assembled Board

The block diagram for the Schematic is shown in Figure 4.

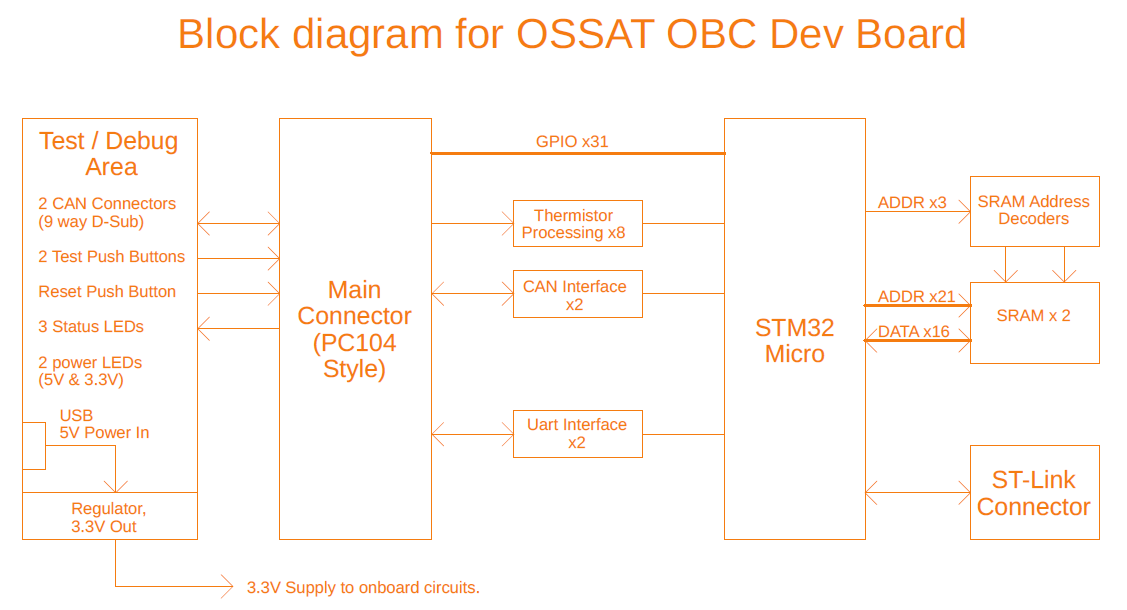


Figure Schematic Block Diagram

## STM32 Microcontroller (STM32H753ZIT)

The STM32 MCU includes a broad set of internal features, some of which are highlighted below:

* 32-bit Arm®-M7 core
* 2Mbyte onboard Flash
* 1Mbyte RAM
* Flexible Memory controller
* Power Management
* Watchdog
* Multiple communication peripherals, including CAN, I2C, SPI, UART
* ADC
* Timers and RTC
* Large number of I/O ports
* STLink / JTAG compatibility

Full details of the MCU are available from the manufacturers data sheet and reference manual, available from the STM web site. Refer to:

* DS12117: STM32H753xl Datasheet (32-bit Arm® Cortex®-M7 480MHz MCUs, 2MB Flash, 1MB RAM, 46 com. and analogue interfaces, crypto)
* RM0433: Reference manual, STM32H742, STM32H743/753 and STM32H750 Value line advanced Arm®-based 32-bit MCUs

## Power source

The board is designed to operate from a USB (5V) power source. Connection is via a Micro-USB connector on the board. Refer to Figure 5.

Current consumption is max 0.5A and typically less than 150mA. Hence standards USB outlets are suitable for providing power.

Note that the USB port does not have any signalling functionality. The only connectivity is power.



Figure Power Connection

The incoming 5V supply from the USB connector is regulated down to 3.3V, to feed the electronics circuits on the board. The 5V input does not feed anything else.

## Clocks

The MCU has an extensive internal clock system and Figure 6, shows just part of it. The configuration options are very flexible.

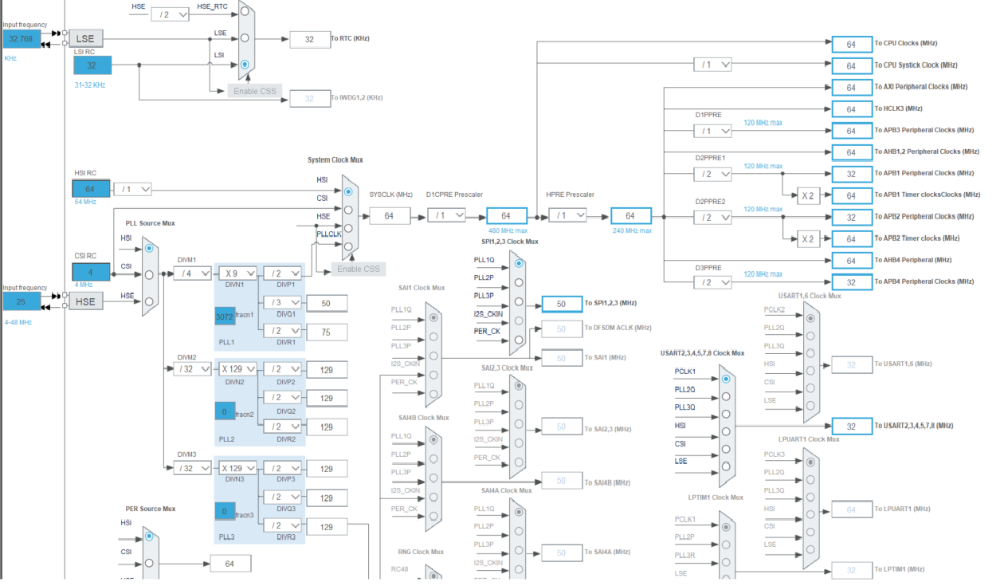


Figure Partial View of Clock System

The MCU has its own on-board oscillators that are used at initial start-up. These allow firmware to be downloaded and run, but timing accuracy will not be particularly good. The crystal oscillators will not function, until firmware is loaded and explicitly turns them on.

The board has two crystal oscillators:

* 25MHz, used for main functions (and can be used for RTC)
* 32.768KHz, used for the Real Time Clock function.

The MCU has a Real Time Clock, whose timing can be derived from one of several sources, included either of the crystals. As this is a development board, there is no auxiliary power source to maintain the clock when power is turned off.

One of the MVCU pins can be configured to provide a Pulse Per second timing source, as required by some systems. This output functions with the test firmware provided by Kispe.

## SRAM 4Mx16bit (8Mx8bit) CMOS Static RAM

The board has 2 SRAM devices for general purpose use. The type currently fitted is ISSI IS61WV204816

They are volatile, so will lose their data when power is removed. Note that the sister board, intended for flight, uses MRAM devices which are non-volatile, but are expensive.

These devices use a parallel bus and are operated by the flexible memory controller (FMC), in the MCU. The FMC permits access as 8 or 16 bits.

Our test software has an example of how to configure these for use. Access times are conservative (>40ns), to ease compatibility with other hardware.

A number of Test Points are included in the design, to aid debugging, if required.

## STLink Programming and Debug interface (with UART)

The STLink interface provides a convenient method if interfacing to a PC, for programming, test and debugging.

To use this interface, you need an STLINK-V3SET made by STM. This is reasonably cheap (<£40) and available from common electronics suppliers. Figure 7 shows the STLink adaptor.

A close-up of a circuit board

Description automatically generated with low confidence

Figure STLink Top View

The STLink is supplied with a short ribbon cable that will connect directly to a 14way micro-header on the OSSAT Dev board. Connection to the PC is via a standard Micro-USB cable and this provides power and comms. Figure 8 shows the underside of the STLink adaptor, with the ribbon cable connected to the OSSAT OBC Dev Board.

A picture containing text, electronics, circuit

Description automatically generated

Figure STLink Connection to OSSAT OBC Dev Board

The STLink is used in conjunction with the STMCube PC app, that allows firmware download and debugging. A typical view of this app is shown in Figure 9.

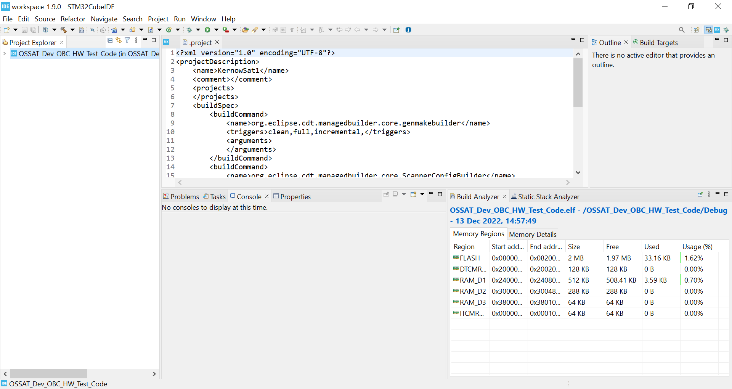


Figure STMCube App

The STLink interface includes a UART (UART3 on the MCU) that can be accessed separately from the PC, e.g. by using a terminal emulator. To implement this, proceed as follows:

1. Ensure the STLink is plugged into the OSSAT Dev board and PC and that the Dev board is switched on.
2. Start a terminal emulator program (e.g. Terraterm).
3. Go to the option for selecting the com port and select the STLink comm port. See Figure 10
4. Set the serial parameters: Typically 115200, 8, N, 1 no flow control. See Figure 11

Once the serial port is set-up, a test menu should appear following a board reset. See Figure 12. Further details are available in the software documentation.

A screenshot of a computer

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Figure Setting Com Port for STLink Terminal

A screenshot of a computer

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Figure Serial Port settings for STLink Terminal

A screenshot of a computer

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Figure Test Menu on STLink Terminal

## 2x CAN Bus channels (with local 120R termination), with D-Sub (9 way sockets)

This board provides two CAN bus interfaces. The CAN Bus is advocated by Kispe for future serial communications within small satellites, because it has several advantages over other alternatives:

* It uses robust differential signalling (rather than ground referenced signalling). This provides good data integrity and low EMI emissions
* There is good availability of buffer chips with automotive temperature range (-40 to +125C)
* Multi-drop
* Built-in error detection
* Good speed / cable length e.g. it can achieve 1MB/sec over 40 metres

Connection is via the 9way D-Sub female connectors (using standard pinout) and the signals are also wired in parallel to the PC104 connectors.

The transceivers on this board operate at 3.3V. Each transceiver has 120 Ohm termination configured as a pair or 60R series resistors, with the centre capacitively coupled to ground, to minimise common mode noise.

The CAN interfaces operate from MCU CAN channels 1 & 2.

It is recommended to have a CAN bus analyser available, to test the CAN buses. This can be connected to the D-Sub connectors.

## 2x UART interface

The board includes two UART ports for general use. These have 3.3V signalling. To reduce The transmit reflections, the TX lines have mild serial termination, while the receive lines include diode termination, which is moderately effective.

Take care not to apply signals that are outside ground or 3V3.

Care should be taken with the connectivity of the UART signals, because they are ground referenced. Either keep signals short, or preferably utilise differential signalling by connecting suitable buffers, e.g. RS422 or RS485.

## 8x Thermistor interface (10K Negative Temperature Coefficient)

The design includes 8x channels for thermistor temperature measurement. The channels are designed to operate with for 10K Ohm (at 25C) Negative Coefficient thermistors, e.g. Measurement Specialists 44006RC. This gives a usable temperature range from below -40C to over 100C. The datasheet for this particular device includes resistance values across its temperature range.

The thermistors should be directly connected and do not require any additional supplies or signal conditioning. The OBC drives the thermistors via on-board 10K pull-up resistors, to produce voltages that are fed into ADCs on the MCU. The signal path includes moderate filtering to reduce noise, however it is suggested that the signals are over-sampled for best noise immunity.

The main 3.3V logic supply is used for both the thermistor power source and the ADC reference, so any voltage fluctuations will self-cancel. The ADC on the MCU should be configured to run over the full 3.3V range. The thermistor circuits are ratiometric, so fluctuations on the supply rail will self-cancel. Hence the MCU on-board voltage reference is not used.

The calculation for the ADC reading is: Rthermistor / (10K+ Rthermistor) x ADCfull-scale.

For example, with an 8bit system and the thermistor listed above at 50C, the thermistor value will be 3.893K Ohm. The ADC output will be 3893/(10000+3893)\*255 = 71, or 47Hex.

## 31x General Purpose I/O lines

The board has 31 general purpose I/O lines that are routed directly to the PC104 connectors. As GPIO lines they can be configured as inputs or outputs, as required, with options to allply pul resistors on inputs, and change drive type on outputs.

If required, the selected GPIO lines can also be allocated to specific peripheral functions on the MCU, including the following:

* Timers
* UARTs
* SPI
* I2C

The use of SPI and I2C may be attractive, but these busses use ground-referenced signalling, which is undesirable for satellites and is therefore discouraged by Kispe. Kispe advocates using the CAN buses for serial communications where possible.

## Debugging Functions

The board includes the following functions to aid debugging:

* MCU Reset Push-Button
* 2x power status LEDs
* 2x push-buttons for general use
* 3x status LEDs for general use

The image in Figure 13shows the Test and I/O area, with a connection to Termistor channel THM04

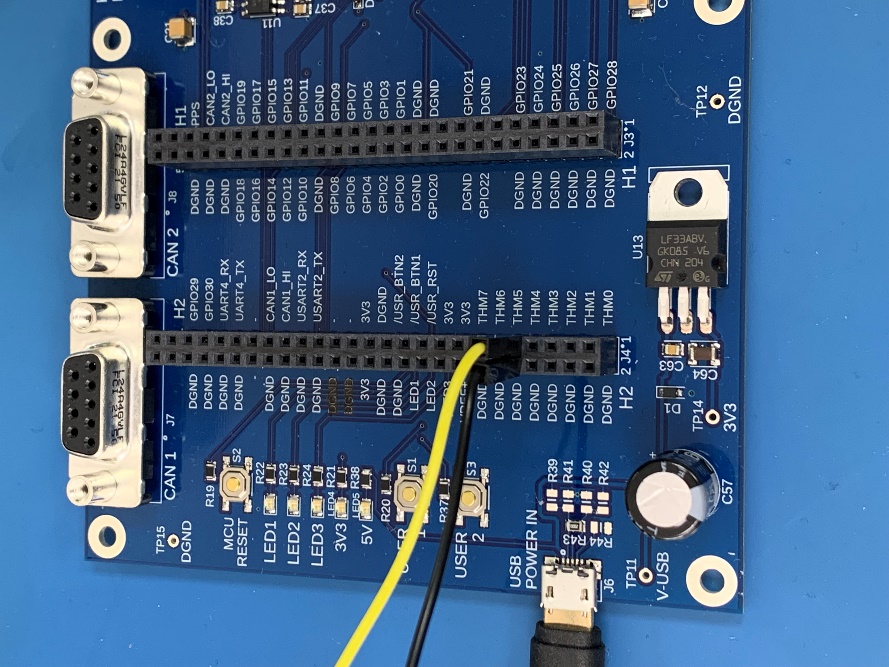


Figure Dev Board Test and I/O Area

The MCU Reset Push-Button is hard-wired to the MCU reset pin. Momentarily pressing the button will reset the MCU..

The 2 power status LEDs are driven directly, via hardware, from the 5V and 3.3V power rails. They confirm power status for those power rails. Note the board also includes Test Points that permit voltages to be measures, if desired.

The two push buttons may be used as desired. **If they are used, then ensure the MCU internal pull-up resistors are turned on.** The basic test firmware supplied by Kispe operates reads these buttons as described in the PCB Verification Document.

The three status LEDs may be used as desired. An active high output on the relevant MCU pin will turn the LED on.

The basic test firmware supplied by Kispe reads the buttons and drives the LEDs, to confirm their function.

# Build and Test

## ESD Precautions

Full ESD precautions must be observed throughout the processes of component handling, build and testing. Failure to observe such precautions could potentially result in component damage or incorrect function.

## Schematic

The Schematic shows the full circuit diagram for the board. Page 1 has a block diagram that provides an overview. The last page contains the revision history

The top left corner of each sheet describes the content of each page.

Connections between sheets and between certain signals within a sheet are denoted by using either power signals or boxed labels.

## BOM

A full bill or Materials for the board is provided as an Excel spreadsheet. This includes Manufacturer information and also shows UK vendor information.

## PCB

The pcb is designed as a 6 layer board, with internal ground planes. It is 1.6mm thick, size 160mm x 100mm. The outer surfaces have a copper flood to ease manufacture of the bare board. Copper is 1oz. Due to density the most narrow tracks & gaps are 0.006. There are no blind vias. Kispe has used blue solder resistor to enable the board to match the project colour scheme. The top and bottom views of the bare board are shown in Figure 14 and Figure 15.

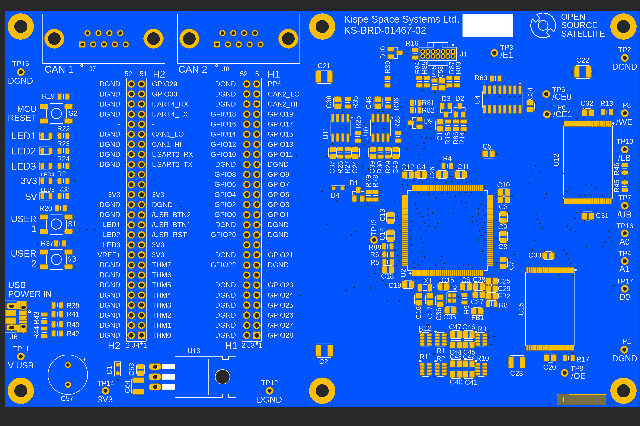


Figure Top view of Bare PCB

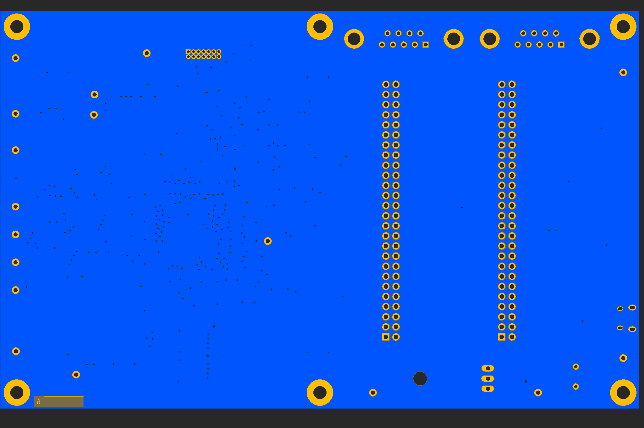


Figure Bottom view of Bare PCB

The manufacturing files for the board are:

* Set of Gerber files
* Drill files
* Set of Pick and Place files
* KS-BRD-01467-02 PCB Layer Stack-Up for OSSAT Dev Board

The Layer Stack-up document provides full details of materials, thicknesses and layer order for the board.

## Assembly

The board only has components on one side, which eases assembly. It has a mix if surface mount and through-hole parts. It can be built using normal assembly techniques.

There are no specific assembly requirements for this board. Please note that the Micro-USB connector is right at the edge of the board, so be careful to ensure it is correctly positioned.

## Test

Once built, the board should be tested in accordance with Kispe; KS-01526-02 Dev Board Verification Procedure. This includes loading the Test firmware and verify correct functionality of the board. The test document lists the test equipment that is required.

To ease test complexity, the some tests use simplified methodologies that operate in conjunction with the Kispe test Firmware. For example the thermistor channels actually configure the ADC pins and digital outputs during the test function, because this not only confirms correct connectivity, but also simplifies verification of the filter components.

# 

# Using the Board

## ESD Precautions

Full ESD precautions must be observed throughout the processes of component handling, build and testing. Failure to observe such precautions could potentially result in component damage or incorrect function.

## General

The board is intended to be used in a laboratory environment.

It is strongly recommended that the board be mounted on 6 short legs (or M3 pillars) or has rubber feet attached to the underside, so it is clear of the bench.

## General Precautions

Please follow the following advice:

* Prior to making any connections, ensure the equipment being connected is turned off.
* Do not exceed 3.3V on any signal connections to the OBC. The GPIO does not have specific over-voltage protection.
* Avoid having the OBC powered down, when connected to external interfaces that are turned on.

## Connection and Configuration

The main interfaces of the board are described in previous sections.

The test buttons and LEDs have specific functions when running the test firmware, but at other times the user is free to reallocate their usage as desired.

Not that the 5V and 3.3V LEDS are hard-wired, so their function cannot be changed.

Connection to the interfaces is via the 9 way D-Sub connectors (CAN Bus) and the two 52 way connectors.

When using the interfaces provided, be sure to configure the MCU correctly. This requirement includes:

* MCU internal operating voltages
* Clocks and operating frequencies
* Flexible memory controller
* CAN and Serial ports
* GPIO
* ADC (Thermistor channels)

The setup requirements include configuring characteristics of ports in use, including input pull resistors and output drive characteristics. **In particular, ensure the MCU internal pull-up resistors are turned on for the Test push-buttons, if they are to be used.**

A screenshot of a cell phone

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