

Sheet: FPGA_JTAG_SPECIAL_PWR

File: FPGA_JTAG_SPECIAL_PWR.sch

Sheet: Buzzer_LEDs

File: Buzzer_LEDs.sch

Vbatt Sheet: FPGA

FPGA

File: FPGA.sch

Sheet: Sensors

fo
50xfo
4.65x

Diff Press

Flow Press

Pat Press

File: Sensors.sch

Sheet: Power Supplies

Σ

+5V

—|>

+5V_SENSE

+3V3

—|>

+3V3-ALWAYS-ON

File: Power_Supplies.sch

USB
→→
+5V

Key Pad

Display

BUF

Sheet: Microcontroller

MCU

File: Microcontroller.sch

USB

JTAG

↑↑
SWD↑↑
UART

Sheet: JTAG

BUF

JMPR

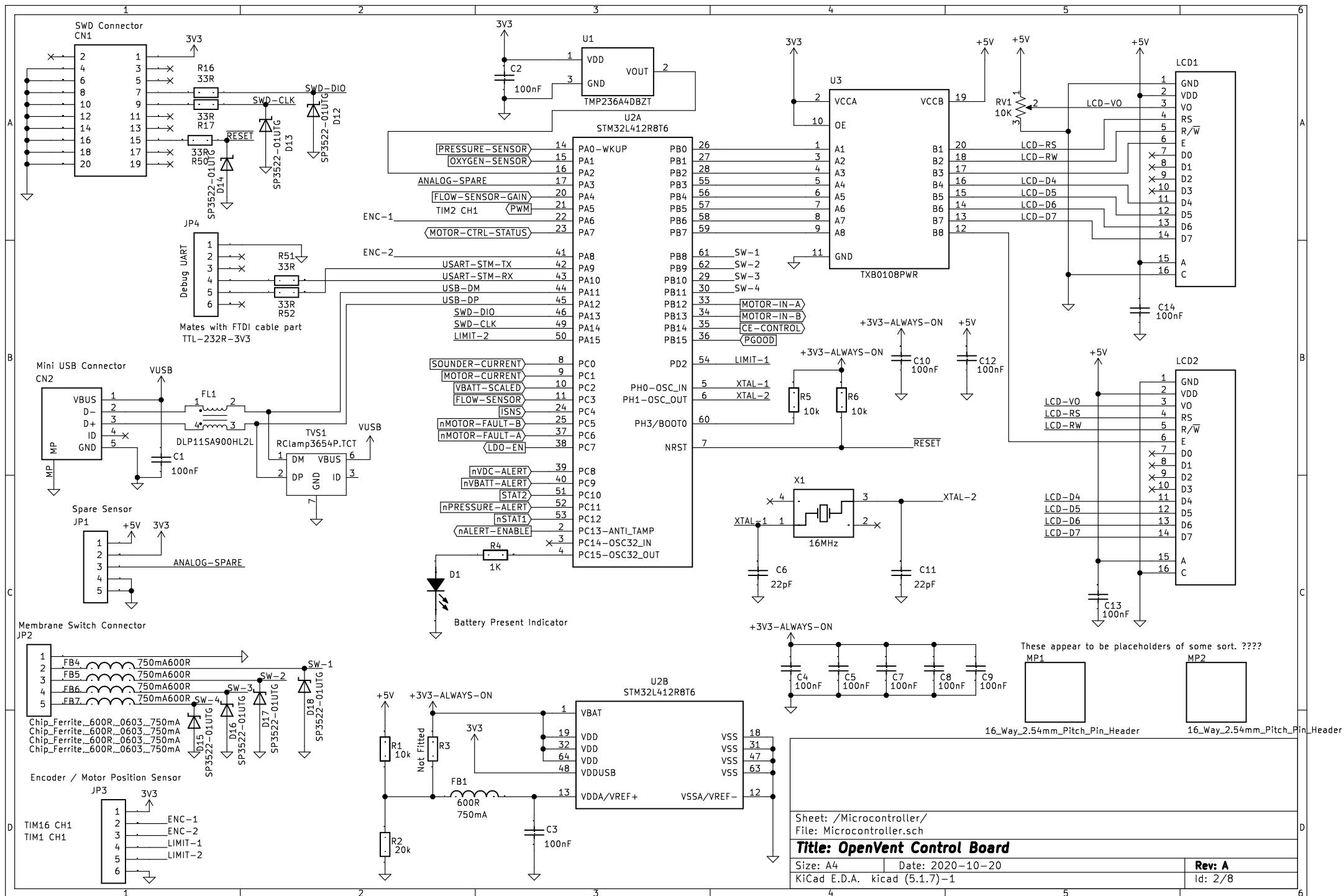
BUF

FTDI
JTAG

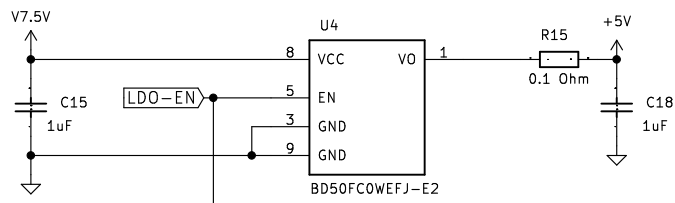
USB-JTAG

File: JTAG.sch

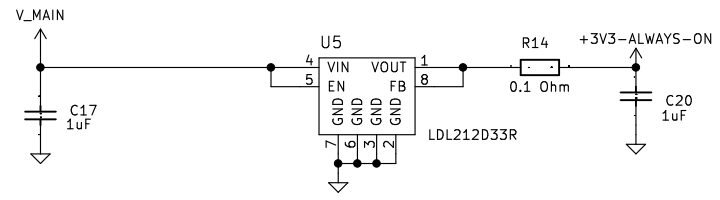
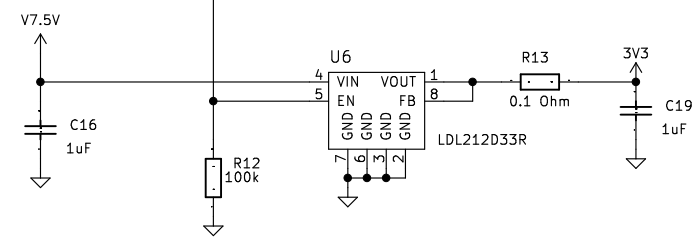
Sheet: /
File: OpenVent.sch**Title: OpenVent Control Board**Size: A3 | Date: 2020-10-20
KiCad E.D.A. kicad (5.1.7)-1Rev: A
Id: 1/8



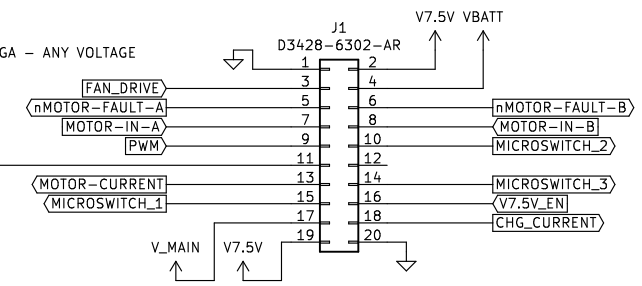
VBATT DOESN'T NEED TO GO INTO MCU IF GOING INTO FPGA
OXYGEN SENSOR MAYBE DOESN'T NEED TO GO TO MCU?



motorcurrent has to go to fpga VIA ADC
(NO NEED TO AMPLIFY) RANGES FROM
0 V TO 5 V DEPENDING ON THE CURRENT GOING TO THE MOTOR

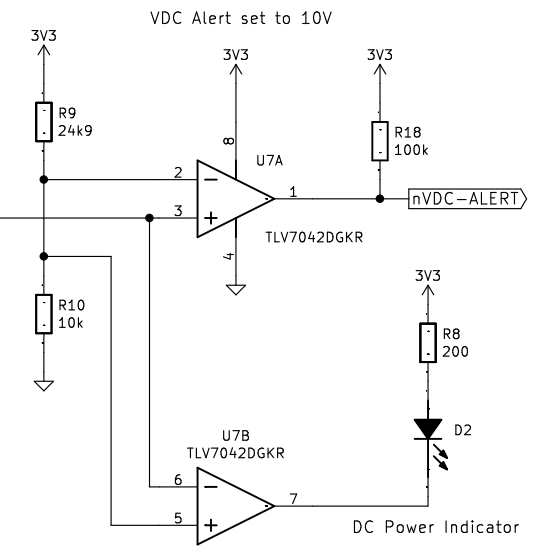


FAN DRIVE NEEDS TO BE GENERATED BY FPGA – ANY VOLTAGE



7.5V EN IS LOGIC TO TURN P
CHARGE CURRENT MAY HAVE
BUFFERED THROUGH AN AM
GOES INTO ADC TO FPGA. J

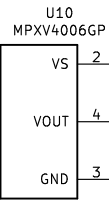
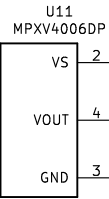
ALL MICRO SWITCHED (LIMIT SWITCHED ON THE GEAR BOX ON THE MOTOR) NEED TO GO TO FPGA. PULL UPS TO WHATEVER LOGIC INPUT



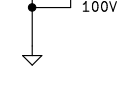
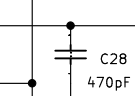
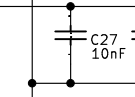
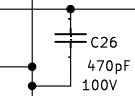
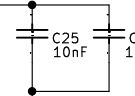
SCALE BATTERY VOLTAGE FOR FPGA

Alternative Flow Sensor Connector

CN4



+5V

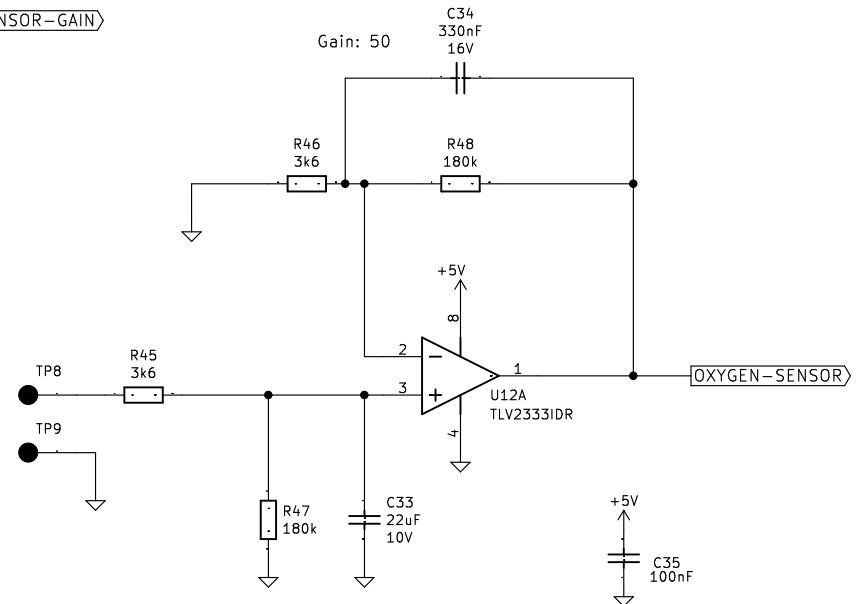
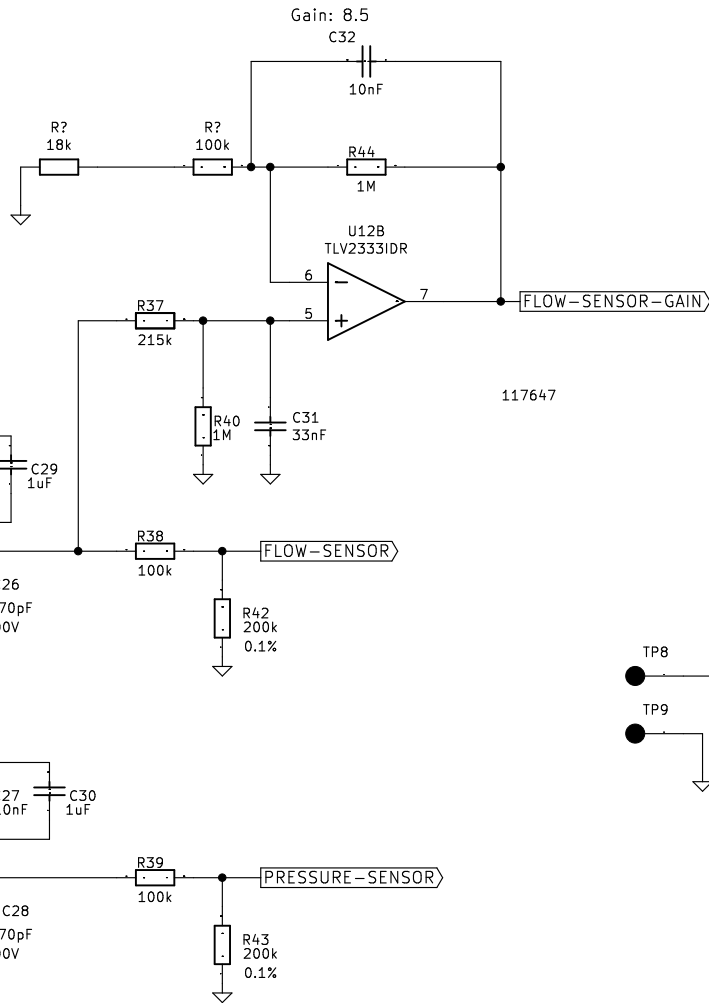


MAKE TWO OF THE 6GP

Darren's Flow sensor, maybe plus opamps or whatever is needed

<https://drive.google.com/file/d/1mZiFeJ4HfEkPdwHjtiVVL5XULqvMIZ-r/view>

Speak with DON ABOUT THE LACK OF PINS FOR EXTRA SENSOR



Sheet: /Sensors/
File: Sensors.sch

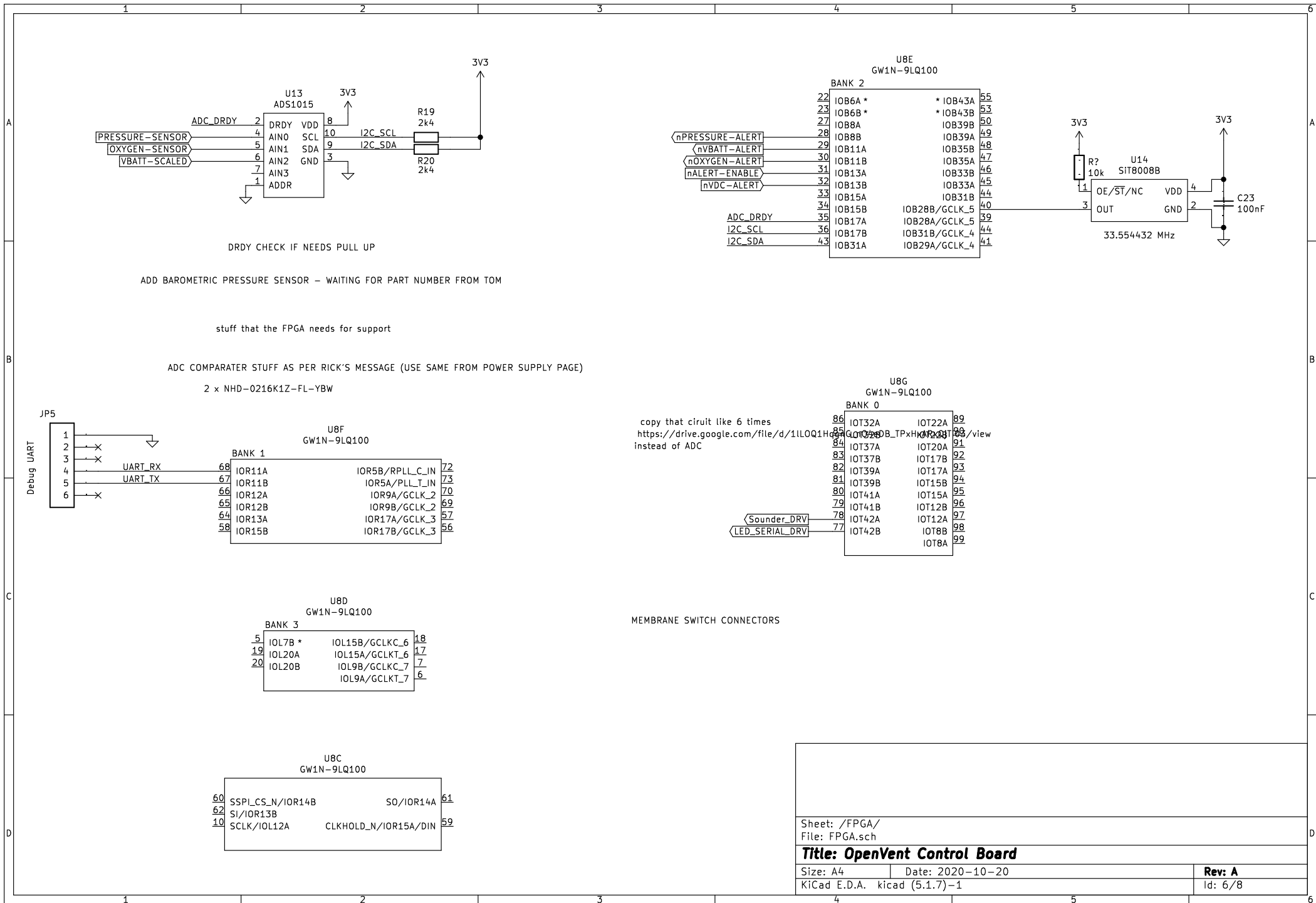
Title: OpenVent Control Board

Size: A4 Date: 2020-10-20

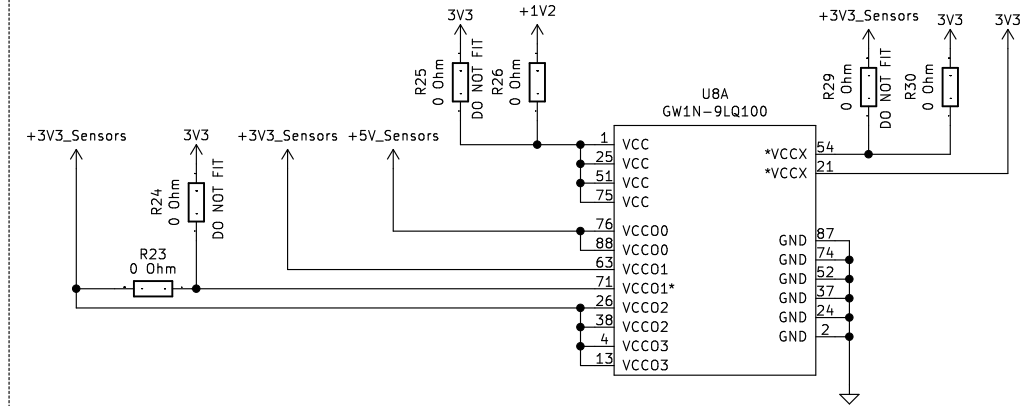
KiCad E.D.A. kicad (5.1.7)-1

Rev: A

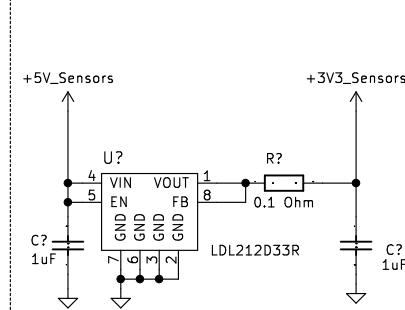
Id: 4/8



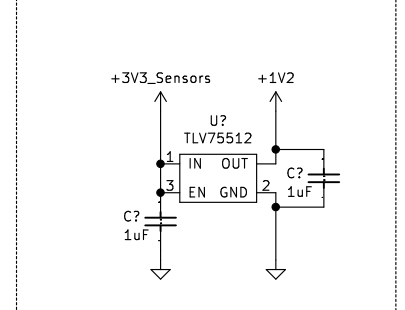
FPGA Power Block



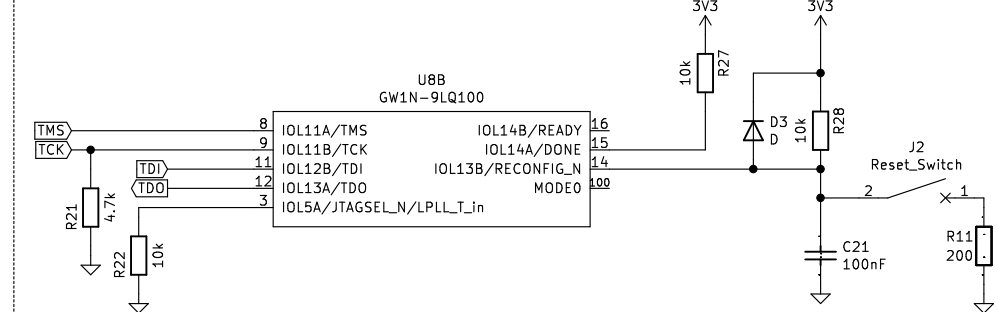
+5V to 3V3 LDO for ADC and 3V3 sensors



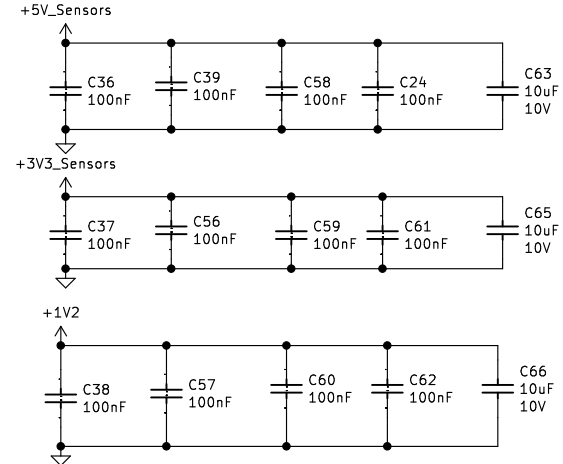
3V3 to 1.2 LDO for VCC



FPGA JTAG



Bypass Caps for Power Block



Sheet: /FPGA JTAG SPECIAL PWR/
File: FPGA_JTAG_SPECIAL_PWR.sch

Title:

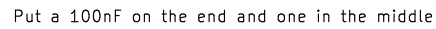
Size: A4

Date:

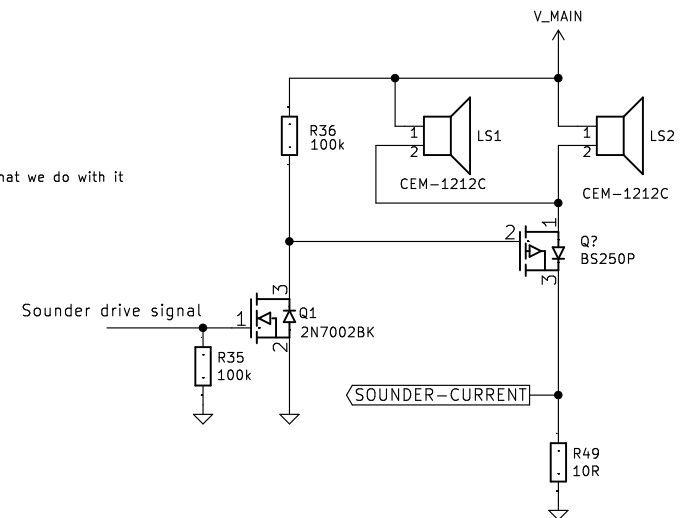
KiCad E.D.A. kicad (5.1.7)-1

Rev:

Id: 7/8



Sounder current coming into pin 8 on the micro



Rev:
Id: 8/8