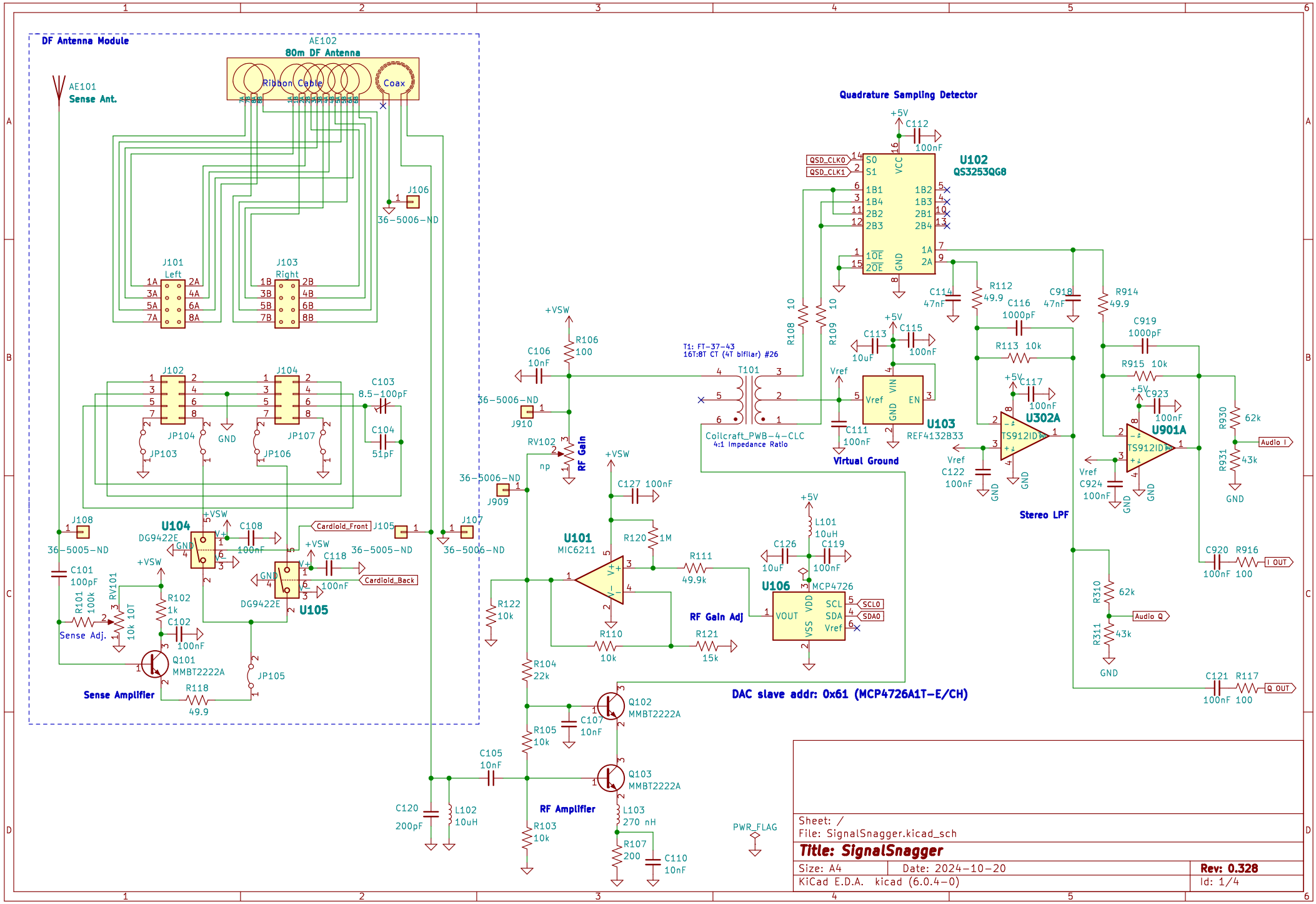
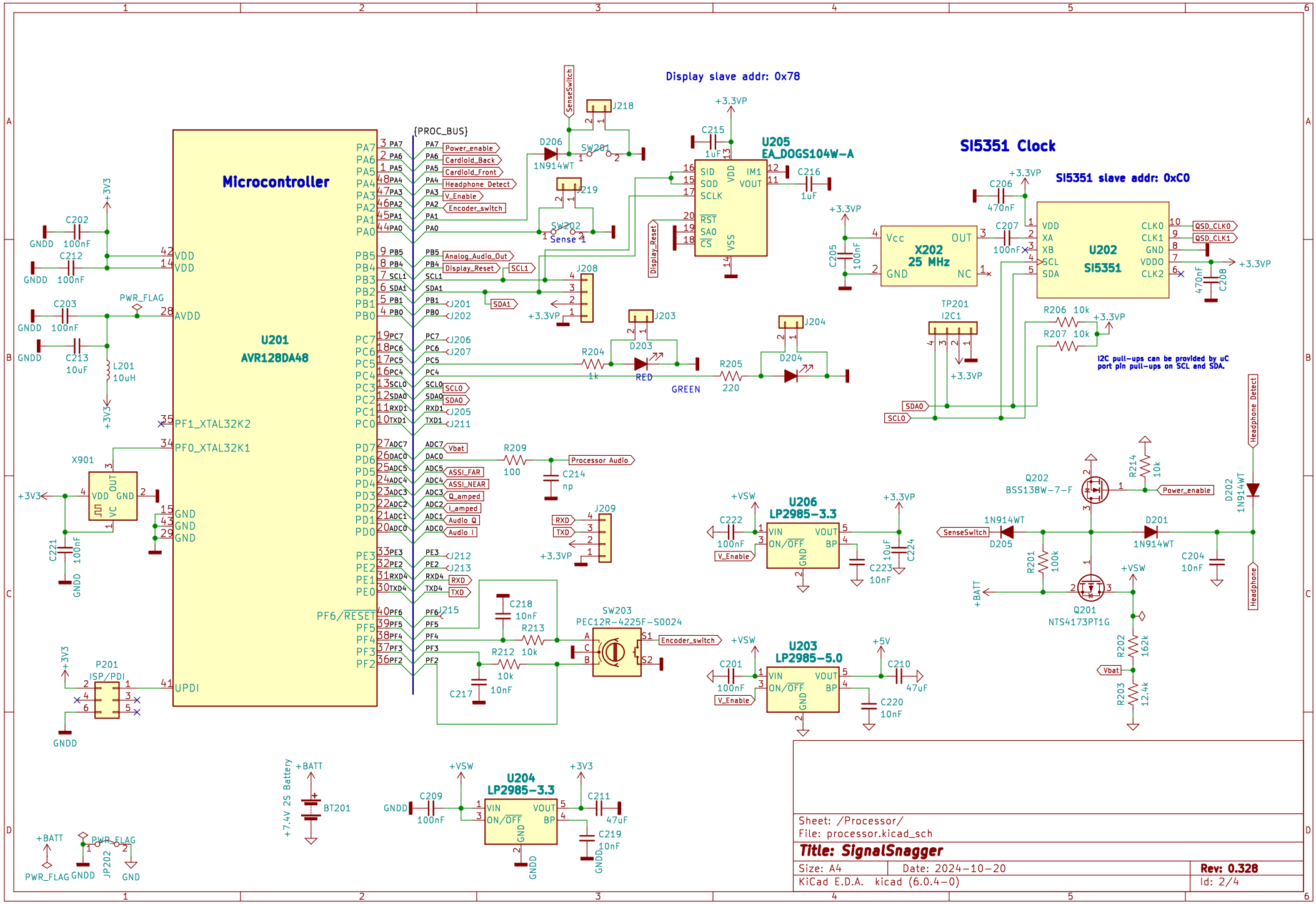
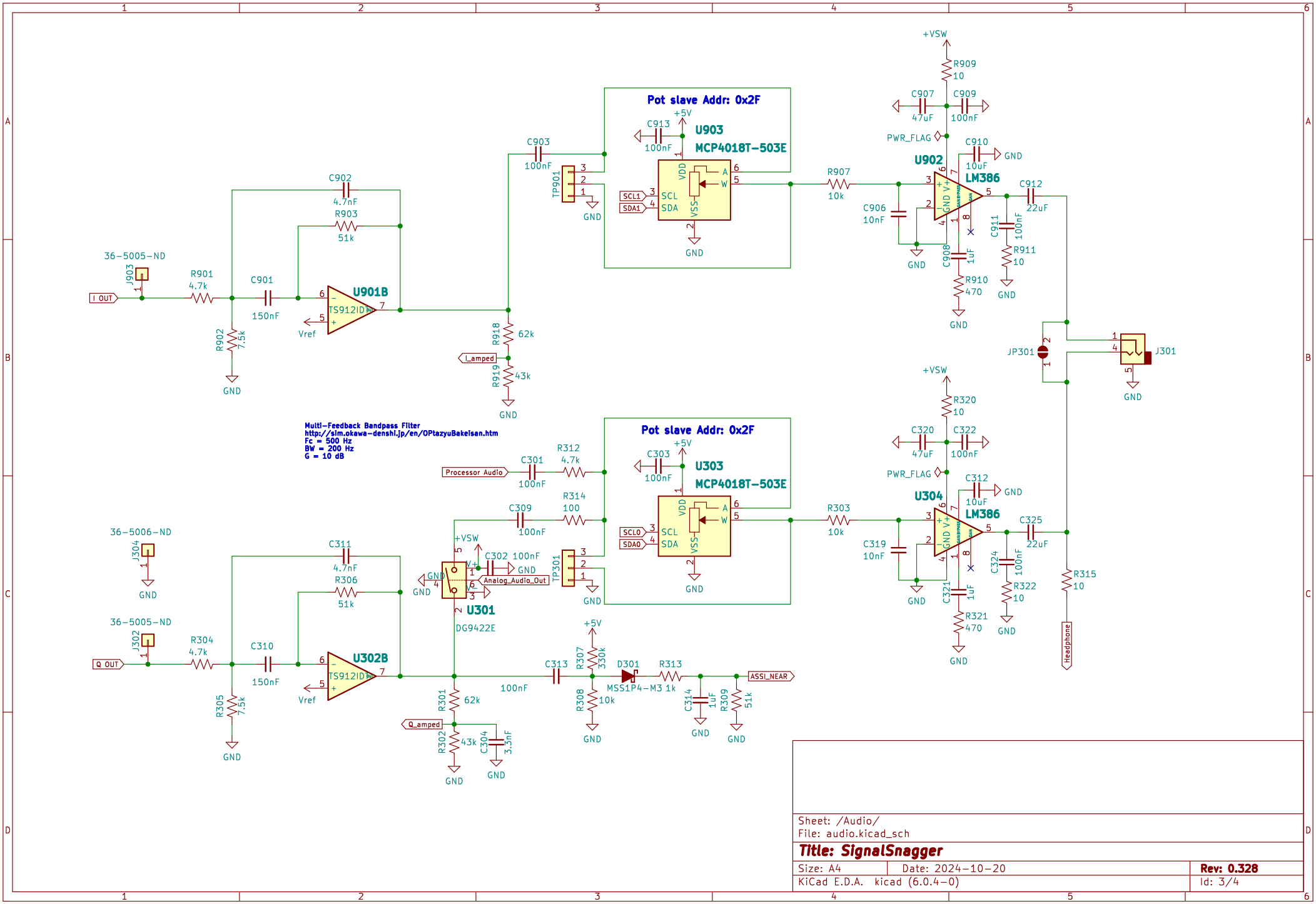


Sheet: /
File: SignalSnagger.kicad_sch

Title: SignalSnagger

Size: A4	Date: 2024-10-20	Rev: 0.328
KiCad E.D.A. kicad (6.0.4-0)		Id: 1/4


Microcontroller
U201
AVR128DA48
{PROC_BUS}
Display slave addr: 0x78
U205
EA_DOGS104W-A
SI5351 Clock
SI5351 slave addr: 0xC0
U202
SI5351
X202
25 MHz
TP201
I2C1
i2C pull-ups can be provided by uC port pin pull-ups on SCL and SDA.
U206
LP2985-3.3
U203
LP2985-5.0
U204
LP2985-3.3
Q202
BSS138W-7-F
Q201
NTS4173PT1G
SW203
PEC12R-4225F-S0024
P201
ISP/PDI
X901
BT201
+7.4V 2S Battery
JP202
Sheet: /Processor/
File: processor.kicad_sch
Title: SignalSnagger
Size: A4
Date: 2024-10-20
Rev: 0.328
KiCad E.D.A. kicad (6.0.4-0)
Id: 2/4


Pot slave Addr: 0x2F
U903
MCP4018T-503E
Pot slave Addr: 0x2F
U303
MCP4018T-503E
U901B
TS912IDT
U302B
TS912IDT
U902
LM386
U304
LM386
U301
DG9422E
Multi-Feedback Bandpass Filter
http://sim.okawa-denshi.jp/en/OPtazyuBakeisan.htm
Fc = 500 Hz
BW = 200 Hz
G = 10 dB
I OUT
Q OUT
I_amped
Q_amped
Processor Audio
Analog_Audio_Out
ASSI_NEAR
Headphone
36-5005-ND
36-5006-ND
MSS1P4-M3
Vref
+VSW
+5V
PWR_FLAG
GND
Sheet: /Audio/
File: audio.kicad_sch
Title: SignalSnagger
Size: A4
Date: 2024-10-20
Rev: 0.328
KiCad E.D.A. kicad (6.0.4-0)
Id: 3/4

Knob401

Note for reference only and use
the pins #'s in the root page of
the schematic. Reason pin 7 and 8
were swapped: to get proper
phasing of this sense loop.

Sheet: /Antenna Diagram/
File: antenna_diagram.kicad_sch

Title: SignalSnagger

Size: A4	Date: 2024-10-20	**Rev: 0.328**
KiCad E.D.A. kicad (6.0.4-0)		Id: 4/4