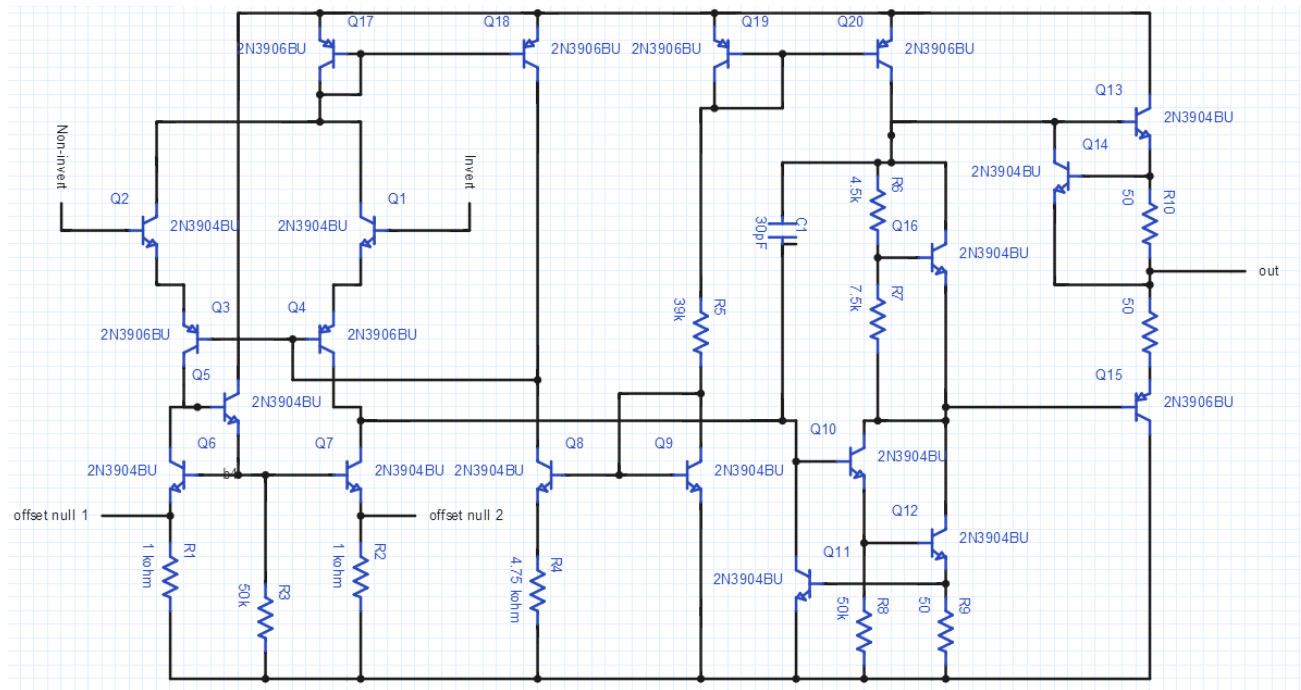


## SEVENTYFOURFUN



A small-scale integrated circuit, the 741 op-amp shares with most op-amps an internal structure consisting of three gain stages:

1. Differential amplifier — provides high differential amplification (gain), with rejection of common-mode signal, low noise, high input impedance, and drives a
2. Voltage amplifier — provides high voltage gain, a single-pole frequency roll-off, and in turn drives the
3. Output amplifier — provides high current gain (low output impedance), along with output current limiting, and output short-circuit protection.

It's that easy!

Well, not really.

WARNING: You should understand the basic equations that rule transistors

$$I_C = \beta I_B$$

$$I_E = (1 + \beta) I_B$$

## What the Heck is a Differential Amplifier Anyhow?

### [Current Mirrors]

Well, before we get into a differential amplifier we must understand the analog building block called a current mirror. A current mirror is a circuit of the configuration in Figure 1. Start with a current  $I_{ref}$  which flows into the transistor Q1. A transistor with its collector tied to its base is called a “diode connected transistor” this creates an ideal diode. In turn, this produces a voltage drop across the transistor Q1 of  $V_{be}$  (about 0.7 volts). Now, since the base and emitter of Q2 is identical and the base-emitter voltage of the transistor Q2 equals the transistor Q1, the same current that flows through Q1, flows through Q2...Well...roughly the same. As you can see the  $I_{mirror}$  is a factor of  $\frac{\beta}{\beta+2}$  which works out to be 98% of the current of Q1.

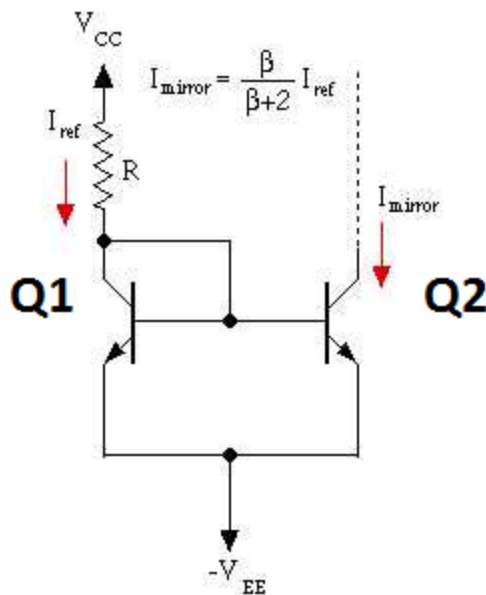


Figure 1

To derive the  $I_{mirror}$  equation:

$$I_{ref} = I_B + I_C$$

$$I_{ref} = I_B + \frac{\beta I_B}{2}$$

$$I_{ref} = \frac{1}{2} I_B [2 + \beta]$$

Therefore,

$$I_B = \frac{2I_{ref}}{2+\beta}$$

$$I_{mirror} = \frac{\beta I_B}{2}$$

$$I_{mirror} = \frac{2\beta I_{ref}}{2(2+\beta)}$$

$$I_{mirror} = \frac{\beta I_{ref}}{\beta+2}$$

### [Differential Amplifiers]

Let me confuse you first and overstate the simplicity of its operation by saying that, simply put, a differential amplifier is a type of amplifier that only amplifies the difference between two voltages and nothing more (idealistically). Besides using different variation of the word amplify and simply way too many times in that last sentence – its operation is a little more complex than I've led you to believe thus far... Lets get into the detail.

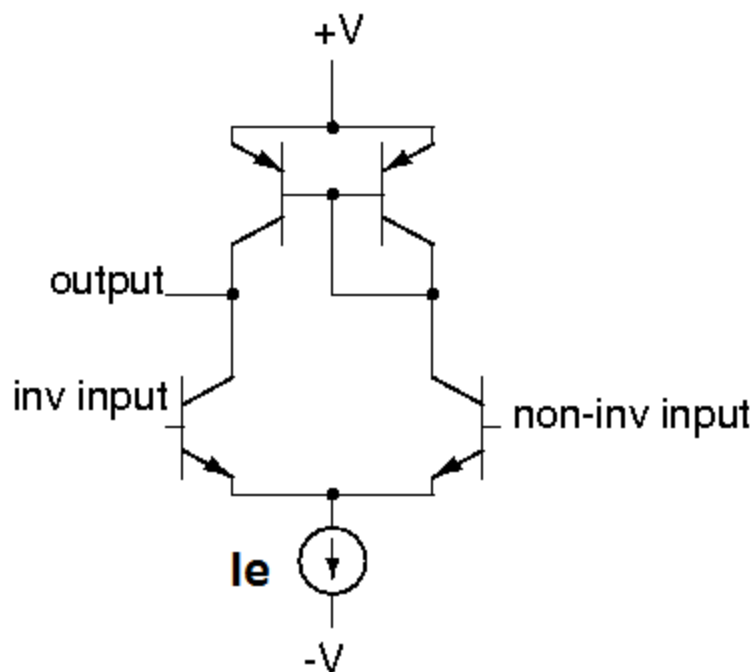


Figure 2

Long-Tailed Pair.

This is a differential amplifier, often referred to as a long-tailed pair. You can see this fundamental analog building block configuration being made between Q17, Q18, Q1 and Q2 of the SEVENFORTYFUN's schematic. The SEVENFORTYFUN has some additional components involved with its differential pair input, but we will get into that later. Q17 and Q18 make the current mirror of the PNP variety. Check your

understanding by working out the math much like we did for the NPN, taking note of the sign differentiation of a PNP, I leave this as an exercise to the reader.

When the voltage at both inputs is equal, then the current  $I_e$  is split equally between the two transistors Q1 and Q2. The purpose of  $I_e$  is to allocate a set amount of current to the two transistors such that when there is a difference at the inputs we get a differential amplifier. That is, when we increase the voltage at the non-inverting input relative to the inverting input Q2 gets more of the current than Q1, and vice-versa. I think this will be made more clear after a study of the simulation below.

#### SEVENFORTYFUN'S SIMULATION

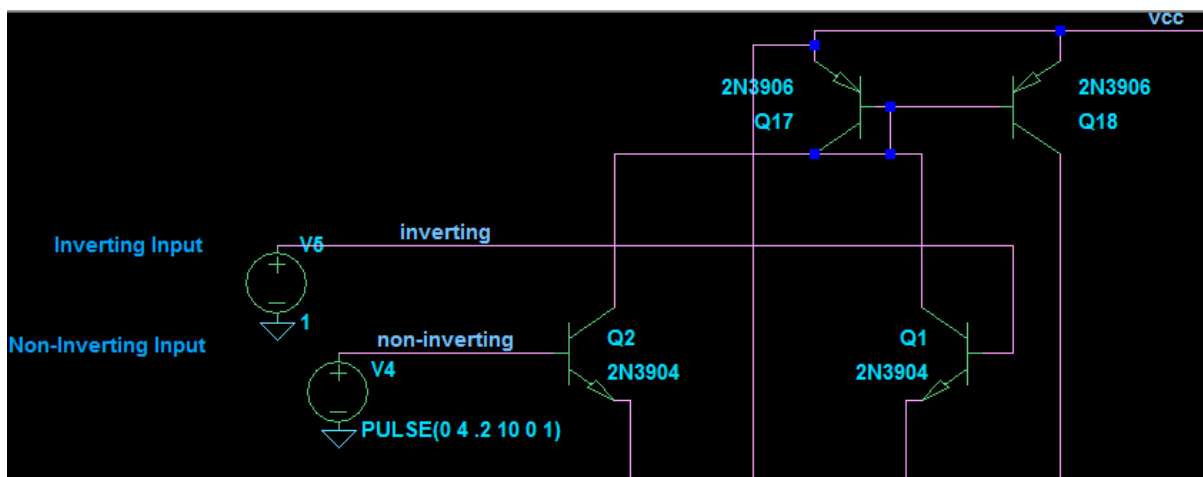
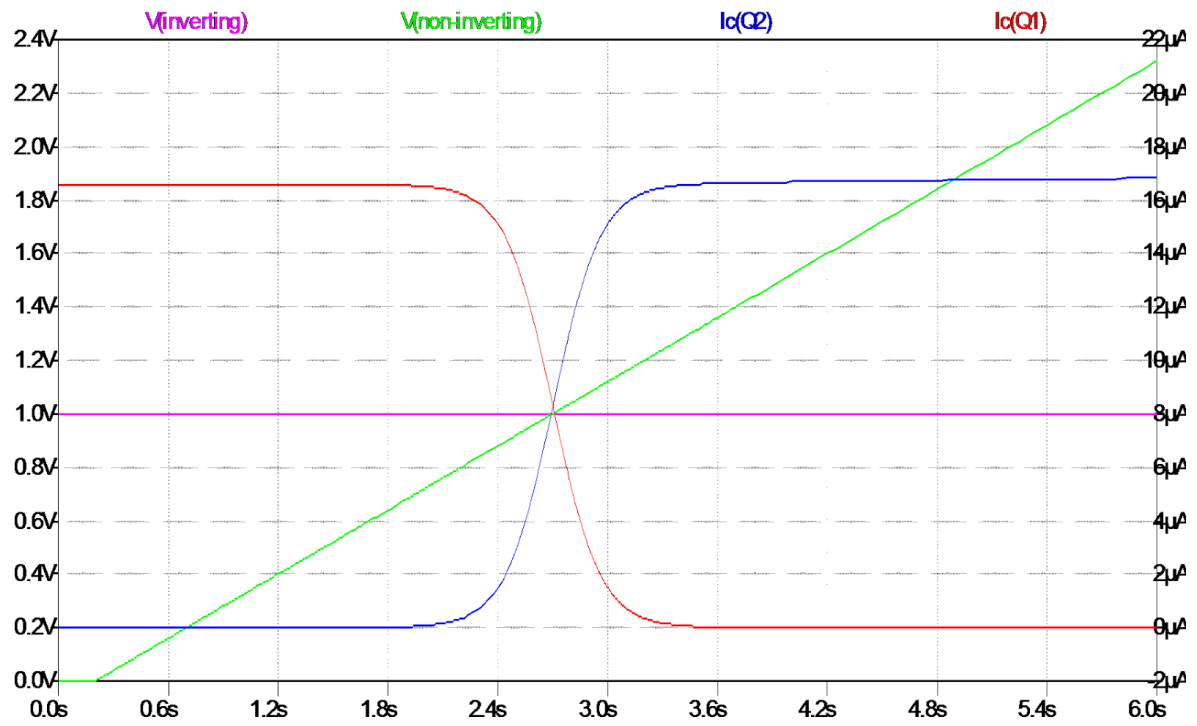
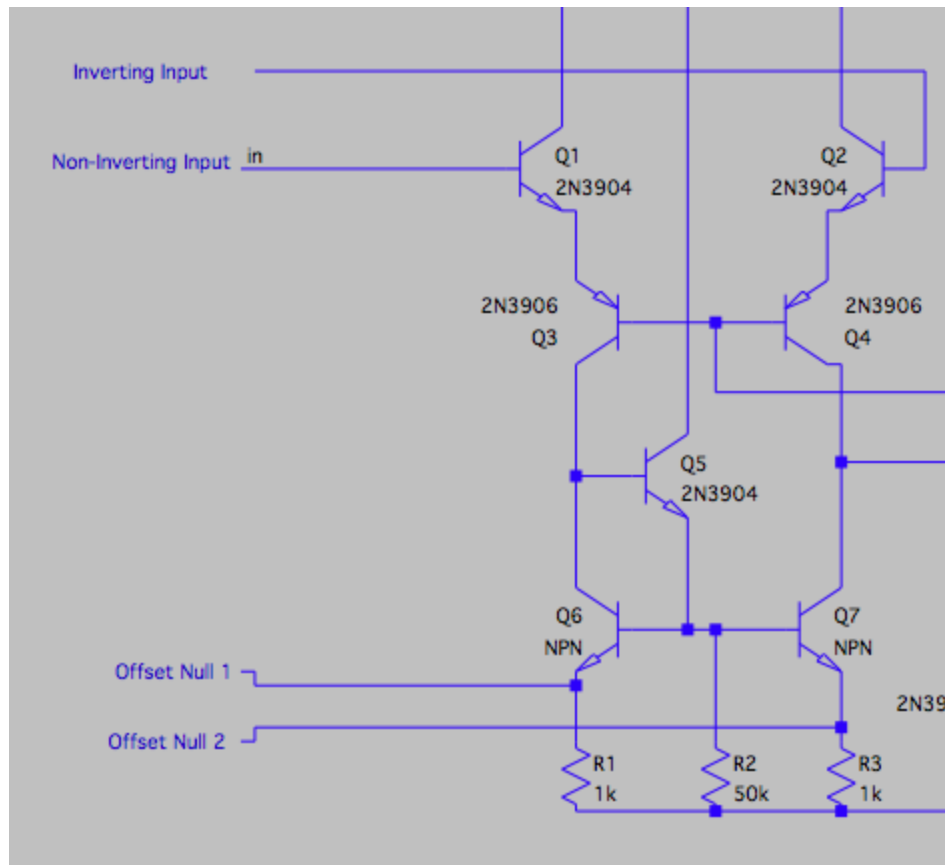


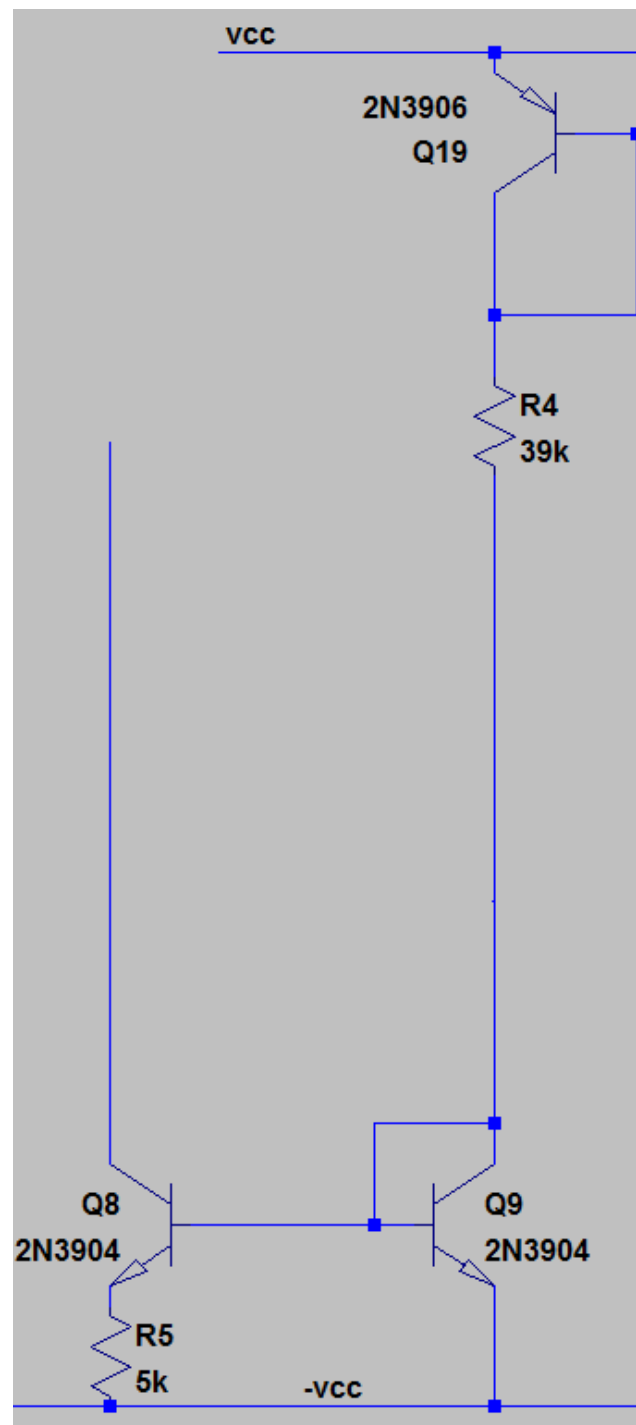
Figure 3(above), Figure 4(below)



In the SEVENFORTYFUN the current  $I_e$  is produced by the additional circuitry in the input stage. The input stage is made up of Q1, Q2, Q3, Q4, Q5, Q6, and Q7.



Q9, Q18 , and R5 are important to the input stage as well because they create the reference current. The the bias for the input stage is created with Q8, Q9 and R4 and current mirror Q17, Q18.



$I_{ref}$  can be calculated as follows:

$$I_{ref} = \frac{V_{cc} - V_{EB19} - V_{BE9} - (-V_{EE})}{R_5}$$

Q8, Q9 and R4 create a widlar current source. The first step to understanding a widlar current source is to do some research on the pioneer and analog legend Bob Widlar, an eccentric personality of the analog world, and inventor of the widlar current mirror, among many other things. He, along with many others I will mention, make up the original analog gods. It's VERY important to read about them.

Anyways, I digress... A Widlar Current source differs from a normal current source because a resistor is added to the emitter of the output stage transistor. In the SevenFortyFun's schematic this is resistor R4. This is more so a practice in saving IC space when designing the chips. Instead of using large resistors to create small currents, the Widlar current source creates small currents with small resistors. To calculate the current  $I_{C8}$ , which is the "output" of the widlar current source follow the KVL around the base emitter loop of this section of the circuit:

$$V_{BE9} = V_{BE8} + I_{E8}R_4 = V_{BE8} + (\beta + 1)I_{B8}R_4$$

That is,

$$\text{Where, } I_{IN} = I_{C9}, I_{OUT} = I_{C8}$$

$$\text{For a BJT, } V_{BE} = V_T \ln \left( \frac{I_C}{I_S} \right) \text{ so,}$$

$$V_T \ln \left( \frac{I_{IN}}{I_{S1}} \right) = V_T \ln \left( \frac{I_{OUT}}{I_{S2}} \right) + I_{OUT}R_4$$

$$I_{OUT}R_4 = V_T \ln \left( \frac{I_{IN}}{I_{OUT}} \right)$$

From here you can solve iteratively.



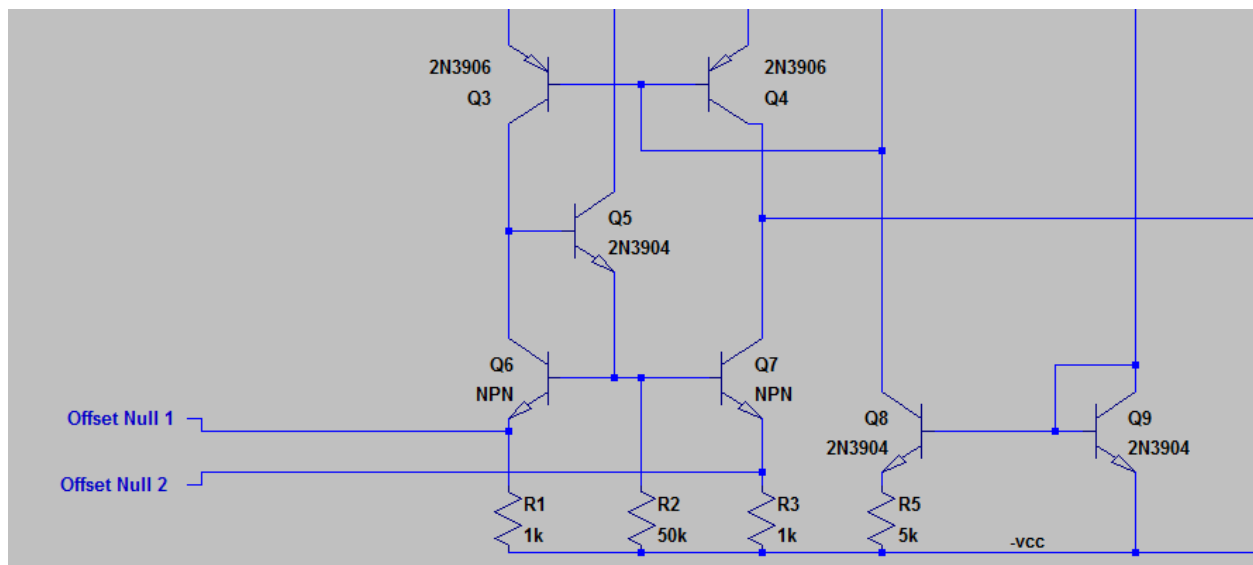
The next important stage is made up by Q3, Q4, Q5, Q6, and Q7. The emitters of the differential input are connected to the emitters of Q3 and Q4, this provides for level shifting, which is required for voltage swing and dc level input at the second stage. The current-mirror load is made up of Q5-Q7 and R1-R3, let's walk through this a little more.

$$I_{C6} = I_{C7}$$

$$I = I_{C4} = I_{C3} = I_{C6} = I_{C7}$$

$$I_{C5} = \frac{2I}{\beta} + \frac{V_{BE7} + IR_3}{R_2} = \frac{2I}{\beta} + \frac{V_T \ln\left(\frac{I}{I_S}\right) + IR_3}{R_2}$$

Hopefully, these equations shed a little more light on the signal path and general functioning of the SEVENFORTYFUN, thus far...I assure you, the input stage is the most complicated part of this circuit.

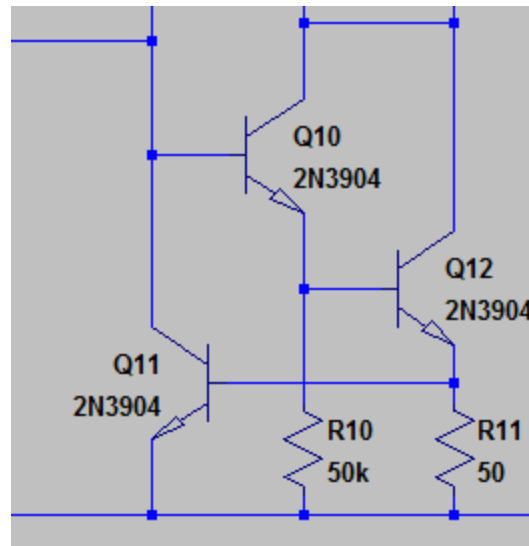


One more feature you may have noticed is the Offset Null 1 and 2. In simulation this is not necessary to tweak, but in real life it will be necessary to include a pot between Offset Null 1 and 2. Why? Well, when there is no difference between the two inputs (Q1 and Q2) you may get a nonzero output. This is due to transistor and resistor mismatches...Nothings perfect! To balance the mismatches out and obtain a zero output when there is no difference in input you put a pot between offset null 1 and 2 and trim it until your output looks good. To read further on the mathematics about this Texas Instruments has already worked out some good maths about the subject as seen here: <http://www.ti.com/lit/an/sloa045/sloa045.pdf>

Now this is great and all, we have a pretty solid input stage, things are looking up, we kind of understand what's going on...But wait! We have a differential input and the SEVENFORTYFUN only has one output. How do we convert the differential input to a single ended signal? Whoa, wait a second, what? Oh don't worry, the creator of the 741 already thought this out for us. The active load (Q5-Q7, R1-R3) create a modified Wilson current mirror. Its purpose it to take the differential input current and make it a single ended signal without the 50% loss of converting from two signals to one. Follow? It gets a little fuzzy, I know. A small signal differential current in Q3 versus Q4 looks summed at the base of Q10. Study the active load schematic closely...It might take some time to absorb this concept, don't worry.

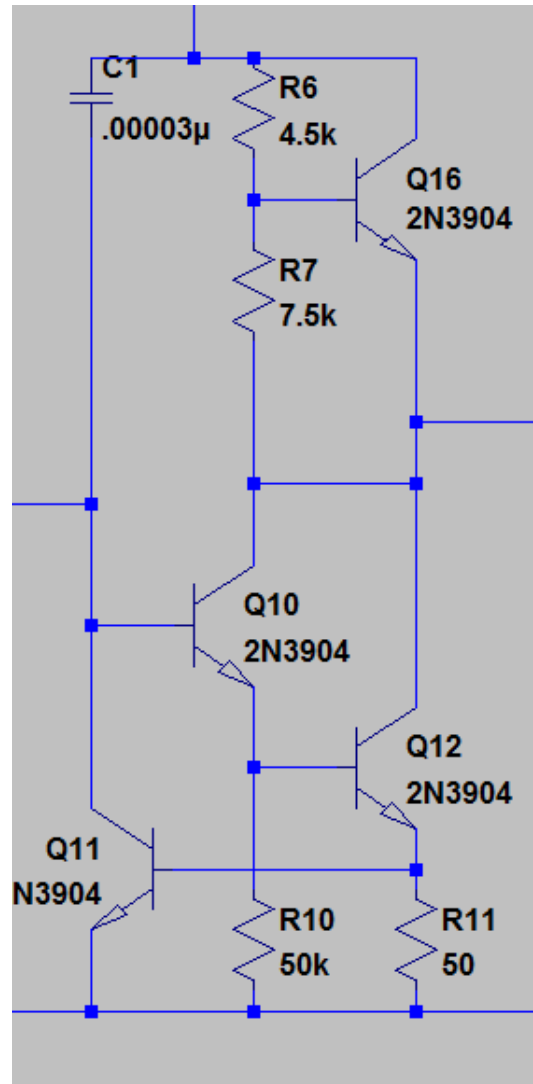
Get it? Got it? Good.

Ok now we finally can move on from that input stage. The single ended signal is fed to Q10. Q10 and Q12 create a Darlington configuration. That is, the current amplified by the first transistor Q10 is subsequently amplified again by Q12. This creates a high current gain ( $\beta * \beta$ ). Q11 exists as a form of negative feedback to prevent saturation. If it gets too high, Q11 turns on and diverts the base current going into Q10 to ground, thus stabilizing the configuration. This amplifier uses the output side of the current mirror created between Q19 and Q20, it is an active load. Active loads lead to significant voltage gain because if the active load were perfect the voltage gain would be infinite if you worked out the thevenin equivalent resistance for a current source

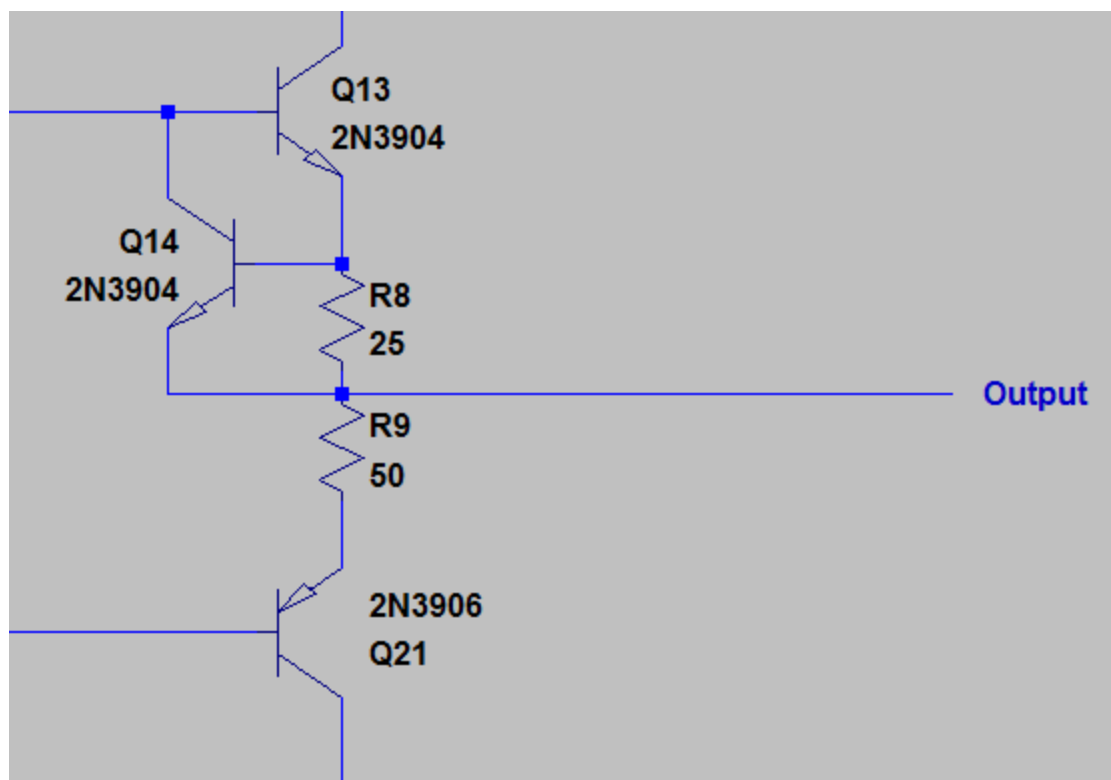


In figure ?? Q16 provides a voltage level shift. The level shifter stage is included to ensure that there is no dc offset in the output signal. DC offset arises from the turn on voltages of the transistors throughout

the circuit. As a exercise run the simulation with and without Q16 noting the differences between the two plots.



Finally we arrive at the output stage! The output stage is composed of Q13, Q14 and Q15. The output stage is a Class AB push pull emitter follower amplifier, go look that up if you're not familiar with the concept. Q13 provides output current limiting much like we saw with Q11. That's it! Go have fun with the PCB and simulation play around with it and I think it will all start coming together.



Some References Used!

<http://users.ece.gatech.edu/~alan/ECE3040/Lectures/Lecture31-The%20u741%20Op%20Amp.pdf>

[http://cc.ee.ntu.edu.tw/~lhlu/eecourses/Electronics2/Electronics\\_Ch10.pdf](http://cc.ee.ntu.edu.tw/~lhlu/eecourses/Electronics2/Electronics_Ch10.pdf)

<https://coefs.uncc.edu/dlsharer/files/2012/04/G2.pdf>