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POWERLINK IP-Core
Altera FPGA Documentation

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I Versions

Version	Date	Comment	Edited by
1.0	Dec 14, 2011	First Edition	Zelenka Joerg

Table 1: Versions

II Safety Notices

Safety notices in this document are organized as follows:

Safety notice	Description
Danger!	Disregarding the safety regulations and guidelines can be life-threatening.
Warning!	Disregarding the safety regulations and guidelines can result in severe injury or heavy damage to material.
Caution!	Disregarding the safety regulations and guidelines can result in injury or damage to material.
Information:	Important information used to prevent errors.
Example:	Functionality is described with an example to prevent errors.

Table 2: Safety notices

III Table of Contents

1 Introduction

The POWERLINK IP-Core is provided as ready-to-use in Altera Quartus II environment with SOPC version 10.1. This documentation presents the integration of the IP-Core into the SOPC environment, as well as timing considerations and interfacing to the software development environment.

If you require detailed information about the POWERLINK IP-Core, please refer to the "POWERLINK IP-Core Generic Documentation" (POWERLINK-IP-Core_Generic.pdf).

2 System-On-a-Programmable-Chip (SOPC) Integration

The POWERLINK IP-Core's "Internal Bus Interface" complies with the Altera Avalon Interface Specification [1], hence there is no extra VHDL wrapper file necessary for converting purpose.

3 Timing Consideration

4 Software Interfacing

5 FPGA Resource Utilization

6 Files

7 Definitions and Abbreviations

AP	Application Processor
BUF	MAC-internal packet buffer
CMD	Command
CMP	Compare Unit
CN	POWERLINK Controlled Node
DPR	Dual Ported RAM
DPRAM	Dual Ported RAM
FF	Flip Flop
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GUI	Graphical User Interface
IP	Intellectual Property
IRQ	Interrupt Request
MII	Media Independent Interface
MN	POWERLINK Managing Node
PCB	Printed Circuit Board
PCP	Powerlink Communication Processor
PDI	Process Data Interface
PDO	Process Data Object
PReq	Poll Request (POWERLINK frame type)
PRes	Poll Response (POWERLINK frame type)
RD	Read
RDY	Ready
RMII	Reduced Media Independent Interface
RO	Read Only
SDO	Service Data Object
SMI	Serial Management Interface (Ethernet phy register access)
SMP	Simple I/O Port
SoA	Start of Asynchronous (POWERLINK frame type)
SoC	Start of Cyclic (POWERLINK frame type)
SPI	Serial Peripheral Interface
SYNC	Synchronization (Clock Domain Crossing)
WR	Write

8 References

[1] Altera: “Avalon Interface Specification”
http://www.altera.com/literature/manual/mnl_avalon_spec.pdf
Version 11.0 (May 2011)

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