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OpenC²: An Open-Source End-to-End Hardware Compiler Development Framework for Digital Compute-in-Memory Macro

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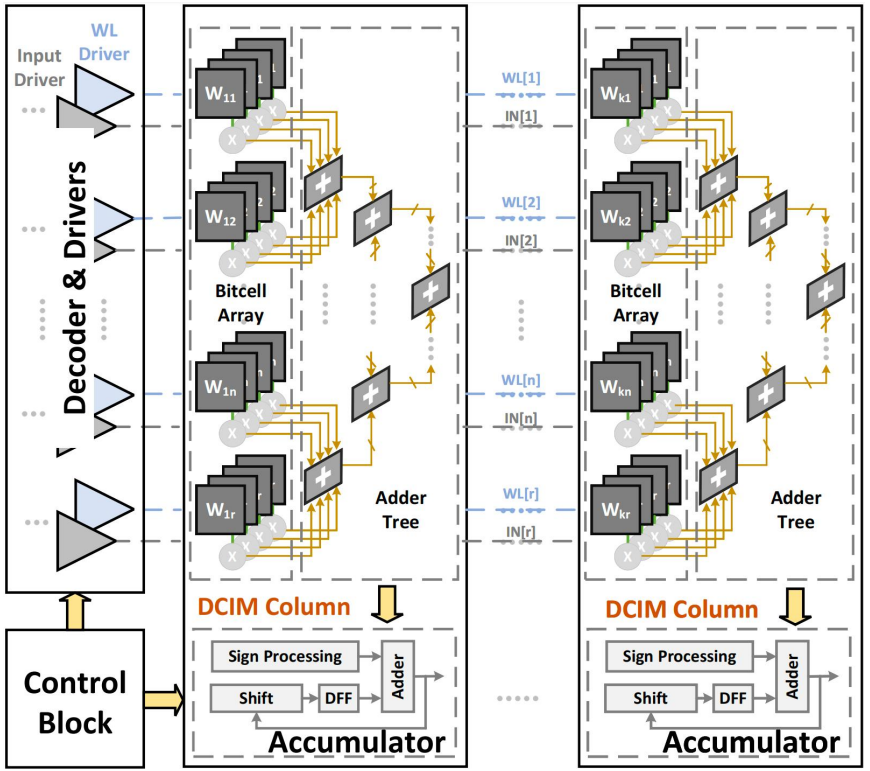
Background

- The success of **DL** depends on both **algorithm advances** and **hardware development**.
- The conventional Von Neumann architecture faces the **"memory wall"** problem, leading to the popularity of **CIM** techniques.
- **Digital CIM** has shown impressive hardware performance improvement in accelerating vector-to-matrix multiplications in DL algorithms.
- Current DCIM designs are highly dependent on **time-consuming manual efforts**.
- Existing DCIM compiler: **privacy**, dependence on **commercial EDA tools**.
- This work proposes **OpenC²** to provide an **open-source** customizable compiler, and serve as a **baseline** for developing DCIM macro compilers.

Floorplan of Digital CIM Macro

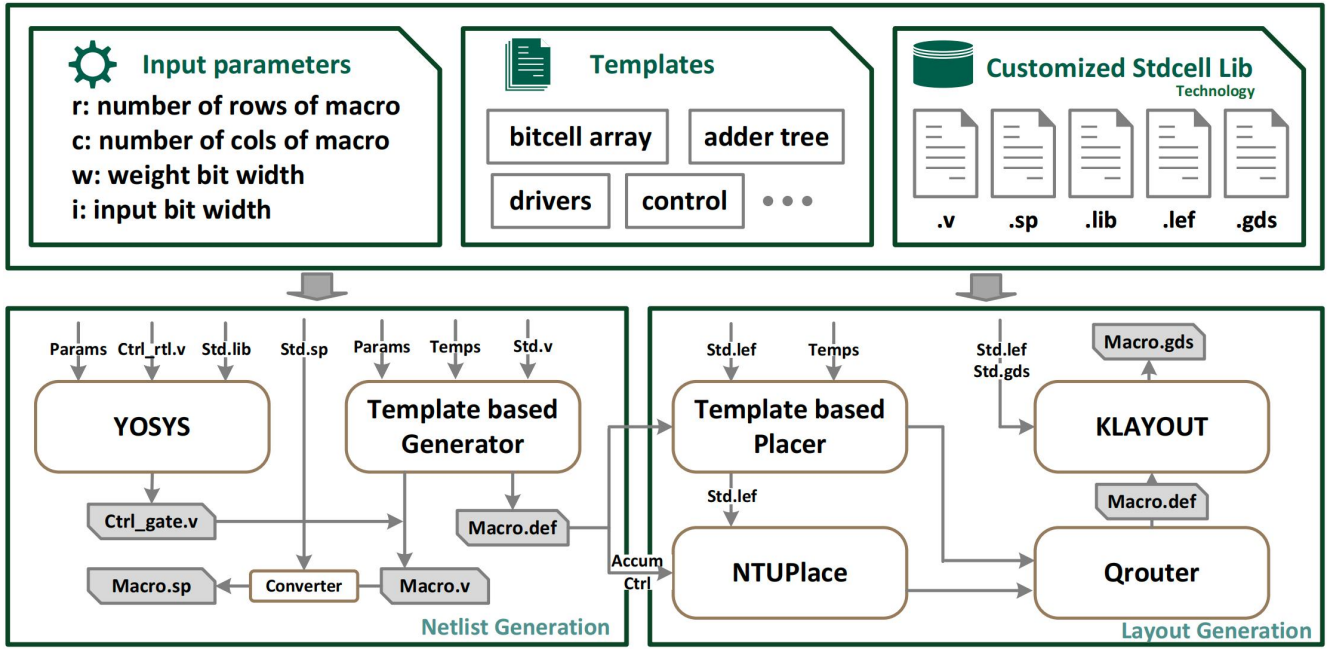
- **Components of DCIM Macro**
  - **Bitcell Array:** Bitcell (SRAM+NOR) + R/W circuit.
  - **Adder Tree:** for partial products in different rows.
  - **Accumulator:** for bit-serial input.
  - **Decoder:** for wordline.
  - **Driver:** for wordline and input.
  - **Cotrol Block.**

- **Parameters to Describe DCIM Macro**
  - **R:** num of rows in DCIM macro.
  - **C:** num of columns in DCIM macro.
  - **W:** weight bit width.
  - **I:** input bit width.



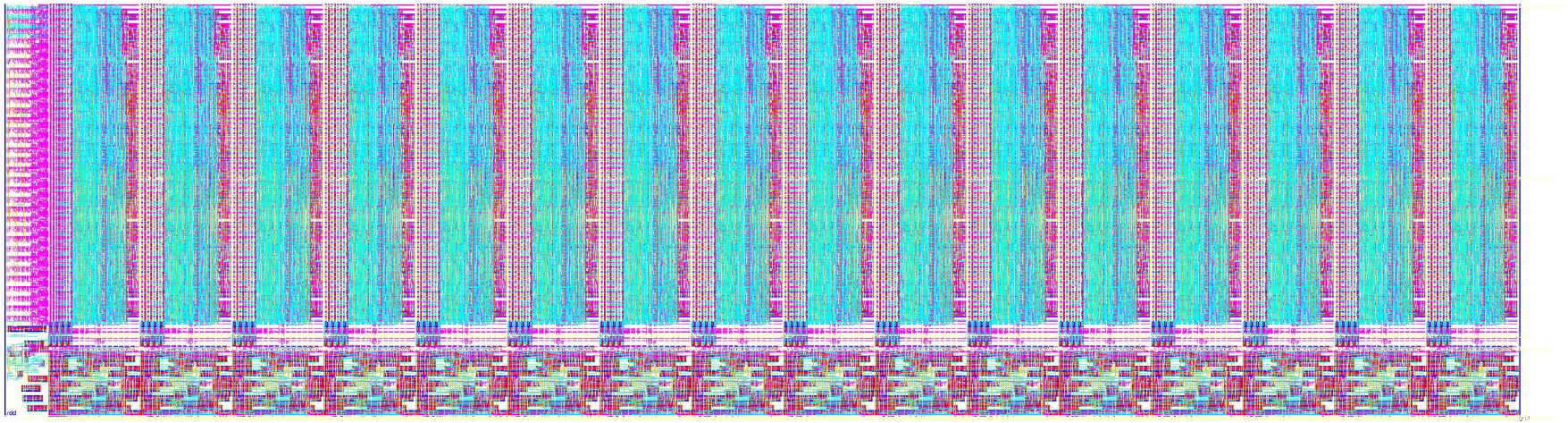
Overall Flow of OpenC²

- **Front-end Netlist Generation**
  - **Output File Format:** VERILOG, SPICE.
  - **Control Block:** RTL template, then synthesis by YOSYS.
  - **Other Components:** Generate netlist directly.
- **Back-end Layout Generation**
  - **Output File Format:** DEF, GDSII.
  - **Hierarchical Physical Design:** 7 sub-modules.
  - **Template-based Placer & Open-source Router.**



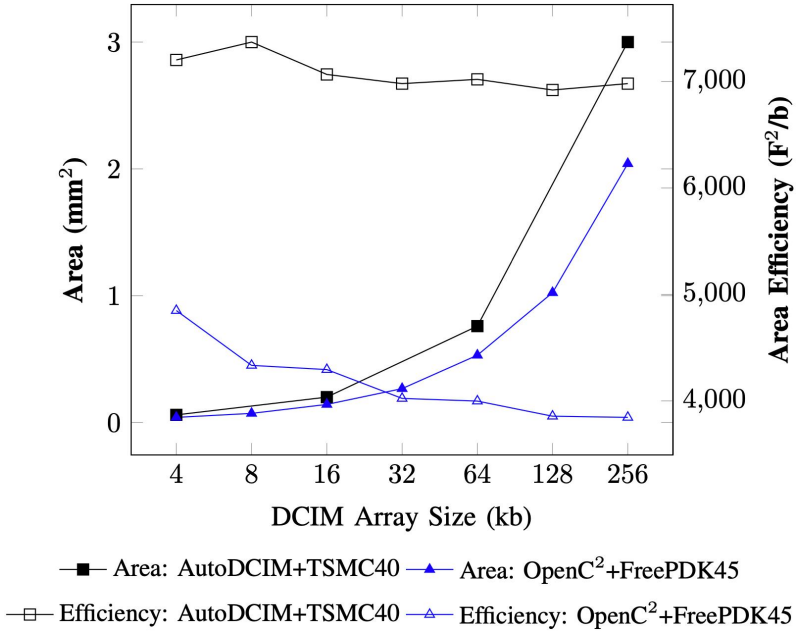
OpenC²-Generated Layout

- **64x64 (4kb) Layout Example for 4-bit by 4-bit Computations.**



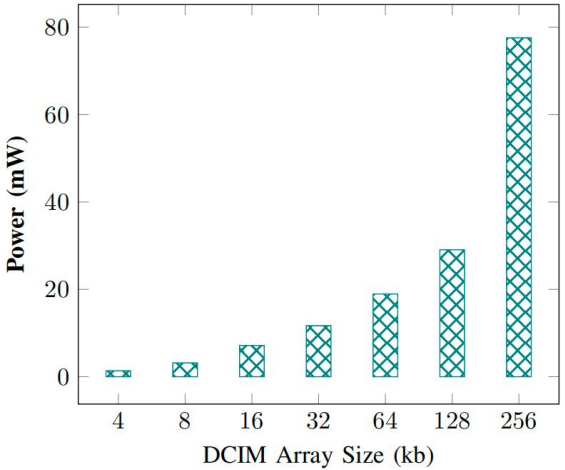
Area Analysis

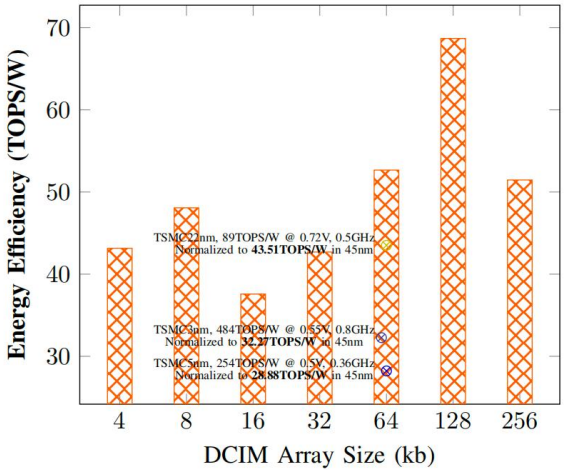
- **OpenC²+FreePDK45 Compare with AutoDCIM+TSMC40:**
  - OpenC² delivered more than a 30% reduction in area across all design sizes.
  - OpenC² delivered an enhancement of over 40% in area efficiency across all design sizes.

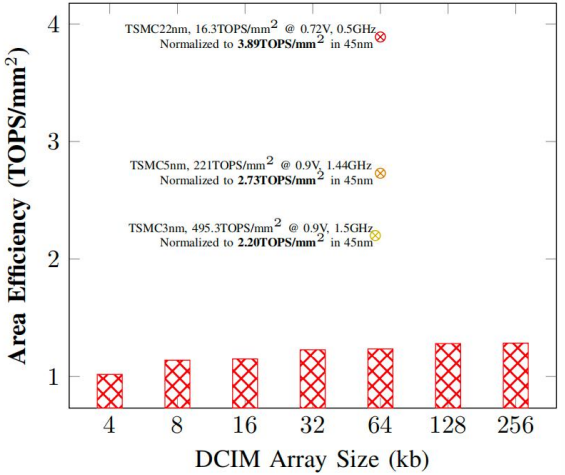


Power and Efficiency Analysis

- **Compare With Some SOTA Silicon Designs:**
  - OpenC²-generated designs @ 1V, 100MHz.
  - Silicon designs: TSMC 22nm, TSMC 5nm, TSMC 3nm.







Thanks for Your Attention!

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