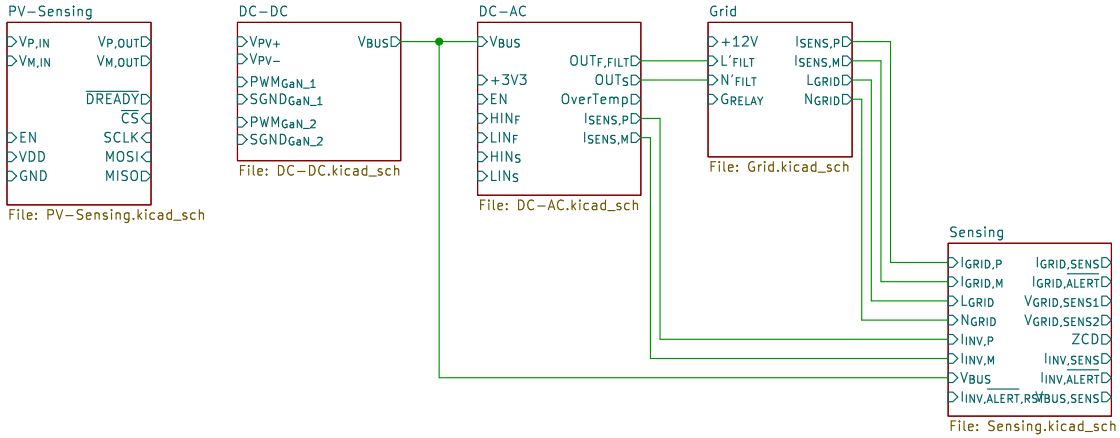


Sheet: /
File: OpenMI.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 1/8

LLC Resonant Transformer

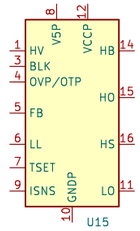
This WIP!
A LLC resonant tank is to be integrated here.
The configuration of this can be found here:
Resonant LLC Transformer Design

Considerations about a LLC controller:

There are a bunch of LLC controller available on the market.
Two possible options are:

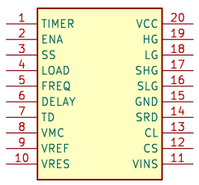
- *UCC25660 from TI (from 2023).*
  750kHz Wide VIN/VOUT Range LLC Controller Optimized for Light-Load Efficiency
  Possible issues:
  - *In datasheet its said that for VCCP "Choose at least 100µF capacitor or combination of capacitors"*

- *ICE2HS01G from Infineon (from 2010).*
  High Performance Resonant Mode Controller for Half-bridge LLC Resonant Converter
  30kHz-1MHz switching frequency range
  Possible issues:
  - *"Maximum switching frequency" is 215kHz but "Recommend Maximum switching frequency" 1000kHz*

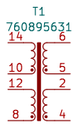


U15
UCC25660

U16
ICE2HS01G

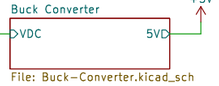


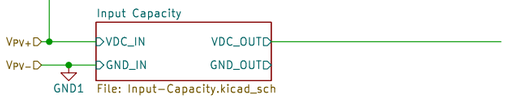
T1
760895631



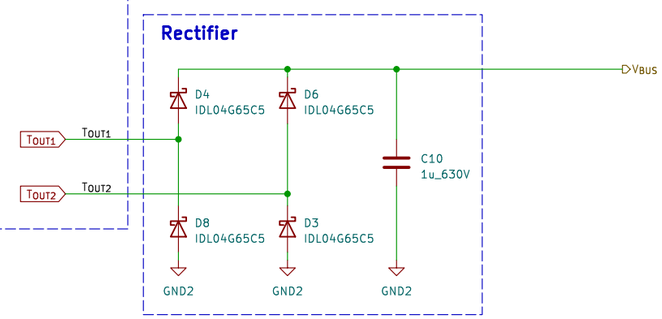
TODO:
Remove 5V global label and use local label?
Use local label

TODO:
Put buck converter on top

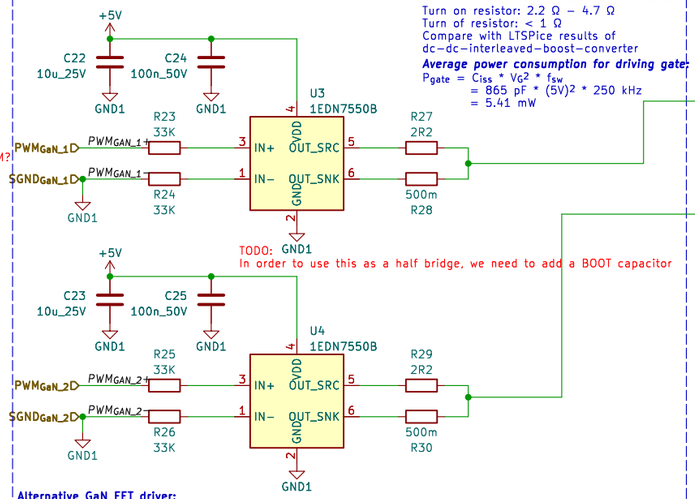




Rectifier

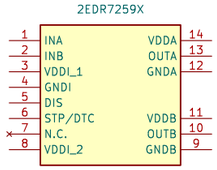


GaN FET Driver



Alternative GaN FET driver:
1EDN7116U, 2A, 3ns, 200V
2EDR7259X, dual channel, 5A, 9A, rise-time 7.5ns@1.8nF, 4.12€@1piece@mouser

U17
2EDR7259X

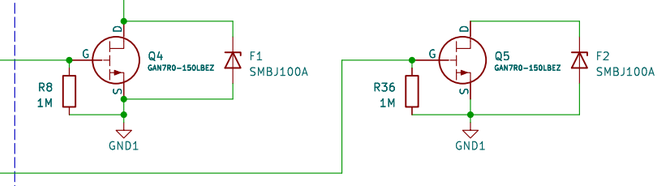


TODO:
Check this alternative?

Gate resistor recommendations in AN5583:
Turn on resistor: 2.2 Ω – 4.7 Ω
Turn of resistor: < 1 Ω
Compare with LTSPice results of
dc-dc-interleaved-boost-converter

Average power consumption for driving gate:
$P_{gate} = C_{iss} * V_G^2 * f_{sw}$
$= 865\ pF * (5V)^2 * 250\ kHz$
$= 5.41\ mW$

GaN FET



Considerations about T_{on} and T_{off} for GaN FET:

With a 250 kHz PWM signal one period is
$T_{PWM} = 1 / 250\ kHz = 4\ us$
With a 9 bit resolution the smallest possible pulse period becomes:
$T_{min} = 1 / (250\ kHz * 29) = 7.81\ ns$
Because the duty cycle will only vary between $0.5 < D < 0.75$, the period T_{on} will vary between
$0.5 * T_{PWM} < T_{on} < 0.75 * T_{PWM}$
$2\ us < T_{on} < 3\ us$

The GAN7R0-150LBEZ has total gate-source charge of
$Q_{GS} = 1.7\ nC$
To compute the time we need to charge Q_{GS} we can compute
$t_{charge\_QGS} = t_{rise\_driver} + Q_{GS} / I_{source\_driver}$
To compute the time we need to remove charge from the gate:
$t_{discharge\_QGS} = t_{rise\_driver} + Q_{GS} / I_{sink\_driver}$

GaN FET driver recommendations according to ST Application Note AN5583
- high sink current I_{sink} to reduce Miller effect (> 3A, 7A peak is very good)
- low sink resistance R_{sink} to reduce bouncing between gate and source (< 1.5 Ω)
- t_{rise}/t_{fall} < 20 ns @ C_{Load} = 2 nF
- $V_{GS,\ ON}$ = 6V
- CMTI (Common mode transient immunity) > 150 kV/us (High CMTI means capability to withstand fast dV/dt without dangerous glitches, jitter or short-circuit)

Considerations about possible GaN FET driver:
1EDN7550B (SOT23-6, 0.75€@1piecse) / 1EDN7550U (TSNP-6, 1.26€@1piece), 4A, 8A, truly differential inputs
1EDNx550 Gate Driver Application Examples And Layout Guidelines
1EDN7550 Product Page

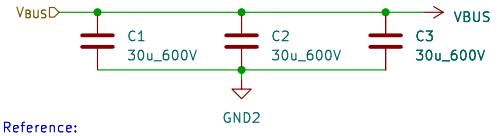
The GAN7R0-150LBEZ has a input capacitance of
$C_{iss} = 865\ pF$
The gate driver 1EDN7550B has rise times of
$t_{rise\_1.8nF} = 6.5\ ns$
$t_{rise\_200pF} = 1\ ns$
So using the GAN7R0-150LBEZ with the 1EDN7550B we can roughly asume:
$t_{rise\_865pf} = (6.5\ ns - 1\ ns) / (1800\ pF - 200\ pF) * 865\ pF$
$= 2.97\ ns$
This results in
$t_{charge\_QGS} = 2.97\ ns + 1.7\ nC / 4\ A = 3.395\ ns$,
which is
$t_{charge\_QGS} / T_{on\_minimal} = 3.395\ ns / 2000\ ns \approx 0.0017$,
so the rise time is at maximum 0.17% of the period time.
The results for the fall time should be roughly similar.

Simulating this in LTSpice with
$R_{Gate\_SNK} = 2.2\ \Omega$
$R_{Gate\_SRC} = 0.5\ \Omega$
results in the following times (measuring V_{GS} from 10% to 90%)
$t_{charge\_QGS} = 8.44\ ns$ → 0.42% of period time
$t_{discharge\_QGS} = 2.59\ ns$ → 0.13% of period time

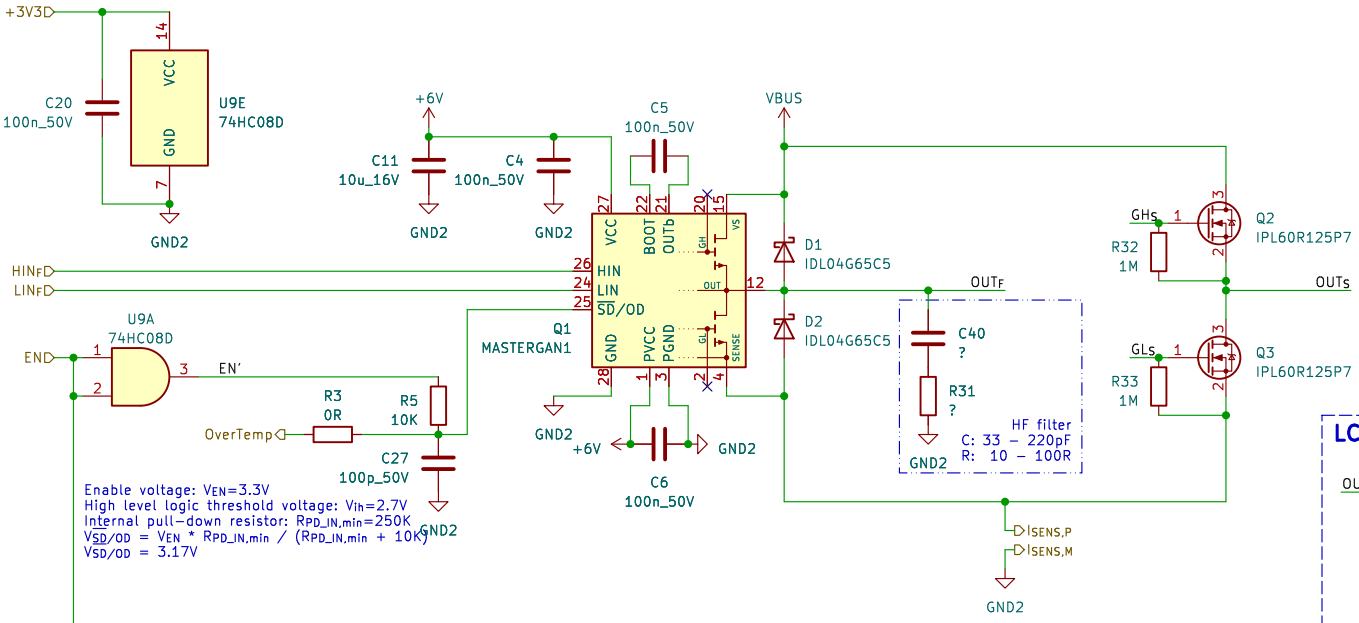
Sheet: /DC-DC/	
File: DC-DC.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. 8.0.2	Id: 2/8

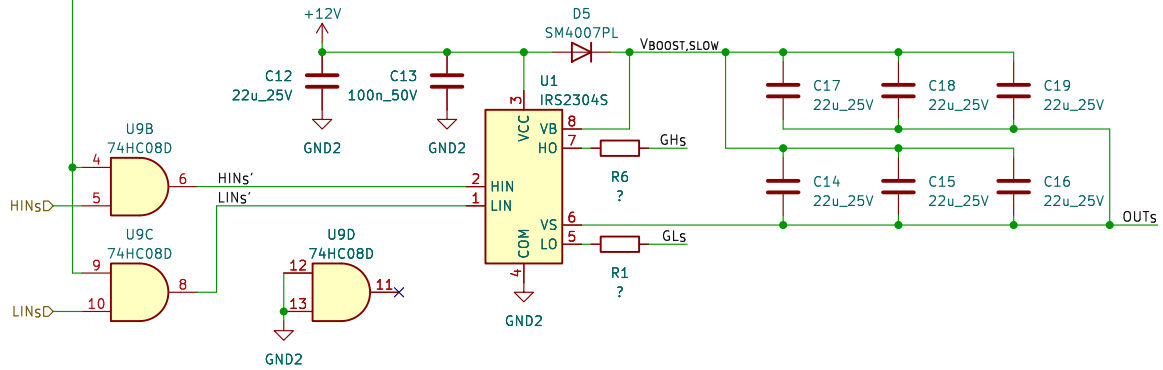
DC bus power decoupling

P_O = 400W
f = 50Hz
V_{bus} = 425V
ΔV = 50V => $V_{bus,min}$ = 400V; $V_{bus,max}$ = 450V
$C_{min} = P_O / (2\pi f * V_{bus} * \Delta V)$ = 59.92uF

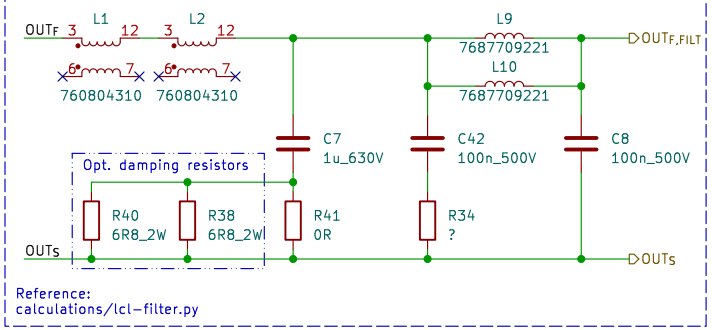


Reference:
DC-Bus Design with Hybrid Capacitor Bank in Single-Phase PV Inverters
https://doi.org/10.1109/IECON.2017.8216408





LCL-Filter



Reference:
calculations/lcl-filter.py

Sheet: /DC-AC/		
File: DC-AC.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 3/8

Line filter

Two different common chokes for two frequency ranges
- 744841330 for high frequencies
- 744822301 for low frequencies

X2: 0.1 – 0.33uF
Y2: 1.0 – 2.2nF

IEC 60384-14 specifies the use of X2 capacitors for "accross the line" and Y2 capacitors for "line to ground" and applications.

The common mode choke for high frequencies is placed near the inverter output to filter he high frequencies first.

Grid and system protection

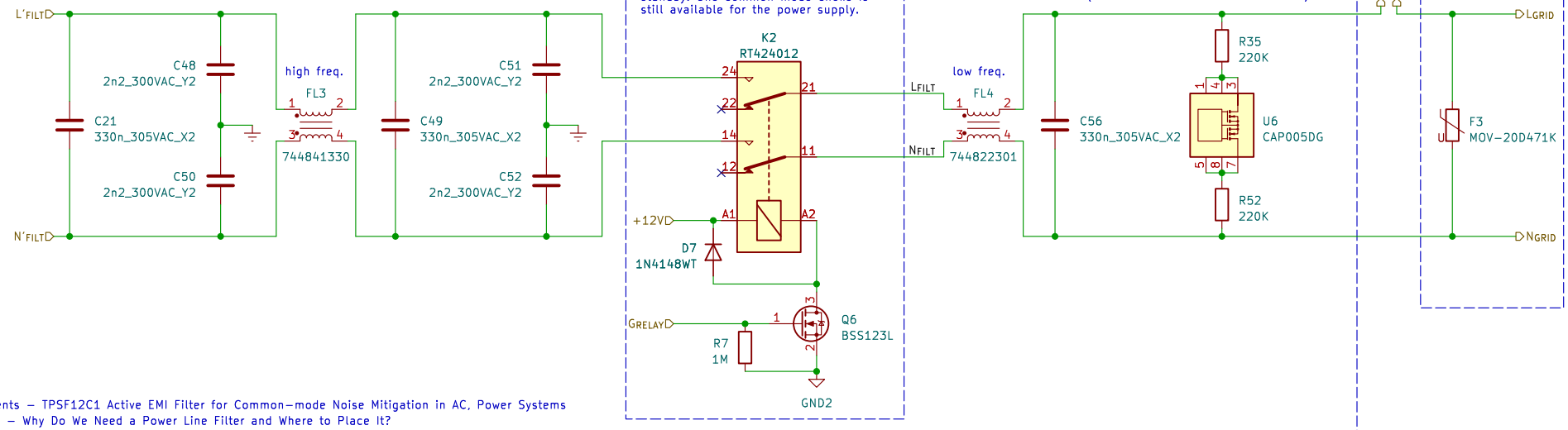
VDE-AR-N 4105 requires two independent protection mechanisms to disconnect the system from the grid in the event of a fault. The relais is one of them. The other one are the gate drivers of the inverter itself.

The relay is close to the line input to reduce copper losses of the filter in standby. One common mode choke is still available for the power supply.

The CAP005DG discharges the X2 and Y2 capacitors below 60V within a second as required by several standards (IEC 60065, IEC 60950, UEC 62368).

Overvoltage transient protection

The varistor protects the the circuit "accross the line".
The Y2 capacitors withstand the overvoltage transients on their own.



See also:
Texas Instruments – TPSF12C1 Active EMI Filter for Common-mode Noise Mitigation in AC, Power Systems
SOS Electronic – Why Do We Need a Power Line Filter and Where to Place It?

Sheet: /Grid/		
File: Grid.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 4/8

Grid current sense

Sensitivity: 264mV/A

U10 MCS1802GS-05 (IP+, IP-, VCC, VIOUT, FILTER, GND)

IGRID,P, IGRID,M, IGRID,OUT

C28 100n_50V, C29 100n_50V, C37 22n_50V, C38 100n_50V, C39 100n_50V

U11 MCP6001T-OT

R2 330R, C36 100n_50V

$f_c = 1 / 2\pi*R*C$, $f_c = 4.8kHz$

Internal filter:
$R_{FI} = 1.5k$
$C_{FI} = 1nF$
with:
$C_{ext} = 22nF$
$f_c = 4.6kHz$

U12A MCP6567-SN, U12B MCP6567-SN, U12C MCP6567-SN

R53 10K, R54 18K, R55 10K, R56 10K

IGRID,SENS, IGRID,ALERT

$I_{ALERT} = 3A$
$V_{OUT@0A} = 1.65V$
$\Rightarrow V_{REF,HIGH} = 1.65V + 3 * 0.264V \approx 2.45V$, $V_{REF,LOW} = 1.65V - 3 * 0.264V \approx 0.85V$

Grid voltage sense

Output swing: $\Delta V/2 = V_{grid,peak} * 10k\Omega / (4*680k\Omega + 10k\Omega) = 1.19V$
Offset: $V_{offset} = 1.65V$

U5A MCP6004-SL, U5B MCP6004-SL, U5C MCP6004-SL, U5D MCP6004-SL, U5E MCP6004-SL

U14 MCP6561-OT

R8 100K, R9 100K, R10 680K, R11 680K, R12 680K, R13 680K, R14 10R, R15 680K, R16 680K, R17 680K, R18 680K, R19 10K, R20 10K, R21 100R, R22 100R, R57 100R

C30 100n_50V, C31 1u_25V, C32 1n_50V, C33 1n_50V, C34 100n_50V, C35 100n_50V, C41 100n_50V, C53 100n_50V, C62 1n_50V

+1.65VREF, LGRID, NGRID, VGRID,OUT, ZCD, VGRID,SENS1, VGRID,SENS2

Reference:
TIDM-SOLARUINV, Grid-tied Solar Micro Inverter with MPPT

Inverter current sense

U2A INA381A2IDGS, U2B INA381A2IDGS, U2C INA381A2IDGS

R46 20mR, R39 330R, R44 330R, R45 10K, R42 10K, R43 100K

C9 100n_50V, C43 100n_50V, C44 100n_50V, C45 10n_50V

IINV,P, IINV,M, IINV,SENS, IINV,ALERT, IINV,ALERT,RST

$I_{RMS} = 400W / 230V = 1.74A$
$I_{max} = 400W / 230V * \sqrt{2} = 2.46A$
$V_{out} = 50 * V_{shunt}$

$R_{shunt} = V_{shunt} / (50 * I_{shunt})$
with $V_{out@1A} = 1V$
$R_{shunt} = 1V / (50 * 1V)$
$R_{shunt} = 0.02\Omega = 20m\Omega$
$P_{loss} = I_{RMS}^2 * R_{shunt} = 60.5mW$

$f_c = 1 / 2\pi*R*C$, $f_c = 4.8kHz$

$f_c = 1 / 2\pi*R*C$, $f_c = 48kHz$

$I_{ALERT} = 3A$
$\Rightarrow V_{REF} = 3V$

DC bus voltage sense

$V_{bus,max} = 450V$
$V_{ref} = 3.3V$
$V_{bus,sens,max} = V_{bus,max} / (R1+R2) * R2 = 3.17V$
$P_{loss} = V_{bus,max}^2 / (R1+R2) = 14mW$

U7 MCP6001T-OT

R47 4M7, R48 4M7, R49 4M7, R50 100K, R51 1K

C46 100n_50V, C47 100n_50V

VBUS, VBUS,SENS

$f_c = 1 / 2\pi*R*C$, $f_c = 1.6kHz$

Sheet: /Sensing/
File: Sensing.kicad_sch

Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 8.0.2 | Id: 5/8

Input Capacity

Calculation of input capacitor for a Boost Converter like suggested in this ***Research Article:***

$C_{boost} \geq D_{max} * V / (8 * f_s^2 * L_{in} * \Delta V)$ | $\Delta V / V = 0.01$
$\geq D_{max} / (8 * f_s^2 * L_{in} * 0.01)$
$\geq 0.7 / (8 * (250\ kHz)^2 * 200\ uH * 0.01)$
$\geq 0.7\ uF$

Because we have two boost converter in parallel, so the nominal input capacity we need is:

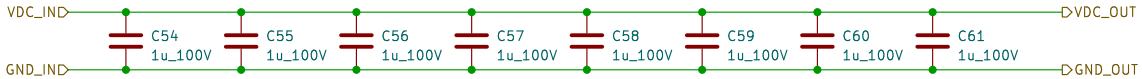
$C_{in,\ nominal} \geq 2 * C_{boost}$
$\geq 1.4\ uF$

By using MLCC capacitor we need to consider especially DC Bias, which for example
for the CL31B105KCHNNN (1.0uF_100V) capacitor is −65% at 60V.
Therefore we should design the input capacitance to be at least:

$C_{in} \geq 100/65 * C_{in,\ nominal}$
$\geq 1.538 * 1.4\ uF$
$\geq 2.15\ uF$

To compensate for other effects (like temperature, aging ...)
and including a little bit of safety margin, we choose:

C_{in} = 8 x 1.0uF_100V



Sheet: /DC−DC/Input Capacity/
File: Input−Capacity.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 6/8

5V Buck Converter

General Considerations

Operating input voltage range: 16 V – 60 V, with a little safety margin we need about 80 – 100 V as maximum input voltag.

What consumers do we have to supply on the primary side?
(1) GaN MOSFET Gate Driver:
Average power consumption for driving gate:
$P_{gate} = C_{iss} * V_G^2 * f_{sw}$
$= 865\ pF * (5V)^2 * 250\ kHz$
$= 5.41\ mW$
For the output voltage of 5 V this results in:
$I_{out,\ 1} = 5.41\ mW / 5\ V = 1.082\ mA$
(2) ADUM120N:
At 5V Operation and max data throughput (100 Mbps):
$I_{out,\ 2} = 8.1\ mA$

This results in a full load current of:
$I_{out} = I_{out,\ 1} + I_{out,\ 2} = 9.182\ mA$

Finding a buck converter which is suited for $V_{in,\ max} = 100\ V$ and $I_{out} = 9.182\ mA$ is hard, most buck converter are rated for much higher output current (typically 500 mA).
A buck converter selection guide from TI can be found here:
https://www.ti.com/lit/sg/slyt729b/slyt729b.pdf
In summary we decide to take a buck converter, which is rated for $I_{out,\ max} = 500\ mA$.
If we would plan to run the buck converter in CCM for such low output current ($I_{out} = 9\ mA$) we would have to use a huge inductor because of the low available ripple current.
Therefore we design the buck converter for the lowest recommended value, which is $I_{out} = 100\ mA$ according to the calculation tool:
https://www.ti.com/lit/zip/snvc226

Enable/Undervoltage Lockout (EN/UVLO)
$V_{IN(on)} = 1.5\ V * (1 + (R_{UV1} / R_{UV2}))$
$= 1.5\ V * (1 + (330\ k\Omega / 47\ k\Omega))$
$= 12.03\ V$

Buck Inductor:
It is recommended to set the ripple current to 30% – 50% of the rated load current, which in this case would be
$\Delta I_L = 0.4 * 100\ mA = 40\ mA$
$\Delta I_L = (V_{OUT} / (f_{SW} * L_O)) * (1 - (V_{OUT} / V_{IN}))$

$L_O = (V_{OUT} / (f_{SW} * \Delta I_L)) * (1 - (V_{OUT} / V_{IN(nom)}))$
$= (5\ V / (500\ kHz * 0.04\ A)) * (1 - (5\ V / 40V))$
$= 218.75\ uH$
-> $L_O = 270\ uH$ with 10% tolerance (e.g. SRR1205-271KL) is in the worst case 243 uH

Maximum Duty Cycle
$D_{max} = V_{OUT} / (V_{IN(max)} * \eta)$
$= 5\ V / 60\ V * 0.7$
≈ 0.12

Input Capacitor:
According to *SLTA055* it is recommended as a general rule of thumb, keeping the input peak to peak ripple amplitude below 75 mV keeps the rms currents in the bulk capacitors within acceptable limits.
The CL31B105KCHNNN 1.0uF_100V X7R capacitor has a rms resistance of:
$R_{ESR@500\ kHz} = 11.76\ m\Omega$
With these numbers we can calculate the minimum input capacitance:
$C_{IN} \geq (I_{OUT} * D\ (1 - D)) / (f_{SW} * (V_{IN(ripple)} - I_{OUT} * R_{ESR}))$
$\geq (0.01\ A * 0.12 * (1 - 0.12)) / (500\ kHz * (75\ mV - 0.01\ A * 11.76\ m\Omega))$
$\geq 0.028\ uF$

Datasheet recommends 2.2 uF high quality X7S or X7R ceramic capacitor but as we calculated before we should get away with way less.
Using CL31B105KCHNNN (1.0uF_100V) capacitor with DC bias -65% at 60V and tolerance of ±10% gives us in the worst case:
$C_{IN\_60V} = 1.0uF * 0.9 * 0.35 = 0.315uF$

TODO:
Double check if assumptions for input capacity are correct?
Maybe use 2 * 1u_100V?

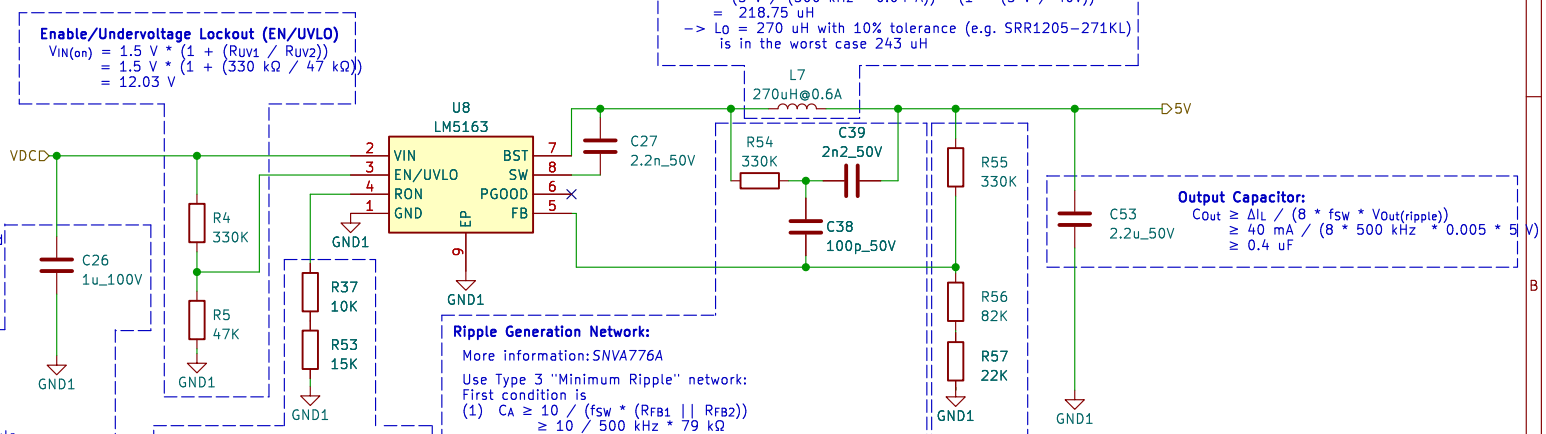
Switching Frequency
Using $R_{RON} = 25\ k\Omega$ results in:
$f_{SW}(kHz) = V_{OUT} * 2500 / R_{RON}(k\Omega)$
$= 500\ kHz$

Ripple Generation Network:
More information: *SNVA776A*

Use Type 3 "Minimum Ripple" network:
First condition is
(1) $C_A \geq 10 / (f_{SW} * (R_{FB1} \parallel R_{FB2}))$
$\geq 10 / 500\ kHz * 79\ k\Omega$
$\geq 253\ pF.$
Second condition is
(2) $R_A * C_A \geq ((V_{IN-nom} - V_{OUT}) * T_{ON(@VIN\_nom)}) / 20\ mV.$
By calculating
$T_{ON(@VIN\_nom)} = D_{VIN\_nom} / f_{SW}$
$= V_{OUT} / (V_{IN\_nom} * \eta * f_{SW})$
$= 5\ V / (48\ V * 0.65 * 500\ kHz)$
$= 0.321\ us$
we get
$R_A * C_A \geq ((V_{IN-nom} - V_{OUT}) * T_{ON(@VIN\_nom)}) / 20\ mV$
$\geq ((48\ V - 5\ V) * 0.321\ us) / 20\ mV$
$\geq 0,00069.$
Rearranging this to R_A gives us:
$R_A \geq 0,00069 / C_A$
To keep R_A within practical limits (100 kΩ < R_A < 1MΩ for low-I_Q converters) we select
$C_A = 2200\ pF$
which gives us
$R_A \geq 313,7\ k\Omega$
Third condition is
(3) $C_B \geq t_{TR-Settling} / (3 * R_{FB1})$
where $t_{TR-Settling}$ is the desired load transient response settling time.
The datasheet calculates with 75 µs settling time, resulting in:
$C_{B,\ 75\ \mu s} \geq 75,8\ pF$
The application note chooses 50 µs settling time, resulting in:
$C_{B,\ 50\ \mu s} \geq 50,5\ pF$
To avoid capacitance fall-off with DC bias, use a COG or NP0 dielectric capacitor for C_B.

Voltage Feedback:
$R_{FB1} = 330\ k\Omega$
$R_{FB2} = (1.2\ V / (V_{OUT} - 1.2\ V)) * R_{FB1}$
$= 6 / 19 * R_{FB1}$
$= 104.21\ k\Omega$

Output Capacitor:
$C_{Out} \geq \Delta I_L / (8 * f_{SW} * V_{out(ripple)})$
$\geq 40\ mA / (8 * 500\ kHz * 0.005 * 5\ V)$
$\geq 0.4\ uF$



Sheet: /DC-DC/Buck Converter/		
File: Buck-Converter.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 7/8

Voltage & current sense

Anti-aliasing filter:
$f_c = 1 / (2\pi * R * C)$
$f_c = 1 / (2\pi\ 1kR * 33nF)$
$f_c = 4.8kHz$

Overvoltage protection:
The diodes protect the inputs of the ADE7912 from overvoltage.
Thanks to the bidirectional use of the diodes, the inputs of the ADE7912 are also protected against transient overvoltages.

Voltage sense

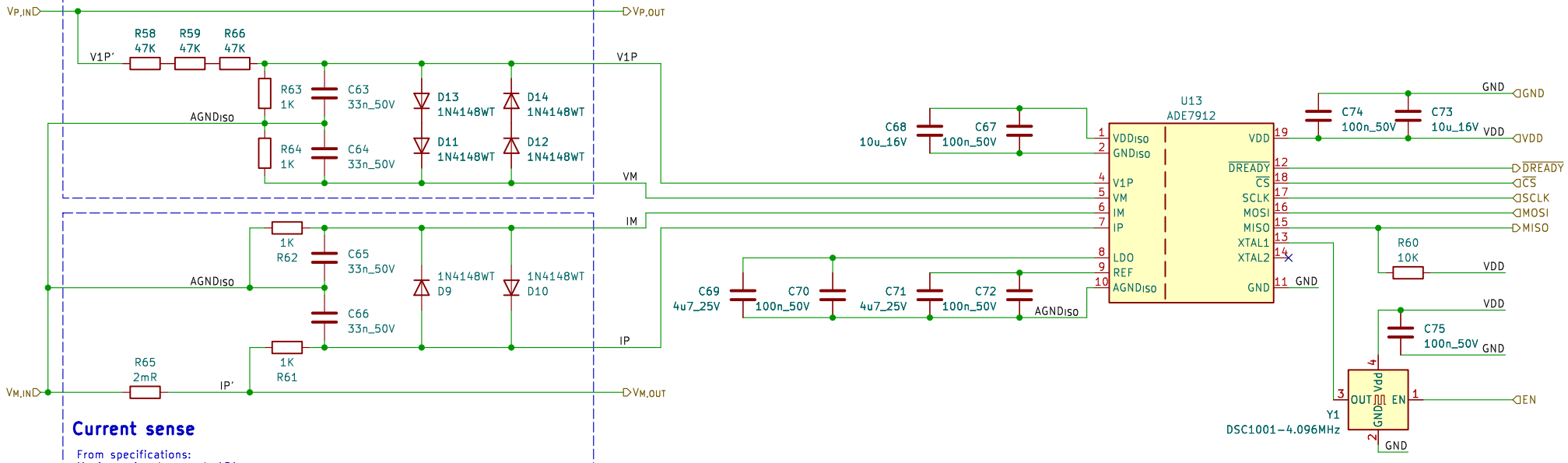
From specifications:
Operating voltage range: 16-60V

Add 20% safety margin:
$U_{max} = 60V * 120\% = 72V$
$U_{V1P,max} = 0.5V$
=> Ideal resistor ratio: 1 / 143
=> $R_1 = 1kR$; $R_2 = 3 * 47kR$

Current sense

From specifications:
Maximum input current: 12A

Add 20% safety margin:
$I_{max} = 60V * 120\% = 14.4V$
$U_{IP,max} = 31.25mV$
=> $P_{max} = U_{IP,max} * I_{max} = 450mW$
=> $R_{max} = U_{IP,max} / I_{max}$
=> $R_{max} = 2.17mR$
=> R = 2mR



Sheet: /PV-Sensing/		
File: PV-Sensing.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.2		Id: 8/8