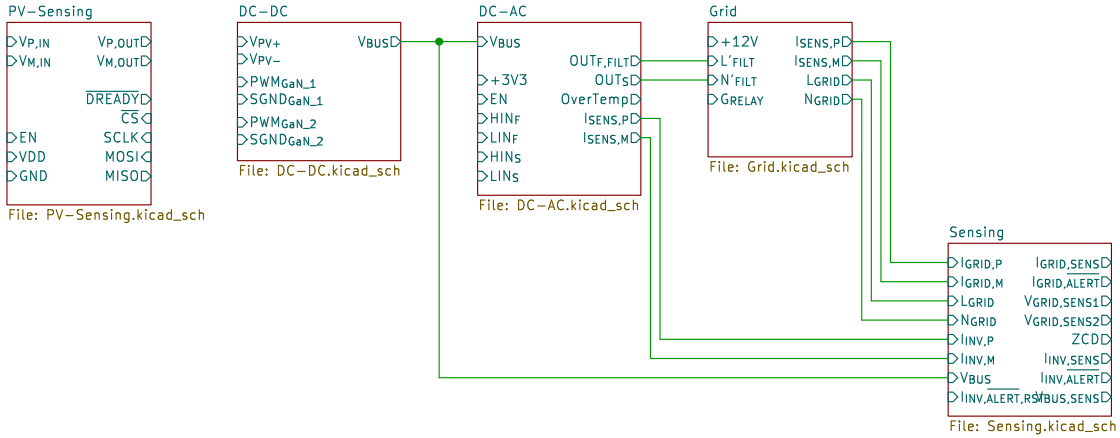

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Input Inductor

Reference:
AN4070 "250 W grid connected microinverter"

Calculation of minimum current value for CCM operation:
We assume we want to keep CCM operation down to
  P_{lim} = 25 W
  V_{in_min} = 30 V

Therefore, the following applies for each input inductor:
  I_{lim} = 1/2 * P_{lim}/V_{in} = 1/2 * 25 W/30 V = 0.417 A = ΔI_{ind}
  $L_{in} \geq (V_{in_min} * D_{switch_max}) / (\Delta I_{ind} * f_s)$
    ≥ (30 V * 0.7) / (0.417 A * 250 kHz)
    ≥ 200 uH

For the maximum current each inductors need to carry we can assume:
  $I_{max_average_inductor}$ = 0.5 * I_{max_input} = 0.5 * 12 A = 6 A
  P_{max_input} = P_{max_output} / η = 400 W / 0.90 = 444 W
  V_{in} = P_{max_input} / I_{max_input} = 444 W / 12 A = 37 V
  ΔI_{ripple} = (V_{in} * D_{switch_max}) / (L_{in} * f_s)
    = (37 V * 0.7) / (200 uH * 250 kHz)
    = 0.518 A
  $I_{peak_inductor}$ = $I_{max_average_inductor}$ + 0.5 * ΔI_{ripple}
    = 6 A + 0.5 * 0.518 A
    = 6.259 A

Under consideration of the calculated values, we choose the 74437429203151 as input inductor. Considerating the tolerance of ±20%:
  $L_{74437429203151_minimal}$ = 150 uH * 0.80 = 120 uH
we need 2 inductors in series which gives us
  L_{in} ≥ 2 * $L_{74437429203151_minimal}$
    ≥ 240 uH
Furthermore we need to considerate that for I = 6.0 A the inductance falls to 90% of the nominal value, which would be in the worst case:
  $L_{in_6.0A}$ = 2 * $L_{74437429203151_minimal}$ * 0.90
    = 216 uH
Therefore we met our condition L_{in} ≥ 200 uH.

TODO:
Remove 5V global label and use local label?
Use local label

TODO:
Put buck converter on top

Buck Converter
VDC
5V
+5V
File: Buck-Converter.kicad_sch

Input Capacity
VDC_IN
GND_IN
VDC_OUT
GND_OUT
VPV+
VPV-
GND1
File: Input-Capacity.kicad_sch

L3 74437429203151
L5 74437429203151
L4 74437429203151
L6 74437429203151

TIN1
TIN2

Transformer

The inductors (= boost converter) create a rise of voltage of
  V_{out_boost} = V_{in} * 1 / (1 − D),
where 0.5 < D ≤ 0.7.
If we take the equation for a transformer and put in the boost converter equation we get
  $N_2 / N_1 = V_2 / V_1$
    = V_{Bus} / V_{out_boost}
    = V_{Bus} * (1 − D) / V_{in}
If we assume V_{Bus} = 380 V, ΔV = 40 V (so $V_{bus,min}$ = 360 V, $V_{bus,max}$ = 400 V), V_{in} = 30 V we get
  N_2 / N_1 = 380 V * (1 − D) / 30 V
For D = 0.5:
  N_2 / N_1 = 6.33
For D = 0.7:
  N_2 / N_1 = 3.80

For V_{Bus} = 425 V, ΔV = 50 V (so $V_{bus,min}$ = 400 V; $V_{bus,max}$ = 450 V):
For D = 0.5:
  N_2 / N_1 = 425 V * (1 − 0.5) / 30 V = 7.08
For D = 0.7:
  N_2 / N_1 = 425 V * (1 − 0.7) / 30 V = 4.25

Take N = 4 and start U_MPPT_MIN > 32V

TOUT1
TOUT2

Rectifier

D4 IDL04G65C5
D6 IDL04G65C5
D8 IDL04G65C5
D3 IDL04G65C5
C10 1u_630V
GND2
VBUS

GaN FET Driver

TODO:
Do we use 5V PWM or 3.3V PWM?

+5V
C22 10u_25V
C24 100n_50V
GND1
U3 1EDN7550B
PWMGAN_1
SGNDGAN_1
R23 33K
R24 33K
R27 2R2
R28 500m
IN+
IN−
VDD
OUT_SRC
OUT_SNK
GND1

C23 10u_25V
C25 100n_50V
U4 1EDN7550B
PWMGAN_2
SGNDGAN_2
R25 33K
R26 33K
R29 2R2
R30 500m

Gate resistor recommendations in AN5583:
Turn on resistor: 2.2 Ω – 4.7 Ω
Turn off resistor: < 1 Ω
Compare with LTSPice results of
dc-dc-interleaved-boost-converter

Average power consumption for driving gate:
P_{gate} = C_{iss} * V_G^2 * f_{sw}
  = 865 pF * (5V)² * 250 kHz
  = 5.41 mW

Alternative GaN FET driver:
1EDN7116U, 2A, 3ns, 200V
2EDR7259X, dual channel, 5A, 9A, rise-time 7.5ns@1.8nF, 4.12€@1piece@mouser

GaN FET

Q4 GAN7R0-150LBEZ
Q5 GAN7R0-150LBEZ
F1 SMBJ100A
F2 SMBJ100A
R8 1M
R36 1M
GND1

Considerations about T_{on} and T_{off} for GaN FET:

With a 250 kHz PWM signal one period is
  T_{PWM} = 1 / 250 kHz = 4 us
With a 9 bit resolution the smallest possible pulse period becomes:
  T_{min} = 1 / (250 kHz * 29) = 7.81 ns
Because the duty cycle will only vary between 0.5 < D < 0.75, the period T_{on} will vary between
  0.5 * T_{PWM} < T_{on} < 0.75 * T_{PWM}
  2 us < T_{on} < 3 us

The GAN7R0-150LBEZ has total gate-source charge of
  Q_{GS} = 1.7 nC
To compute the time we need to charge Q_{GS} we can compute
  t_{charge_QGS} = t_{rise_driver} + Q_{GS} / I_{source_driver}
To compute the time we need to remove charge from the gate:
  $t_{discharge_QGS}$ = t_{rise_driver} + Q_{GS} / I_{sink_driver}

GaN FET driver recommendations according to ST Application Note AN5583
- high sink current I_{sink} to reduce Miller effect (> 3A, 7A peak is very good)
- low sink resistance R_{sink} to reduce bouncing between gate and source (< 1.5 Ω)
- trise/tfall < 20 ns @ C_{Load} = 2 nF
- $V_{GS,\ ON}$ = 6V
- CMTI (Common mode transient immunity) > 150 kV/us (High CMTI means capability to withstand fast dV/dt without dangerous glitches, jitter or short-circuit)

Considerations about possible GaN FET driver:
1EDN7550B (SOT23-6, 0.75€@1piecse) / 1EDN7550U (TSNP-6, 1.26€@1piece), 4A, 8A, truly differential inputs
1EDNx550 Gate Driver Application Examples And Layout Guidelines
1EDN7550 Product Page

The GAN7R0-150LBEZ has a input capacitance of
  C_{iss} = 865 pF
The gate driver 1EDN7550B has rise times of
  $t_{rise_1.8nF}$ = 6.5 ns
  t_{rise_200pF} = 1 ns
So using the GAN7R0-150LBEZ with the 1EDN7550B we can roughly asume:
  t_{rise_865pf} = (6.5 ns − 1 ns) / (1800 pF − 200 pF) * 865 pF
    = 2.97 ns
This results in
  t_{charge_QGS} = 2.97 ns + 1.7 nC / 4 A = 3.395 ns,
which is
  t_{charge_QGS} / $T_{on_minimal}$ = 3.395 ns / 2000 ns ≈ 0.0017,
so the rise time is at maximum 0.17% of the period time.
The results for the fall time should be roughly similar.

Simulating this in LTSpice with
  R_{Gate_SNK} = 2.2 Ω
  R_{Gate_SRC} = 0.5 Ω
results in the following times (measuring V_{GS} from 10% to 90%)
  t_{charge_QGS} = 8.44 ns → 0.42% of period time
  $t_{discharge_QGS}$ = 2.59 ns → 0.13% of period time

Sheet: /DC-DC/
File: DC-DC.kicad_sch
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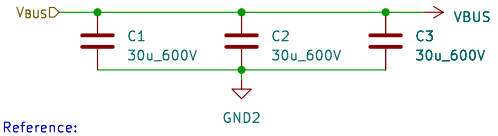
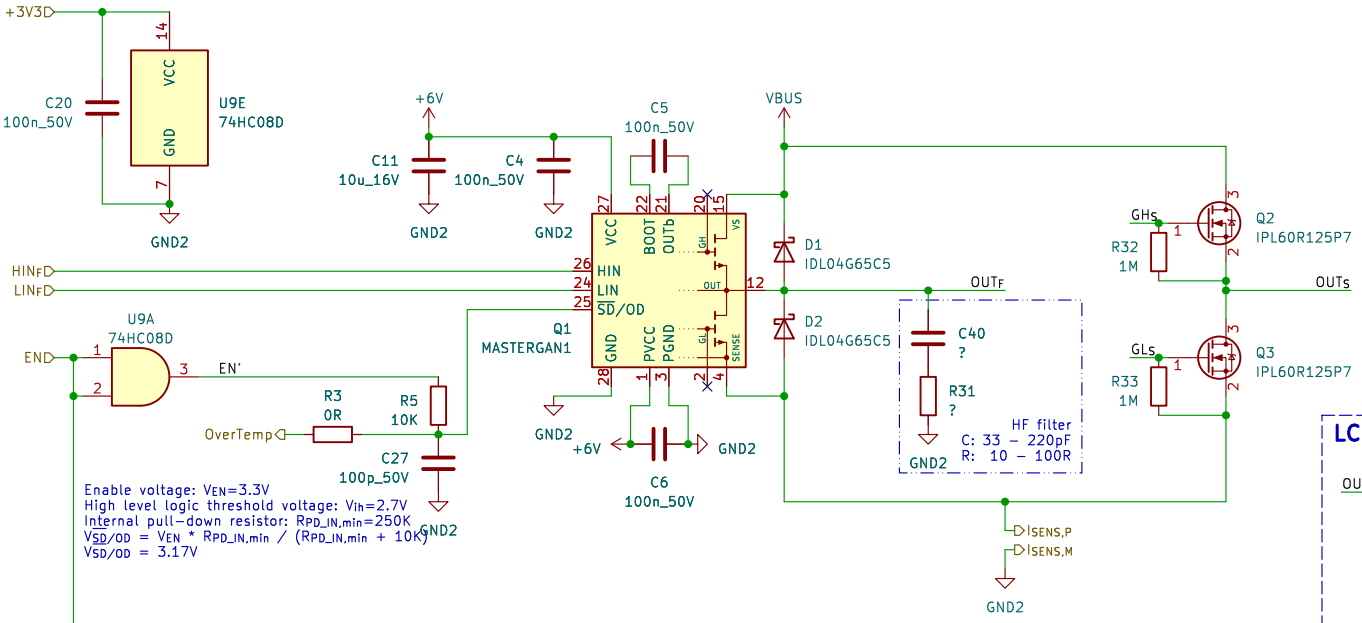
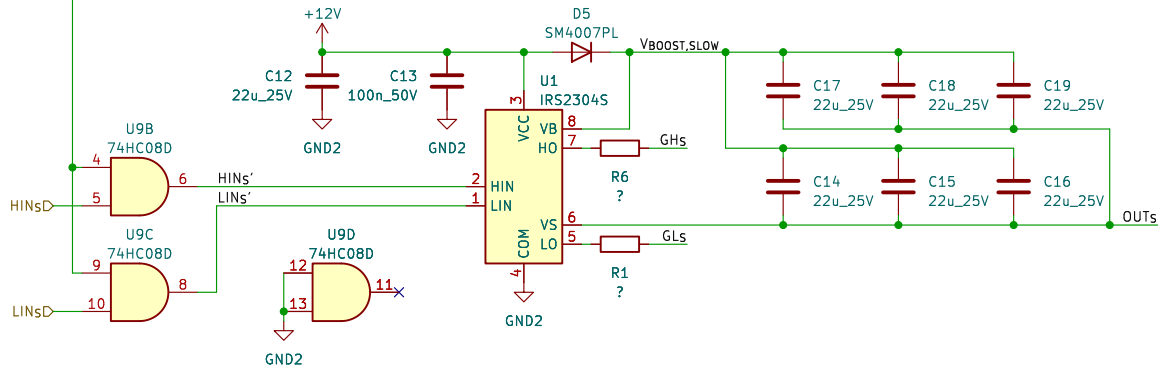
DC bus power decoupling

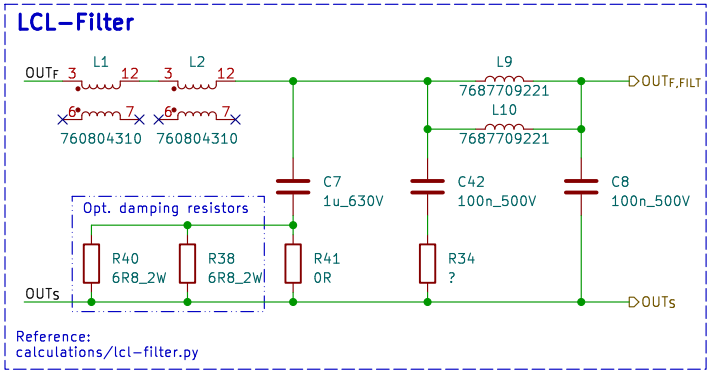
P_O = 400W
f = 50Hz
V_{bus} = 425V
ΔV = 50V => $V_{bus,min}$ = 400V; $V_{bus,max}$ = 450V
$C_{min} = P_O / (2\pi f * V_{bus} * \Delta V)$ = 59.92uF



Reference:
DC-Bus Design with Hybrid Capacitor Bank in Single-Phase PV Inverters
https://doi.org/10.1109/IECON.2017.8216408







Sheet: /DC-AC/		
File: DC-AC.kicad_sch		
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Line filter

Two different common chokes for two frequency ranges
- 744841330 for high frequencies
- 744822301 for low frequencies

X2: 0.1 – 0.33uF
Y2: 1.0 – 2.2nF

IEC 60384-14 specifies the use of X2 capacitors for "accross the line" and Y2 capacitors for "line to ground" and applications.

The common mode choke for high frequencies is placed near the inverter output to filter he high frequencies first.

Grid and system protection

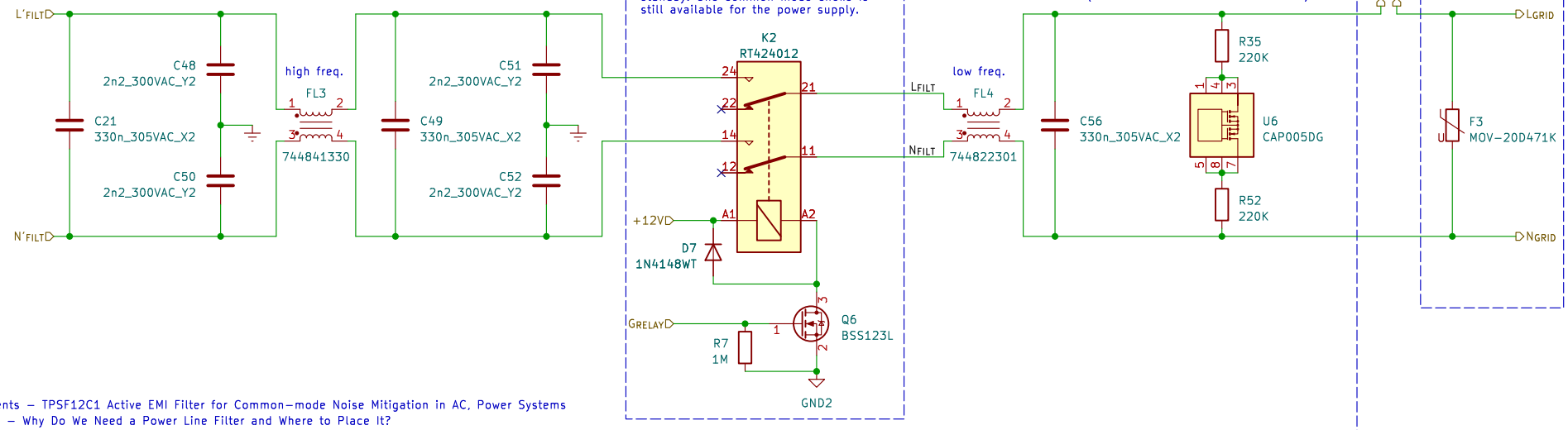
VDE-AR-N 4105 requires two independent protection mechanisms to disconnect the system from the grid in the event of a fault. The relais is one of them. The other one are the gate drivers of the inverter itself.

The relay is close to the line input to reduce copper losses of the filter in standby. One common mode choke is still available for the power supply.

The CAP005DG discharges the X2 and Y2 capacitors below 60V within a second as required by several standards (IEC 60065, IEC 60950, UEC 62368).

Overvoltage transient protection

The varistor protects the the circuit "accross the line".
The Y2 capacitors withstand the overvoltage transients on their own.



See also:
Texas Instruments – TPSF12C1 Active EMI Filter for Common-mode Noise Mitigation in AC, Power Systems
SOS Electronic – Why Do We Need a Power Line Filter and Where to Place It?

Sheet: /Grid/ File: Grid.kicad_sch		
Title:		
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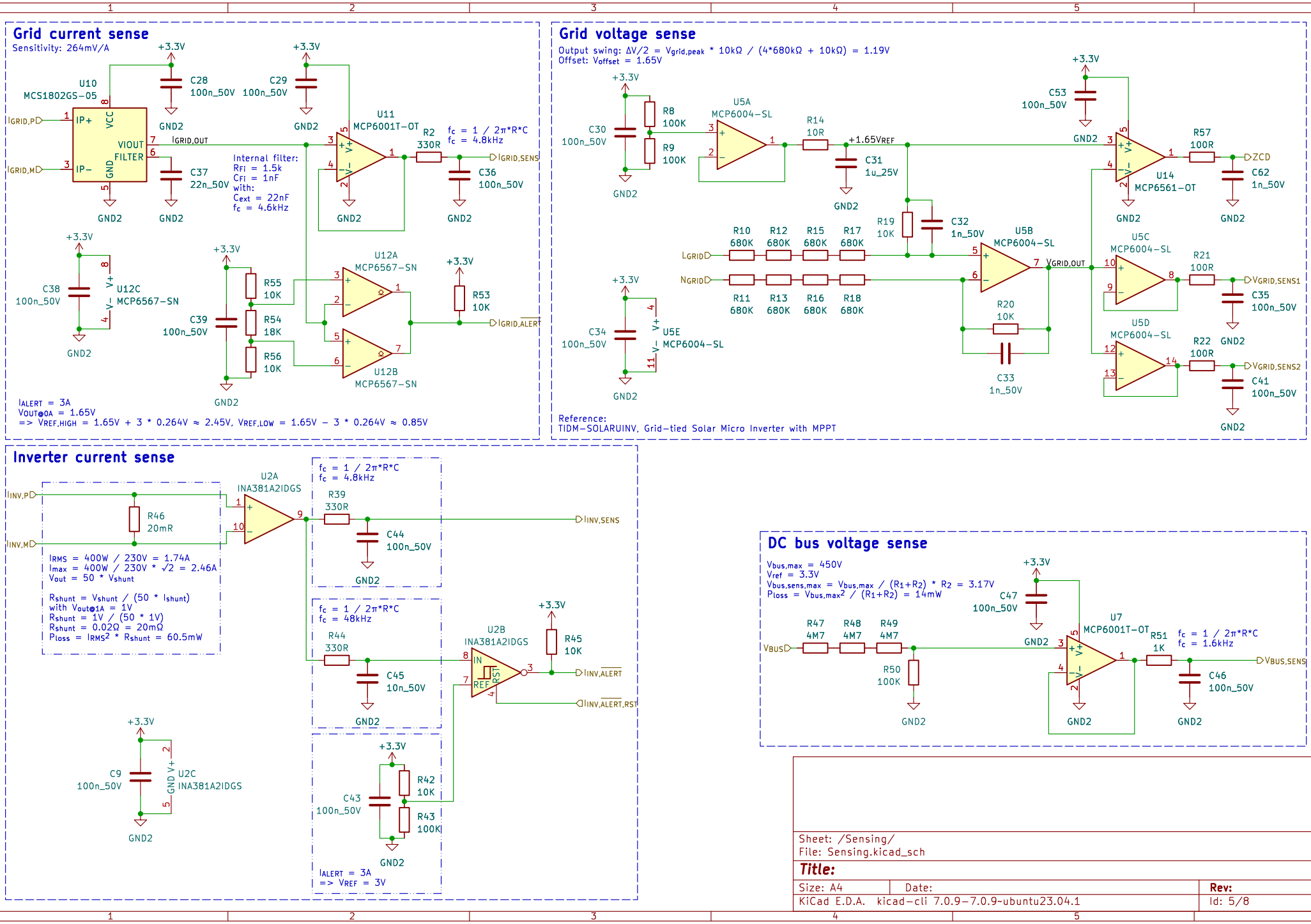
Grid current sense
Sensitivity: 264mV/A
U10
MCS1802GS-05
IP+
IP-
VCC
VIOUT
FILTER
GND
IGRID,P
IGRID,M
IGRID,OUT
C28
100n_50V
C29
100n_50V
C37
22n_50V
U11
MCP6001T-OT
R2
330R
fc = 1 / 2π*R*C
fc = 4.8kHz
IGRID,SENS
C36
100n_50V
Internal filter:
RFI = 1.5k
CFI = 1nF
with:
CEXT = 22nF
fc = 4.6kHz
+3.3V
GND2
C38
100n_50V
U12C
MCP6567-SN
C39
100n_50V
R55
10K
R54
18K
R56
10K
U12A
MCP6567-SN
U12B
MCP6567-SN
R53
10K
IGRID,ALERT
IALERT = 3A
VOUT@0A = 1.65V
=> VREF,HIGH = 1.65V + 3 * 0.264V ≈ 2.45V, VREF,LOW = 1.65V - 3 * 0.264V ≈ 0.85V
Grid voltage sense
Output swing: ΔV/2 = Vgrid,peak * 10kΩ / (4*680kΩ + 10kΩ) = 1.19V
Offset: Voffset = 1.65V
C30
100n_50V
R8
100K
R9
100K
U5A
MCP6004-SL
R14
10R
+1.65VREF
C31
1u_25V
C53
100n_50V
U14
MCP6561-OT
R57
100R
ZCD
C62
1n_50V
R19
10K
C32
1n_50V
U5B
MCP6004-SL
LGRID
NGRID
R10
680K
R12
680K
R15
680K
R17
680K
R11
680K
R13
680K
R16
680K
R18
680K
R20
10K
C33
1n_50V
VGRID,OUT
U5C
MCP6004-SL
R21
100R
VGRID,SENS1
C35
100n_50V
U5D
MCP6004-SL
R22
100R
VGRID,SENS2
C41
100n_50V
C34
100n_50V
U5E
MCP6004-SL
Reference:
TIDM-SOLARUINV, Grid-tied Solar Micro Inverter with MPPT
Inverter current sense
IINV,P
IINV,M
R46
20mR
U2A
INA381A2IDGS
IRMS = 400W / 230V = 1.74A
Imax = 400W / 230V * √2 = 2.46A
Vout = 50 * Vshunt
Rshunt = Vshunt / (50 * Ishunt)
with Vout@1A = 1V
Rshunt = 1V / (50 * 1V)
Rshunt = 0.02Ω = 20mΩ
Ploss = IRMS² * Rshunt = 60.5mW
fc = 1 / 2π*R*C
fc = 4.8kHz
R39
330R
C44
100n_50V
IINV,SENS
fc = 1 / 2π*R*C
fc = 48kHz
R44
330R
C45
10n_50V
U2B
INA381A2IDGS
R45
10K
IINV,ALERT
IINV,ALERT,RST
C9
100n_50V
U2C
INA381A2IDGS
C43
100n_50V
R42
10K
R43
100K
IALERT = 3A
=> VREF = 3V
DC bus voltage sense
Vbus,max = 450V
Vref = 3.3V
Vbus,sens,max = Vbus,max / (R1+R2) * R2 = 3.17V
Ploss = Vbus,max² / (R1+R2) = 14mW
C47
100n_50V
U7
MCP6001T-OT
VBUS
R47
4M7
R48
4M7
R49
4M7
R50
100K
R51
1K
fc = 1 / 2π*R*C
fc = 1.6kHz
VBUS,SENS
C46
100n_50V
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Input Capacity

Calculation of input capacitor for a Boost Converter like suggested in this ***Research Article:***

$C_{boost} \geq D_{max} * V / (8 * f_s^2 * L_{in} * \Delta V)$ | $\Delta V / V = 0.01$
$\geq D_{max} / (8 * f_s^2 * L_{in} * 0.01)$
$\geq 0.7 / (8 * (250\ kHz)^2 * 200\ uH * 0.01)$
$\geq 0.7\ uF$

Because we have two boost converter in parallel, so the nominal input capacity we need is:

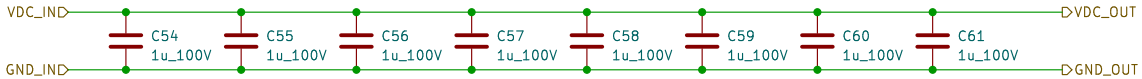
$C_{in,\ nominal} \geq 2 * C_{boost}$
$\geq 1.4\ uF$

By using MLCC capacitor we need to consider especially DC Bias, which for example
for the CL31B105KCHNNN (1.0uF_100V) capacitor is −65% at 60V.
Therefore we should design the input capacitance to be at least:

$C_{in} \geq 100/65 * C_{in,\ nominal}$
$\geq 1.538 * 1.4\ uF$
$\geq 2.15\ uF$

To compensate for other effects (like temperature, aging ...)
and including a little bit of safety margin, we choose:

C_{in} = 8 x 1.0uF_100V



Sheet: /DC−DC/Input Capacity/
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5V Buck Converter

General Considerations

Operating input voltage range: 16 V – 60 V, with a little safety margin we need about 80 – 100 V as maximum input voltag.

What consumers do we have to supply on the primary side?
(1) GaN MOSFET Gate Driver:
Average power consumption for driving gate:
$P_{gate} = C_{iss} * V_G^2 * f_{sw}$
$= 865\ pF * (5V)^2 * 250\ kHz$
$= 5.41\ mW$
For the output voltage of 5 V this results in:
$I_{out,1} = 5.41\ mW / 5\ V = 1.082\ mA$
(2) ADUM120N:
At 5V Operation and max data throughput (100 Mbps):
$I_{out,2} = 8.1\ mA$

This results in a full load current of:
$I_{out} = I_{out,1} + I_{out,2} = 9.182\ mA$

Finding a buck converter which is suited for $V_{in,max} = 100\ V$ and $I_{out} = 9.182\ mA$ is hard, most buck converter are rated for much higher output current (typically 500 mA).
A buck converter selection guide from TI can be found here:
https://www.ti.com/lit/sg/slyt729b/slyt729b.pdf
In summary we decide to take a buck converter, which is rated for $I_{out,max} = 500\ mA$.
If we would plan to run the buck converter in CCM for such low output current ($I_{out} = 9\ mA$) we would have to use a huge inductor because of the low available ripple current.
Therefore we design the buck converter for the lowest recommended value, which is $I_{out} = 100\ mA$ according to the calculation tool:
https://www.ti.com/lit/zip/snvc226

Enable/Undervoltage Lockout (EN/UVLO)
$V_{IN(on)} = 1.5\ V * (1 + (R_{UV1} / R_{UV2}))$
$= 1.5\ V * (1 + (330\ k\Omega / 47\ k\Omega))$
$= 12.03\ V$

Buck Inductor:
It is recommended to set the ripple current to 30% – 50% of the rated load current, which in this case would be
$\Delta I_L = 0.4 * 100\ mA = 40\ mA$
$\Delta I_L = (V_{OUT} / (f_{SW} * L_O)) * (1 - (V_{OUT} / V_{IN}))$

$L_O = (V_{OUT} / (f_{SW} * \Delta I_L)) * (1 - (V_{OUT} / V_{IN(nom)}))$
$= (5\ V / (500\ kHz * 0.04\ A)) * (1 - (5\ V / 40V))$
$= 218.75\ uH$
-> $L_O = 270\ uH$ with 10% tolerance (e.g. SRR1205-271KL) is in the worst case 243 uH

L7
270uH@0.6A

U8
LM5163
VIN, EN/UVLO, RON, GND, BST, SW, PGOOD, FB, EP

VDCI

C26
1u_100V

R4
330K

R5
47K

R37
10K

R53
15K

C27
2.2n_50V

R54
330K

C39
2n2_50V

C38
100p_50V

R55
330K

R56
82K

R57
22K

C53
2.2u_50V

5V

GND1

Maximum Duty Cycle
$D_{max} = V_{OUT} / (V_{IN(max)} * \eta)$
$= 5\ V / 60\ V * 0.7$
≈ 0.12

Input Capacitor:
According to *SLTA055* it is recommended as a general rule of thumb, keeping the input peak to peak ripple amplitude below 75 mV keeps the rms currents in the bulk capacitors within acceptable limits.
The CL31B105KCHNNN 1.0uF_100V X7R capacitor has a rms resistance of:
$R_{ESR@500\ kHz} = 11.76\ m\Omega$
With these numbers we can calculate the minimum input capacitance:
$C_{IN} \geq (I_{OUT} * D\ (1 - D)) / (f_{SW} * (V_{IN(ripple)} - I_{OUT} * R_{ESR}))$
$\geq (0.01\ A * 0.12 * (1 - 0.12)) / (500\ kHz * (75\ mV - 0.01\ A * 11.76\ m\Omega))$
$\geq 0.028\ uF$

Datasheet recommends 2.2 uF high quality X7S or X7R ceramic capacitor but as we calculated before we should get away with way less.
Using CL31B105KCHNNN (1.0uF_100V) capacitor with DC bias -65% at 60V and tolerance of ±10% gives us in the worst case:
$C_{IN_60V} = 1.0uF * 0.9 * 0.35 = 0.315uF$

TODO:
Double check if assumptions for input capacity are correct?
Maybe use 2 * 1u_100V?

Switching Frequency
Using $R_{RON} = 25\ k\Omega$ results in:
$f_{SW}(kHz) = V_{OUT} * 2500 / R_{RON}(k\Omega)$
$= 500\ kHz$

Ripple Generation Network:
More information: *SNVA776A*

Use Type 3 "Minimum Ripple" network:
First condition is
(1) $C_A \geq 10 / (f_{SW} * (R_{FB1} \parallel R_{FB2}))$
$\geq 10 / 500\ kHz * 79\ k\Omega$
$\geq 253\ pF.$
Second condition is
(2) $R_A * C_A \geq ((V_{IN-nom} - V_{OUT}) * T_{ON(@V_{IN_nom})}) / 20\ mV.$
By calculating
$T_{ON(@V_{IN_nom})} = D_{V_{IN_nom}} / f_{SW}$
$= V_{OUT} / (V_{IN_nom} * \eta * f_{SW})$
$= 5\ V / (48\ V * 0.65 * 500\ kHz)$
$= 0.321\ us$
we get
$R_A * C_A \geq ((V_{IN-nom} - V_{OUT}) * T_{ON(@V_{IN_nom})}) / 20\ mV$
$\geq ((48\ V - 5\ V) * 0.321\ us) / 20\ mV$
$\geq 0,00069.$
Rearranging this to R_A gives us:
$R_A \geq 0,00069 / C_A$
To keep R_A within practical limits (100 kΩ < R_A < 1MΩ for low-IQ converters) we select
$C_A = 2200\ pF$
which gives us
$R_A \geq 313,7\ k\Omega$
Third condition is
(3) $C_B \geq t_{TR-Settling} / (3 * R_{FB1})$
where $t_{TR-Settling}$ is the desired load transient response settling time.
The datasheet calculates with 75 µs settling time, resulting in:
$C_{B,\ 75\ \mu s} \geq 75,8\ pF$
The application note chooses 50 µs settling time, resulting in:
$C_{B,\ 50\ \mu s} \geq 50,5\ pF$
To avoid capacitance fall-off with DC bias, use a COG or NP0 dielectric capacitor for C_B.

Output Capacitor:
$C_{Out} \geq \Delta I_L / (8 * f_{SW} * V_{out(ripple)})$
$\geq 40\ mA / (8 * 500\ kHz * 0.005 * 5\ V)$
$\geq 0.4\ uF$

Voltage Feedback:
$R_{FB1} = 330\ k\Omega$
$R_{FB2} = (1.2\ V / (V_{OUT} - 1.2\ V)) * R_{FB1}$
$= 6 / 19 * R_{FB1}$
$= 104.21\ k\Omega$

Sheet: /DC-DC/Buck Converter/
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Voltage & current sense

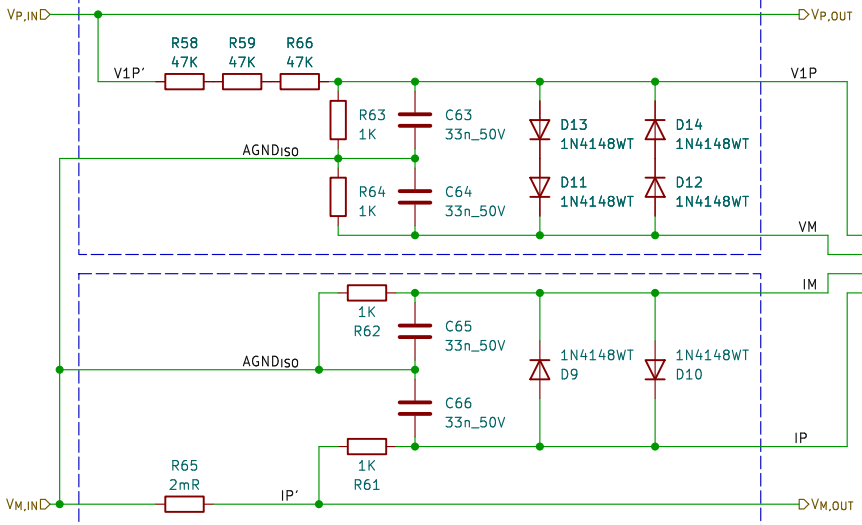
Anti-aliasing filter:
$f_c = 1 / (2\pi * R * C)$
$f_c = 1 / (2\pi\ 1kR * 33nF)$
$f_c = 4.8kHz$

Overvoltage protection:
The diodes protect the inputs of the ADE7912 from overvoltage.
Thanks to the bidirectional use of the diodes, the inputs of the ADE7912 are also protected against transient overvoltages.

Voltage sense

From specifications:
Operating voltage range: 16-60V

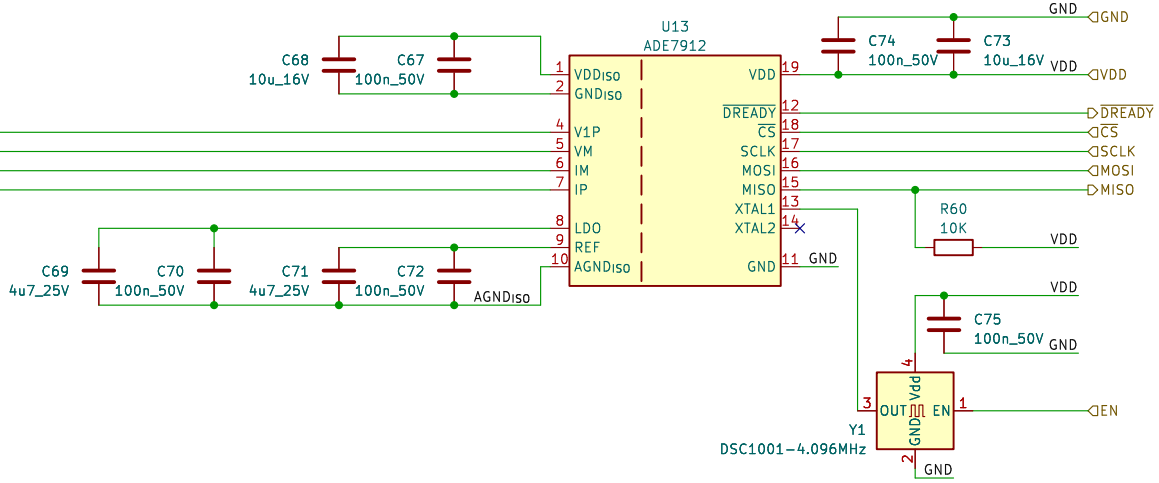
Add 20% safety margin:
$U_{max} = 60V * 120\% = 72V$
$U_{V1P,max} = 0.5V$
=> Ideal resistor ratio: 1 / 143
=> $R_1 = 1kR$; $R_2 = 3 * 47kR$



Current sense

From specifications:
Maximum input current: 12A

Add 20% safety margin:
$I_{max} = 60V * 120\% = 14.4V$
$U_{IP,max} = 31.25mV$
=> $P_{max} = U_{IP,max} * I_{max} = 450mW$
=> $R_{max} = U_{IP,max} / I_{max}$
=> $R_{max} = 2.17mR$
=> $R = 2mR$



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