

Input Inductor

Reference:
ANA070 "250 W grid connected microinverter"

Calculation of minimum current value for CCM operation:
We assume we want to keep CCM operation down to
 $P_{lim} = 25\text{ W}$
 $V_{in_min} = 30\text{ V}$
Therefore, the following applies for each input inductor:
 $I_{lim} = 1/2 * P_{lim}/V_{in} = 1/2 * 25\text{ W}/30\text{ V} = 0.417\text{ A} = \Delta I_{ind}$
 $L_{in} \geq (V_{in_min} * D_{switch_max}) / (\Delta I_{ind} * f_s)$
 $\geq (30\text{ V} * 0.7) / (0.417\text{ A} * 250\text{ kHz})$
 $\geq 200\text{ uH}$

For the maximum current each inductors need to carry we can assume:
 $I_{max_average_inductor} = 0.5 * I_{max_input} = 0.5 * 12\text{ A} = 6\text{ A}$
 $P_{max_input} = P_{max_output} / \eta = 400\text{ W} / 0.90 = 444\text{ W}$
 $V_{in} = P_{max_input} / I_{max_input} = 444\text{ W} / 12\text{ A} = 37\text{ V}$
 $\Delta I_{ripple} = (V_{in} * D_{switch_max}) / (L_{in} * f_s)$
 $= (37\text{ V} * 0.7) / (200\text{ uH} * 250\text{ kHz})$
 $= 0.518\text{ A}$
 $I_{peak_inductor} = I_{max_average_inductor} + 0.5 * \Delta I_{ripple}$
 $= 6\text{ A} + 0.5 * 0.518\text{ A}$
 $= 6.259\text{ A}$

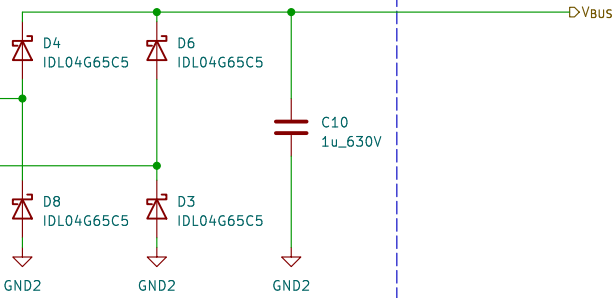
Under consideration of the calculated values, we choose the 74437429203151 as input inductor. Considering the tolerance of $\pm 20\%$:
 $L_{74437429203151_minimal} = 150\text{ uH} * 0.80 = 120\text{ uH}$
we need 2 inductors in series which gives us
 $L_{in} \geq 2 * L_{74437429203151_minimal}$
 $\geq 240\text{ uH}$
Furthermore we need to considerate that for $I = 6.0\text{ A}$ the inductance falls to 90% of the nominal value, which would be in the worst case:
 $L_{in_6.0A} = 2 * L_{74437429203151_minimal} * 0.90$
 $= 216\text{ uH}$
Therefore we met our condition $L_{in} \geq 200\text{ uH}$.

Transformer

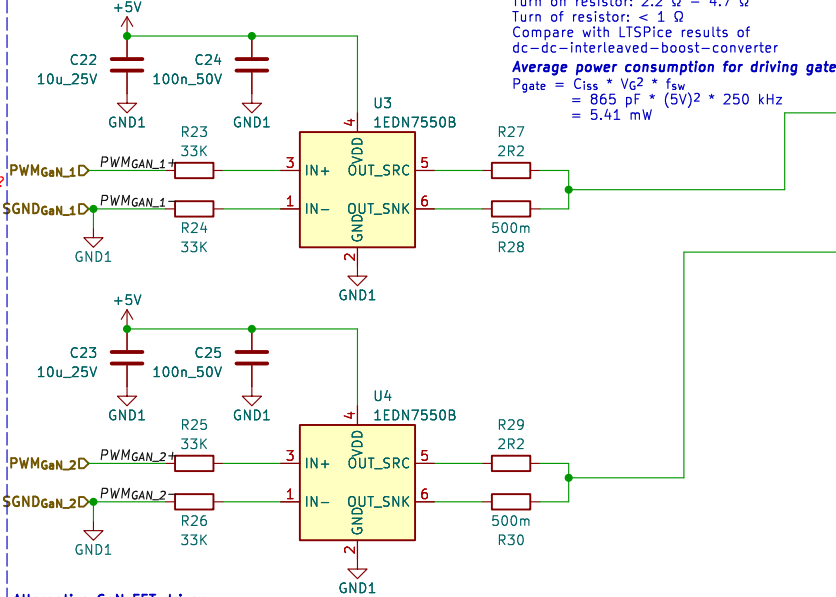
The inductors (= boost converter) create a rise of voltage of
 $V_{out_boost} = V_{in} * 1 / (1 - D)$,
where $0.5 < D \leq 0.7$.
If we take the equation for a transformer and put in the boost converter equation we get
 $N_2 / N_1 = V_2 / V_1$
 $= V_{Bus} / V_{out_boost}$
 $= V_{Bus} * (1 - D) / V_{in}$
If we assume $V_{Bus} = 380\text{ V}$, $\Delta V = 40\text{ V}$ (so $V_{bus,min} = 360\text{ V}$, $V_{bus,max} = 400\text{ V}$), $V_{in} = 30\text{ V}$ we get
 $N_2 / N_1 = 380\text{ V} * (1 - D) / 30\text{ V}$
For $D = 0.5$:
 $N_2 / N_1 = 6.33$
For $D = 0.7$:
 $N_2 / N_1 = 3.80$
For $V_{Bus} = 425\text{ V}$, $\Delta V = 50\text{ V}$ (so $V_{bus,min} = 400\text{ V}$; $V_{bus,max} = 450\text{ V}$):
For $D = 0.5$:
 $N_2 / N_1 = 425\text{ V} * (1 - 0.5) / 30\text{ V} = 7.08$
For $D = 0.7$:
 $N_2 / N_1 = 425\text{ V} * (1 - 0.7) / 30\text{ V} = 4.25$

Take $N = 4$ and start $U_{MPPT_MIN} > 32\text{ V}$

Rectifier

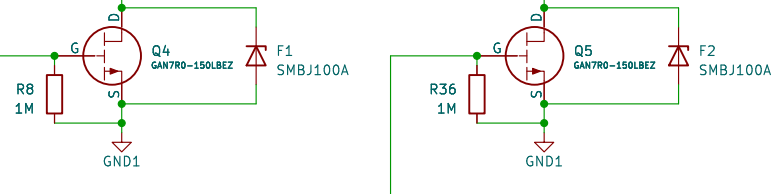


GaN FET Driver



Alternative GaN FET driver:
1EDN7116U, 2A, 3ns, 200V
2EDR7259X, dual channel, 5A, 9A, rise-time 7.5ns@1.8nF, 4.12€@1piece@mouser

GaN FET



Considerations about Ton and Toff for GaN FET:

With a 250 kHz PWM signal one period is
 $T_{PWM} = 1 / 250\text{ kHz} = 4\text{ us}$
With a 9 bit resolution the smallest possible pulse period becomes:
 $T_{min} = 1 / (250\text{ kHz} * 2^9) = 7.81\text{ ns}$
Because the duty cycle will only vary between $0.5 < D < 0.75$, the period T_{on} will vary between
 $0.5 * T_{PWM} < T_{on} < 0.75 * T_{PWM}$
 $2\text{ us} < T_{on} < 3\text{ us}$

The GAN7R0-150LBEZ has total gate-source charge of
 $Q_{GS} = 1.7\text{ nC}$
To compute the time we need to charge Q_{GS} we can compute
 $t_{charge_QGS} = t_{rise_driver} + Q_{GS} / I_{source_driver}$
To compute the time we need to remove charge from the gate:
 $t_{discharge_QGS} = t_{rise_driver} + Q_{GS} / I_{sink_driver}$

GaN FET driver recommendations according to ST Application Note AN5583

- high sink current I_{sink} to reduce Miller effect ($> 3\text{ A}$, 7A peak is very good)
- low sink resistance R_{sink} to reduce bouncing between gate and source ($< 1.5\text{ }\Omega$)
- $t_{rise}/t_{fall} < 20\text{ ns}$ @ $C_{load} = 2\text{ nF}$
- $V_{GS_ON} = 6\text{ V}$
- CMTI (Common mode transient immunity) $> 150\text{ kV/us}$ (High CMTI means capability to withstand fast dV/dt without dangerous glitches, jitter or short-circuit)

Considerations about possible GaN FET driver:

1EDN7550B (SOT23-6, 0.75€@1piece) / 1EDN7550U (TSNP-6, 1.26€@1piece), 4A, 8A, truly differential inputs
1EDNx550 Gate Driver Application Examples And Layout Guidelines
1EDN7550 Product Page

The GAN7R0-150LBEZ has a input capacitance of
 $C_{iss} = 865\text{ pF}$
The gate driver 1EDN7550B has rise times of
 $t_{rise_1.8nF} = 6.5\text{ ns}$
 $t_{rise_200pF} = 1\text{ ns}$
So using the GAN7R0-150LBEZ with the 1EDN7550B we can roughly assume:
 $t_{rise_865pF} = (6.5\text{ ns} - 1\text{ ns}) / (1800\text{ pF} - 200\text{ pF}) * 865\text{ pF}$
 $= 2.97\text{ ns}$

This results in
 $t_{charge_QGS} = 2.97\text{ ns} + 1.7\text{ nC} / 4\text{ A} = 3.395\text{ ns}$,
which is
 $t_{charge_QGS} / T_{on_minimal} = 3.395\text{ ns} / 2000\text{ ns} \approx 0.0017$,
so the rise time is at maximum 0.17% of the period time.
The results for the fall time should be roughly similar.

Simulating this in LTSpice with
 $R_{gate_SNK} = 2.2\text{ }\Omega$
 $R_{gate_SRC} = 0.5\text{ }\Omega$
results in the following times (measuring V_{GS} from 10% to 90%)
 $t_{charge_QGS} = 8.44\text{ ns} \rightarrow 0.42\%$ of period time
 $t_{discharge_QGS} = 2.59\text{ ns} \rightarrow 0.13\%$ of period time

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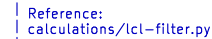
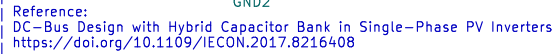
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$P_0 = 400\text{W}$
 $f = 50\text{Hz}$
 $V_{\text{bus}} = 425\text{V}$
 $\Delta V = 50\text{V} \Rightarrow V_{\text{bus,min}} = 400\text{V}; V_{\text{bus,max}} = 450\text{V}$
 $C_{\text{min}} = P_0 / (2\pi f * V_{\text{bus}} * \Delta V) = 59.92\mu\text{F}$



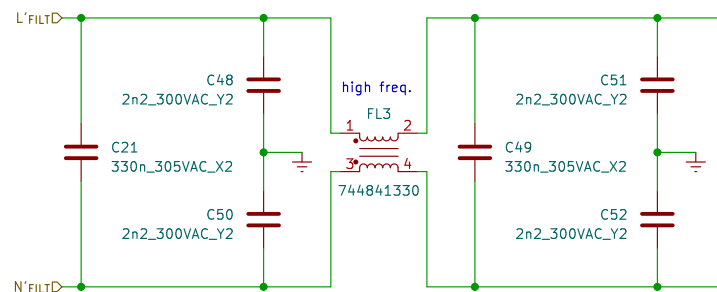
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Line filter

Two different common chokes for two frequency ranges
 - 744841330 for high frequencies
 - 744822301 for low frequencies
 X2: 0.1 - 0.33uF
 Y2: 1.0 - 2.2nF

IEC 60384-14 specifies the use of X2 capacitors for "across the line" and Y2 capacitors for "line to ground" and applications.

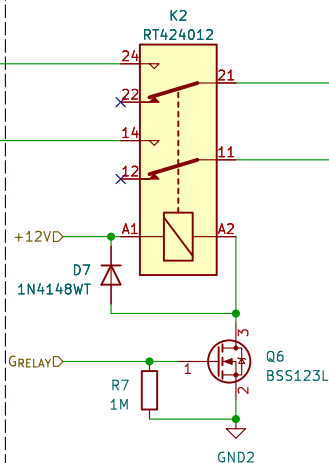
The common mode choke for high frequencies is placed near the inverter output to filter the high frequencies first.



Grid and system protection

VDE-AR-N 4105 requires two independent protection mechanisms to disconnect the system from the grid in the event of a fault. The relays are one of them. The other one is the gate drivers of the inverter itself.

The relay is close to the line input to reduce copper losses of the filter in standby. One common mode choke is still available for the power supply.



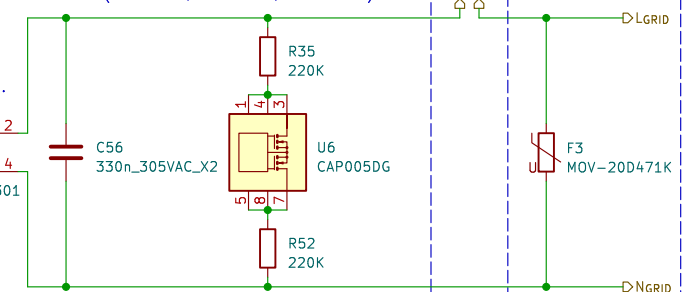
See also:

Texas Instruments - TPSF12C1 Active EMI Filter for Common-mode Noise Mitigation in AC, Power Systems
 SOS Electronic - Why Do We Need a Power Line Filter and Where to Place It?

Overvoltage transient protection

The varistor protects the circuit "across the line". The Y2 capacitors withstand the overvoltage transients on their own.

The CAP005DG discharges the X2 and Y2 capacitors below 60V within a second as required by several standards (IEC 60065, IEC 60950, UEC 62368).



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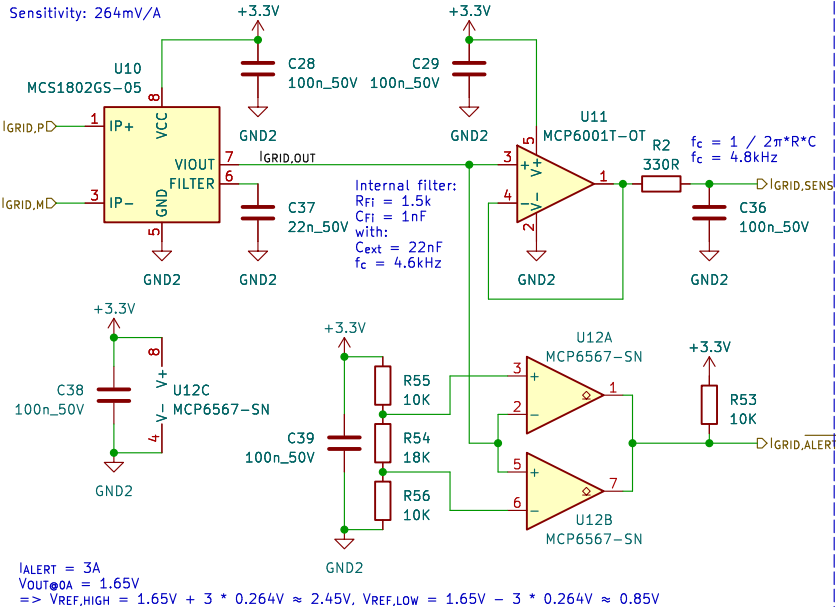
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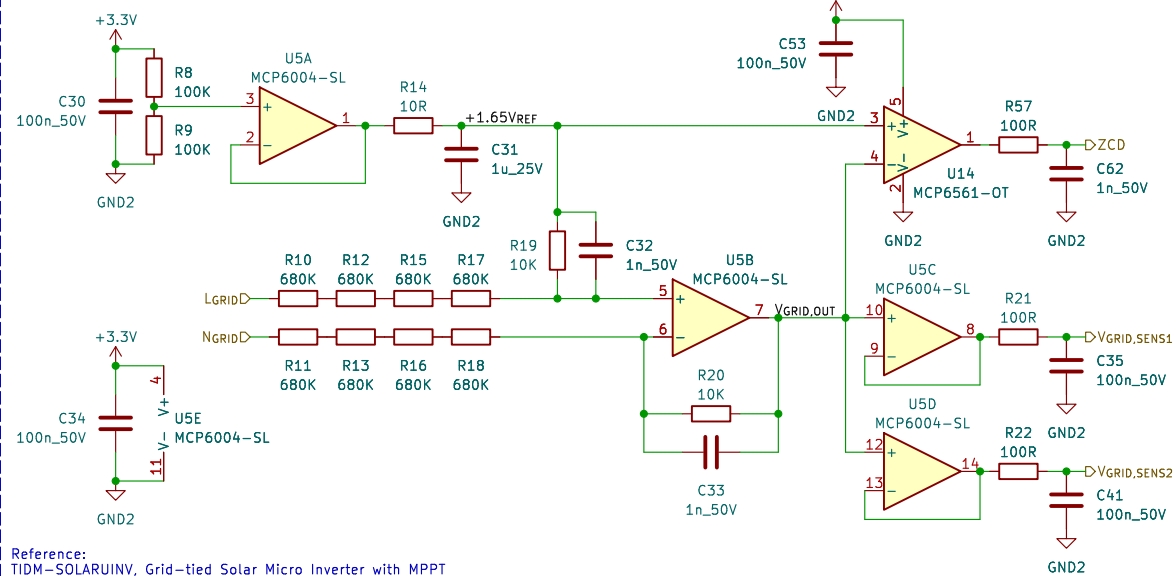
Grid current sense

Sensitivity: 264mV/A

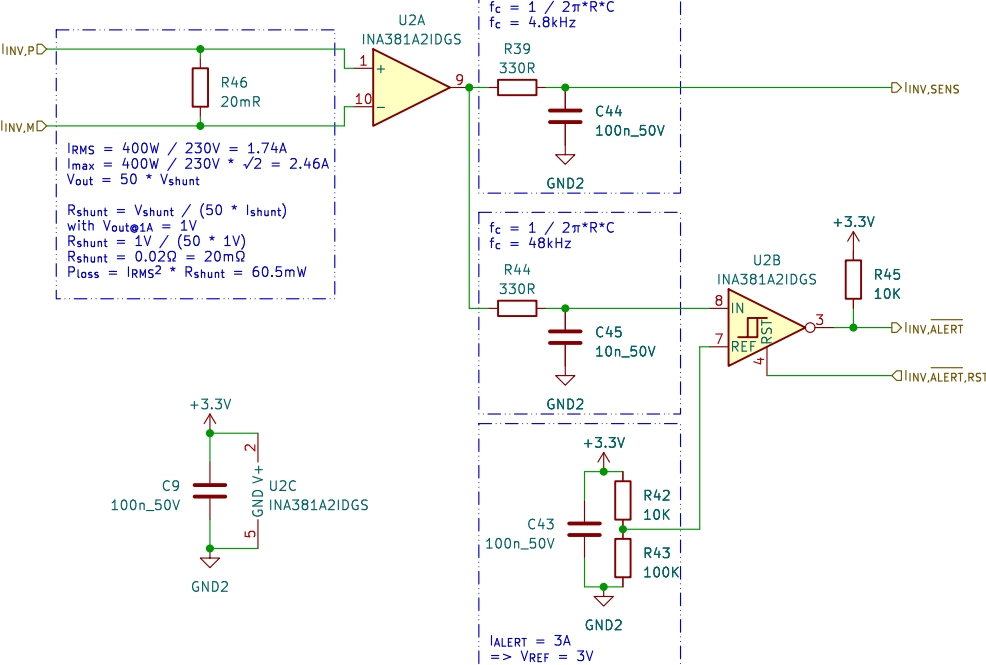


Grid voltage sense

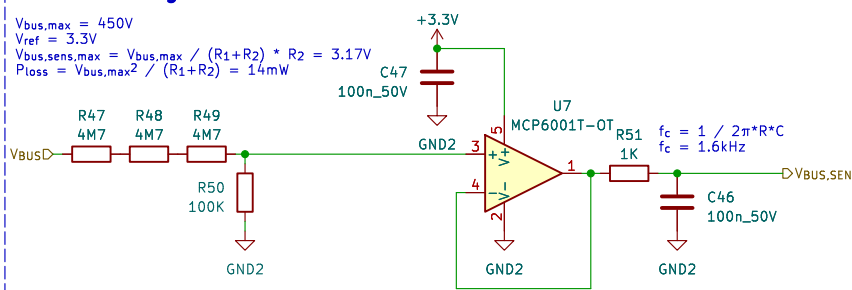
Output swing: $\Delta V/2 = V_{grid,peak} * 10k\Omega / (4*680k\Omega + 10k\Omega) = 1.19V$
 Offset: $V_{offset} = 1.65V$



Inverter current sense



DC bus voltage sense



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Input Capacity

Calculation of input capacitor for a Boost Converter like suggested in the [Research Article](#):

$$C_{boost} \geq \frac{D_{max} \cdot V}{(8 \cdot f_s^2 \cdot L_{in} \cdot \Delta V)} \quad | \Delta V / V = 0.01$$
$$\geq \frac{D_{max}}{(8 \cdot f_s^2 \cdot L_{in} \cdot 0.01)}$$
$$\geq 0.7 / (8 \cdot (250 \text{ kHz})^2 \cdot 200 \text{ uH} \cdot 0.01)$$
$$\geq 0.7 \text{ uF}$$

Because we have two boost converter in parallel, so the nominal input capacity we need is:

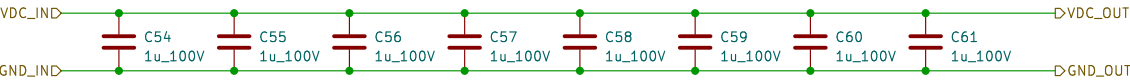
$$C_{in, nominal} \geq 2 \cdot C_{boost}$$
$$\geq 1.4 \text{ uF}$$

By using MLCC capacitor we need to consider especially DC Bias, which for example for the CL31B105KCHNNN (1.0uF_100V) capacitor is -65% at 60V. Therefore we should design the input capacitance to be at least:

$$C_{in} \geq 100/65 \cdot C_{in, nominal}$$
$$\geq 1.538 \cdot 1.4 \text{ uF}$$
$$\geq 2.15 \text{ uF}$$

To compensate for other effects (like temperature, aging ...) and including a little bit of safety margin, we choose:

$$C_{in} = 8 \times 1.0\text{uF}_{100\text{V}}$$



5V Buck Converter

General Considerations

Operating input voltage range: 16 V – 60 V, with a little safety margin we need about 80 – 100 V as maximum input voltage.

What consumers do we have to supply on the primary side?

(1) GaN MOSFET Gate Driver:

Average power consumption for driving gate:

$$\begin{aligned} P_{\text{gate}} &= C_{\text{iss}} * V_{\text{G}}^2 * f_{\text{sw}} \\ &= 865 \text{ pF} * (5\text{V})^2 * 250 \text{ kHz} \\ &= 5.41 \text{ mW} \end{aligned}$$

For the output voltage of 5 V this results in:

$$I_{\text{out},1} = 5.41 \text{ mW} / 5 \text{ V} = 1.082 \text{ mA}$$

(2) ADUM120N:

At 5V Operation and max data throughput (100 Mbps):

$$I_{\text{out},2} = 8.1 \text{ mA}$$

This results in a full load current of:

$$I_{\text{out}} = I_{\text{out},1} + I_{\text{out},2} = 9.182 \text{ mA}$$

Finding a buck converter which is suited for $V_{\text{in,max}} = 100 \text{ V}$ and $I_{\text{out}} = 9.182 \text{ mA}$ is hard, most buck converter are rated for much higher output current (typically 500 mA).

A buck converter selection guide from TI can be found here:

<https://www.ti.com/lit/sg/slyt729b/slyt729b.pdf>

In summary we decide to take a buck converter, which is rated for $I_{\text{out,max}} = 500 \text{ mA}$.

If we would plan to run the buck converter in CCM for such low output current ($I_{\text{out}} = 9 \text{ mA}$) we would have to use a huge inductor because of the low available ripple current.

Therefore we design the buck converter for the lowest recommended value, which is $I_{\text{out}} = 100 \text{ mA}$ according to the calculation tool:

<https://www.ti.com/lit/zip/snvc226>

Maximum Duty Cycle

$$\begin{aligned} D_{\text{max}} &= V_{\text{OUT}} / (V_{\text{IN(max)}} * \eta) \\ &= 5 \text{ V} / 60 \text{ V} * 0.7 \\ &\approx 0.12 \end{aligned}$$

Input Capacitor:

According to SLTA055 it is recommended as a general rule of thumb, keeping the input peak to peak ripple amplitude below 75 mV keeps the rms currents in the bulk capacitors within acceptable limits.

The CL31B105KCHNNN 1.0uF_100V X7R capacitor has a rms resistance of:

$$\text{RESR@500 kHz} = 11.76 \text{ m}\Omega$$

With these numbers we can calculate the minimum input capacitance:

$$\begin{aligned} C_{\text{IN}} &\geq (I_{\text{out}} * D * (1 - D)) / (f_{\text{sw}} * (V_{\text{IN(ripple)}} - I_{\text{out}} * \text{RESR})) \\ &\approx (0.01 \text{ A} * 0.12 * (1 - 0.12)) / (500 \text{ kHz} * (75 \text{ mV} - 0.01 \text{ A} * 11.76 \text{ m}\Omega)) \\ &\approx 0.028 \text{ uF} \end{aligned}$$

Datasheet recommends 2.2 uF high quality X7S or X7R ceramic capacitor

but as we calculated before we should get away with way less.

Using CL31B105KCHNNN (1.0uF_100V) capacitor with DC bias –65% at 60V and tolerance of ±10% gives us in the worst case:

$$C_{\text{IN,60V}} = 1.0\text{uF} * 0.9 * 0.35 = 0.315\text{uF}$$

TODO:

Double check if assumptions
for input capacity are correct?
Maybe use 2 * 1u_100V?

Enable/Undervoltage Lockout (EN/UVLO)

$$\begin{aligned} V_{\text{IN(on)}} &= 1.5 \text{ V} * (1 + (R_{\text{UV1}} / R_{\text{UV2}})) \\ &= 1.5 \text{ V} * (1 + (330 \text{ k}\Omega / 47 \text{ k}\Omega)) \\ &= 12.03 \text{ V} \end{aligned}$$

Switching Frequency

$$\begin{aligned} \text{Using } R_{\text{RON}} &= 25 \text{ k}\Omega \text{ results in:} \\ f_{\text{sw}}(\text{kHz}) &= V_{\text{OUT}} * 2500 / R_{\text{RON}}(\text{k}\Omega) \\ &= 500 \text{ kHz} \end{aligned}$$

Buck Inductor:

It is recommended to set the ripple current to 30% – 50% of the rated load current, which in this case would be

$$\Delta I_L = 0.4 * 100 \text{ mA} = 40 \text{ mA}$$

$$\Delta I_L = (V_{\text{OUT}} / (f_{\text{sw}} * L_o)) * (1 - (V_{\text{OUT}} / V_{\text{IN}}))$$

$$\begin{aligned} L_o &= (V_{\text{OUT}} / (f_{\text{sw}} * \Delta I_L)) * (1 - (V_{\text{OUT}} / V_{\text{IN(nom)}})) \\ &= (5 \text{ V} / (500 \text{ kHz} * 0.04 \text{ A})) * (1 - (5 \text{ V} / 40\text{V})) \\ &= 218.75 \text{ uH} \end{aligned}$$

-> $L_o = 270 \text{ uH}$ with 10% tolerance (e.g. SRR1205–271KL) is in the worst case 243 uH

Output Capacitor:

$$\begin{aligned} C_{\text{OUT}} &\geq \Delta I_L / (8 * f_{\text{sw}} * V_{\text{OUT(ripple)}}) \\ &\geq 40 \text{ mA} / (8 * 500 \text{ kHz} * 0.005 * 5 \text{ V}) \\ &\geq 0.4 \text{ uF} \end{aligned}$$

Ripple Generation Network:

More information: SNVA776A

Use Type 3 "Minimum Ripple" network:

First condition is

$$\begin{aligned} (1) \quad C_A &\geq 10 / (f_{\text{sw}} * (R_{\text{FB1}} || R_{\text{FB2}})) \\ &\geq 10 / 500 \text{ kHz} * 79 \text{ k}\Omega \\ &\geq 253 \text{ pF} \end{aligned}$$

Second condition is

$$(2) \quad R_A * C_A \geq ((V_{\text{IN(nom)}} - V_{\text{OUT}}) * T_{\text{ON}}(V_{\text{IN(nom)}})) / 20 \text{ mV}$$

By calculating

$$\begin{aligned} T_{\text{ON}}(V_{\text{IN(nom)}}) &= D V_{\text{IN(nom)}} / f_{\text{sw}} \\ &= V_{\text{OUT}} / (V_{\text{IN(nom)}} * \eta * f_{\text{sw}}) \\ &= 5 \text{ V} / (48 \text{ V} * 0.65 * 500 \text{ kHz}) \\ &= 0.321 \text{ us} \end{aligned}$$

we get

$$\begin{aligned} R_A * C_A &\geq ((V_{\text{IN(nom)}} - V_{\text{OUT}}) * T_{\text{ON}}(V_{\text{IN(nom)}})) / 20 \text{ mV} \\ &\geq ((48 \text{ V} - 5 \text{ V}) * 0.321 \text{ us}) / 20 \text{ mV} \\ &\geq 0.00069 \end{aligned}$$

Rearranging this to R_A gives us:

$$R_A \geq 0.00069 / C_A$$

To keep R_A within practical limits (100 k Ω < R_A < 1M Ω for low- I_o converters) we select

$$C_A = 2200 \text{ pF}$$

which gives us

$$R_A \geq 313.7 \text{ k}\Omega$$

Third condition is

$$(3) \quad C_B \geq t_{\text{tr-Settling}} / (3 * R_{\text{FB1}})$$

where $t_{\text{tr-Settling}}$ is the desired load transient response settling time.

The datasheet calculates with 75 μs settling time, resulting in:

$$C_B, 75 \mu\text{s} \geq 75.8 \text{ pF}$$

The application note chooses 50 μs settling time, resulting in:

$$C_B, 50 \mu\text{s} \geq 50.5 \text{ pF}$$

To avoid capacitance fall-off with DC bias, use a COG or NPO dielectric capacitor for C_B .

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