

SOM1 A & B

A

MIO:
- route as SE50
- must be 1.8V compatible

B

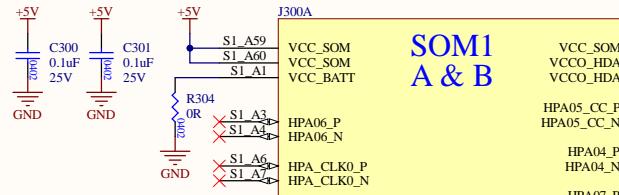
PS-GTR Transceivers:
- Route DP data lines as stripline
- 90 ohm differential impedance
- length match to +0.5mil
- maximum 2 via transitions

C

Boot Mode: QSPI
PS_MODE[3:0] = 0010

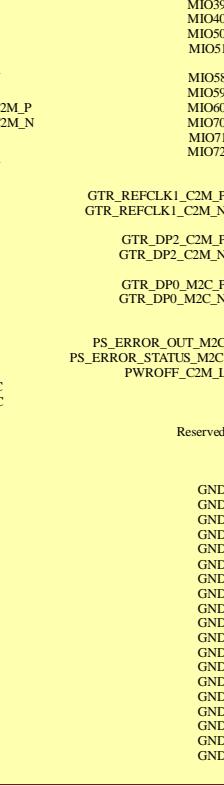
D

UART1 TX
D304 ESD321DYAR
UART1 RX
D305 ESD321DYAR



**SOM1
A & B**

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V _{CC} _SOM	5V (4.75V - 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V _{CC} _BATT	1.20 - 1.50V	150 nA - 3850 nA	External battery input for the RTC
V _{CCO_HPA}	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 66
V _{CCO_HPB}	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 65
V _{CCO_HPC}	1.00V - 1.80V	1.0A	Voltage rail for HPIO bank 64
V _{CCO_HDA}	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 45
V _{CCO_HOB}	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 43
V _{CCO_HDC}	1.20V - 3.30V	1.0A	Voltage rail for HDIO bank 44

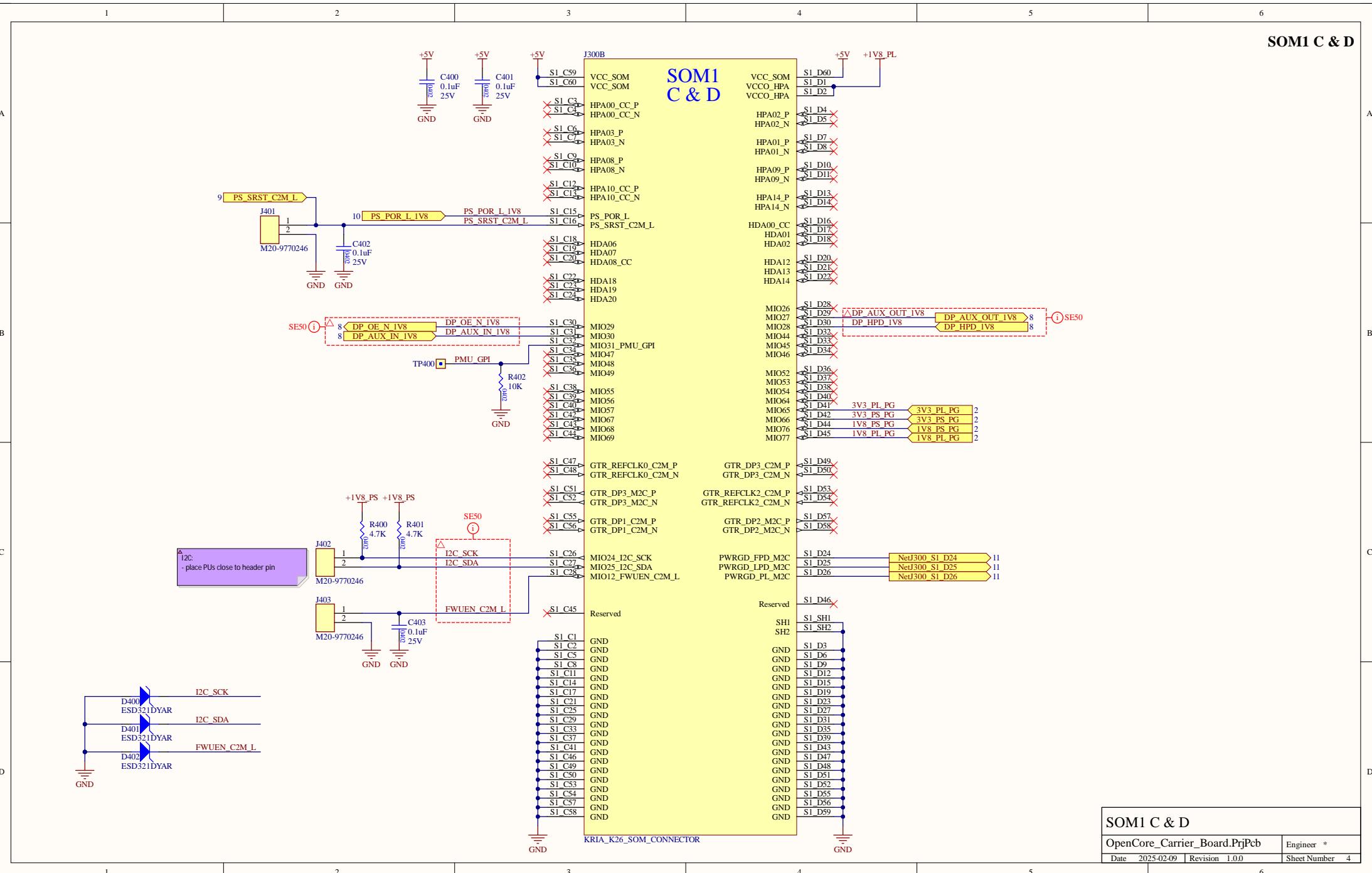


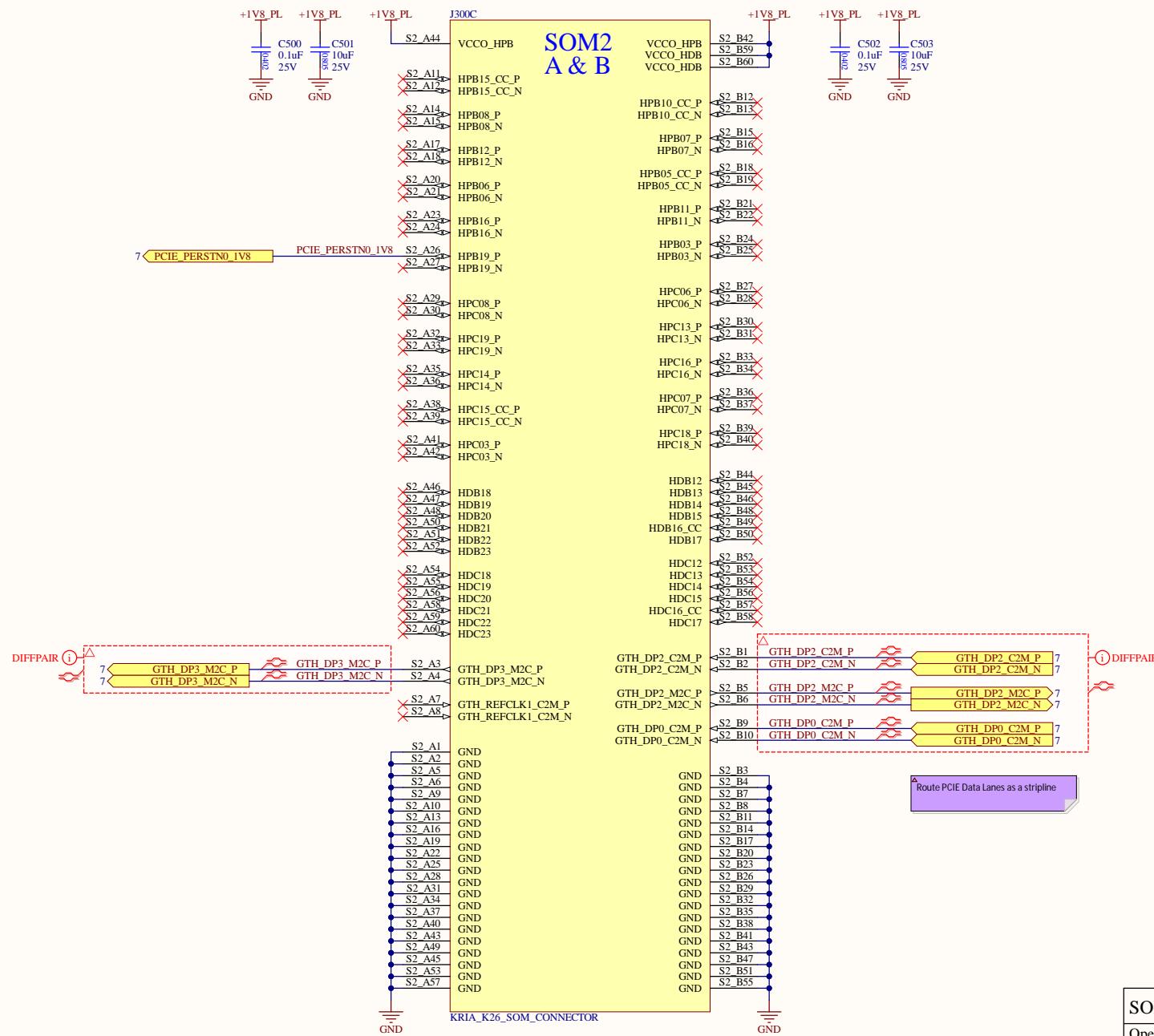
KRIA_K26_SOM_CONNECTOR

SOM1 A & B

OpenCore_Carrier_Board.PjPcb	Engineer *
Date 2025-02-09	Revision 1.00

Sheet Number 3



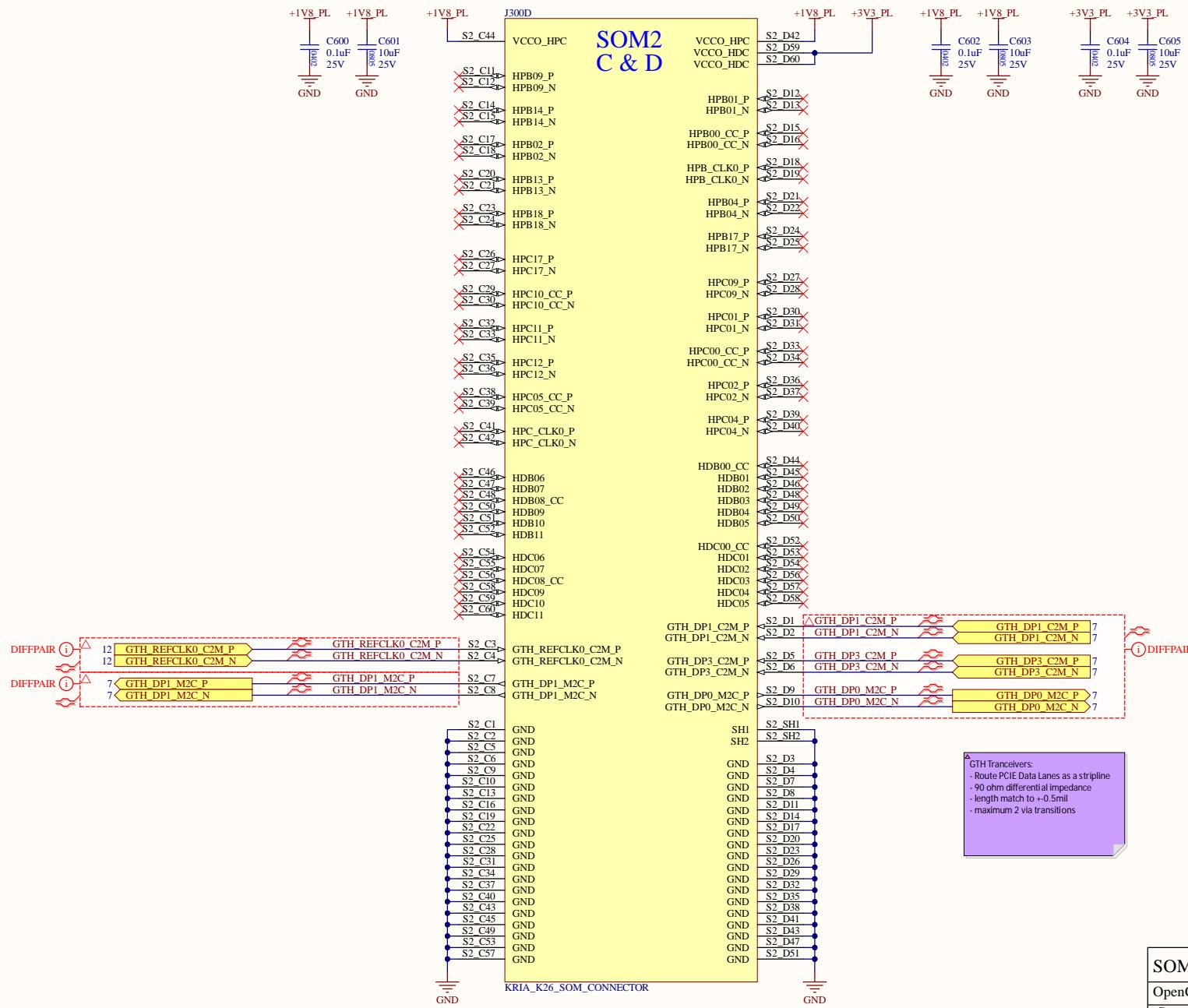
SOM2 A & B**SOM2 A & B**

OpenCore_Carrier_Board.PrjPcb	Engineer *
Date 2025-02-09	Revision 1.00

Sheet Number

5

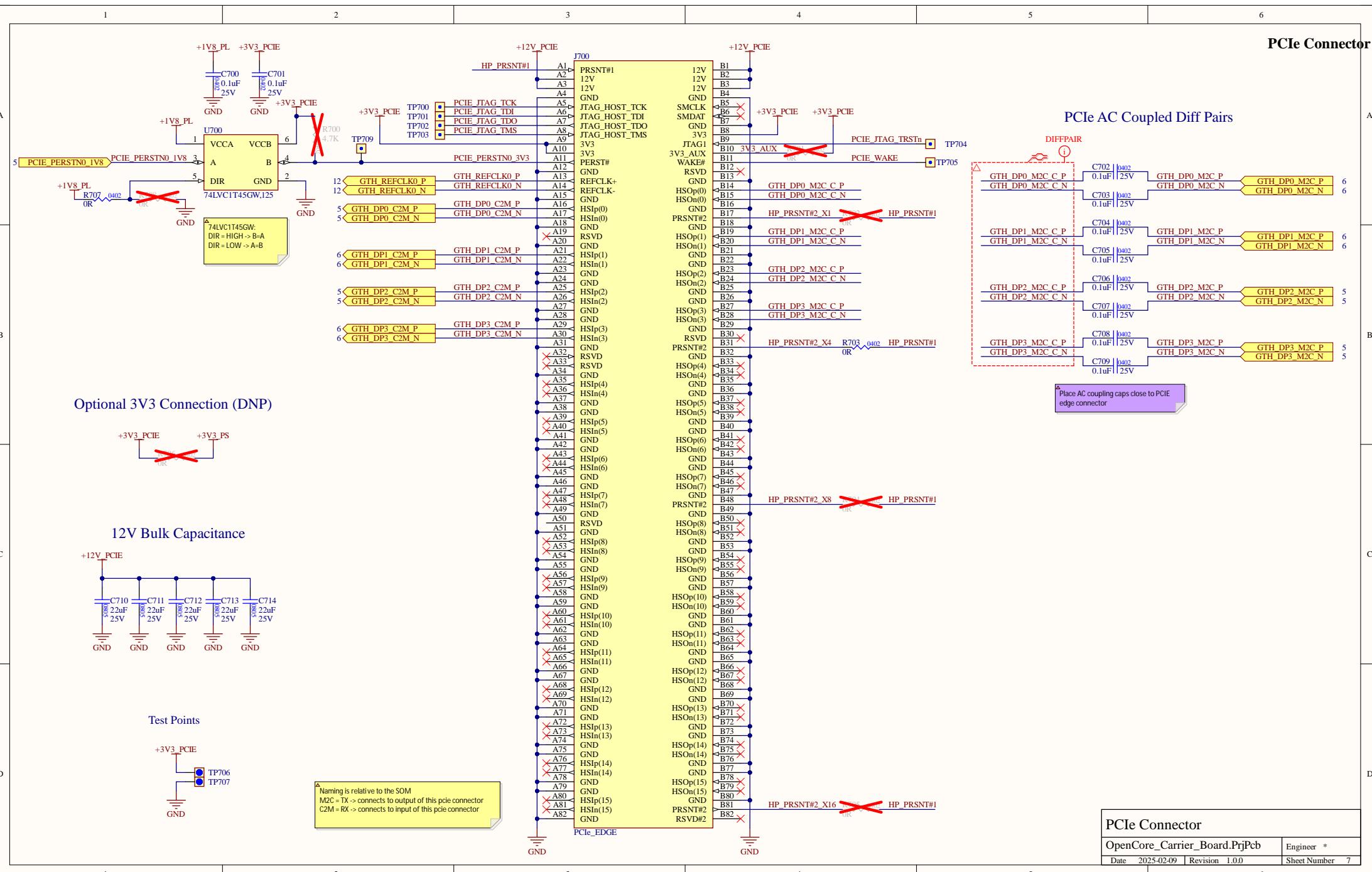
SOM2 C & D

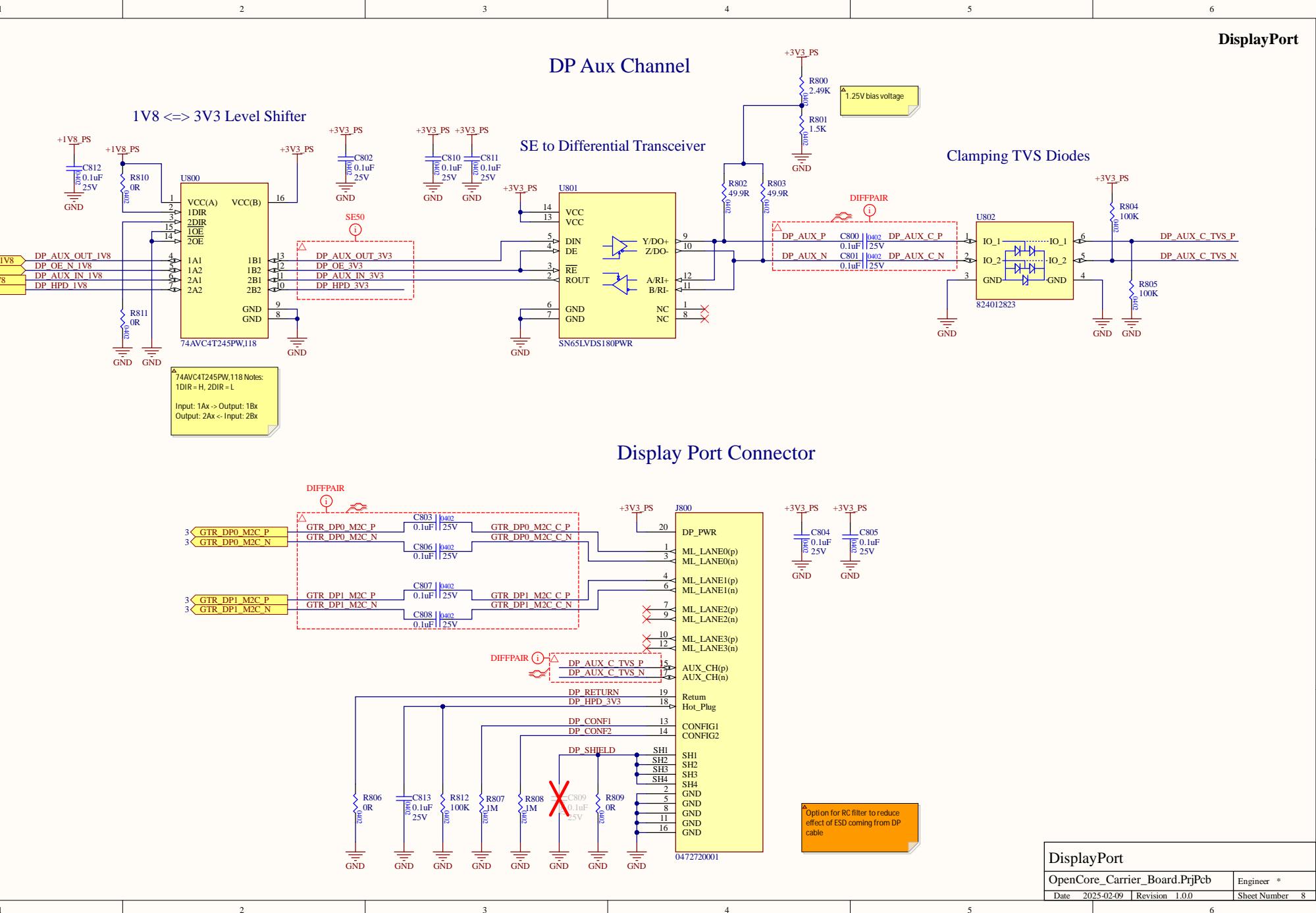


SOM2 C & D

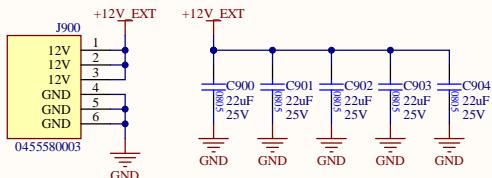
OpenCore_Carrier_Board.PrjPcb	Engineer *	
Date 2025-02-09	Revision 1.0.0	Sheet Number 6

PCIe Connector

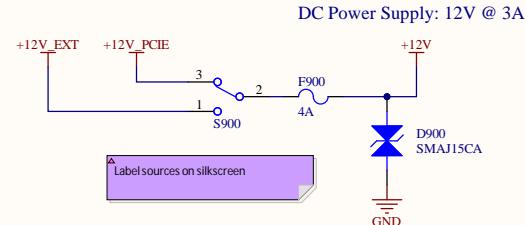




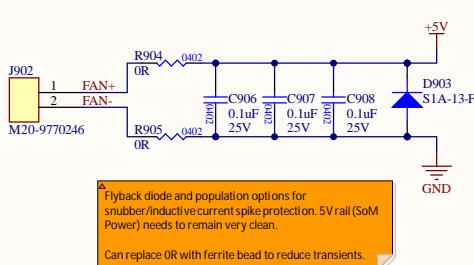
External 12V Supply



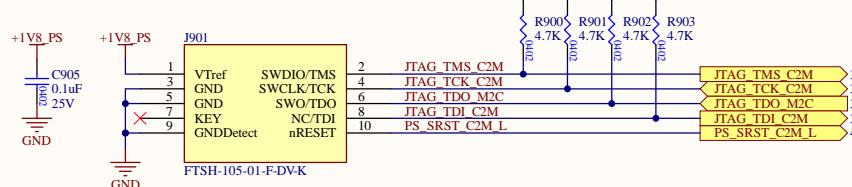
PCIE/EXT Supply Switch



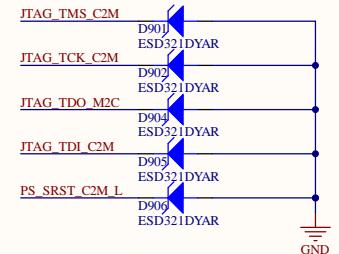
SOM Fan Header



JTAG Connector



ESD Diodes

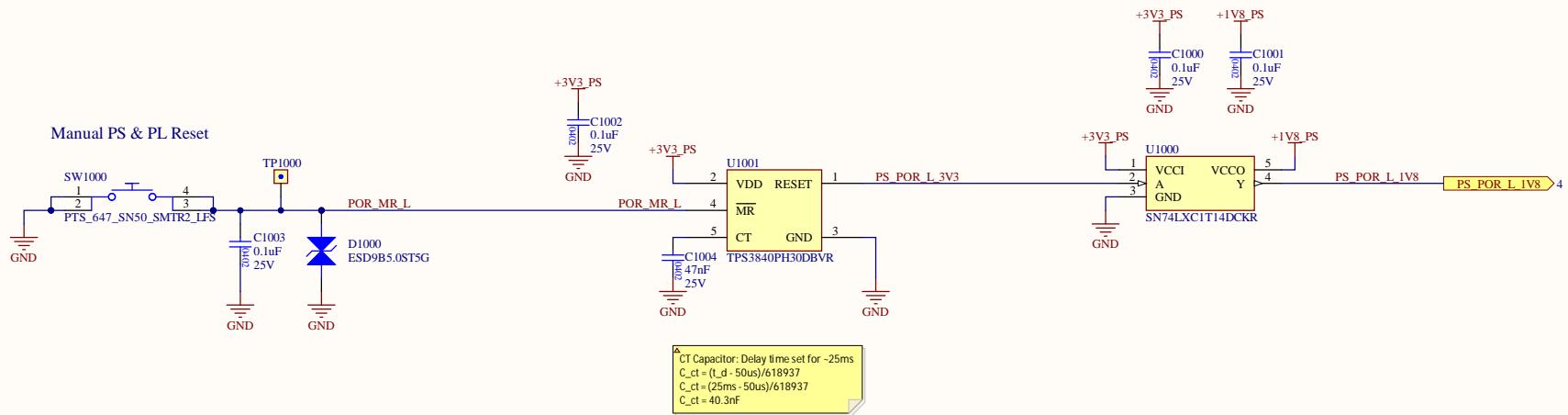


Connectors

OpenCore_Carrier_Board.PnjPcb	Engineer *
Date 2025-02-09	Revision 1.00

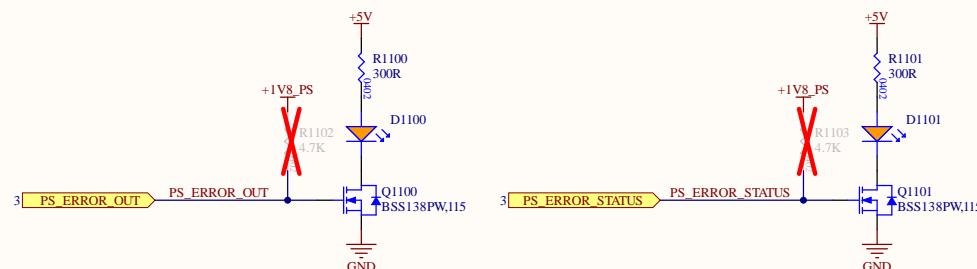
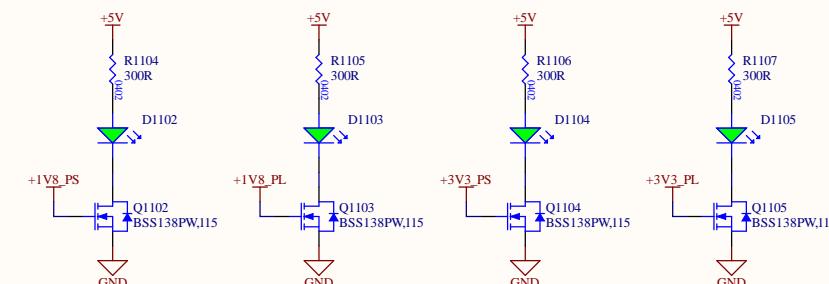
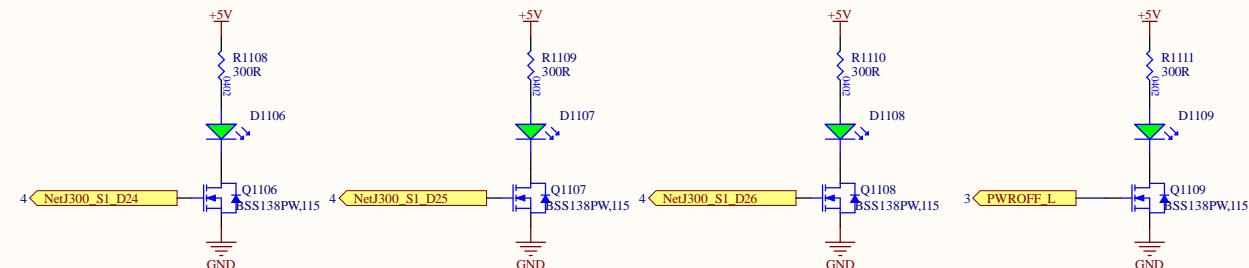
Sheet Number 9

Reset Logic



Reset Logic

OpenCore_Carrier_Board.PrjPcb	Engineer *
Date 2025-02-09	Revision 1.00 Sheet Number 10

LEDs**Error Indicators****Power Supply Indicators****Power Status****LEDs**

OpenCore_Carrier_Board.PrjPcb	Engineer *
Date 2025-02-09	Revision 1.00

2

A

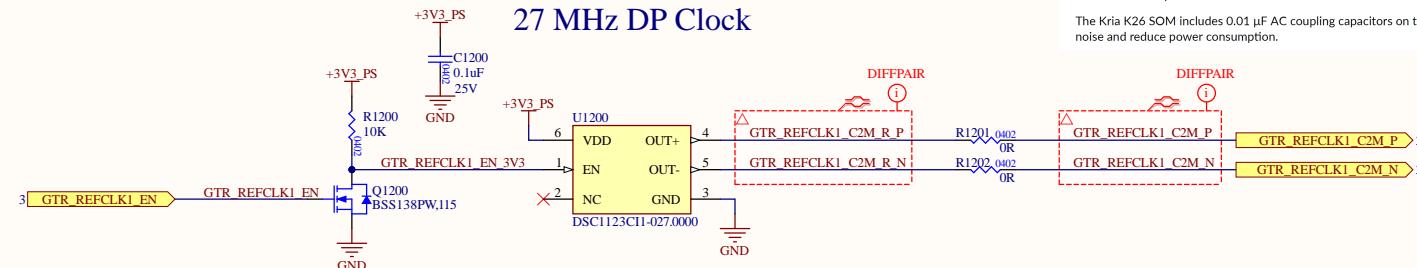
1

Transceiver Reference Clocks

Both the PS-GTR and PL-GTH transceivers differential clock signals (REFCLKs) must meet following signal integrity requirements.

- The target differential impedance of 100Ω.
 - Match P and N differential signals to within ± 0.5 mils of each other.
 - REFCLK to all other signal spacing should be five times the distance between the signal to the nearest GND plane.

The Kria K26 SOM includes 0.01 μ F AC coupling capacitors on the MGTRCLKs to minimize noise and reduce power consumption.



B

10

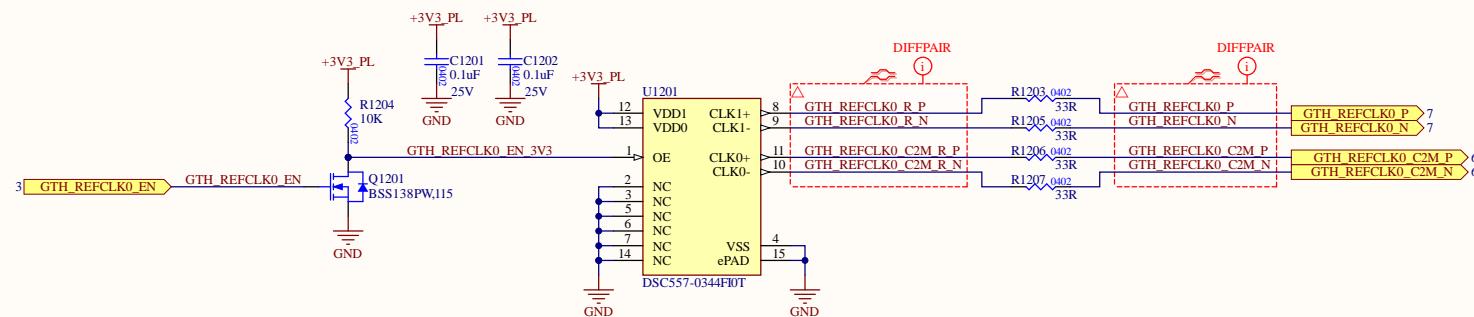
C

10

D

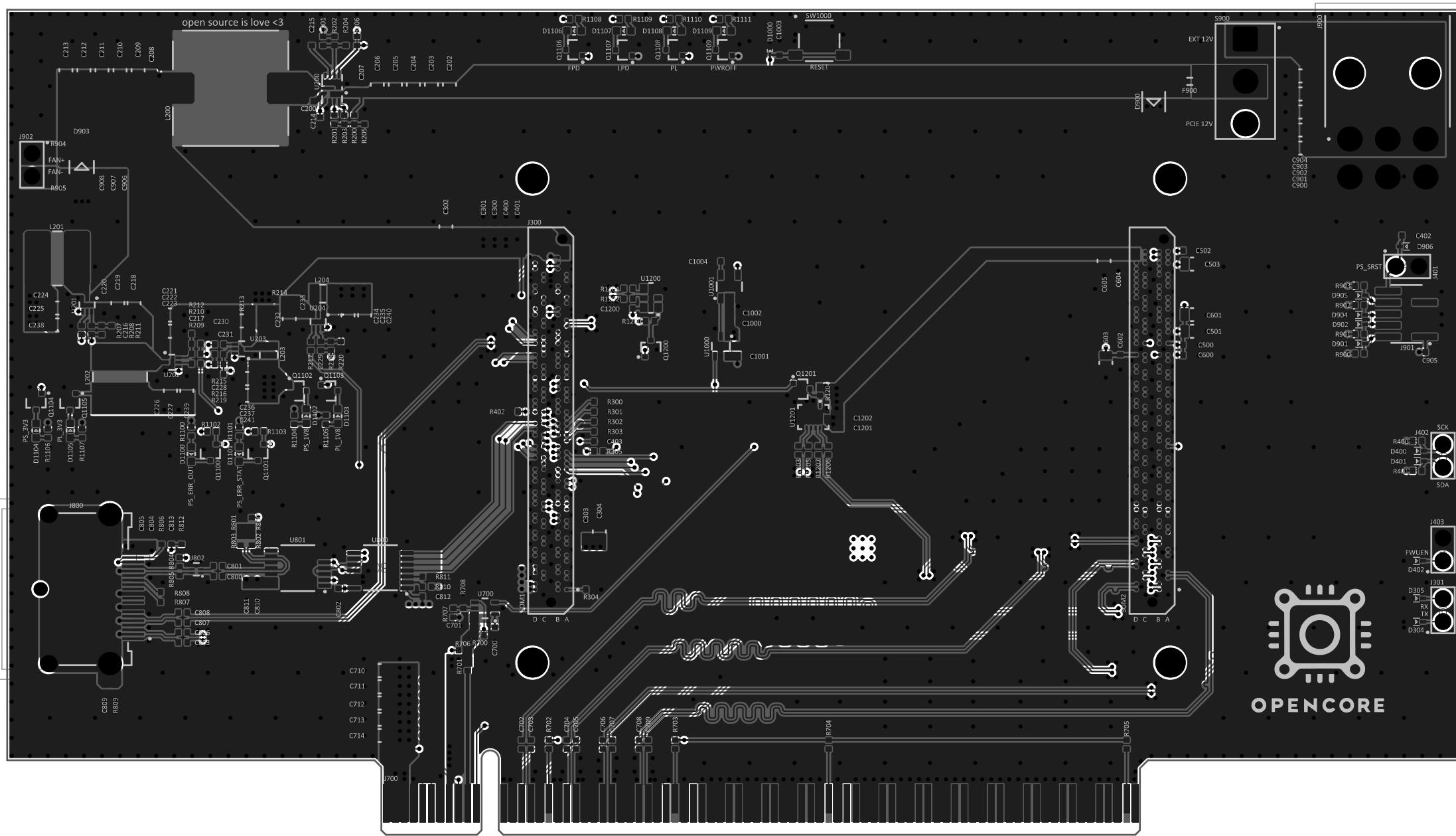
1

2x 100MHz PCIe Clock



- GND recommended on NC pins
- optional 33R termination resistor
- ePAD on device is not electrically connected

*	
OpenCore_Carrier_Board.PrjPcb	Engineer *



Board Stack Report