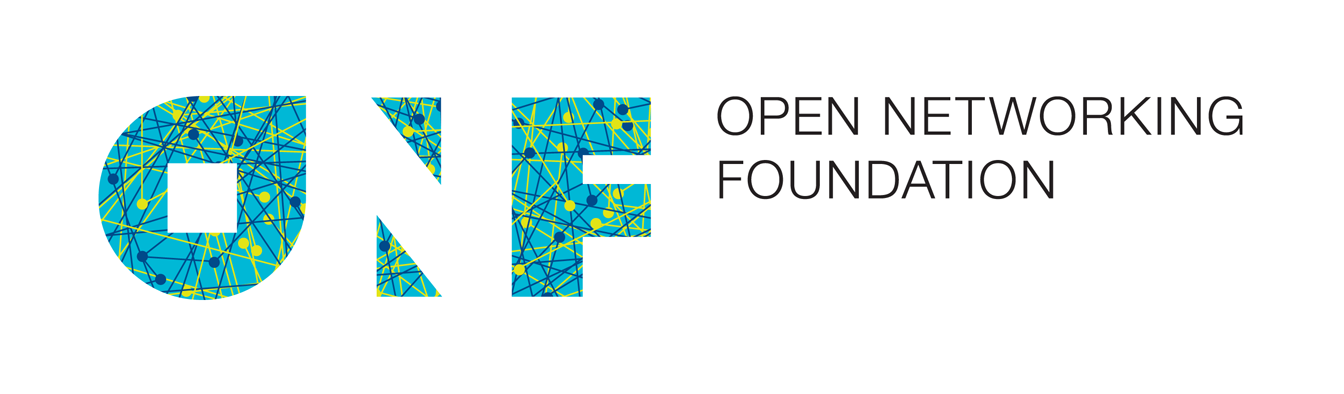
<config>  
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</config>

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Change path substrings above from “{path for output files}\” to your local path for the output files and “{path for CoreModel}\” to your local path for the Core Model. <drop/>

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Core Information Model (CoreModel)

TR-512.16

CPU and Memory

Version 1.5

December 2019

ONF Document Type: Technical Recommendation

ONF Document Name: Core Information Model version 1.5

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    - if “Update Table…” dialogue appears select “Update entire table”
  + Repeat “update fields” 2 more times (on the same large block of text)
    - if “Update Table…” dialogue appears select “Update entire table”
* Remove reviewer comment

Note that the table of contents and figures need to be updated several times as the table length changes the page numbering and the cross references will need to be re-updated.

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Document History

| **Version** | **Date** | **Description of Change** |
| --- | --- | --- |
| 1.0 |  | Initial version |
|  |  |  |
|  |  |  |
|  |  |  |

# Introduction

This document is an addendum to the TR-512\_v1.5 ONF Core Information Model and forms part of the description of the ONF-CIM. For general overview material and references to the other parts refer to [TR-512.1](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\TR-512.1_v1.3_OnfCoreIm-Overview.pdf).

## References

For a full list of references see [TR-512.1](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\TR-512.1_v1.3_OnfCoreIm-Overview.pdf).

## Definitions

For a full list of definition see [TR-512.1](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\TR-512.1_v1.3_OnfCoreIm-Overview.pdf).

## Conventions

See [TR-512.1](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\TR-512.1_v1.3_OnfCoreIm-Overview.pdf) for an explanation of:

* UML conventions
* Lifecycle Stereotypes
* Diagram symbol set

## Viewing UML diagrams

Some of the UML diagrams are very dense. To view them either zoom (sometimes to 400%) or open the associated image file (and zoom appropriately) or open the corresponding UML diagram via Papyrus (for each figure with a UML diagram the UML model diagram name is provided under the figure or within the figure).

## Understanding the figures

Figures showing fragments of the model using standard UML symbols and also figures illustrating application of the model are provided throughout this document. Many of the application-oriented figures also provide UML class diagrams for the corresponding model fragments (see [TR-512.1](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\TR-512.1_v1.3_OnfCoreIm-Overview.pdf) for diagram symbol sets). All UML diagrams depict a subset of the relationships between the classes, such as inheritance (i.e. specialization), association relationships (such as aggregation and composition), and conditional features or capabilities. Some UML diagrams also show further details of the individual classes, such as their attributes and the data types used by the attributes.

# Introduction to CPU and Memory

A data dictionary that sets out the details of all classes, data types and attributes is also provided ([TR-512.DD](file:///C:\Users\ndavis\git\ONFInfoModel\OnfModel\CoreGendoc\ModelDescriptions\TR-512.DD_v1.3_OnfCoreIm-DataDictionary.pdf)).

Note that this model excludes CPU and Memory physical inventory, which is covered by the existing Equipment model.

## Overview

CPU and Memory are two parts of the compute model (Storage is the third and is covered in a separate document).

With current compute architectures, CPU and storage are closely tied together, often via a CPU bus and memory bus).

This model is designed to represent compute architectures in a technology independent manner for management of those compute resources.

## Existing open standards

There doesn’t appear to be a single comprehensive model that could be adopted.

The DMTF CIM and SNIA Swordfish / DMTF Redfish has some related classes and OpenConfig has CPU and memory in system / openconfig-system.yang .

## CPU

The original CPUs consisted of many physical units ( <http://www.megaprocessor.com/index.html> ).

They then were implemented in a single chip ( <https://spectrum.ieee.org/tech-history/silicon-revolution/chip-hall-of-fame-intel-4004-microprocessor> ).

Now a single chip (socket) may contain many CPU cores, and a core may run more than one thread. So we need to be clear what our definition of a ‘logical CPU’ is.

If a CPU is symmetric (all cores the same specification) then use one physical entry per CPU.

If a CPU is asymmetric, then use one physical entry per group of similar CPU cores

For example an asymmetric CPU may have 4 + 4 cores ( 4 \* 1.8 GHz Type-A + 1.4 GHz Type-B) and hence 2 entries , each of 4 cores would be used

Note that CPU chip(s) may be FRU or non FRU inventory – here we are interested in the processor function.

## Memory

Memory chip(s) / SIMM DIMM modules may be FRU or non FRU inventory – here we are interested in the memory capabilities and capacity.

## Pooling

Note that the decision was made to have a single compute pool rather than separate Storage, CPU and memory pools[[1]](#footnote-1), because :

* CPU and memory are usually tightly coupled (vie the CPU and memory buses) and the pool can then allocate these consistently
* *Sometimes* storage is tightly coupled with CPU and memory and the pool can then allocate these consistently (local attached un-sharable storage)

Note also that the pools aren’t hierarchical (deliberately no ComputePool contained in self-join)

* The association StorageExtentPoolEntryIsLogical allows an output from one pool to become the input of another pool
* This needs to form a directed acyclic graph (no loops)

Note that there is no association linking the pool inputs and outputs. The ordering of the inputs allows the input to output extent mapping to be determined.

Assume that there will be a large number of simple pools rather than few large complex pools with complex mappings.

## Partitioning and Aggregation

The partitioning and aggregation of CPU and memory is subtly different from that of Storage.

With Storage, in theory each extent can be considered separately. Some extents could come from a disk A, some from disk B. With a sensible pool allocation there is no need to worry about segmenting the pool.

With CPU and storage we have 2 issues :

1. The pool needs to remember and enforce segmentation (resource chunks)
2. The pool needs to pair CPU and Memory segments

For example if there are 2 blade servers Blade-A and Blade-B.

* I can’t allocate a software process CPU from Blade-A and memory Blade-B.
* I can’t give a software thread half its CPU requirements from Blade-A and half from Blade-B.
* I can’t give a software thread half its memory requirements from Blade-A and half from Blade-B.

A multi-threaded application may be able to run across multiple CPU/memory pairs but it would have to know the segmentation.

This model will use the following :

* Class ComputePoolSegment is defined to allow the definition of ‘segments’
* Inputs to the pool can be optionally assigned to a segment
* Each pool input and output also has an optional segmentId UUID
* If an input entry has a segmentId, than no output can be assigned that ‘crosses’ the segment (Each output can only relate to 1 segmentId)
* Multiple inputs can only be combined if both have no segmentId or if both have the same segmentId
* If an input entry has a segmentId, then it should be propagated to any outputs (fill out the output segmentId with the input segmentId)
* If a CPU output has a segmentId then it can only be used with memory with the same segmentId (and visa-versa)
* Each segment should have its own internal number range in the pool

## Items for Further Investigation

What units should we use for memory sizes – bytes, kiB, MiB … ?

What units should we use for CPU - Hz, kHz, MHz … ?

* Note that Kubernetes works in units of CPU, where   
  “One CPU, in Kubernetes, is equivalent to a *Hyperthread* on a bare-metal Intel processor with Hyperthreading”
* A CPU hardware thread is also called a vCPU (virtual CPU)

Note that we should try and avoid using floating point numbers for the quantities as the rounding proves problematic

# CPU and Memory model detail

ComputePool – a pool that manages ComputePoolEntries. These entries can consist of Storage, Memory and CPU resources. This document only considers CPU and memory entries.

ComputePoolEntry – An abstract class used as the parent of Storage, Memory and CPU pool entries. Note that this class is subclassed by input and output variants – clarifying the role each entry plays and also allowing the inputs and outputs to be separately ordered.

ComputePoolInputEntry – An abstract class used as the parent of Storage, Memory and CPU pool input entries.

ComputePoolOutputEntry – An abstract class used as the parent of Storage, Memory and CPU pool output entries.

ComputePoolSegment – allows for instance CPU and Memory that need to be kept together to be grouped

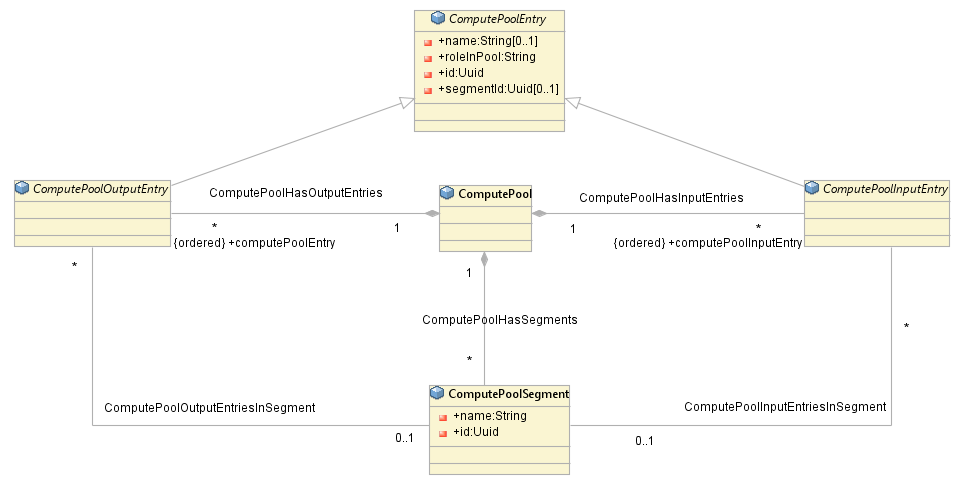


Figure 1 – Compute Pool

## CPU

CpuPoolPhysicalEntry – a ComputePoolInputEntry for a CPU. It contains attributes specific to the CPU implementation and can be related to the Equipment providing the CPU.

CpuPoolLogicalEntry – a ComputePoolInputEntry for CPU capacity and capability from another ComputePool

CpuCoreAllocation – the output from a ComputePool. This output can be allocated to another ComputePool where it could be further manipulated.

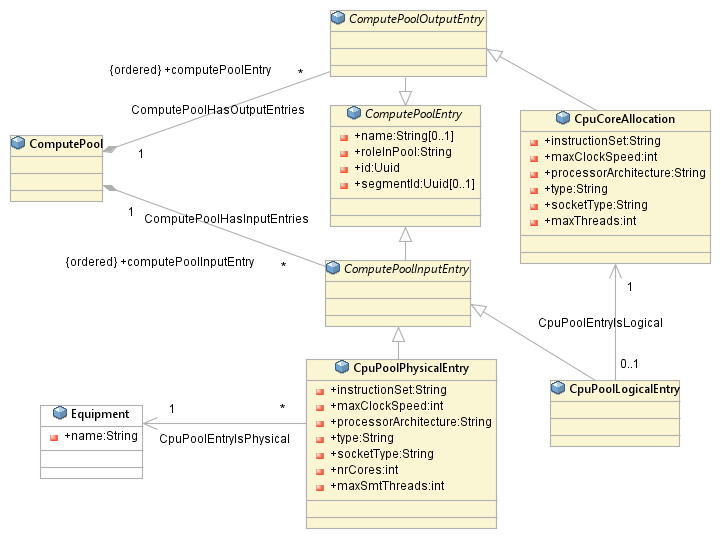


Figure 2 – CPU model

## Memory

MemoryPoolPhysicalEntry – a ComputePoolInputEntry for memory. It contains attributes specific to the memory implementation and can be related to the Equipment providing the memory.

MemoryPoolLogicalEntry – a ComputePoolInputEntry for memory capacity and capability from another ComputePool

MemoryBlockAllocation - – the output from a ComputePool. This output can be allocated to another ComputePool where it could be further manipulated.

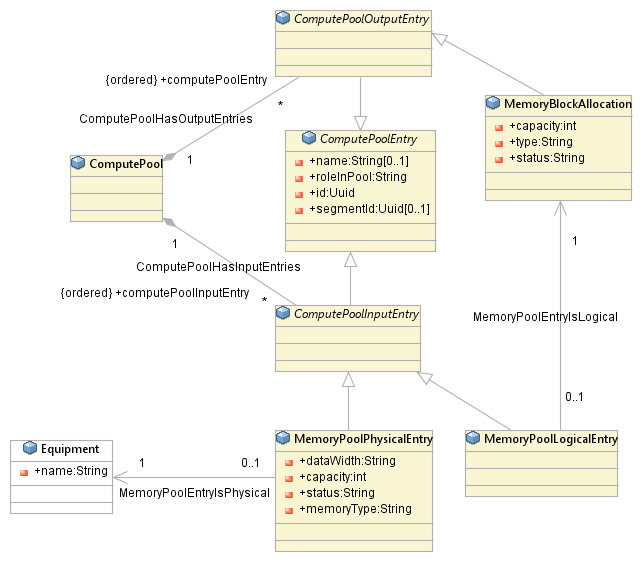


Figure 3 – Memory model

## Relationship to Running Software

It may also be of interest to show the consumption of CPU and Memory capacity by running software (which is what CPU and memory is provided for).

The Software model is covered in TR-512.12.



Figure 4 - Running software use of CPU and Memory

## Examples

### A simple compute example

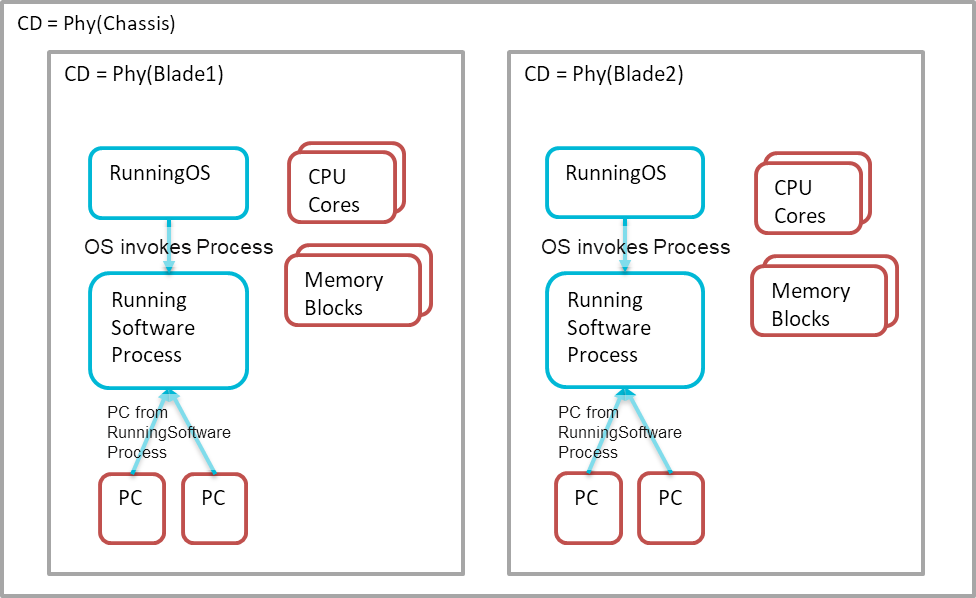


Figure 5 - Simple Compute example

This simple example shows how the concepts in the model fit together.

There is traceability from the physical equipment instances to the CPU and Memory functionality and from there to the running software that is using the functionality.

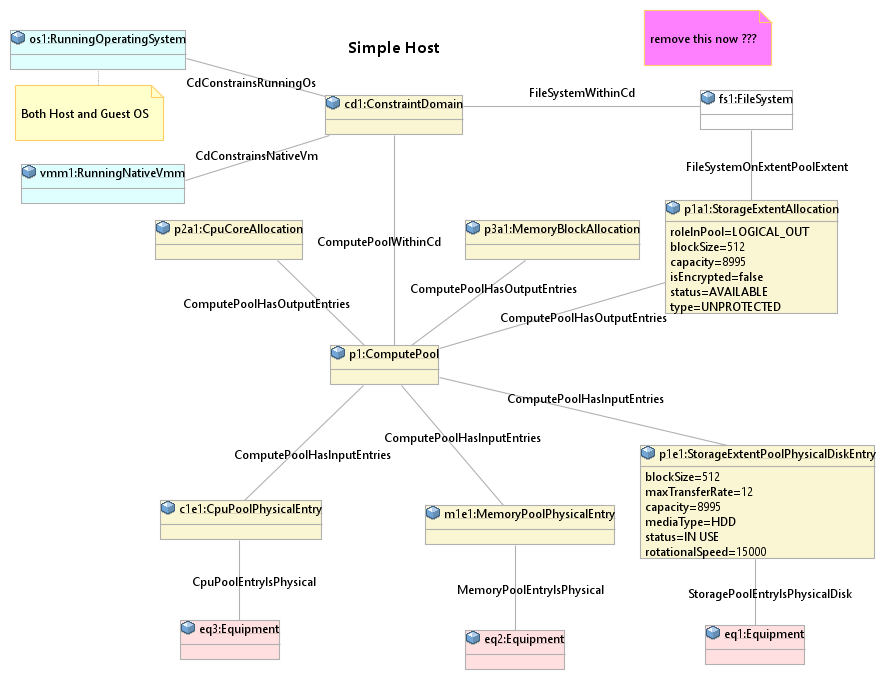


Figure 6 - Compute example instance diagram

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* insert a line in “Normal” style<drop/>
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  + TR-512.GT\_v1.3\_OnfCoreIm-CommonGendocTemplate-Fragments.docx <drop/>

Template version 0.0.10 17 September 2017 <drop/>

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<arg name=’packageName’ type=’String’/><drop/>  
[if (not cl.qualifiedName.contains(packageName))]<drop/>  
[else] <drop/>  
[if(cl.name.contains(className))]<drop/>

Qualified Name: [cl.qualifiedName/]

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<dropEmpty>[cleanAndFormat(co.\_body.clean())/]</dropEmpty>

[/for]<drop/>  
[if (cl.isAbstract)]<drop/>

This class is abstract.

[/if]<drop/>

[if (cl.oclAsType(uml::Class).general ->notEmpty())]<drop/>

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[for (gen:Class | cl.oclAsType(uml::Class).general)]<drop/>

* [gen.name/]

[/for]<drop/>

[/if]<drop/>

[for (st:Stereotype | cl.getAppliedStereotypes())]<drop/>  
[if(not st.name.contains(‘OpenModelClass’))]<drop/>

This class is [st.name/].

[else] <drop/>  
[/if]<drop/>  
[/for]<drop/>  
[else] <drop/>  
[/if]  
[/if]  
</fragment><drop/>

# Fragment: Insert standard diagram <drop/>

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<arg name=’p’ type=’uml::Package’/><drop/>  
<arg name=’diagramName’ type=’String’/><drop/>  
<arg name=’diagramTitle’ type=’String’/><drop/>

[for (d:Diagram|p.getPapyrusDiagrams())]<drop/>

[if d.name.contains(diagramName)]

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CoreModel diagram: [d.name/]

Figure 5-1 [diagramTitle/]

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CoreModel diagram: [d.name/]

Figure 6-1 [diagramTitle/]

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[/for]<drop/>  
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[if(not st.name.contains(‘Obsolete’))]

| [p.name/] | [for (st:Stereotype | p.getAppliedStereotypes())]<drop/>  [if(not st.name.contains(‘OpenModelAttribute’))] [st.name/]  [/if]<drop/>  [/for]<drop/>  Do NOT remove the previous line as word throws an error if the cell is empty <drop/> | [if p.ownedComment->notEmpty()]<drop/>  [for (c:Comment | p.ownedComment)] <drop/>  [cleanAndFormat(c.\_body.clean())/]  [/for]  [else] [if (p.name.contains (‘\_’))]See referenced class  [else]To be provided  [/if]<drop/>  [/if]<drop/>  Do NOT remove the previous line as word throws an error if the cell is empty <drop/> |
| --- | --- | --- |

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[/if]<drop/>

[/for]<drop/>  
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# Fragment: Insert attribute row brief <drop/>

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# Fragment: Start attribute table brief <drop/>

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<arg name=’cl’ type=’uml::Class’/><drop/>

|  |  |  |
| --- | --- | --- |
| **Attribute Name** | **Lifecycle Stereotype (empty = Mature)** | **Description** |

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# Fragment: Insert Attribute table brief <drop/>

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[if cl.ownedAttribute->notEmpty()]<drop/>

Table 1: Attributes for [cl.name/]

<table><drop/>

[cl.insertAttributeTableHeader ()/]

[for (p:Property|cl.ownedAttribute)]<drop/>

[if (not p.name.contains(‘\_’))]<drop/>

[p.insertAttributeRowBrief ()/]

[/if]<drop/>

[/for]<drop/>

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<arg name=’p3’ type=‘String’/><drop/>  
<arg name=’p4’ type=‘String’/><drop/>  
<arg name=’p5’ type=‘String’/><drop/>  
<arg name=’p6’ type=‘String’/><drop/>  
<arg name=’p7’ type=‘String’/><drop/>  
<arg name=’p8’ type=‘String’/><drop/>  
<arg name=’p9’ type=‘String’/><drop/>  
<arg name=’p10’ type=‘String’/><drop/>  
[if cl.ownedAttribute->notEmpty()]<drop/>

Table 1: Attributes for [cl.name/]

<table><drop/>

[cl.insertAttributeTableHeader ()/]

[for (p:Property|cl.ownedAttribute)]<drop/>

[if (p.name.contains(p1) or p.name.contains(p2) or p.name.contains(p3) or p.name.contains(p4) or p.name.contains(p5) or p.name.contains(p6) or p.name.contains(p7) or p.name.contains(p8) or p.name.contains(p9) or p.name.contains(p10))]<drop/>

[if (not p.name.contains(‘\_’))]<drop/>

[p.insertAttributeRowBrief ()/]

[/if]<drop/>

[/if]<drop/>

[if (p.name.contains(p1) or p.name.contains(p2) or p.name.contains(p3) or p.name.contains(p4) or p.name.contains(p5) or p.name.contains(p6) or p.name.contains(p7) or p.name.contains(p8) or p.name.contains(p9) or p.name.contains(p10))]<drop/>

[if (p.name.contains(‘\_’))]<drop/>

[p.insertAttributeRowBrief ()/]

[/if]<drop/>

[/if]<drop/>

[/for]<drop/>

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[/if]<drop/>

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# Fragment: Insert DataType <drop/>

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Qualified Name: [dt.qualifiedName/]

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[/for]<drop/>  
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Inherits properties from:

[for (tp:DataType | dt.oclAsType(uml::DataType).general)]<drop/>

* [tp.name/]

[/for]<drop/>

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* [gen.name/]

[/for]<drop/>

[/if]<drop/>

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|  |  |  |
| --- | --- | --- |
| **Attribute Name** | **Lifecycle Stereotype (empty = Mature)** | **Description** |

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# Fragment: Insert Data Type Attribute table brief <drop/>

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[/for]<drop/>

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[/if]<drop/>

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Qualified Name: [dt.qualifiedName/]

[for (co:Comment | dt.ownedComment)]<drop/>

<dropEmpty>[cleanAndFormat(co.\_body.clean())/]</dropEmpty>

[/for]<drop/>

Applied stereotypes:

[if dt.getAppliedStereotypes()->notEmpty()] <drop/>

[for (st:Stereotype | dt.getAppliedStereotypes())]<drop/>

* [st.name/]

[/for]<drop/>

[else] No stereotypes applied

[/if]<drop/>

[if (dt.oclAsType(uml::DataType).general ->notEmpty())]<drop/>

Inherits literals from:

[for (tp:DataType | dt.oclAsType(uml::DataType).general)]<drop/>

* [tp.name/]

[/for]

[/if]<drop/>

[if (dt.oclAsType(Enumeration).ownedLiteral->notEmpty())]<drop/>

Contains Enumeration Literals:

[for (e:EnumerationLiteral|dt.oclAsType(Enumeration).ownedLiteral)]<drop/>

* [e.name/]:
  + [for (co:Comment | e.ownedComment)]<drop/>
  + <dropEmpty>[cleanAndFormat(co.\_body.clean())/]
  + </dropEmpty>[/for]<drop/>
  + [if dt.getAppliedStereotypes()->notEmpty()] <drop/>
  + Applied stereotypes:
    - [for (st:Stereotype | e.getAppliedStereotypes())]<drop/>
    - [st.name/]
    - [/for]<drop/>
  + [/if]<drop/>

[/for]<drop/>

[/if]<drop/>

</fragment><drop/>

1. Note that this document only considers CPU and memory entries. [↑](#footnote-ref-1)