



LEO Development Board for Jz4740

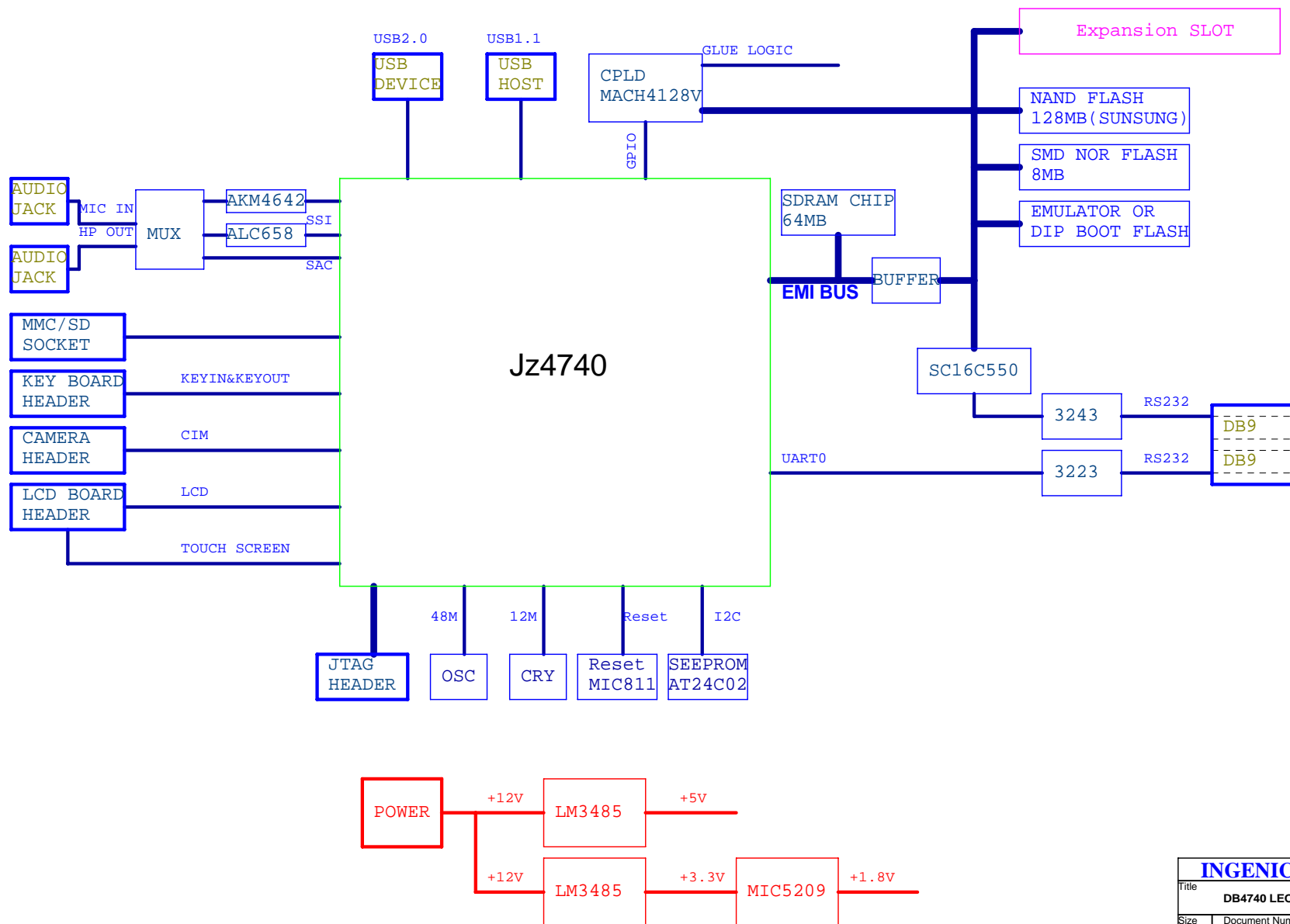
Schematic Revision 1.0

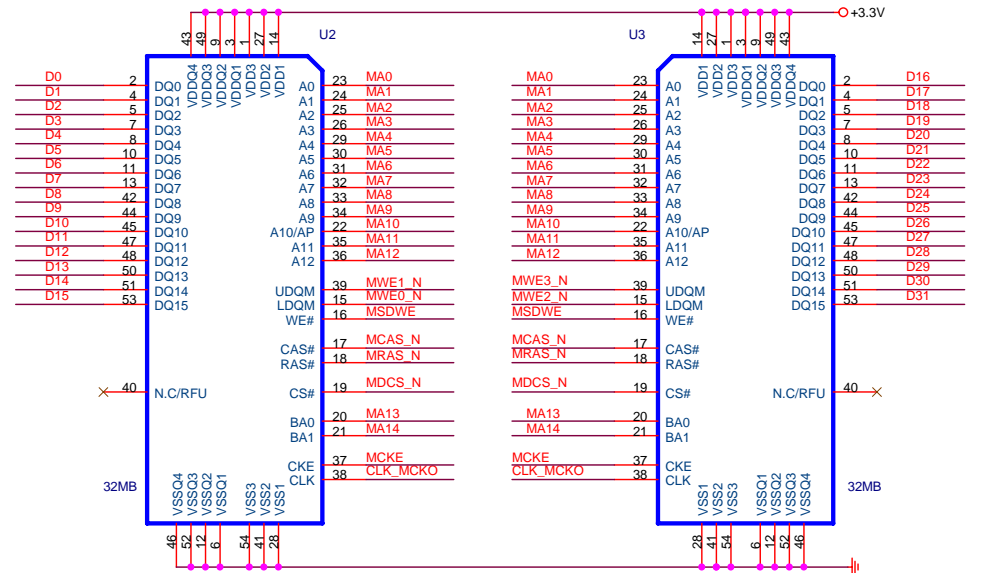
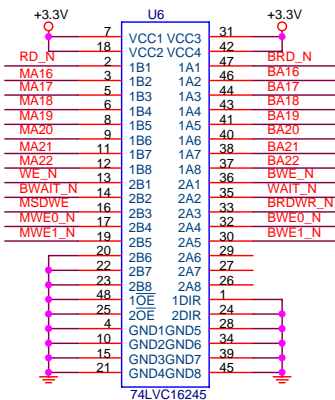
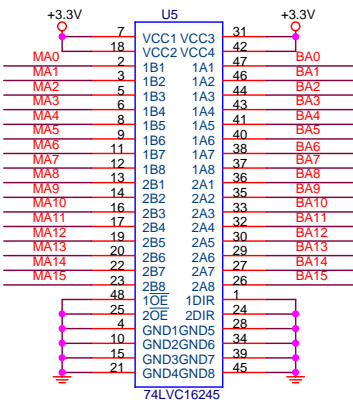
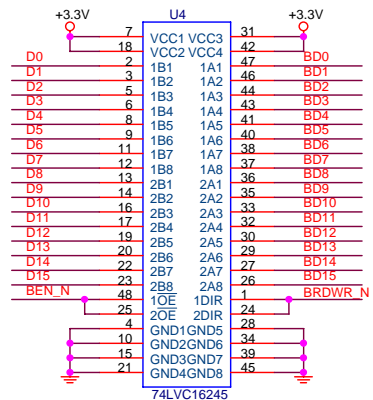
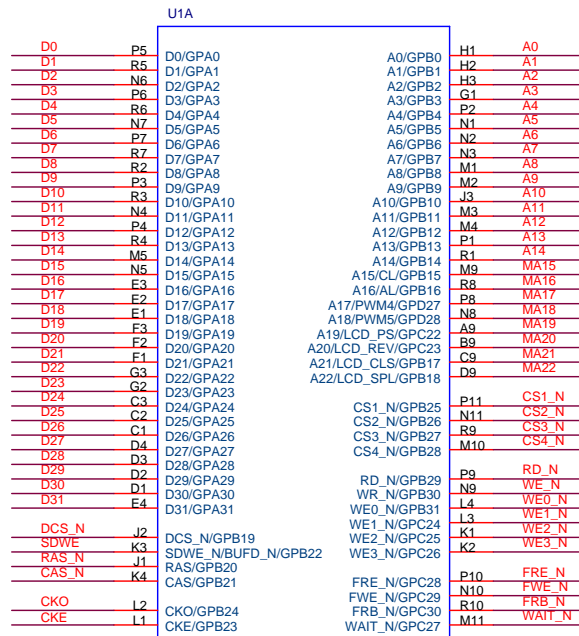
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LEO

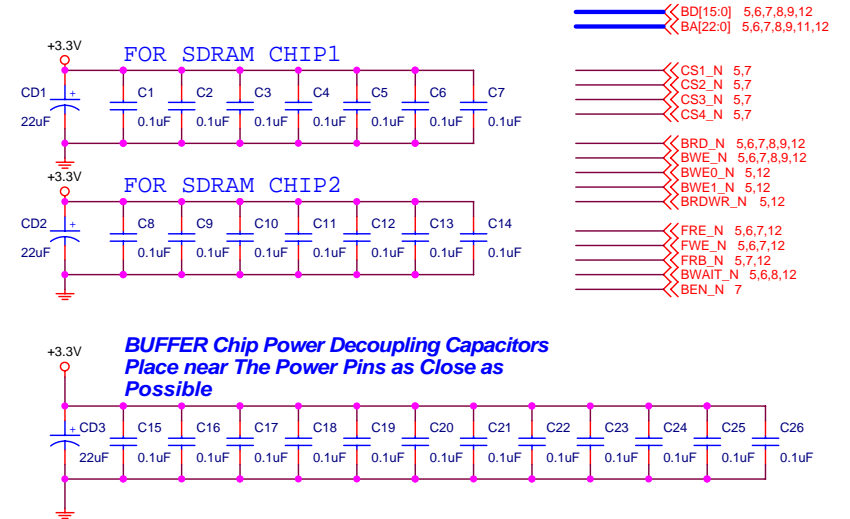
INGENIC Semiconductor Corporation
System Technology Department
Release Data: 2007.3.1

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DUAL 256M bit SDRAM



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	Jz4740_EMI&SDRAM&Buffers	1.0	
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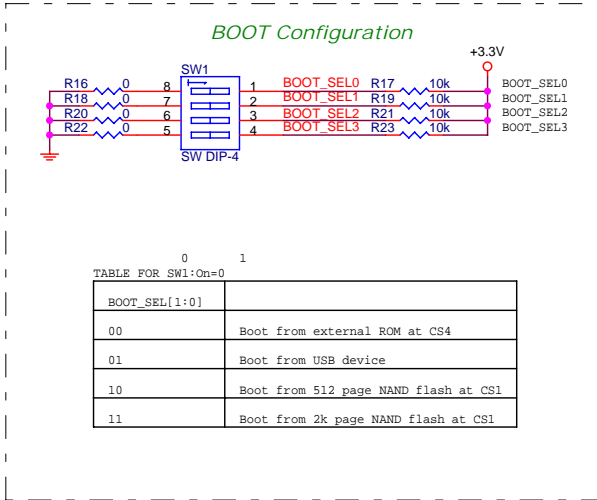
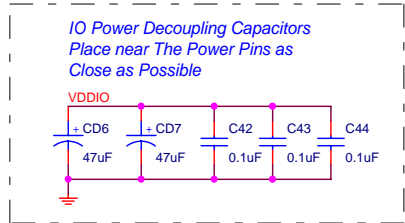
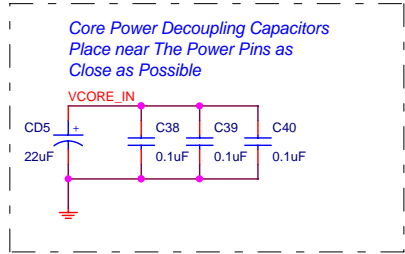
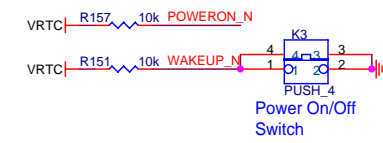
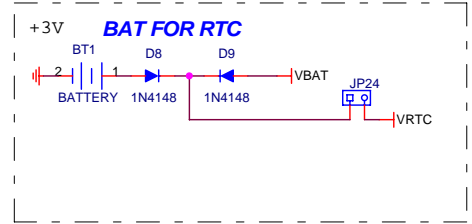
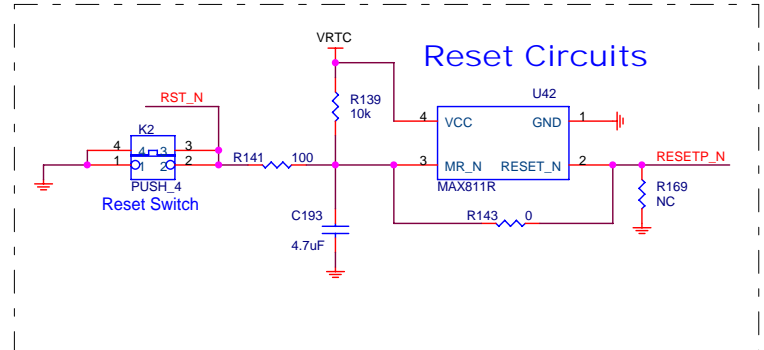
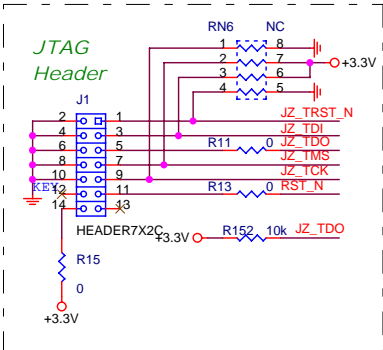
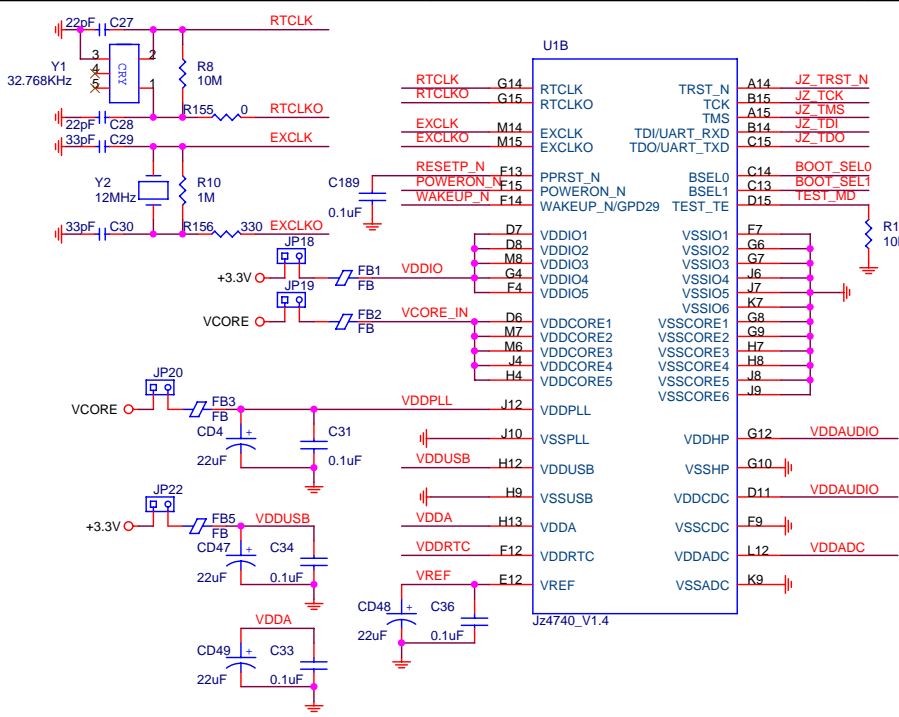
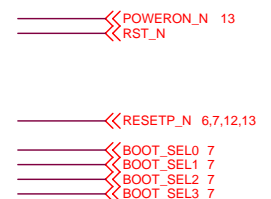
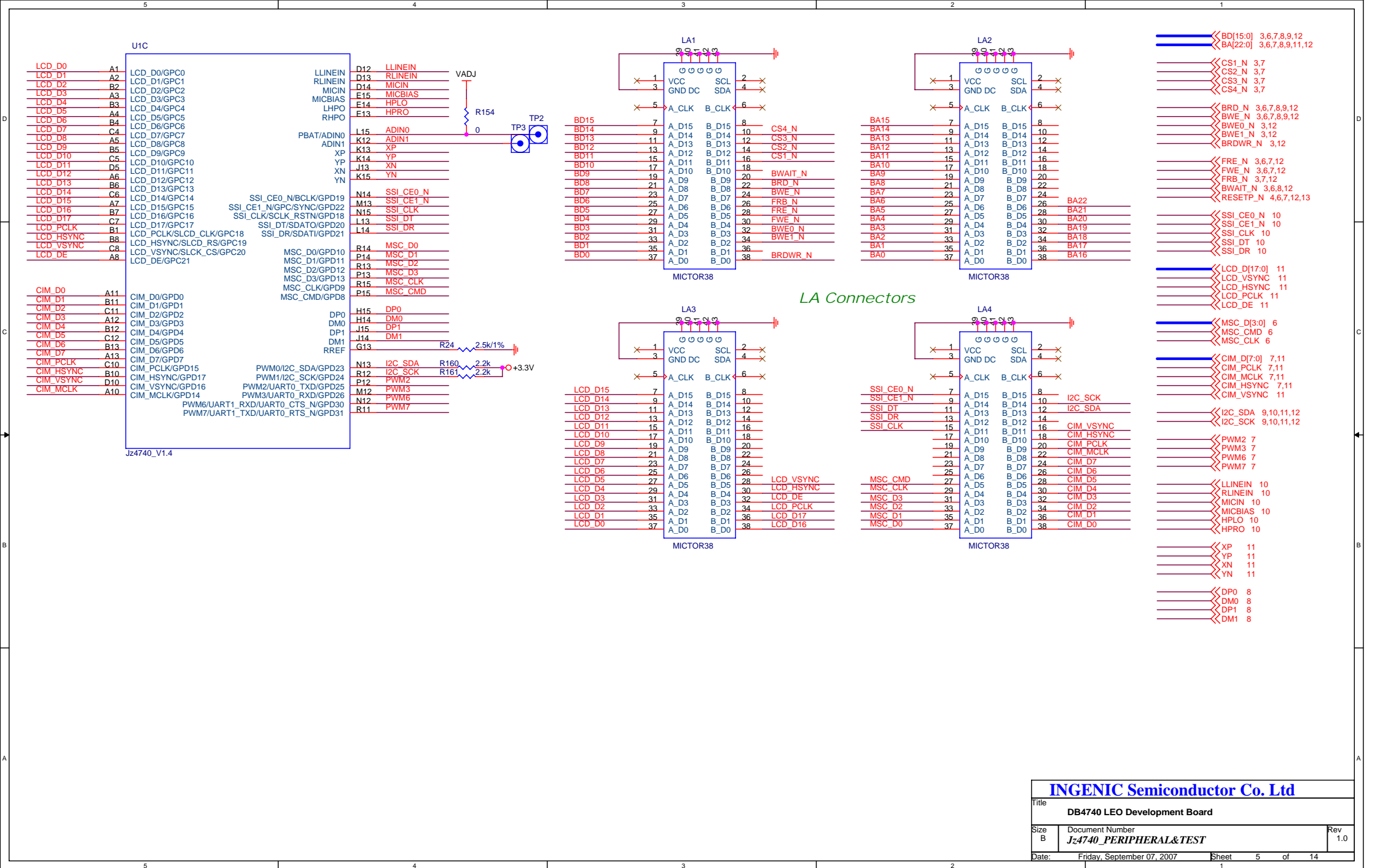


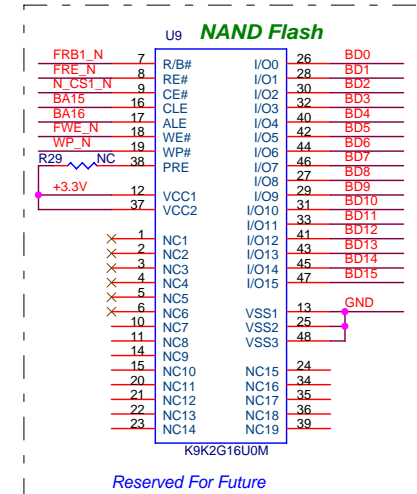
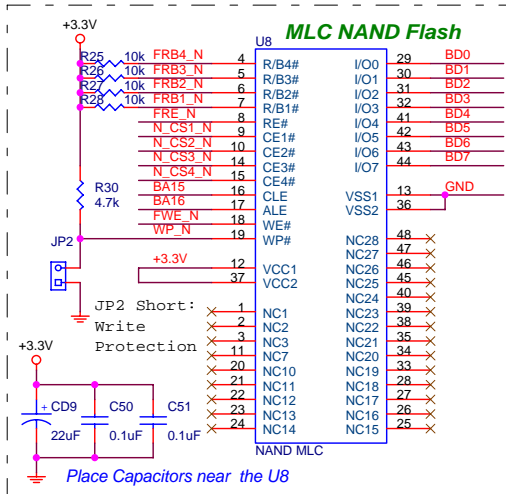
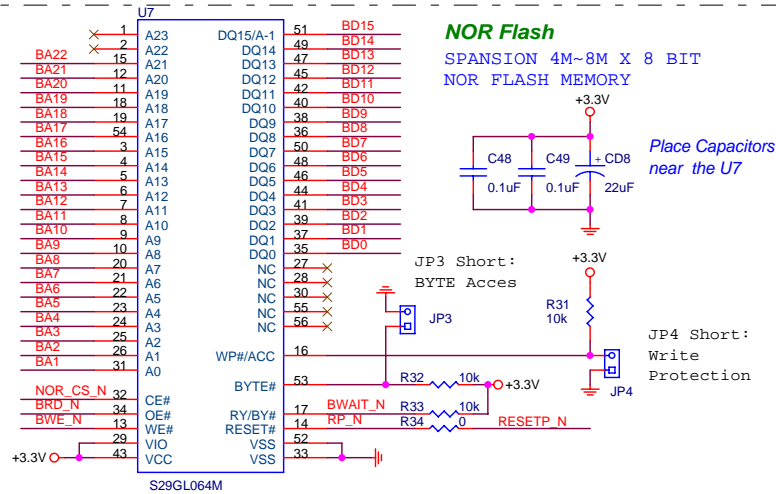
TABLE FOR SW1:On=0	
BOOT_SEL[1:0]	
00	Boot from external ROM at CS4
01	Boot from USB device
10	Boot from 512 page NAND flash at CS1
11	Boot from 2k page NAND flash at CS1



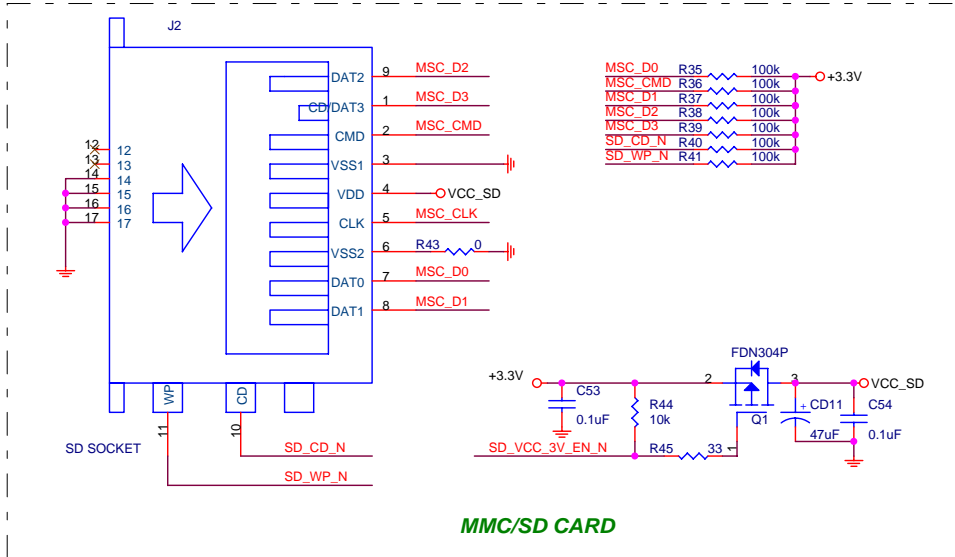
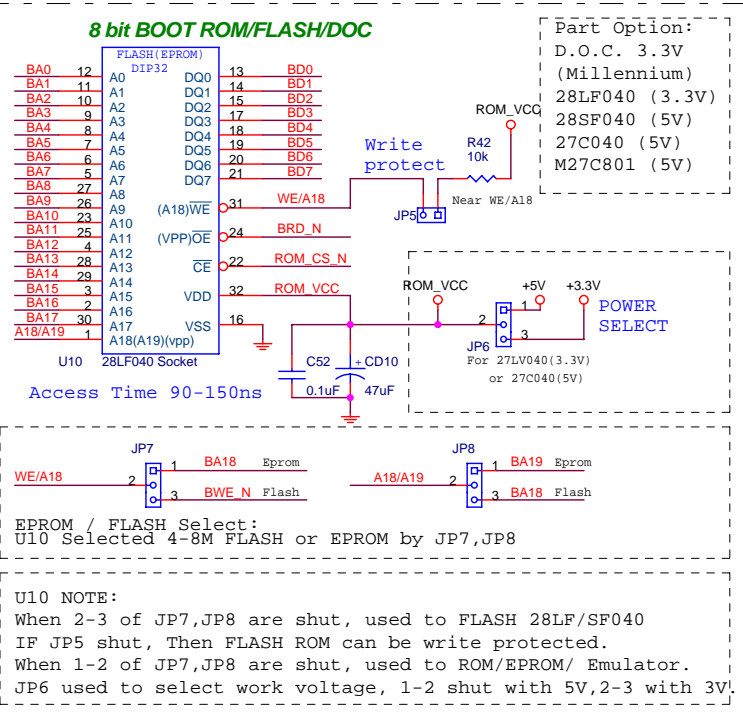


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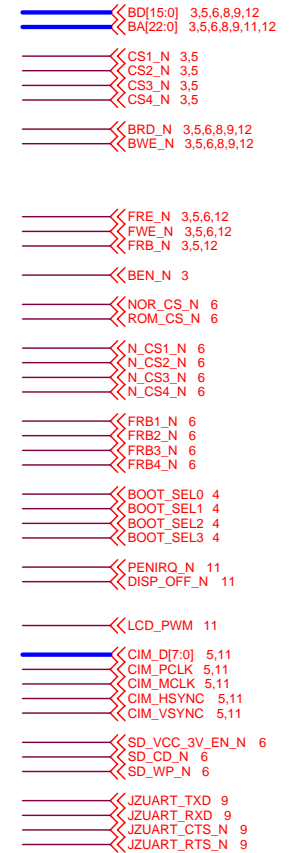
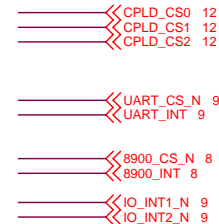
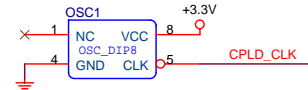
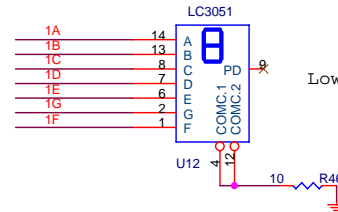
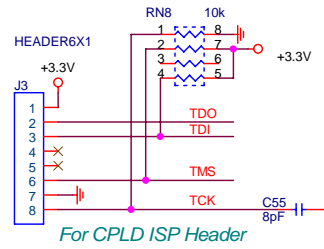
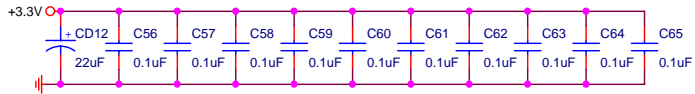
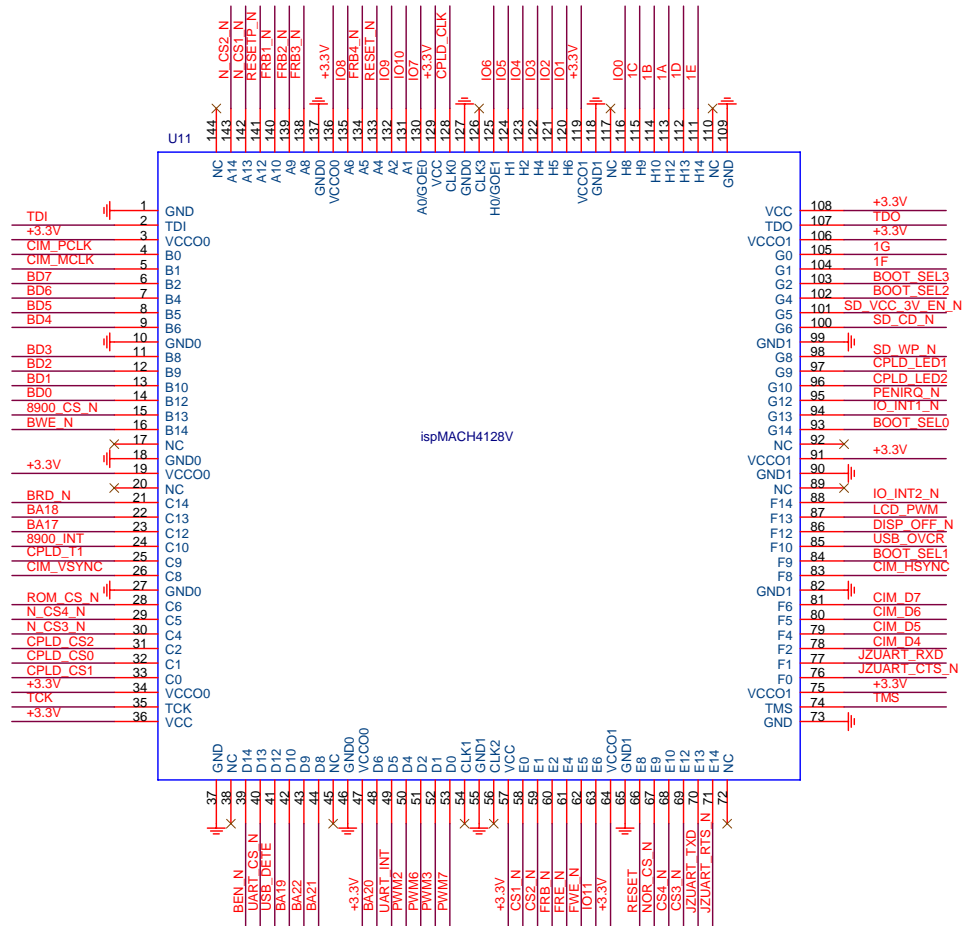


NOR_CS_N 7
ROM_CS_N 7
N_CS1_N 7
N_CS2_N 7
N_CS3_N 7
N_CS4_N 7

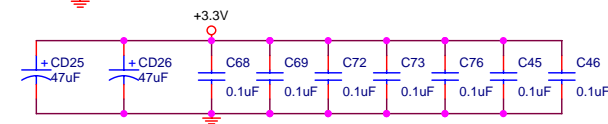
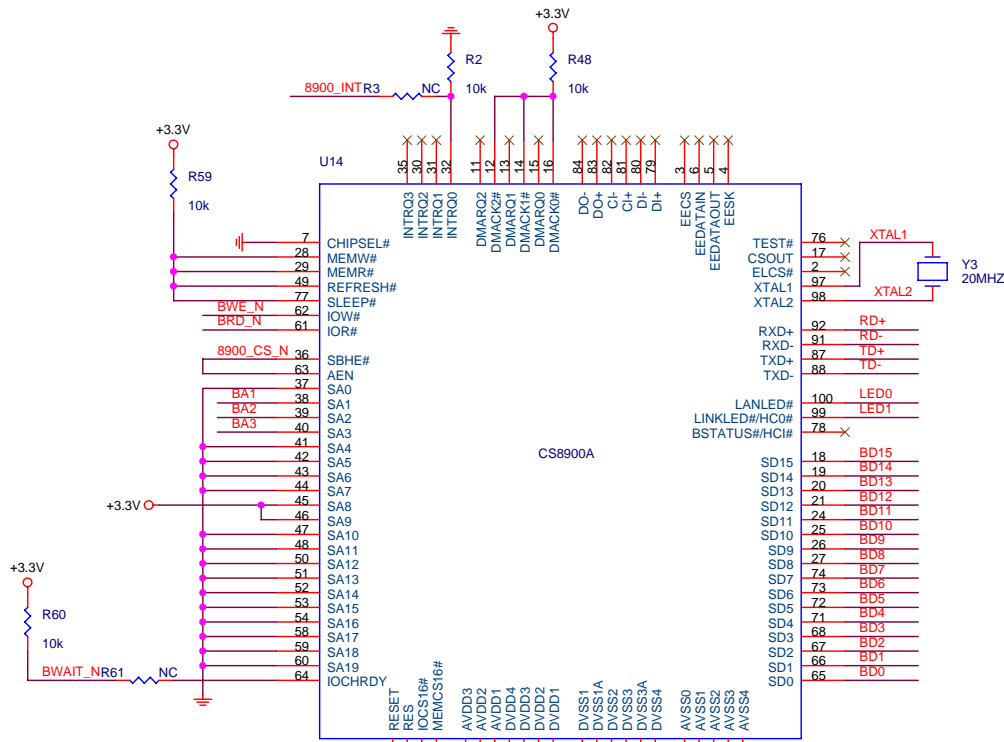


FRB1_N 7
FRB2_N 7
FRB3_N 7
FRB4_N 7
BRDWR_N 3,5,12
FRE_N 3,5,7,12
FWE_N 3,5,7,12
RESETP_N 4,7,12,13
BA[22:0] 3,5,7,8,9,11,12
BD[15:0] 3,5,7,8,9,12
BRD_N 3,5,7,8,9,12
BWE_N 3,5,7,8,9,12
BWAIT_N 3,5,8,12
MSC_D[3:0] 5
MSC_CMD 5
MSC_CLK 5
SD_VCC_3V_EN_N
SD_CD_N
SD_WP_N

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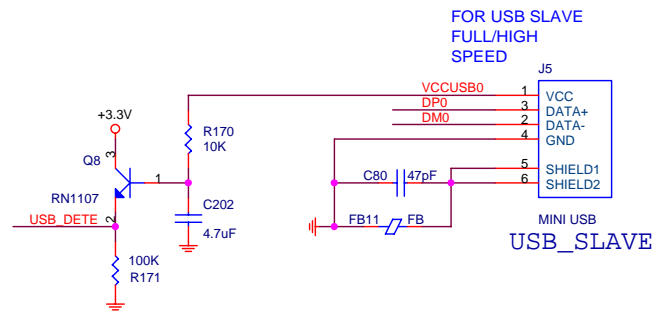
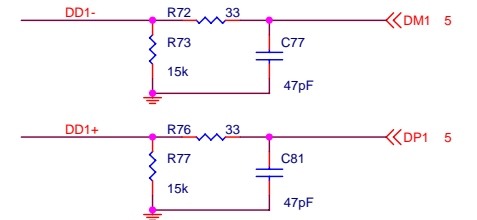
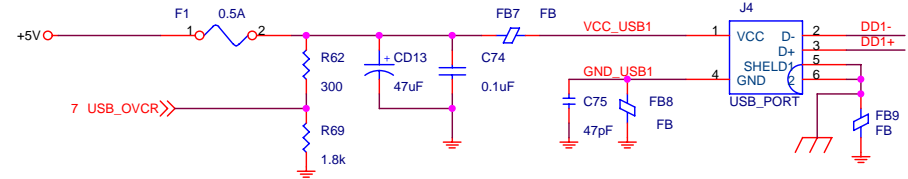
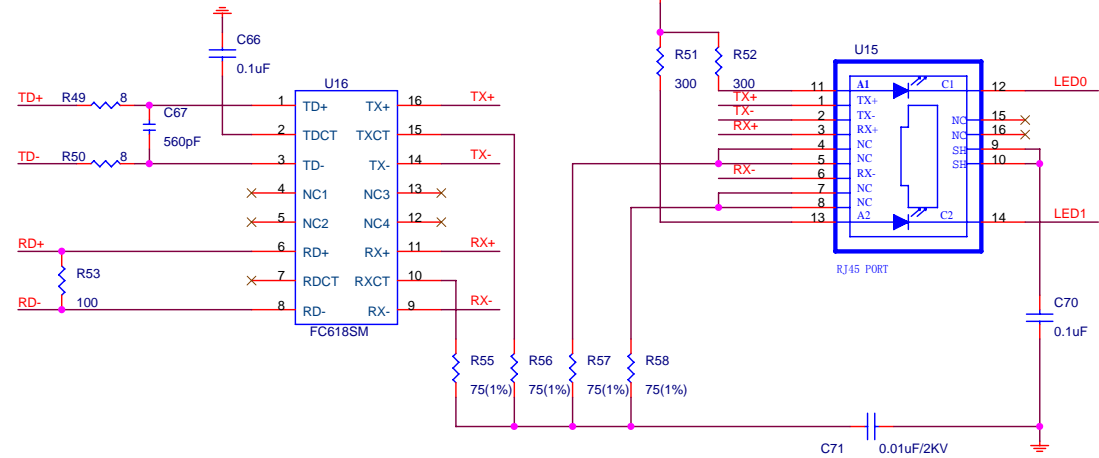


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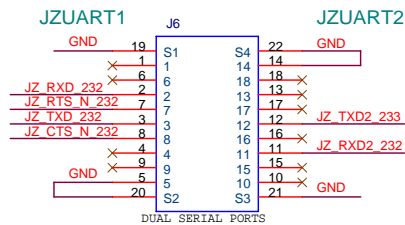
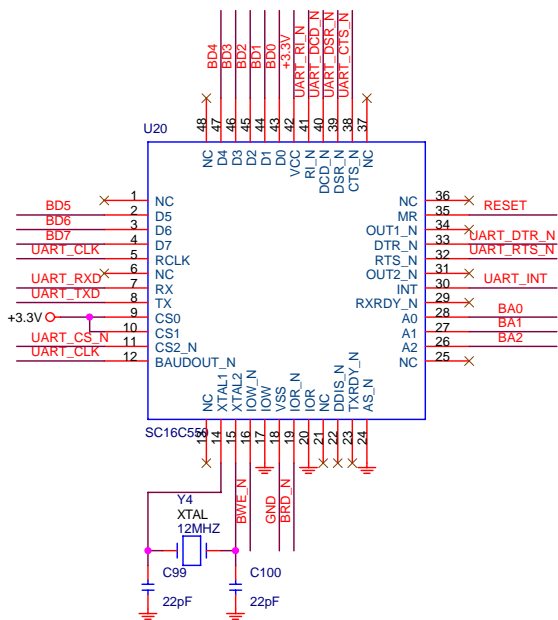


BD[15:0] 3,5,6,7,9,12
 BA[22:0] 3,5,6,7,9,11,12
 BWAIT_N 3,5,6,12
 RESET 7,9,11,12

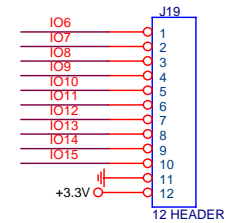
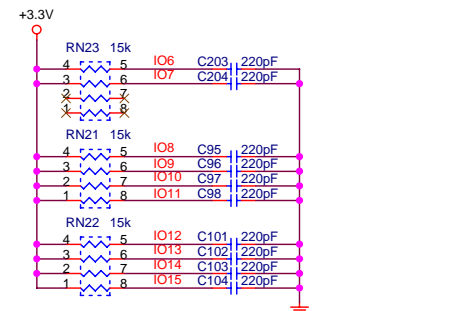
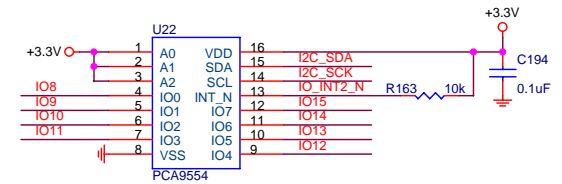
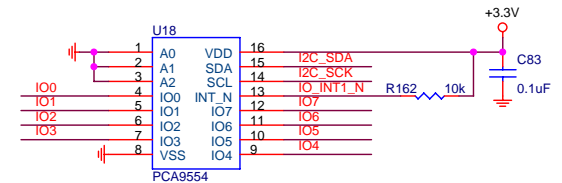
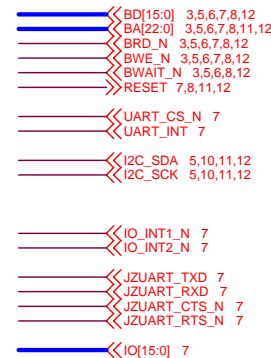
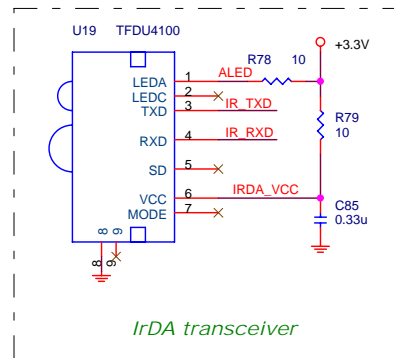
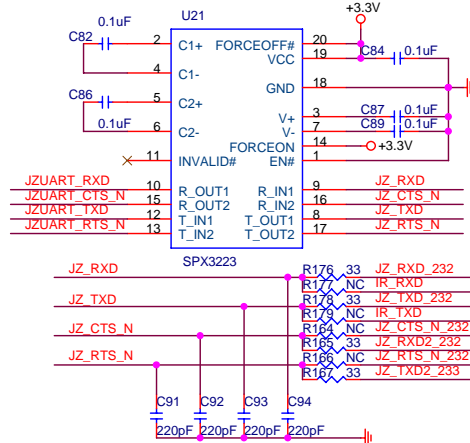
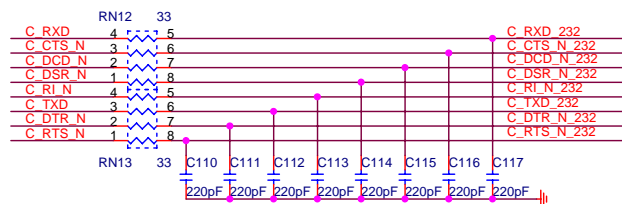
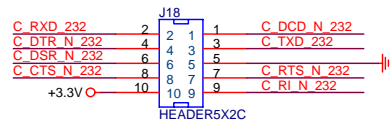
BRD_N 3,5,6,7,9,12
 BWE_N 3,5,6,7,9,12
 8900_CS_N 7
 8900_INT 7



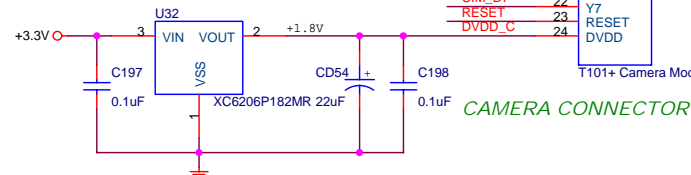
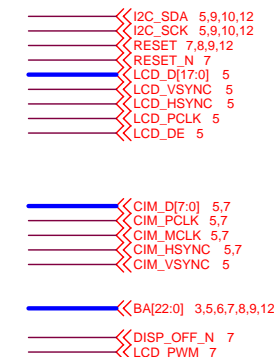
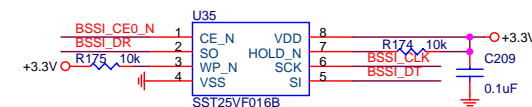
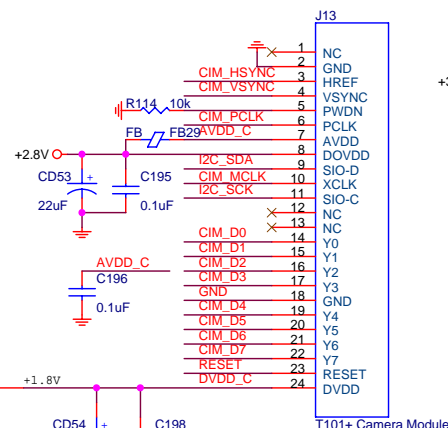
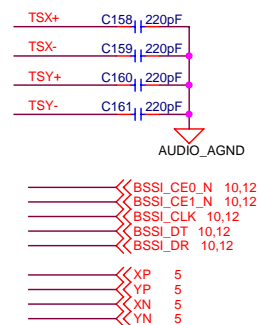
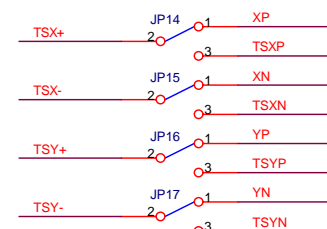
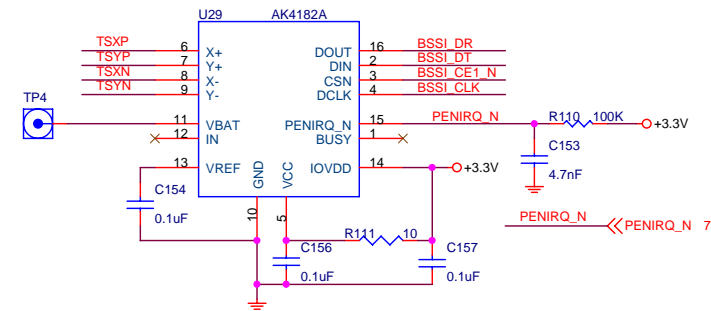
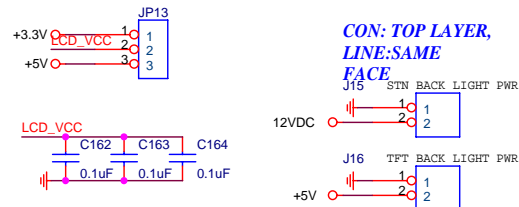
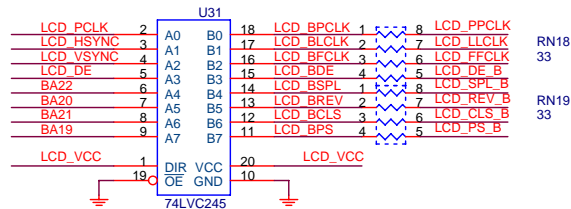
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EXT_UART



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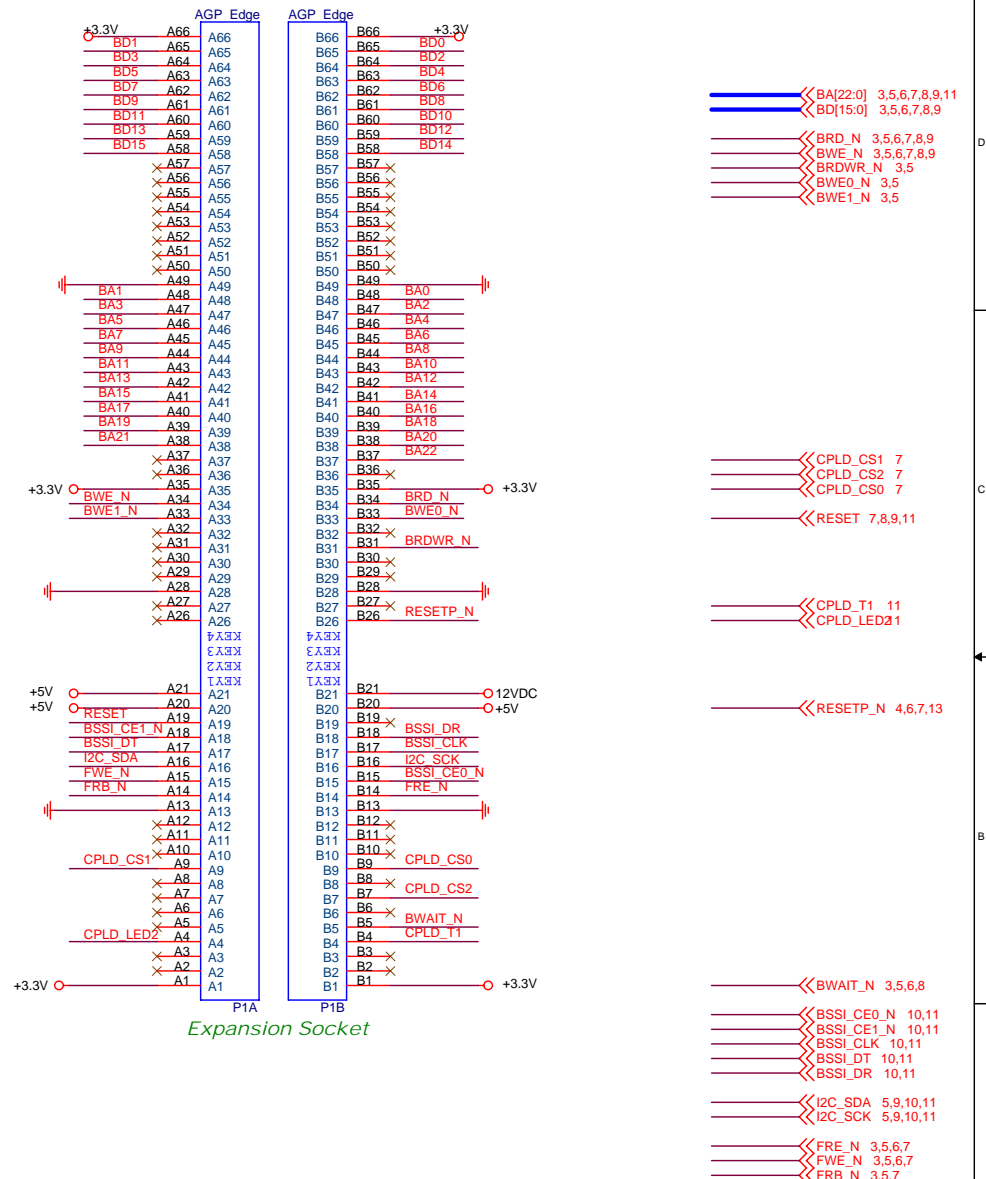
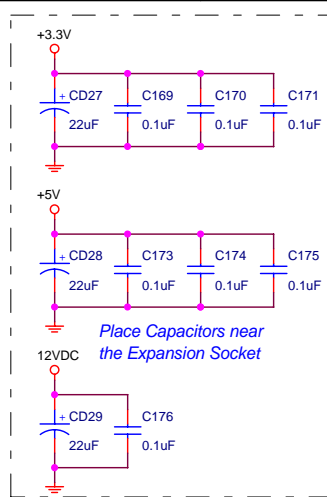
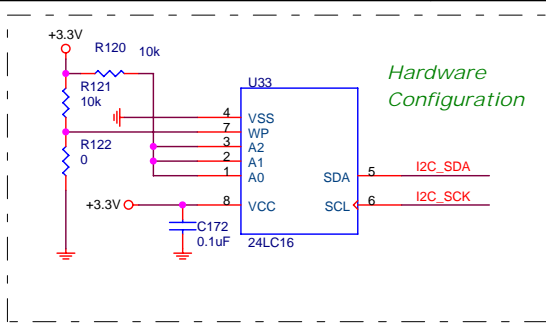
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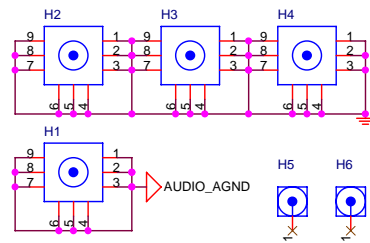
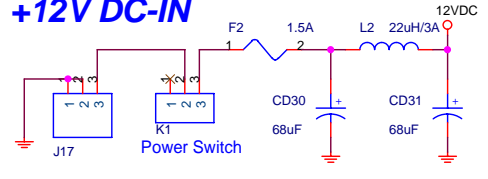
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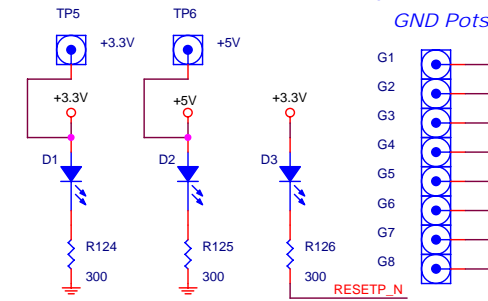
Rev
1.0



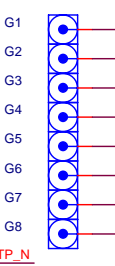
+12V DC-IN



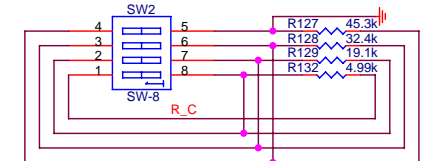
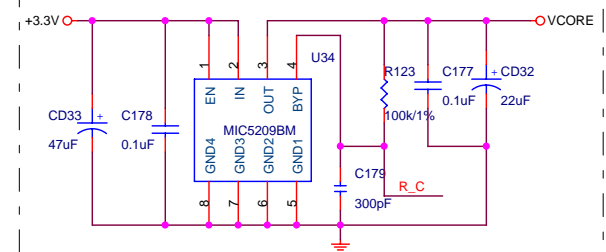
Power Supply Indicators



GND Pots



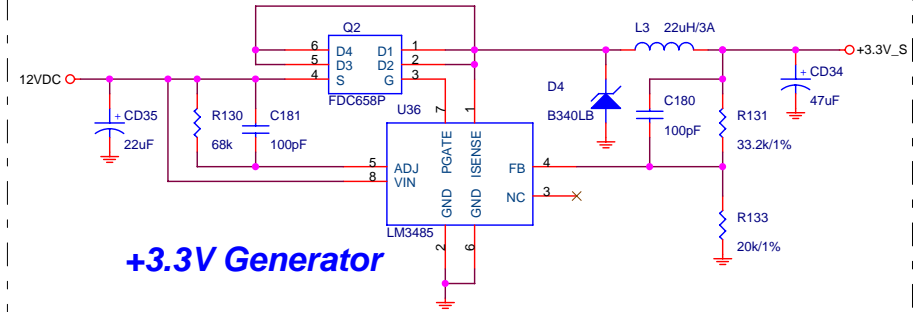
VCORE Generator



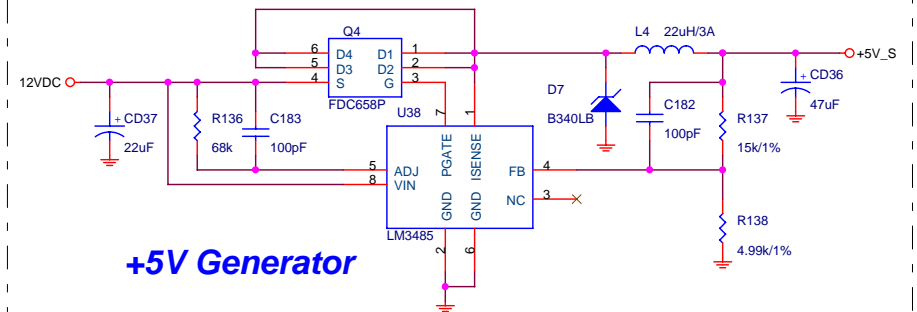
CORE VOLTAGE TABLE (0:OFF,1:ON):

SW3 CODE (1,2,3,4)	CORE VOLTAGE
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0,0,1,1	1.54V
1,1,0,1	1.64V
0,1,0,1	1.70V
1,1,1,0	1.80V
1,0,0,1	1.88V
0,0,0,1	1.94V
1,0,1,0	2.04V
0,0,1,0	2.10V
1,1,0,0	2.20V
0,0,0,0	2.50V

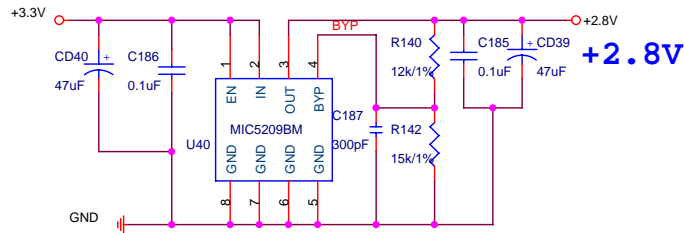
+3.3V Generator



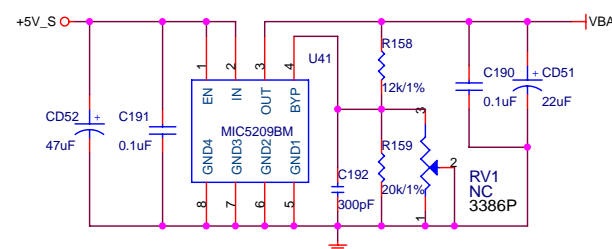
+5V Generator



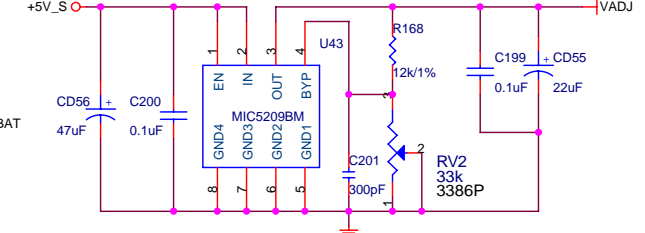
+2.8V Generator



VRTC Generator



VADJ Generator



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LEO Development Board for Jz4740 Schematics

Revision History

Data	Revision	Change
Mar 1 2007	Rev1.0	1. First Revision
Apr 15 2007	Rev1.1	1. Corrected the Jz4740 lib definition. 2. Add the CD46,CD47,CD48,CD49. 3. Modified the USB Device circuit. 4. Changed the RTL8029 to CS8900A.