I94100 CMSIS BSP Revision History

Revision 3.05.003 (Released 2019-10-24)

- [Fixed]
  - I2S incorrect clock calculations and PCM mode setting constant.
  - Fixed PB5 I2C0 MFP define in sys.h.
  - Fixed PLL parameter calculation in clk.c & CLK_GetPLLClockFreq u32PllFreq calculation in clk.h.
  - Incorrect VAD power threshold constant define in vad.h and VAD_WriteBIQCoeff() in vad.c.
  - Fixed setting data flash base issue in FMC_RW sample.
  - ISP_HID/ISP_UART remove bank erase to fix data flash erase issue.
  - Fixed USBD_UAC_DMIC_DPWM_PDMA issue when “Listen to this device” is checked.
  - Fixed incorrect SYS_RCADJ register address.
- [Revise]
  - Revised “SPI_IS_BUSY()” using optimal method.
  - ISP_HID code change to interrupt approach.
  - Revised USBD DM pin mode setting in USBD_Open() in usbd.c.

Revision 3.05.002 (Released 2018-10-02)

- [Fixed]
  - "I2S_Slave_DPWM" might occur two channels swapping.
  - WindowsTool in "USBD_HID_Transfer", "USBD_Printer_And_HID_Transfer" and "USBD_VCOM_And_HIDTransfer" has incorrect target PID. Resulting "HIDTransferTest.exe" could not work properly.
- [Revise]
  - Move buffer update process from main loop to EP3_IRQHandler, to prevent noise. Revised samples: "USBD_UAC_DMIC_DPWM_PDMA_4CH", "USBD_UAC_DPWM", "USBD_UAC_DMIC_DPWM_PDMA" and "USBD_UAC_I2S_Output"

Revision 3.05.001 (Released 2018-09-25)

- [Note]
  - This version is target for EVB that using "12.288 MHz External Crystal". Before using this BSP, please make sure your external crystal is 12.288 MHz.
- [Add]
  - "SPI_QuadFlash" Demonstrate how to use SPI quad-mode to read/write data to external SPI-FLash.
  - "USBD_UAC_85L40_PDMA_4CH_VolCtrl" Demonstrate how to implement a USB 4-channel recording device using codec NAU85L40. "USBD_UAC_85L40_PDMA_4CH_NoVolCtrl" is without volume control version.
  - "USBD_UAC_DMIC_DPWM_PDMA_4CH" Demonstrate how to implement a USB 4-channel recording and playback device using DMIC and DPWM.
  - "USBD_UAC_DMIC_PDMA_4CH" Demonstrate how to implement a USB 4-channel recording device using DMIC.
  - "USBD_UAC_I2S_Output" Demonstrate how to implement a UAC device and output audio data by I2S.

    - "I2S_Slave_DPWM" Demonstrate how to implement a I2S slave device to receive audio data from master and playback by DPWM.
    - "USBD_UAC_85L40_DPWM_PDMA_4CH_VolCtrl" Demonstrate how to implement a USB 4-channel recording playback device using codec NAU85L40 and DPWM.
- [Revised]
    - Revise "Set_ModuleClock" API for new USBD default clock source setting and USBD related samples for new I94100 ver.D.
    - Revise "I2S_Master", "I2S_DPWM_85L40", "I2S_DPWM_85L40_PDMA", "USBD_UAC_85L40_PDMA", "USBD_UAC_85L40_PDMA_4CH" PLL frequency to be compatible with the new HXT frequency.
    - "FMC_ISPCTL" has new gerister, "PT" ISP Flash Program Time, at the FMC_ISPCTL[10:8].
    - Revise VID and PID to USBD related samples.
- [Fixed]
    - SPI_Open return incorrecty peripheral frequency.
    - Revise startup_I94100.s to avoid WIC not reset after wake-up.
    - "FMC_IAP" All NVIC interrupt request need to be disabled before remapping.
    - "USB_Mass_Storage_DataFlash" LDO overdrive needs to be enabled if the HCLK is over 160 MHz.
    - "SYS_SPDMode_Wakeup" The SRAM retention check addres might be used by other variable after wake-up.
    - API "CLK_EnablePLL" has incorrect Input Divider - NR limitation.
    - API "CLK_SetPCLKDivider" has incorrect PCLKDIV calculation.

Revision 3.00.002 (Released 2017-05-17)

- EADC samples add extend sampling time.

Revision 3.00.001 (Released 2017-05-09)

- Add trim HIRC 48.000/49.152 MHz selection and checking.
- Modify IPs module reset calling flow.

Revision 3.00.000 (Released 2017-04-18)

- Initial Release.

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