

# NuMicro<sup>®</sup> Family 1T 8051-based Microcontroller

# N76E003 Series BSP Revision History

The information described in this document is the exclusive intellectual property of Nuvoton Technology Corporation and shall not be reproduced without permission from Nuvoton.

Nuvoton is providing this document only for reference purposes of NuMicro microcontroller based system design. Nuvoton assumes no responsibility for errors or omissions.

All data and specifications are subject to change without notice.

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com



# N76E003 BSP for KEIL C51 Revision History

# Reversion 2.00 (Release 2023-11-1)

KEIL/IAR/NuEclipse all in one package.

### Reversion 1.06 (Release 2018-7-2)

Modified "Watchdog\_Reset" project. Added check CONFIG WDT setting, enable WDT reset if disable.

Renamed "printf UART1" to "UART1 printf". Optimize UART1 printf putchar setting.

Added project "UARTO printf".

Added Project "ADC multi channel"

Modified "Modify IAP\_Dataflash\_EEPROM" as XRAM buffer mode.

Modifiied "ADC Bandgap VDD noDelay" add loop function to check VDD value.

Modifyied "IAP MoidfyHIRC" read data from RCTRIM0 and RCTROM1.

Fixed "PWM INT" not into interrupt issue.

## Reversion 1.05 (Release 2018-1-29)

Modified "Modify IAP\_Dataflash\_EEPROM" the XRAM code issue and add 16bit combine sample. Fix XRAM address error

Added define UART1 as printf output function sample project.

Removed I2C slave project waiting interrupt stop issue.

Removed "ADC\_bandgap\_VDD", replaced with "ADC\_Bandgap\_VDD\_noDelay" Project demo for use bandgap value to calculate VDD value.

# Reversion 1.04 (Release 2017-12-28)

Modified "Modify IAP\_Dataflash\_EEPROM" the XRAM code issue and add 16bit combine sample.

Added "Watch dog reset disable" sample project.

Removed SFR\_Macro.h set\_BOV2 define.

### Reversion 1.03 (Release 2017-11-2)

Modified ADC read band-gap and calculate VDD demo.

Modified UART0 project option setting.

Modified IAP Dataflash EEPROM the XRAM storage address start from 0x280.

Modified function define.h file define of Set All GPIO Quasi Mode P0M2.

Modified function\_define.h file TIMER0\_MODE3\_ENABLE / TIMER1\_MODE3\_ENABLE setting.

#### Reversion 1.02 (Release 2017-6-20)

Added POR disable instruction in startup.a51

Added ADC read band-gap and calculate VDD value demo

Added ADC 16 times optimize demo

Add read UCID sample code

Modified Timer 2 capture sample setting.

Modified I2C EEPROM demo code, add check SI status, modify error check process.

# Reversion 1.01 (Release 2017-1-20)

Fixed PWM interrupt initial setting in Function\_define.h

Fixed SFR list add P1.6 / P1.7 define in N76E003.h

Added SPI Flash 25Q16 read / write demo.

Added SPI master / slave control demo code, include interrupt and polling.

# Reversion 1.00 (Release 2016-11-15)

Initial release version



# **Important Notice**

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

Please note that all data and specifications are subject to change without notice.

All the trademarks of products and companies mentioned in this datasheet belong to their respective owners