2 July 2024

FPGA Meetup

Code Blame 975 lines (880 loc) · 43.9 KB

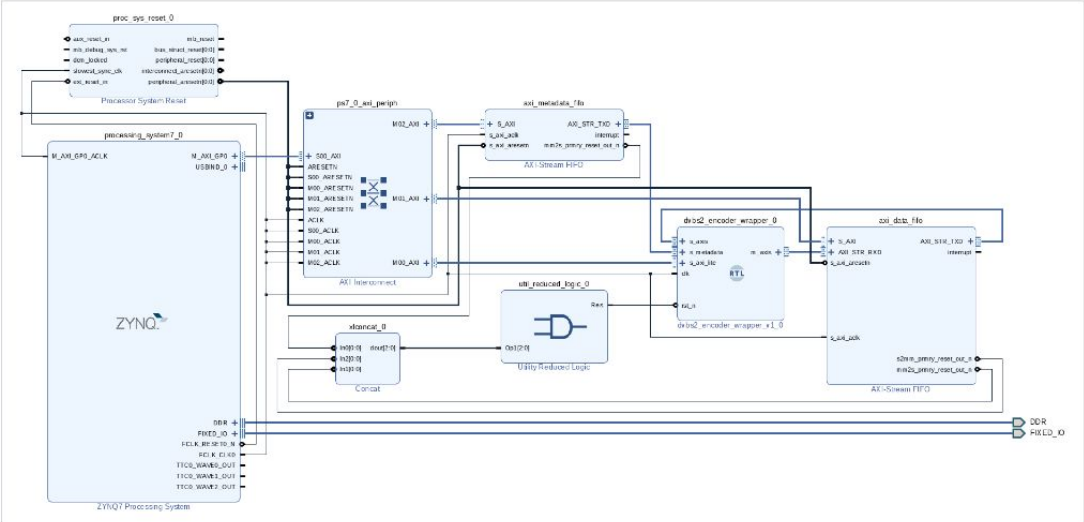
```
880       -- Register map decoder
881       regmap_block : block
882         signal s_axi_awaddr_32 : std_logic_vector(31 downto 0) := (others => '0');
883         signal s_axi_araddr_32 : std_logic_vector(31 downto 0) := (others => '0');
884       begin
885         s_axi_awaddr_32(s_axi_awaddr'range) <= s_axi_awaddr;
886         s_axi_araddr_32(s_axi_araddr'range) <= s_axi_araddr;
887
888         regmap_u : entity work.dvbs2_encoder_regs
889           generic map (
890             AXI_ADDR_WIDTH => 32,
891             BASEADDR       => (others => '0'))
892           port map (
893             -- Clock and Reset
894             axi_aclk    => clk,
895             axi_aresetn => rst_n,
896             -- AXI Write Address Channel
897             s_axi_awaddr  => s_axi_awaddr_32,
898             s_axi_awprot  => (others => '0'),
899             s_axi_awvalid => s_axi_awvalid,
900             s_axi_awready => s_axi_awready,
901             -- AXI Write Data Channel
902             s_axi_wdata   => s_axi_wdata,
903             s_axi_wstrb   => s_axi_wstrb,
904             s_axi_wvalid  => s_axi_wvalid,
905             s_axi_wready  => s_axi_wready,
906             -- AXI Read Address Channel
907             s_axi_araddr  => s_axi_araddr_32,
908             s_axi_arprot  => (others => '0'),
909             s_axi_arvalid => s_axi_arvalid,
910             s_axi_arready => s_axi_arready,
911             -- AXI Read Data Channel
912             s_axi_rdata   => s_axi_rdata,
913             s_axi_rresp   => s_axi_rresp,
914             s_axi_rvalid  => s_axi_rvalid,
915             s_axi_rready  => s_axi_rready,
916             -- AXI Write Response Channel
917             s_axi_bresp   => s_axi_bresp,
918             s_axi_bvalid  => s_axi_bvalid,
919             s_axi_bready  => s_axi_bready,
920             -- User Ports
921             user2regs     => user2regs,
922             regs2user     => regs2user);
923       end block regmap_block;
924
```

README.md

ZC706

This directory contains scripts to build a test design on the ZC706 evaluation board. An AXI Stream FIFO is used to loop data to/from the DVB encoder.

The design's block diagram is shown below



ZC706 test design block diagram

Memory map

Address range	Name
`0x43C0_0000` to `0x43C0_FFFF`	`axi_data_fifo/S_AXI`
`0x43C1_0000` to `0x43C1_FFFF`	`dvbs2_encoder_wrapper_0/s_axi_lite`
`0x43C2_0000` to `0x43C0_FFFF`	`axi_metadata_fifo/S_AXI`

Data interface

Data is sent to the DVB encoder using `axi_data_fifo/AXI_STR_TXD`, while frame configuration is sent using `axi_metadata_fifo/AXI_STR_TXD`. The mapping between metadata values and frame parameters is show below:

s_axis.tid value	Frame length	Constellation	Code rate
0x00	FECFRAME_SHORT	QPSK	1/4
0x01	FECFRAME_SHORT	QPSK	1/3
0x02	FECFRAME_SHORT	QPSK	2/5
0x03	FECFRAME_SHORT	QPSK	1/2
0x04	FECFRAME_SHORT	QPSK	3/5
0x05	FECFRAME_SHORT	QPSK	2/3
0x06	FECFRAME_SHORT	QPSK	3/4
0x07	FECFRAME_SHORT	QPSK	4/5
0x08	FECFRAME_SHORT	QPSK	5/6
0x09	FECFRAME_SHORT	QPSK	8/9
0x0A	FECFRAME_SHORT	QPSK	9/10
0x0B	FECFRAME_SHORT	8PSK	1/4
0x0C	FECFRAME_SHORT	8PSK	1/3
0x0D	FECFRAME_SHORT	8PSK	2/5

dvbs2_encoder

Description	n/a
Default base address	`0x0`
Register width	32 bits
Default address width	32 bits
Register count	47
Range	4888 bytes
Revision	347

Overview

Offset	Name	Description	Type
`0x0`	config		REG
`0x4`	ldpc_fifo_status		REG
`0x8`	frames_in_transit		REG
		Radius for 16APSK and 32APSK constellation mapping.R0 uses bits 15:0, R1 uses bits	

Registers

Offset	Name	Description	Type	Access	Attributes
`0x0`	config		REG	R/W	
	[17:0] physical_layer_scrambler_shift_reg_init	Initial value for the physical layer's scrambler X vector, used to set a device's gold code.			
	[18] enable_dummy_frames				
	[19] swap_input_data_byte_endianness	Changes input data byte endianness. Has no effect if input data width is 8.			
	[20] swap_output_data_byte_endianness				
	[21] force_output_ready	Ignores external m_tready and force the internal value to 1			
`0x4`	ldpc_fifo_status		REG	R	