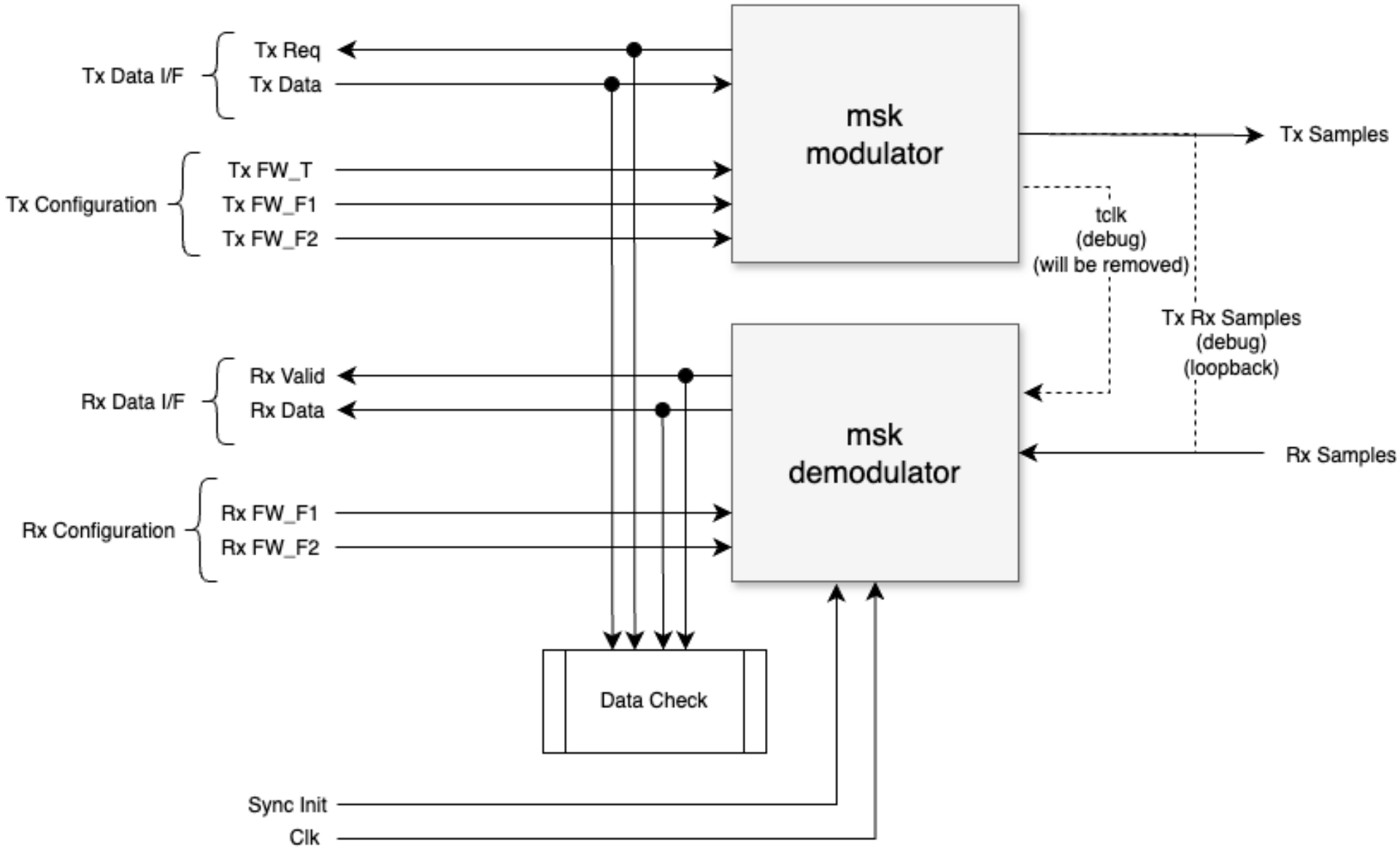
11 June 2024

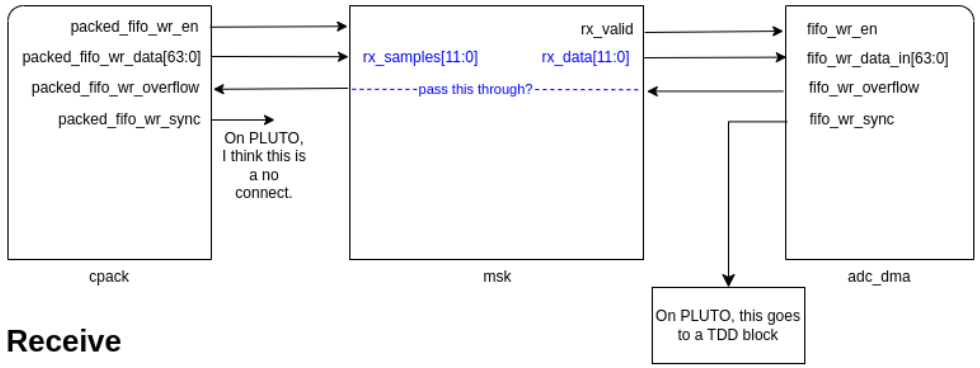
ORI FPGA Meetup

MSK TOP


Tx Data I/F
Tx Req
Tx Data
Tx Configuration
Tx FW_T
Tx FW_F1
Tx FW_F2
msk
modulator
Tx Samples
tclk
(debug)
(will be removed)
Tx Rx Samples
(debug)
(loopback)
Rx Data I/F
Rx Valid
Rx Data
msk
demodulator
Rx Samples
Rx Configuration
Rx FW_F1
Rx FW_F2
Data Check
Sync Init
Clk

Opulent Voice Minimum Shift Key TCL Connections

ORI
Version 1
7 June 2024

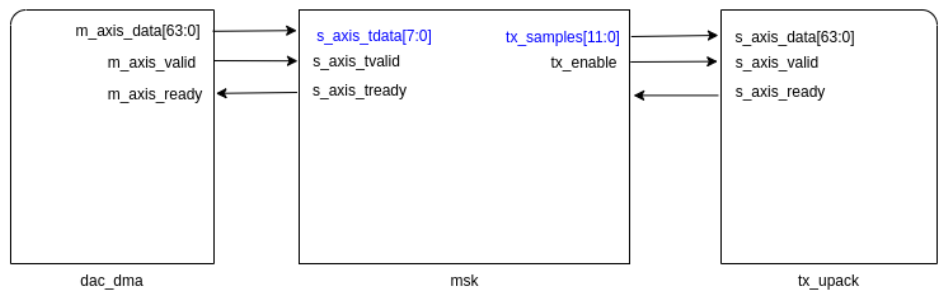


Receive

Connections required for the receiver functions. FIFO-centric.

Items in blue will need to be adjusted for the 64-bit bus width in the PLUTO reference design. The packed_fifo_wr_enable feels functionally like a s_axis_valid signal to me. I don't think I have anything to hook it up to yet.

Should we pass through the overflow signal? Or would that cause problems?



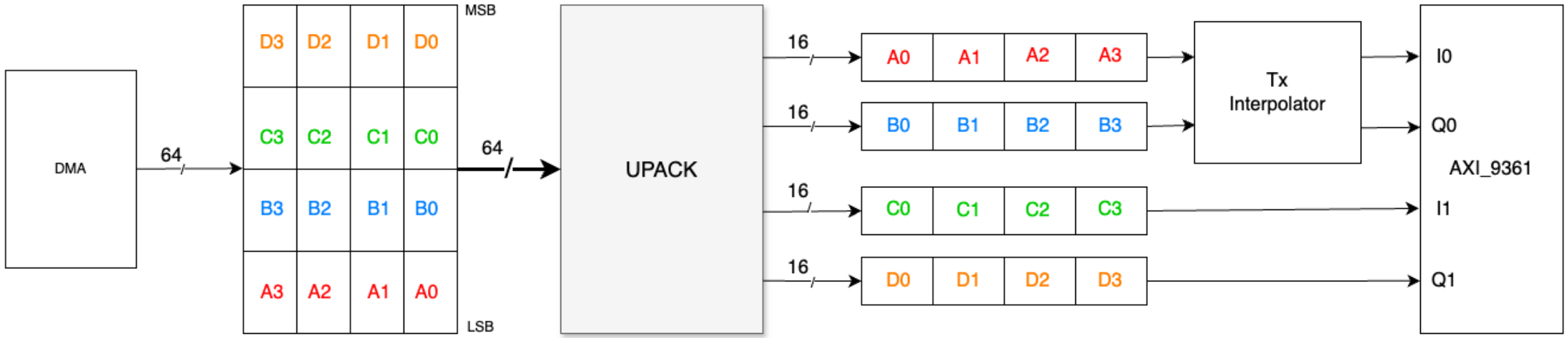
Transmit

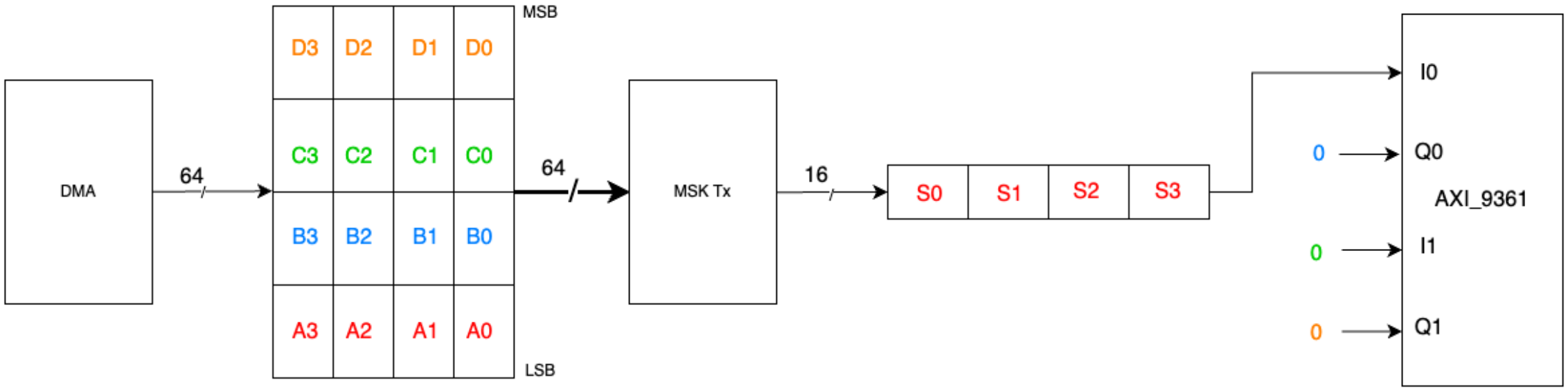
Connections required for the transmitter functions. AXIS-centric.

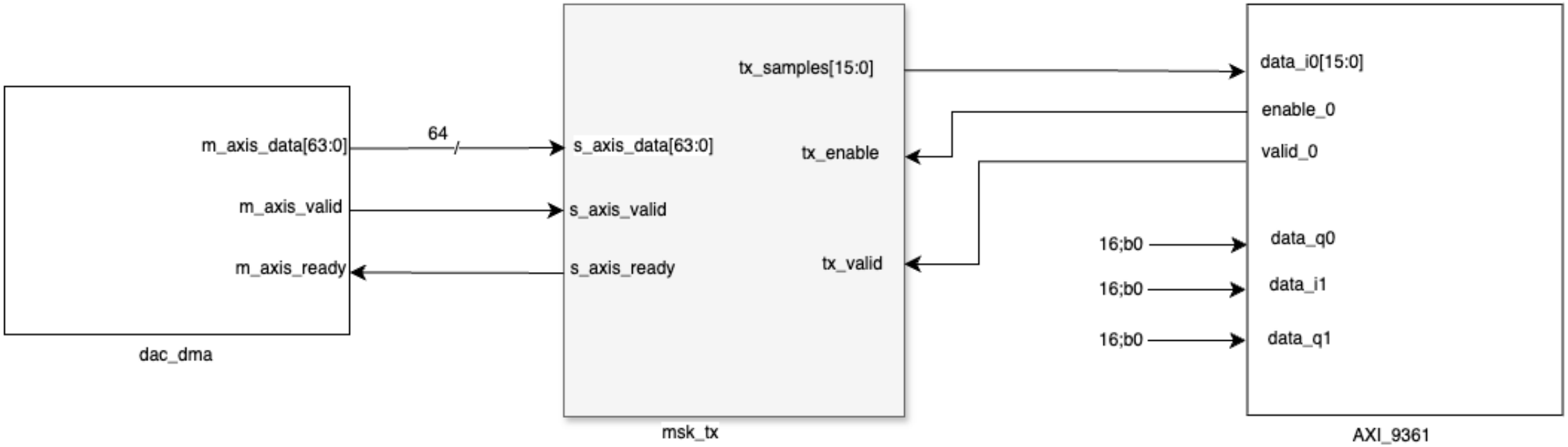
we'll need our own m_axis_ready input in order to know if the tx_upack is not ready to receive any data. According to the user guide, this should be a very rare situation, as the transmit side is very lock-step. I believe the upack block is the last one in the transmitter with AXIS flow control.

the data bus will need to be sized up a bit.

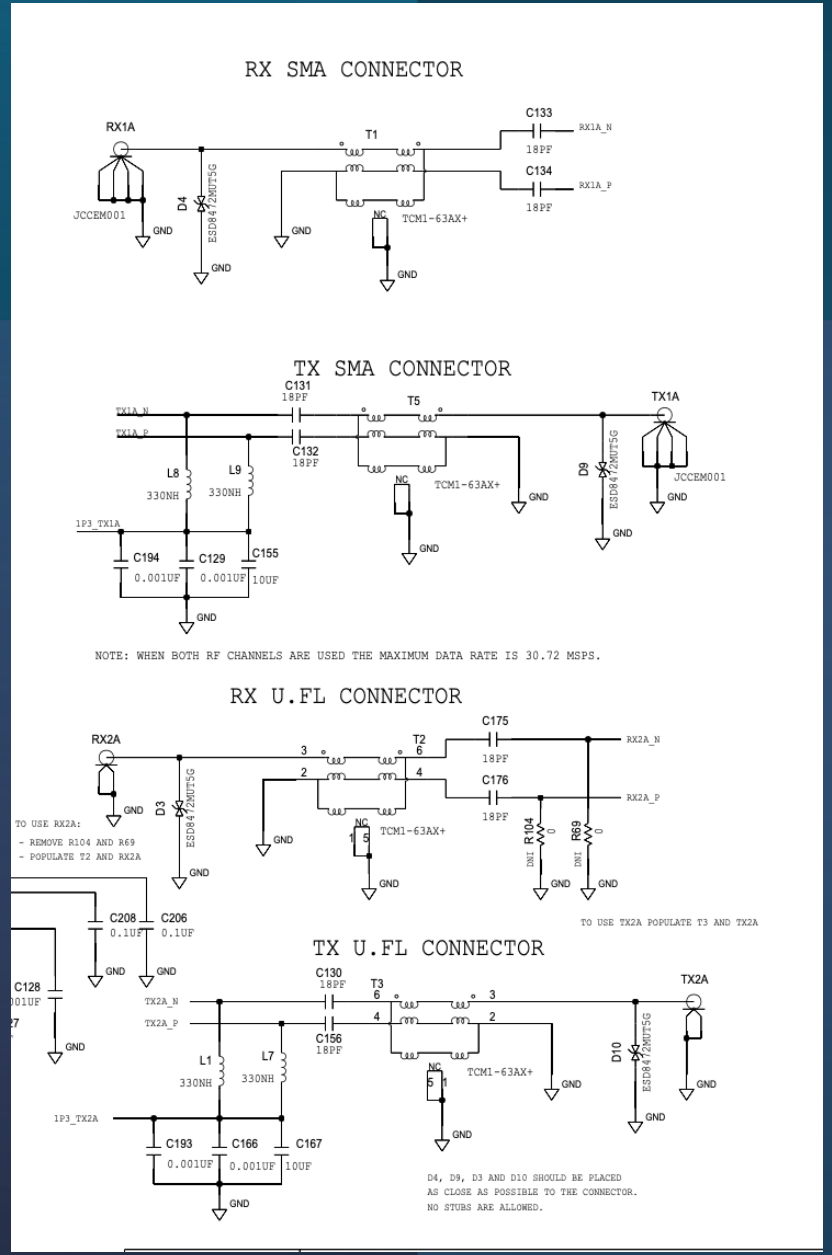
We are treating the DMA data as data, and not IQ samples. We are providing transmit data to the I channel, and zeroing out the Q.

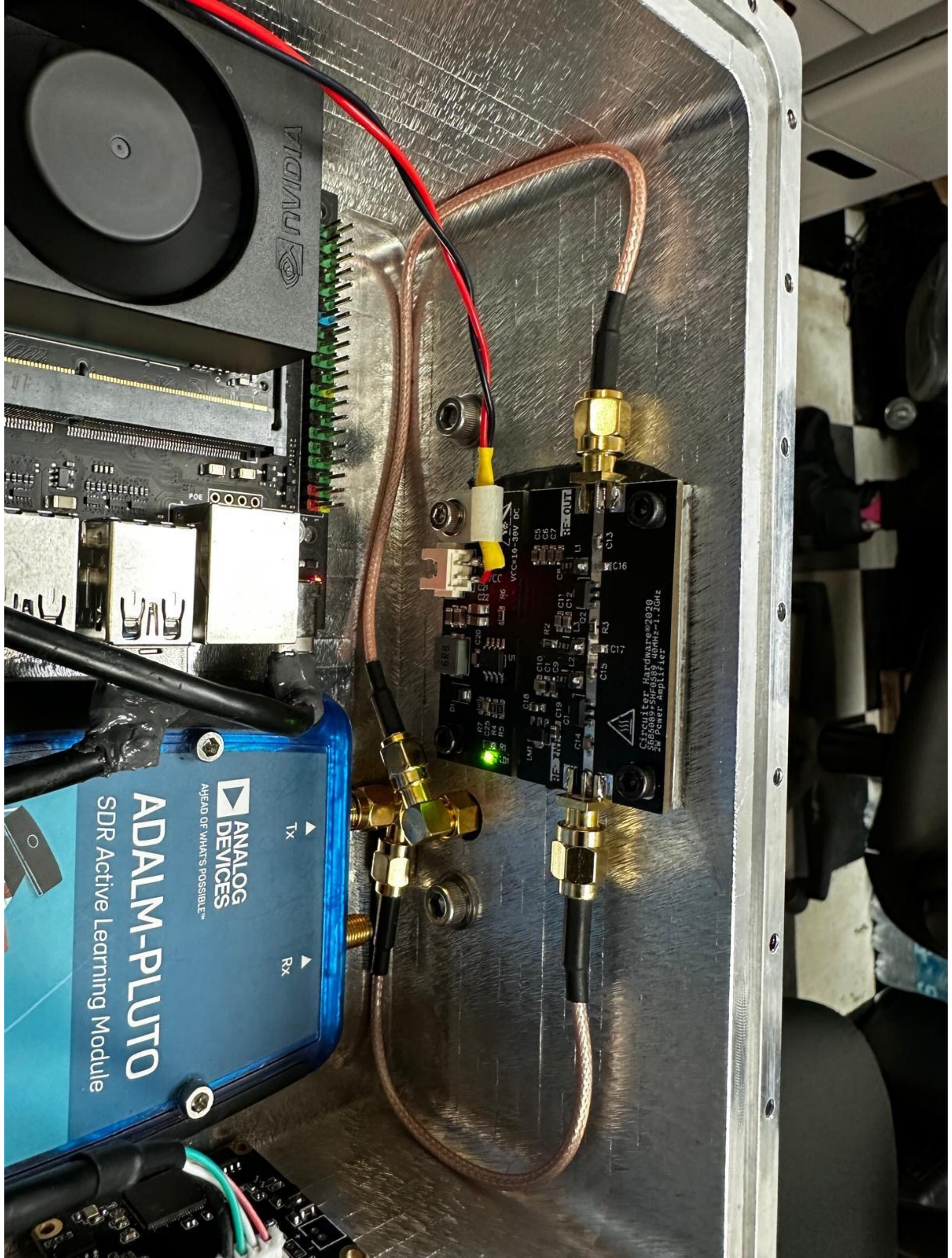

DMA
64
D3
D2
D1
D0
C3
C2
C1
C0
B3
B2
B1
B0
A3
A2
A1
A0
MSB
LSB
64
UPACK
16
16
16
16
A0
A1
A2
A3
B0
B1
B2
B3
C0
C1
C2
C3
D0
D1
D2
D3
Tx
Interpolator
I0
Q0
AXI_9361
I1
Q1


DMA
64
D3
D2
D1
D0
C3
C2
C1
C0
B3
B2
B1
B0
A3
A2
A1
A0
MSB
LSB
64
MSK Tx
16
S0
S1
S2
S3
I0
0
Q0
AXI_9361
0
I1
0
Q1


m_axis_data[63:0]
64
m_axis_valid
m_axis_ready
dac_dma
s_axis_data[63:0]
s_axis_valid
s_axis_ready
tx_samples[15:0]
tx_enable
tx_valid
msk_tx
data_i0[15:0]
enable_0
valid_0
16;b0
16;b0
16;b0
data_q0
data_i1
data_q1
AXI_9361

Second Transmitter Connections on the PLUTO




NVIDIA
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™
ADALM-PLUTO
SDR Active Learning Module
Tx
Rx

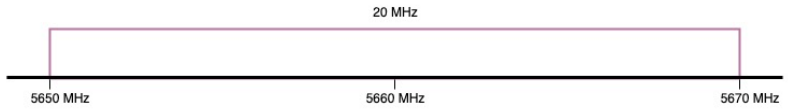

UPR
Puerto Rico Space Grant Consortium
NASA
NASA
Partner
NASA Cooperative Agreement 80NSSC20M0052
UNIVERSITY OF PUERTO RICO
BioSPHERE
NASA WALLOPS FLIGHT FACILITY – ROCKSAT-X

Haifuraiya Channel Plan

ORI (Ken Easton, Michelle Thompson)
8 June 2024 Version 3

Opulent Voice bitrate 27,100 * 2 = 54,200 bps
99% bandwidth for MSK is 1.2 * Tb = 65,040 Hz
null-to-null bandwidth for MSK is 1.5 * Tb = 81,300 Hz

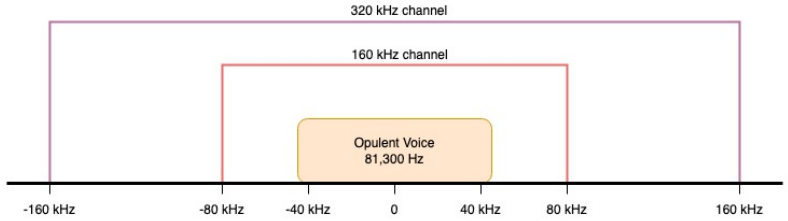
a 2^n * 20 kHz based approach to the system design gives channels of 20, 40, 80, **160**, **320**



amateur satellite uplink frequency allocation

IQ sample rate set in TES / (number of polyphase channels * oversampling factor) = channel bandwidth
40.96 MHz / (64 * 2) = 320 kHz
40.96 MHz / (128 * 2) = 160 kHz

allocation / channel bandwidth = number of channels in allocation
20 MHz / 320 kHz = 62.5
Channels 63 and 64 are not usable in this scheme.
20 MHz / 160 kHz = 125
Channels 126 - 128 are not usable in this scheme.



frequency relative to center of channel

What would the allocation have to be in order to use all of the polyphase channels with the achievable IQ sample rate?
allocation / channel bandwidth = number of channels in allocation
20.48 MHz / 320 kHz = 64
20.48 MHz / 160 kHz = 128

The allocation is derived from a voluntary band plan.
It is legal to transmit 480 kHz above 5670 MHz in all regions.
Transmissions at 5670.48 MHz do not impinge on a calling frequency or weak signal work.

Question: Shall we specify a 20 MHz or a 20.48 MHz bandwidth for Haifuraiya satellite uplink?
Answer: 20 MHz due to parts availability and we comply with the band plan. Giving up the top few channels is not enough of a disadvantage to outweigh the advantages of the 20 MHz RF BW setting.