

## Pluto\_MSK\_Modem address map

- Absolute Address: 0x0
- Base Offset: 0x0
- Size: 0x43C0006C

Offset	Identifier	Name
0x43C00000	pluto_msk_regs	Pluto MSK Registers

## pluto\_msk\_regs address map

- Absolute Address: 0x43C00000
- Base Offset: 0x43C00000
- Size: 0x6C

### MSK Modem Configuration and Status Registers

Offset	Identifier	Name
0x00	Hash_ID_Low	Pluto MSK FPGA Hash ID - Lower 32-bits
0x04	Hash_ID_High	Pluto MSK FPGA Hash ID - Upper 32-bits
0x08	MSK_Init	MSK Modem Control 0
0x0C	MSK_Control	MSK Modem Control 1
0x10	MSK_Status	MSK Modem Status 0
0x14	Tx_Bit_Count	MSK Modem Status 1
0x18	Tx_Enable_Count	MSK Modem Status 2
0x1C	Fb_FreqWord	Bitrate NCO Frequency Control Word
0x20	TX_F1_FreqWord	Tx F1 NCO Frequency Control Word
0x24	TX_F2_FreqWord	Tx F2 NCO Frequency Control Word
0x28	RX_F1_FreqWord	Rx F1 NCO Frequency Control Word
0x2C	RX_F2_FreqWord	Rx F2 NCO Frequency Control Word
0x30	LPF_Config_0	PI Controller Configuration and Low-pass Filter Configuration
0x34	LPF_Config_1	PI Controller Configuration Configuration Register 1
0x38	Tx_Data_Width	Modem Tx Input Data Width
0x3C	Rx_Data_Width	Modem Rx Output Data Width
0x40	PRBS_Control	PRBS Control 0
0x44	PRBS_Initial_State	PRBS Control 1
0x48	PRBS_Polynomial	PRBS Control 2
0x4C	PRBS_Error_Mask	PRBS Control 3
0x50	PRBS_Bit_Count	PRBS Status 0
0x54	PRBS_Error_Count	PRBS Status 1
0x58	LPF_Accum_F1	F1 PI Controller Accumulator
0x5C	LPF_Accum_F2	F2 PI Controller Accumulator
0x60	axis_xfer_count	MSK Modem Status 3
0x64	Rx_Sample_Discard	Rx Sample Discard

Offset	Identifier	Name
0x68	LPF_Config_2	PI Controller Configuration Configuration Register 2

#### Hash\_ID\_Low register

- Absolute Address: 0x43C00000
- Base Offset: 0x0
- Size: 0x4

Bits	Identifier	Access	Reset	Name
31:0	hash_id_lo	r	0xAAAA5555	Hash ID Lower 32-bits

**hash\_id\_lo field** Lower 32-bits of Pluto MSK FPGA Hash ID

#### Hash\_ID\_High register

- Absolute Address: 0x43C00004
- Base Offset: 0x4
- Size: 0x4

Bits	Identifier	Access	Reset	Name
31:0	hash_id_hi	r	0x5555AAAA	Hash ID Upper 32-bits

**hash\_id\_hi field** Upper 32-bits of Pluto MSK FPGA Hash ID

#### MSK\_Init register

- Absolute Address: 0x43C00008
- Base Offset: 0x8
- Size: 0x4

Synchronous initialization of MSK Modem functions, does not affect configuration registers.

Bits	Identifier	Access	Reset	Name
0	txrxinit	rw	0x1	Tx/Rx Init Enable
1	txinit	rw	0x1	Tx Init Enable
2	rxinit	rw	0x1	Rx Init Enable

**txrxinit field** 0 -> Normal modem operation 1 -> Initialize Tx and Rx

**txinit field** 0 -> Normal Tx operation 1 -> Initialize Tx

**rxinit field** 0 -> Normal Rx operation 1 -> Initialize Rx

#### MSK\_Control register

- Absolute Address: 0x43C0000C
- Base Offset: 0xC
- Size: 0x4

MSK Modem Configuration and Control

Bits	Identifier	Access	Reset	Name
0	ptt	rw	0x0	Push-to-Talk Enable
1	loopback_ena	rw	0x0	Modem Loopback Enable
2	rx_invert	rw	0x0	Rx Data Invert Enable
3	clear_counts	rw	0x0	Clear Status Counters

**ptt field** 0 -> PTT Disabled 1 -> PTT Enabled

**loopback\_ena field** 0 -> Modem loopback disabled 1 -> Modem loopback enabled

**rx\_invert field** 0 -> Rx data normal 1 -> Rx data inverted

**clear\_counts field** Clear Tx Bit Counter and Tx Enable Counter

#### MSK\_Status register

- Absolute Address: 0x43C00010
- Base Offset: 0x10
- Size: 0x4

Modem status bits

Bits	Identifier	Access	Reset	Name
0	demod_sync_lock	r	0x0	Demodulator Sync Status
1	tx_enable	r	0x0	AD9363 DAC Interface Tx Enable Input Active
2	rx_enable	r	0x0	AD9363 ADC Interface Rx Enable Input Active
3	tx_axis_valid	r	0x0	Tx S_AXIS_VALID

**demod\_sync\_lock field** Demodulator Sync Status - not currently implemented

**tx\_enable field** 1 -> Data to DAC Enabled 0 -> Data to DAC Disabled

**rx\_enable field** 1 -> Data from ADC Enabled 0 -> Data from ADC Disabled

**tx\_axis\_valid field** 1 -> S\_AXIS\_VALID Enabled 0 -> S\_AXIS\_VALID Disabled

#### **Tx\_Bit\_Count register**

- Absolute Address: 0x43C00014
- Base Offset: 0x14
- Size: 0x4

Modem status data

Bits	Identifier	Access	Reset	Name
31:0	tx_bit_counter	r	0x0	Tx Bit Count

**tx\_bit\_counter field** Count of data requests made by modem

#### **Tx\_Enable\_Count register**

- Absolute Address: 0x43C00018
- Base Offset: 0x18
- Size: 0x4

Modem status data

Bits	Identifier	Access	Reset	Name
31:0	tx_ena_counter	r	0x0	Tx Enable Count

**tx\_ena\_counter field** Number of clocks on which Tx Enable is active

#### **Fb\_FreqWord register**

- Absolute Address: 0x43C0001C
- Base Offset: 0x1C
- Size: 0x4

Set Modem Data Rate

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	Frequency Control Word

**config\_data field** Sets the center frequency of the NCO as  $FW = F_n * 2^{32}/F_s$ , where  $F_n$  is the desired NCO frequency, and  $F_s$  is the NCO sample rate

#### TX\_F1\_FreqWord register

- Absolute Address: 0x43C00020
- Base Offset: 0x20
- Size: 0x4

Set Modulator F1 Frequency

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	Frequency Control Word

**config\_data field** Sets the center frequency of the NCO as  $FW = F_n * 2^{32}/F_s$ , where  $F_n$  is the desired NCO frequency, and  $F_s$  is the NCO sample rate

#### TX\_F2\_FreqWord register

- Absolute Address: 0x43C00024
- Base Offset: 0x24
- Size: 0x4

Set Modulator F2 Frequency

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	Frequency Control Word

**config\_data field** Sets the center frequency of the NCO as  $FW = F_n * 2^{32}/F_s$ , where  $F_n$  is the desired NCO frequency, and  $F_s$  is the NCO sample rate

#### RX\_F1\_FreqWord register

- Absolute Address: 0x43C00028
- Base Offset: 0x28
- Size: 0x4

Set Demodulator F1 Frequency

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	Frequency Control Word

**config\_data field** Sets the center frequency of the NCO as  $FW = F_n * 2^{32}/F_s$ , where  $F_n$  is the desired NCO frequency, and  $F_s$  is the NCO sample rate

### **RX\_F2\_FreqWord register**

- Absolute Address: 0x43C0002C
- Base Offset: 0x2C
- Size: 0x4

Set Demodulator F2 Frequency

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	Frequency Control Word

**config\_data field** Sets the center frequency of the NCO as  $FW = F_n * 2^{32}/F_s$ , where  $F_n$  is the desired NCO frequency, and  $F_s$  is the NCO sample rate

### **LPF\_Config\_0 register**

- Absolute Address: 0x43C00030
- Base Offset: 0x30
- Size: 0x4

Configure PI controller and low-pass filter

Bits	Identifier	Access	Reset	Name
0	lpf_freeze	rw	0x0	Freeze the accumulator's current value
1	lpf_zero	rw	0x0	Hold the PI Accumulator at zero
7:2	prbs_reserved	w	0x0	—
31:8	lpf_alpha	rw	0x0	Lowpass IIR filter alpha

**lpf\_freeze field** 0 -> Normal operation 1 -> Freeze current value

**lpf\_zero field** 0 -> Normal operation 1 -> Zero and hold accumulator

**lpf\_alpha field** Value controls the filter rolloff

### **LPF\_Config\_1 register**

- Absolute Address: 0x43C00034
- Base Offset: 0x34
- Size: 0x4

Configures PI Controller I-gain and divisor

Bits	Identifier	Access	Reset	Name
23:0	i_gain	rw	0x0	Integral Gain Value

Bits	Identifier	Access	Reset	Name
31:24	i_shift	rw	0x0	Integral Gain Bit Shift

**i\_gain field** Value m of 0-16,777,215 sets the integral multiplier

**i\_shift field** Value n of 0-32 sets the integral divisor as  $2^{-n}$

#### **Tx\_Data\_Width register**

- Absolute Address: 0x43C00038
- Base Offset: 0x38
- Size: 0x4

Set the parallel data width of the parallel-to-serial converter

Bits	Identifier	Access	Reset	Name
7:0	data_width	rw	0x8	Modem input/output data width

**data\_width field** Set the data width of the modem input/output

#### **Rx\_Data\_Width register**

- Absolute Address: 0x43C0003C
- Base Offset: 0x3C
- Size: 0x4

Set the parallel data width of the serial-to-parallel converter

Bits	Identifier	Access	Reset	Name
7:0	data_width	rw	0x8	Modem input/output data width

**data\_width field** Set the data width of the modem input/output

#### **PRBS\_Control register**

- Absolute Address: 0x43C00040
- Base Offset: 0x40
- Size: 0x4

Configures operation of the PRBS Generator and Monitor

Bits	Identifier	Access	Reset	Name
0	prbs_sel	rw	0x0	PRBS Data Select
1	prbs_error_insert	w	0x0	PRBS Error Insert
2	prbs_clear	w	0x0	PRBS Clear Counters
3	prbs_manual_sync	w	0x0	PRBS Manual Sync
15:4	prbs_reserved	w	0x0	—
31:16	prbs_sync_threshold	w	0x0	PRBS Auto Sync Threshold

**prbs\_sel field** 0 -> Select Normal Tx Data 1 -> Select PRBS Tx Data

**prbs\_error\_insert field** 0 -> 1 : Insert bit error in Tx data (both Normal and PRBS) 1 -> 0 : Insert bit error in Tx data (both Normal and PRBS)

**prbs\_clear field** 0 -> 1 : Clear PRBS Counters 1 -> 0 : Clear PRBS Counters

**prbs\_manual\_sync field** 0 -> 1 : Synchronize PRBS monitor 1 -> 0 : Synchronize PRBS monitor

**prbs\_sync\_threshold field** 0 : Auto Sync Disabled N > 0 : Auto sync after N errors

#### PRBS\_\_Initial\_State register

- Absolute Address: 0x43C00044
- Base Offset: 0x44
- Size: 0x4

PRBS Initial State

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	PRBS Seed

**config\_data field** Sets the starting value of the PRBS generator

#### PRBS\_\_Polynomial register

- Absolute Address: 0x43C00048
- Base Offset: 0x48
- Size: 0x4

PRBS Polynomial



Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	PRBS Polynomial

**config\_data field** Bit positions set to ‘1’ indicate polynomial feedback positions

#### PRBS\_Error\_Mask register

- Absolute Address: 0x43C0004C
- Base Offset: 0x4C
- Size: 0x4

PRBS Error Mask

Bits	Identifier	Access	Reset	Name
31:0	config_data	rw	0x0	PRBS Error Mask

**config\_data field** Bit positions set to ‘1’ indicate bits that are inverted when a bit error is inserted

#### PRBS\_Bit\_Count register

- Absolute Address: 0x43C00050
- Base Offset: 0x50
- Size: 0x4

PRBS Bits Received

Bits	Identifier	Access	Reset	Name
31:0	status_data	r	0x0	PRBS Bits Received

**status\_data field** Number of bits received by the PRBS monitor since last BER can be calculated as the ratio of received bits to errored-bits

#### PRBS\_Error\_Count register

- Absolute Address: 0x43C00054
- Base Offset: 0x54
- Size: 0x4

PRBS Bit Errors

Bits	Identifier	Access	Reset	Name
31:0	status_data	r	0x0	PRBS Bit Errors

**status\_data field** Number of errored-bits received by the PRBS monitor since last sync BER can be calculated as the ratio of received bits to errored-bits

#### **LPF\_Accum\_F1 register**

- Absolute Address: 0x43C00058
- Base Offset: 0x58
- Size: 0x4

Value of the F1 PI Controller Accumulator

Bits	Identifier	Access	Reset	Name
31:0	status_data	r	0x0	PI Controller Accumulator Value

**status\_data field** PI Controller Accumulator Value

#### **LPF\_Accum\_F2 register**

- Absolute Address: 0x43C0005C
- Base Offset: 0x5C
- Size: 0x4

Value of the F2 PI Controller Accumulator

Bits	Identifier	Access	Reset	Name
31:0	status_data	r	0x0	PI Controller Accumulator Value

**status\_data field** PI Controller Accumulator Value

#### **axis\_xfer\_count register**

- Absolute Address: 0x43C00060
- Base Offset: 0x60
- Size: 0x4

Modem status data

Bits	Identifier	Access	Reset	Name
31:0	xfer_count	r	0x0	S_AXIS Transfers

**xfer\_count field** Number completed S\_AXIS transfers

**Rx\_Sample\_Discard register**

- Absolute Address: 0x43C00064
- Base Offset: 0x64
- Size: 0x4

Configure samples discard operation for demodulator

Bits	Identifier	Access	Reset	Name
7:0	rx_sample_discard	rw	0x0	Rx Sample Discard Value
15:8	rx_nco_discard	rw	0x0	Rx NCO Sample Discard Value

**rx\_sample\_discard field** Number of Rx samples to discard

**rx\_nco\_discard field** Number of NCO samples to discard

**LPF\_Config\_2 register**

- Absolute Address: 0x43C00068
- Base Offset: 0x68
- Size: 0x4

Configures PI Controller I-gain and divisor

Bits	Identifier	Access	Reset	Name
23:0	p_gain	rw	0x0	Proportional Gain Value
31:24	p_shift	rw	0x0	Proportional Gain Bit Shift

**p\_gain field** Value m of 0-16,777,215 sets the proportional multiplier

**p\_shift field** Value n of 0-32 sets the proportional divisor as  $2^{-n}$