

# A Robust MSK demodulator through DSP

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**Abstract** — A Minimum Shift Keying (MSK) or Fast Frequency Shift Keying (FFSK) coherent demodulating algorithm is discussed. Both carrier synchronisation and optimal symbol correlation are done within two decision switched Costas loops, each operating at one of the reference signal frequencies. Simulation shows the demodulator to be robust against phase distortion and frequency drift in the received signal. The receiver is relatively simple and well suited to a DSP or digital implementation.

## I INTRODUCTION

This paper describes some preliminary results of work done on the development of a modem specifically for low earth orbiting satellites communicating in the VHF and UHF amateur radio frequency bands [6]. Microsatellites of this kind are built and operated by the Centre for Spacecraft Engineering Research at the University of Surrey (UoSAT), and one is at an advanced stage of planning at Stellenbosch University (SUNSAT).

The communications channel in the amateur microsatellite environment has some characteristics which inherently constrain the choice of modulation scheme:

- Transmitter power in the satellite is small, limiting the received signal-to-noise ratio at low satellite elevations.
- Non-linear (Class C) amplifier design is used in the satellite transmitter for high power efficiency and simplicity.
- A narrow-band FM channel is used.
- The channel has inherent Doppler shifts and phase distortion.
- There is a growing demand for higher data rates on the downlink, especially on satellites with earth imaging equipment.

MSK [3] in principle fits these constraints well. It has a constant envelope which survives non-linear amplification with minimal distortion; it is bandwidth efficient; and it has the same probability of error as coherent antipodal PSK [9]. Compared to the widely used discriminator detected FSK, MSK offers a 3 to 4dB improvement

in required carrier power at a bit error rate (BER) in the order of  $10^{-3}$  to  $10^{-4}$ .

With the transmitter design currently being implemented at UoSAT, it will be possible to generate continuous phase MSK modulation by simply frequency modulating the local oscillator with rectangular pulses. The pulse amplitude is set to generate the MSK frequency deviation of half the bit rate. It should also be possible to receive MSK, albeit suboptimally, with the established base of FSK discriminator equipment.

Previous work by the authors led to the achievement of MSK carrier synchronisation by embedding a DSP algorithm within an analogue phase lock loop [7]. That particular approach is now seen to be limited and unnecessarily complicated.

The demodulator is based neither on the classical quadrature description of MSK [2, 5] nor the serial description [4]. Massey [8] describes the data detector/decoder used here and proves its optimality. This paper extends that work by adding carrier and bit synchronisation.

Despite the theoretical appeal of MSK there seems to be a paucity of practical developments in working modems. It may be that practical systems tend to founder on the difficulty of designing sufficiently robust demodulators. Two alternative practical approaches to MSK demodulator design are described by Suzuki *et al* [11] and Del Re and Fantacci [10].

## II ANALOGUE INTERFACE

The demodulator described here is a digital signal processor (DSP). Its front end comprises an analogue-to-digital converter (ADC) which samples the signal at about five times the bit rate. This is preceded by bandpass filtering and the final local oscillator (LO) stage, as illustrated in Figure 1. The bandpass filter is centred on the intermediate frequency (IF) of the input signal, which we leave unspecified, but it would typically be around the usual 455 kHz. The LO frequency is set to mix the IF down to a centre frequency of  $1\frac{1}{4}$  times the bit rate. This we call the *nominal signal*, which is the input to the DSP unit. Its spectrum is shown in Fig-

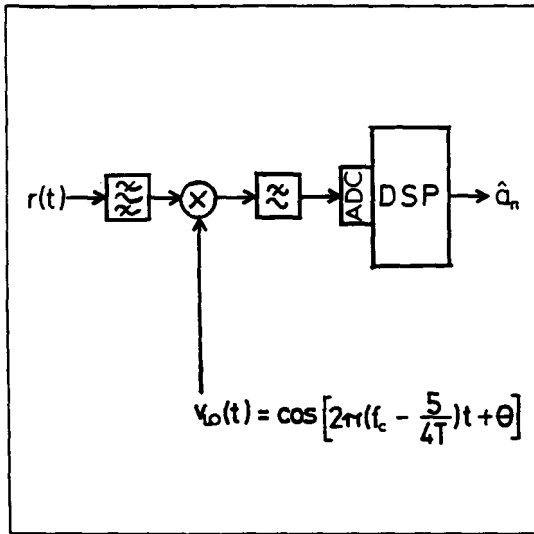


Figure 1: Analogue interface.

Figure 2 with the local oscillator frequency regarded as the origin.

Note that there is no requirement to synchronise the sampling instants to the bit intervals. A certain amount of leeway is also allowed in the exact number of samples per bit interval; the sampling rate need not be an integral multiple of the bit rate. This confers an important freedom to the overall system design which is not always found in DSP systems.

A practical note on the role of the bandpass filter: In the assumed receiver the LO frequency is below the input frequency. Therefore the lower cutoff frequency of the filter should coincide with this LO frequency  $f_{LO}$  in order to prevent image noise from mixing into the DSP system. Similarly, the upper cutoff frequency of the filter should be at  $f_{LO} + 2\frac{1}{2}$  times the bit rate, in order to limit the noise bandwidth to within the Nyquist frequency, as set by the sampling rate. Apart from limiting the noise bandwidth at the extreme upper and lower limits, the filter does not seek to minimise the noise into the demodulator. Figure 2 shows the MSK signal spectrum and the range of possible filter responses.

### III THE MSK SIGNAL

Several definitions of MSK exist, differing only in the coding applied to the data. For the purpose of this paper, a definition of MSK will be assumed in which the binary input data has a one-to-one mapping to the two signalling frequencies. This definition was first described by de Buda [2] as Fast Frequency Shift Keying, but we will keep to the more generic term, MSK.

Figure 3 illustrates how the MSK signal might be gener-

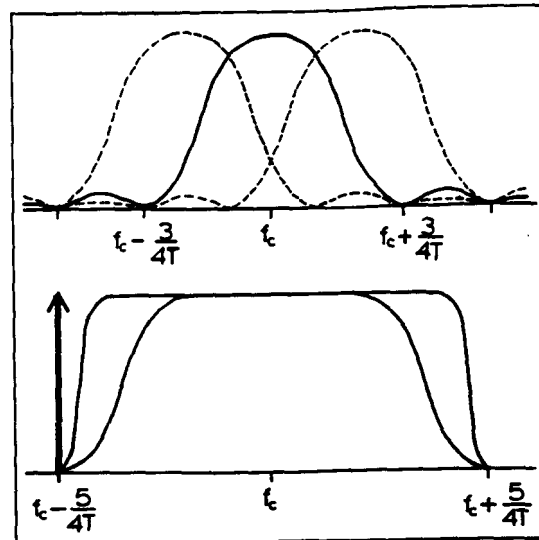


Figure 2: Bandpass filter response and IF MSK spectrum. The impulse represents the LO frequency.

ated. The current input data bit  $a_n \in \{-1, +1\}$  is passed through two level shifters (the  $\Sigma$  adders scale their output by a factor  $\frac{1}{2}$ ) to select one of two carrier signals, given by

$$\begin{aligned} s_1(t) &= \sin(2\pi f_1 t + \phi), \\ s_2(t) &= \sin(2\pi f_2 t + \phi). \end{aligned}$$

$f_1$  and  $f_2$  are the two signalling frequencies, and  $\phi$  is an arbitrary phase offset. The input  $b_n \in \{-1, +1\}$  toggles every bit interval. The combination of this inverting input and the differential encoder can be shown to maintain phase continuity of the transmitted output  $s(t)$  for any data input. The average carrier frequency for random data is  $f_c = (f_1 + f_2)/2$ , the symbol period is  $T$ , and the deviation ratio is  $|f_2 - f_1|T = \frac{1}{2}$  for MSK.

One essential characteristic of MSK is that the waveform will accumulate exactly half a cycle difference in phase in one bit interval between the two possible data states. The key to understanding the demodulator is to realise that whenever the nominal signal is switched to the lower signalling frequency it will be either exactly in phase or opposite phase to a suitably synchronised reference oscillator at the lower signalling frequency. Equally, when the input is switched to the higher signalling frequency that waveform will be either in-phase or anti-phase with a continuously running reference at this higher frequency. This is true for an MSK input signal of arbitrary carrier frequency and phase offset.

### IV DSP IMPLEMENTATION

The demodulator may best be described as running dual decision switched Costas loops [1] at the two signalling

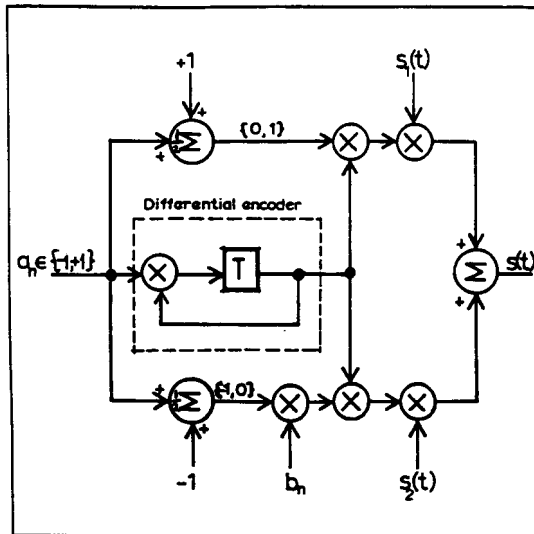


Figure 3: Generation of MSK signal.

frequencies, tracking the received signal in phase and frequency, and simultaneously demodulating it by correlation detection over two bit intervals. Figure 4 gives an overview.

#### A Data Detection

The correlator detectors are shown in Figure 5. The two reference oscillators  $r_1(t)$  and  $r_2(t)$  are locked in phase and frequency to the two possible carrier signals when the system is in lock. The integrators are reset at the start of every bit interval and sampled at the end of every bit interval, thus correlating the input signal with each of the reference waveforms. Since we expect the MSK signal to be either exactly in-phase or anti-phase with one of  $r_1(t)$  or  $r_2(t)$ , we expect to achieve either positive or negative correlation in one channel and a smaller correlation in the other, at the end of every bit interval.

Zero correlation does not generally obtain between sinusoidal signals whose difference in frequency accumulates to half a cycle in the integrating interval. But the MSK signal is deceptive in the respect that the two possible signalling frequencies are orthogonal over two bit intervals. In our decoder a decoding decision is based on correlation over the previous two bit intervals. It can be demonstrated that the outputs of the correlators are then orthogonal, when combined in the manner shown in Figure 5.

The input  $c_n \in \{-1, +1\}$  is derived from the bit timing clock and alternates its sign every bit interval, keeping track of the half cycle difference which accumulates between the two reference oscillators in that time.

The correlator samples are then summed over two bit

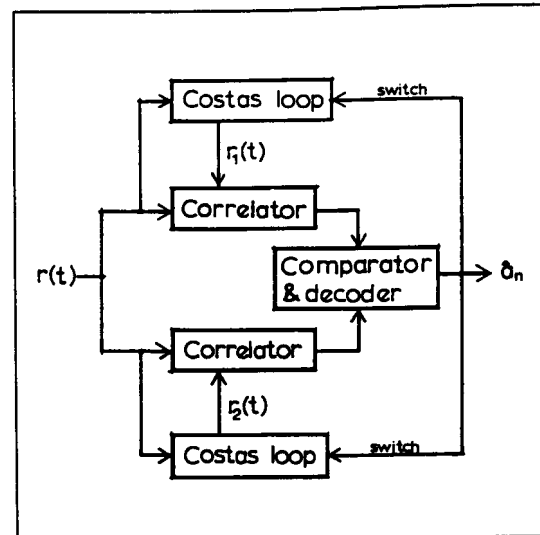


Figure 4: Demodulator block diagram.

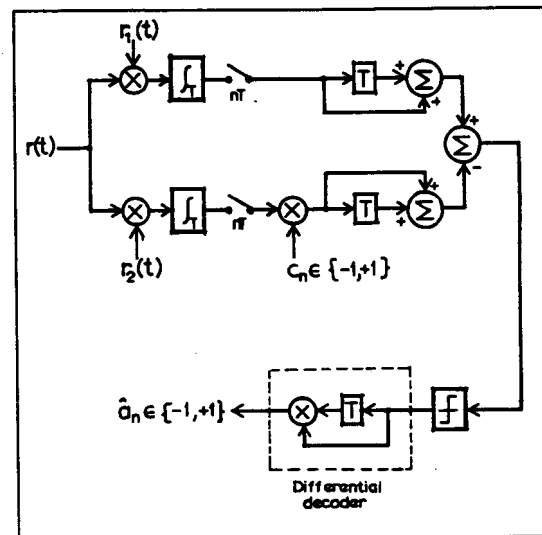


Figure 5: Data detection and decoding.

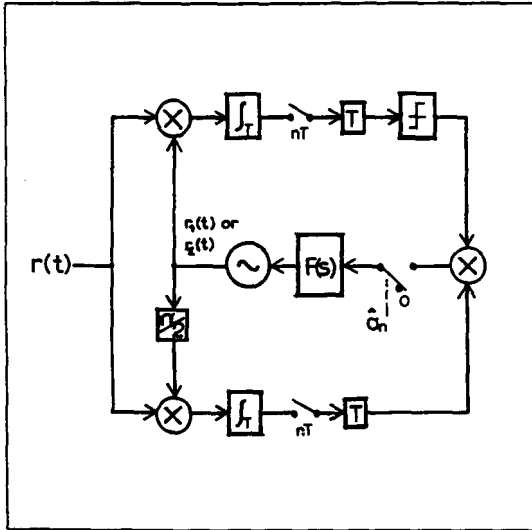


Figure 6: Decision switched Costas loop.

periods and compared, providing an optimal decision for the transmitted data  $a_n$  [8]. The output is then differentially decoded to give the final data estimate  $\hat{a}_n$ .

#### B Carrier Synchronisation

As described so far, the system is assumed to be in lock. In a practical implementation, the Costas loop oscillators would have to be steered to bring the signal within the lock-in range of the loops. In the simulation a simple zero crossing counting discriminator was used, which can certainly be improved upon.

A Costas loop [1] for one of the two channels is shown in Figure 6. The other channel has a similar loop. The voltage controlled oscillator (VCO) provides a reference signal  $r_1(t)$  or  $r_2(t)$ . The in-phase arm of the loop is identical to the correlator described before, and is in fact shared to reduce the receiver complexity.

From the Costas loop's viewpoint, the MSK signal contains the correct signalling frequency on average only half the time. For the rest of the time, the signal is tracked by the other loop. It is therefore necessary to inform it when to track and when to "free-wheel". The data estimate  $\hat{a}_n$  is used to switch the phase error through to the loop filter whenever the input is relevant. There is a dependence on the data being quasi-random or at least alternating: an indefinite run of unipolar data would prevent one of the loops from acquiring or holding lock.

The loop filter constants were found heuristically to give good tracking performance.

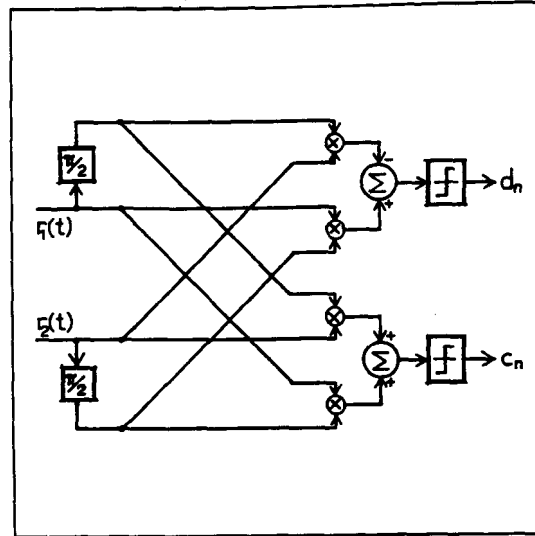


Figure 7: Clock recovery.

#### C Clock Recovery

The bit timing clock is recovered from the reference oscillators as shown in Figure 7. Multiplying the two reference signals together extracts an oscillating signal running at the difference frequency, which for MSK is exactly half the bit rate. The bit boundaries occur at the zero crossings of  $d_n$  while  $c_n$ , which is in quadrature with  $d_n$ , provides the alternating sign needed for data detection.

Note that the overall system is tightly integrated. Carrier recovery cannot take place unless a clock signal has been recovered and data is being decoded. The clock cannot be recovered unless the carrier has been recovered and data is being decoded. Data cannot be decoded unless both carrier and clock are being recovered! It is interesting that the demodulator can be made to 'pull itself up by its bootstraps'.

#### V PERFORMANCE

The system was tested in simulation for

- its response to phase or time steps;
- its response to frequency steps;
- its response to continuous phase modulation; and
- its BER in an additive white gaussian noise (AWGN) channel.

If the reference oscillators are assigned arbitrary incorrect phases while the system is in lock, it can be shown that the carrier and clock timings are simultaneously disturbed. In other words not only is the demodulator

not correlating correctly, but the decisions on when to read and reset the correlators and delays are incorrectly phased. We believe such a phase step to be a reasonable, if incomplete, way of testing demodulator performance in a rough phase distorting channel.

The demodulator shows an *unlimited* tolerance to step-like phase and timing perturbations. Both the carrier and clock states can be entirely wrong in a  $2\pi$  phase circle, yet data recovery is almost immediate and almost error free. The Costas loops are back to normal in about 40 bit intervals. They manage to hold lock through phase steps even in extremely noisy conditions with values such as 5dB for  $E_b/N_0$ .

Figure 8 shows a typical simulation run. The top trace is the sampled noisy input signal ( $E_b/N_0 = 7dB$ ), which has just been subjected to an abrupt phase step of  $90^\circ$ . The middle trace shows how the recovered bit timing clock and the two reference oscillator frequencies adjust to the new phase. The bottom two traces are the decoded and transmitted data values, showing some decoding errors.

The system copes with *frequency steps* without losing lock as long as the steps are within the loop bandwidth. The largest acceptable step was found to be about 2% of the bit rate in a mildly noisy channel with an  $E_b/N_0$  of 12dB. The loop bandwidth can be increased somewhat by changing the gains of the loop filter, but not much more could be gained without risking some instability. Figure 9 shows the system adjusting to a frequency step, with  $E_b/N_0 = 12dB$ .

Perhaps the toughest test to which to expose the demodulator is to impose sinusoidal *phase modulation* on the simulated AWGN channel. It was found that it can deal with peak phase offsets of at least  $40^\circ$  at any modulating frequency and with  $E_b/N_0 = 10dB$  throughout.

When the modulation rate is sufficiently slow, so that the loops can track the deviation, the peak deviation can be increased. At a modulation rate of 0.005 times the bit rate a peak deviation of  $120^\circ$  is easily tracked. Tracking performance is maintained even at the limits of the input frequency, with the average carrier frequency equal to  $\frac{3}{4}$  or  $1\frac{3}{4}$  times the bit rate.

It is also of interest to test the demodulator under very high noise conditions, not in the hope of getting good error performance, but to test that tracking is maintained. With  $E_b/N_0$  set to 3dB, the demodulator holds lock and tracks a phase modulated channel with a reduced peak deviation of  $20^\circ$  at any modulating frequency.

The BER performance is summarised in Figure 10.

These results are only from simulation at present. Practical work is being undertaken to test performance of a real modem on a working radio link to see if these encouraging results can be confirmed.

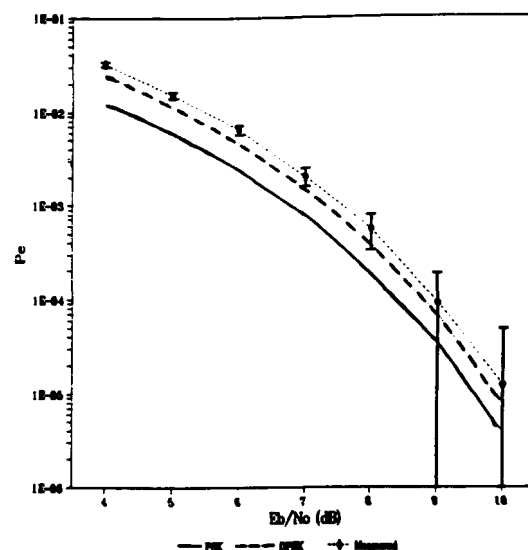


Figure 10: BER performance.

## VI CONCLUSION

The proposed MSK demodulator combines a detector/decoder of Massey's with a novel carrier and clock acquisition scheme. Simulation shows it to have substantial tolerance to phase and frequency perturbations, even at very low signal to noise ratios. It is robust against arbitrary phase or time steps in the received signal, from which it recovers, usually without data loss, within about 40 bit intervals. It survives unwanted phase modulation of any frequency up to a peak deviation of  $40^\circ$  without losing lock, as well as frequency steps in the signal of about 2% of the bit rate. The BER versus  $E_b/N_0$  performance is close to the antipodal coherent signalling benchmark, with an implementation loss of less than 0.2dB at a BER of  $10^{-4}$ .

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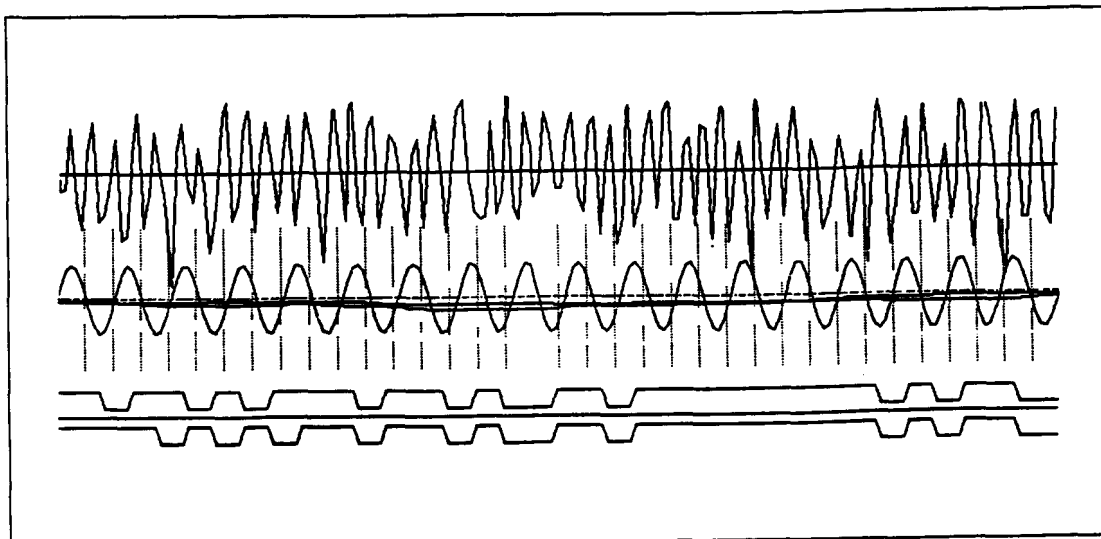


Figure 8: Simulation of phase step.

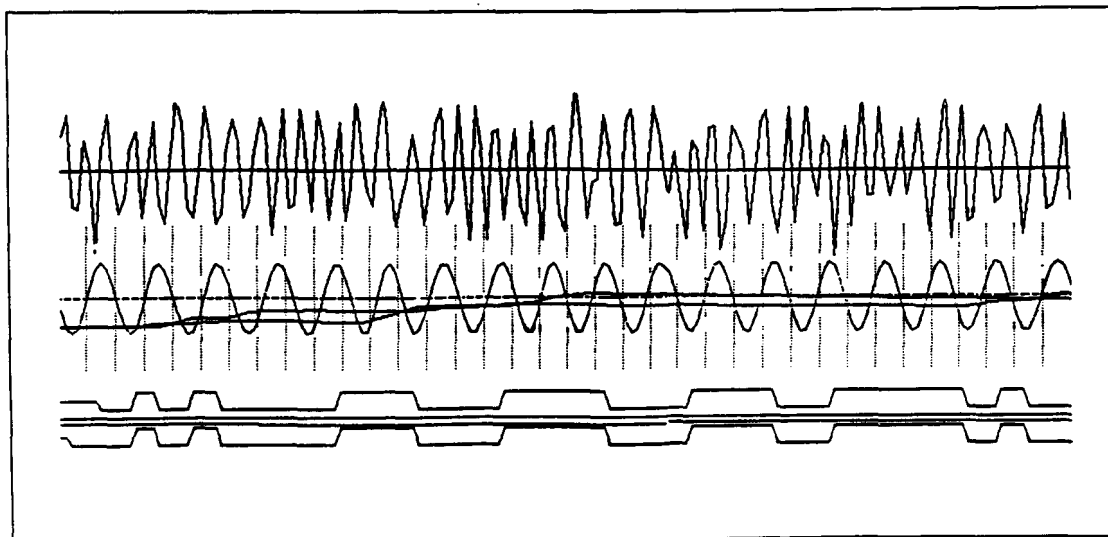


Figure 9: Simulation of frequency step.