## Pluto_MSK_Modem address map

- Absolute Address: 0x0
- Base Offset: 0x0
- Size: 0x43C00058

| Offset | Identifier | Name |
|---|---|---|
| 0x43C00000 | pluto_msk_regs | Pluto MSK Registers |

## pluto_msk_regs address map

- Absolute Address: 0x43C00000
- Base Offset: 0x43C00000
- Size: 0x58

MSK Modem Configuration and Status Registers

| Offset | Identifier | Name |
|---|---|---|
| 0x00 | Hash_ID_Low | Pluto MSK FPGA Hash ID - Lower 32-bits |
| 0x04 | Hash_ID_High | Pluto MSK FPGA Hash ID - Upper 32-bits |
| 0x08 | MSK_Init | MSK Modem Control 0 |
| 0x0C | MSK_Control | MSK Modem Control 1 |
| 0x10 | MSK_Status | MSK Modem Status 1 |
| 0x14 | Tx_Bit_Count | MSK Modem Status 2 |
| 0x18 | Tx_Enable_Count | MSK Modem Status 3 |
| 0x1C | Fb_FreqWord | Bitrate NCO Frequency Control Word |
| 0x20 | F1_FreqWord | FSK f1 NCO Frequency Control Word |
| 0x24 | F2_FreqWord | FSK f2 NCO Frequency Control Word |
| 0x28 | LPF_Config_0 | PI Controller Configuration and Low-pass Filter Configuration |
| 0x2C | LPF_Config_1 | PI Controller Configuration and Low-pass Filter Configuration |
| 0x30 | Tx_Data_Width | Modem Tx Input Data Width |
| 0x34 | Rx_Data_Width | Modem Rx Output Data Width |
| 0x38 | PRBS_Control | PRBS Control 0 |
| 0x3C | PRBS_Initial_State | PRBS Control 1 |
| 0x40 | PRBS_Polynomial | PRBS Control 2 |
| 0x44 | PRBS_Error_Mask | PRBS Control 3 |
| 0x48 | PRBS_Bit_Count | PRBS Status 0 |
| 0x4C | PRBS_Error_Count | PRBS Status 1 |
| 0x50 | LPF_Accum_F1 | F1 PI Controller Accumulator |
| 0x54 | LPF_Accum_F2 | F2 PI Controller Accumulator |

### Hash_ID_Low register

- Absolute Address: 0x43C00000

- Base Offset: 0x0
- Size: 0x4

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | hash_id_lo | r | 0xAAAA5555 | Hash ID Lower 32-bits |

**hash_id_lo field** Lower 32-bits of Pluto MSK FPGA Hash ID

**Hash_ID_High register**

- Absolute Address: 0x43C00004
- Base Offset: 0x4
- Size: 0x4

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | hash_id_hi | r | 0x5555AAAA | Hash ID Upper 32-bits |

**hash_id_hi field** Upper 32-bits of Pluto MSK FPGA Hash ID

**MSK_Init register**

- Absolute Address: 0x43C00008
- Base Offset: 0x8
- Size: 0x4

Synchronous initialization of MSK Modem functions, does not affect configuration registers.

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | init | rw | 0x1 | Init Enable |

**init field** 0 -> Normal modem operation 1 -> Initialize modem

**MSK_Control register**

- Absolute Address: 0x43C0000C
- Base Offset: 0xC
- Size: 0x4

MSK Modem Configuration and Control

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | ptt | rw | 0x0 | Push-to-Talk Enable |
| 1 | loopback_ena | rw | 0x0 | Modem Loopback Enable |
| 2 | rx_invert | rw | 0x0 | Rx Data Invert Enable |
| 3 | clear_counts | rw | 0x0 | Clear Status Counters |

**ptt field** 0 -> PTT Disabled 1 -> PTT Enabled

**loopback_ena field** 0 -> Modem loopback disabled 1 -> Modem loopback enabled

**rx_invert field** 0 -> Rx data normal 1 -> Rx data inverted

**clear_counts field** Clear Tx Bit Counter and Tx Enable Counter

**MSK_Status register**

- Absolute Address: 0x43C00010
- Base Offset: 0x10
- Size: 0x4

Modem status bits

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | demod_sync_lock | r | 0x0 | Demodulator Sync Status |
| 1 | tx_enable | r | 0x0 | AD9363 DAC Interface Tx Enable Input Active |
| 2 | rx_enable | r | 0x0 | AD9363 ADC Interface Rx Enable Input Active |

**demod_sync_lock field** Demodulator Sync Status - not currently implemented

**tx_enable field** 1 -> Data to DAC Enabled 0 -> Data to DAC Disabled

**rx_enable field** 1 -> Data from ADC Enabled 0 -> Data from ADC Disabled

**Tx_Bit_Count register**

- Absolute Address: 0x43C00014
- Base Offset: 0x14
- Size: 0x4

Modem status data

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data_req_count | rw | 0x0 | Tx Bit Count |

**data_req_count field** Count of data requests made by modem

**Tx_Enable_Count register**

- Absolute Address: 0x43C00018
- Base Offset: 0x18
- Size: 0x4

Modem status data

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data_req_count | rw | 0x0 | Tx Enable Count |

**data_req_count field** Number of clocks on which Tx Enable is active

**Fb_FreqWord register**

- Absolute Address: 0x43C0001C
- Base Offset: 0x1C
- Size: 0x4

Set Modem Data Rate

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

**F1_FreqWord register**

- Absolute Address: 0x43C00020
- Base Offset: 0x20
- Size: 0x4

Set Modem Data Rate

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### F2_FreqWord register

- Absolute Address: 0x43C00024
- Base Offset: 0x24
- Size: 0x4

Set Modem Data Rate

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### LPF_Config_0 register

- Absolute Address: 0x43C00028
- Base Offset: 0x28
- Size: 0x4

Configure PI controller and low-pass filter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | lpf_freeze | rw | 0x0 | Freeze the accumulator's current value |
| 1 | lpf_zero | rw | 0x0 | Hold the PI Accumulator at zero |
| 31:16 | lpf_alpha | rw | 0x0 | Lowpass IIR filter alpha |

**lpf_freeze field** 0 -> Normal operation 1 -> Freeze current value

**lpf_zero field** 0 -> Normal operation 1 -> Zero and hold accumulator

**lpf_alpha field** Value controls the filter rolloff

**LPF_Config_1 register**

- Absolute Address: 0x43C0002C
- Base Offset: 0x2C
- Size: 0x4

Configure PI controller and low-pass filter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 15:0 | i_gain | rw | 0x0 | Sets the integral gain of the PI controller integrator |
| 31:16 | p_gain | rw | 0x0 | Sets the proportional gain of the PI controller integrator |

**i_gain field** Integral gain value

**p_gain field** Proportional gain value

**Tx_Data_Width register**

- Absolute Address: 0x43C00030
- Base Offset: 0x30
- Size: 0x4

Set the parallel data width of the parallel-to-serial converter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 7:0 | data_width | rw | 0x8 | Modem input/output data width |

**data_width field** Set the data width of the modem input/output

**Rx_Data_Width register**

- Absolute Address: 0x43C00034
- Base Offset: 0x34
- Size: 0x4

Set the parallel data width of the serial-to-parallel converter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 7:0 | data_width | rw | 0x8 | Modem input/output data width |

**data_width field** Set the data width of the modem input/output

**PRBS_Control register**

- Absolute Address: 0x43C00038
- Base Offset: 0x38
- Size: 0x4

Configures operation of the PRBS Generator and Monitor

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | prbs_sel | rw | 0x0 | PRBS Data Select |
| 1 | prbs_error_insert | w | 0x0 | PRBS Error Insert |
| 2 | prbs_clear | w | 0x0 | Reserved |
| 3 | prbs_sync | w | 0x0 | PRBS Sync |

**prbs_sel field** 0 -> Select Normal Tx Data 1 -> Select PRBS Tx Data

**prbs_error_insert field** 0 -> No error insertion 1 -> Insert bit error in Tx data (both Normal and PRBS)

**prbs_clear field** Reserved

**prbs_sync field** 0 -> Normal Operation 1 -> Synchronize PRBS monitor

**PRBS_Initial_State register**

- Absolute Address: 0x43C0003C
- Base Offset: 0x3C
- Size: 0x4

PRBS Initial State

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Seed |

**config_data field** Sets the starting value of the PRBS generator

**PRBS_Polynomial register**

- Absolute Address: 0x43C00040
- Base Offset: 0x40
- Size: 0x4

PRBS Polynomial

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Polynomial |

**config_data field** Bit positions set to '1' indicate polynomial feedback positions

**PRBS_Error_Mask register**

- Absolute Address: 0x43C00044
- Base Offset: 0x44
- Size: 0x4

PRBS Error Mask

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Error Mask |

**config_data field** Bit positions set to '1' indicate bits that are inverted when a bit error is inserted

**PRBS_Bit_Count register**

- Absolute Address: 0x43C00048
- Base Offset: 0x48
- Size: 0x4

PRBS Bits Received

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | — | PRBS Bits Received |

**status_data field** Number of bits received by the PRBS monitor since last BER can be calculated as the ratio of received bits to errored-bits

**PRBS_Error_Count register**

- Absolute Address: 0x43C0004C
- Base Offset: 0x4C
- Size: 0x4

PRBS Bit Errors

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | — | PRBS Bit Errors |

**status_data field** Number of errored-bits received by the PRBS monitor since last sync BER can be calculated as the ratio of received bits to errored-bits

### LPF_Accum_F1 register

- Absolute Address: 0x43C00050
- Base Offset: 0x50
- Size: 0x4

Value of the F1 PI Controller Accumulator

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | — | PI Controller Accumulator Value |

**status_data field** PI Controller Accumulator Value

### LPF_Accum_F2 register

- Absolute Address: 0x43C00054
- Base Offset: 0x54
- Size: 0x4

Value of the F2 PI Controller Accumulator

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | — | PI Controller Accumulator Value |

**status_data field** PI Controller Accumulator Value