## Pluto_MSK_Modem address map

- Absolute Address: 0x0
- Base Offset: 0x0
- Size: 0x43C00090

| Offset | Identifier | Name |
|---|---|---|
| 0x43C00000 | pluto_msk_regs | Pluto MSK Registers |

## pluto_msk_regs address map

- Absolute Address: 0x43C00000
- Base Offset: 0x43C00000
- Size: 0x90

MSK Modem Configuration and Status Registers

| Offset | Identifier | Name |
|---|---|---|
| 0x00 | Hash_ID_Low | Pluto MSK FPGA Hash ID - Lower 32-bits |
| 0x04 | Hash_ID_High | Pluto MSK FPGA Hash ID - Upper 32-bits |
| 0x08 | MSK_Init | MSK Modem Control 0 |
| 0x0C | MSK_Control | MSK Modem Control 1 |
| 0x10 | MSK_Status | MSK Modem Status 0 |
| 0x14 | Tx_Bit_Count | MSK Modem Status 1 |
| 0x18 | Tx_Enable_Count | MSK Modem Status 2 |
| 0x1C | Fb_FreqWord | Bitrate NCO Frequency Control Word |
| 0x20 | TX_F1_FreqWord | Tx F1 NCO Frequency Control Word |
| 0x24 | TX_F2_FreqWord | Tx F2 NCO Frequency Control Word |
| 0x28 | RX_F1_FreqWord | Rx F1 NCO Frequency Control Word |
| 0x2C | RX_F2_FreqWord | Rx F2 NCO Frequency Control Word |
| 0x30 | LPF_Config_0 | PI Controller Configuration and Low-pass Filter Configuration |
| 0x34 | LPF_Config_1 | PI Controller Configuration Configuration Register 1 |
| 0x38 | Tx_Data_Width | Modem Tx Input Data Width |
| 0x3C | Rx_Data_Width | Modem Rx Output Data Width |
| 0x40 | PRBS_Control | PRBS Control 0 |
| 0x44 | PRBS_Initial_State | PRBS Control 1 |
| 0x48 | PRBS_Polynomial | PRBS Control 2 |
| 0x4C | PRBS_Error_Mask | PRBS Control 3 |
| 0x50 | PRBS_Bit_Count | PRBS Status 0 |
| 0x54 | PRBS_Error_Count | PRBS Status 1 |
| 0x58 | LPF_Accum_F1 | F1 PI Controller Accumulator |
| 0x5C | LPF_Accum_F2 | F2 PI Controller Accumulator |
| 0x60 | axis_xfer_count | MSK Modem Status 3 |
| 0x64 | Rx_Sample_Discard | Rx Sample Discard |

| Offset | Identifier | Name |
|---|---|---|
| 0x68 | LPF_Config_2 | PI Controller Configuration Configuration Register 2 |
| 0x6C | f1_nco_adjust | F1 NCO Frequency Adjust |
| 0x70 | f2_nco_adjust | F2 NCO Frequency Adjust |
| 0x74 | f1_error | F1 Error Value |
| 0x78 | f2_error | F2 Error Value |
| 0x7C | Tx_Sync_Ctrl | Transmitter Sync Control |
| 0x80 | Tx_Sync_Cnt | Transmitter Sync Duration |
| 0x84 | lowpass_ema_alpha1 | Exponential Moving Average Alpha |
| 0x88 | lowpass_ema_alpha2 | Exponential Moving Average Alpha |
| 0x8C | rx_power | Receive Power |

**Hash_ID_Low register**

- Absolute Address: 0x43C00000
- Base Offset: 0x0
- Size: 0x4

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | hash_id_lo | r | 0xAAAA5555 | Hash ID Lower 32-bits |

**hash_id_lo field** Lower 32-bits of Pluto MSK FPGA Hash ID

**Hash_ID_High register**

- Absolute Address: 0x43C00004
- Base Offset: 0x4
- Size: 0x4

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | hash_id_hi | r | 0x5555AAAA | Hash ID Upper 32-bits |

**hash_id_hi field** Upper 32-bits of Pluto MSK FPGA Hash ID

**MSK_Init register**

- Absolute Address: 0x43C00008
- Base Offset: 0x8
- Size: 0x4

Synchronous initialization of MSK Modem functions, does not affect configuration registers.

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | txrxinit | rw | 0x1 | Tx/Rx Init Enable |
| 1 | txinit | rw | 0x1 | Tx Init Enable |
| 2 | rxinit | rw | 0x1 | Rx Init Enable |

**txrxinit field** 0 -> Normal modem operation 1 -> Initialize Tx and Rx

**txinit field** 0 -> Normal Tx operation 1 -> Initialize Tx

**rxinit field** 0 -> Normal Rx operation 1 -> Initialize Rx

**MSK_Control register**

- Absolute Address: 0x43C0000C
- Base Offset: 0xC
- Size: 0x4

MSK Modem Configuration and Control

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | ptt | rw | 0x0 | Push-to-Talk Enable |
| 1 | loopback_ena | rw | 0x0 | Modem Loopback Enable |
| 2 | rx_invert | rw | 0x0 | Rx Data Invert Enable |
| 3 | clear_counts | rw | 0x0 | Clear Status Counters |
| 4 | diff_encoder_loopback | rw | 0x0 | Differential Encoder -> Decoder Loopback Enable |

**ptt field** 0 -> PTT Disabled 1 -> PTT Enabled

**loopback_ena field** 0 -> Modem loopback disabled 1 -> Modem loopback enabled

**rx_invert field** 0 -> Rx data normal 1 -> Rx data inverted

**clear_counts field** Clear Tx Bit Counter and Tx Enable Counter

**diff_encoder_loopback field** 0 -> Differential Encoder -> Decoder loopback disabled 1 -> Differential Encoder -> Decoder loopback enabled

**MSK_Status register**

- Absolute Address: 0x43C00010
- Base Offset: 0x10
- Size: 0x4

Modem status bits

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | demod_sync_lock | r | 0x0 | Demodulator Sync Status |
| 1 | tx_enable | r | 0x0 | AD9363 DAC Interface Tx Enable Input Active |
| 2 | rx_enable | r | 0x0 | AD9363 ADC Interface Rx Enable Input Active |
| 3 | tx_axis_valid | r | 0x0 | Tx S_AXIS_VALID |

**demod_sync_lock field** Demodulator Sync Status - not currently implemented

**tx_enable field** 1 -> Data to DAC Enabled 0 -> Data to DAC Disabled

**rx_enable field** 1 -> Data from ADC Enabled 0 -> Data from ADC Disabled

**tx_axis_valid field** 1 -> S_AXIS_VALID Enabled 0 -> S_AXIS_VALID Disabled

**Tx_Bit_Count register**

- Absolute Address: 0x43C00014
- Base Offset: 0x14
- Size: 0x4

Modem status data

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | tx_bit_counter | r | 0x0 | Tx Bit Count |

**tx_bit_counter field** Count of data requests made by modem

**Tx_Enable_Count register**

- Absolute Address: 0x43C00018
- Base Offset: 0x18
- Size: 0x4

Modem status data

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | tx_ena_counter | r | 0x0 | Tx Enable Count |

**tx_ena_counter field** Number of clocks on which Tx Enable is active

### Fb_FreqWord register

- Absolute Address: 0x43C0001C
- Base Offset: 0x1C
- Size: 0x4

Set Modem Data Rate

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### TX_F1_FreqWord register

- Absolute Address: 0x43C00020
- Base Offset: 0x20
- Size: 0x4

Set Modulator F1 Frequency

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### TX_F2_FreqWord register

- Absolute Address: 0x43C00024
- Base Offset: 0x24
- Size: 0x4

Set Modulator F2 Frequency

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### RX_F1_FreqWord register

- Absolute Address: 0x43C00028
- Base Offset: 0x28
- Size: 0x4

Set Demodulator F1 Frequency

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### RX_F2_FreqWord register

- Absolute Address: 0x43C0002C
- Base Offset: 0x2C
- Size: 0x4

Set Demodulator F2 Frequency

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | Frequency Control Word |

**config_data field** Sets the center frequency of the NCO as FW = Fn * 2^32/Fs, where Fn is the desired NCO frequency, and Fs is the NCO sample rate

### LPF_Config_0 register

- Absolute Address: 0x43C00030
- Base Offset: 0x30
- Size: 0x4

Configure PI controller and low-pass filter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | lpf_freeze | rw | 0x0 | Freeze the accumulator's current value |
| 1 | lpf_zero | rw | 0x0 | Hold the PI Accumulator at zero |
| 7:2 | prbs_reserved | w | 0x0 | — |
| 31:8 | lpf_alpha | rw | 0x0 | Lowpass IIR filter alpha |

**lpf_freeze field** 0 -> Normal operation 1 -> Freeze current value

**lpf_zero field** 0 -> Normal operation 1 -> Zero and hold accumulator

**lpf_alpha field** Value controls the filter rolloff

**LPF_Config_1 register**

- Absolute Address: 0x43C00034
- Base Offset: 0x34
- Size: 0x4

Configures PI Controller I-gain and divisor

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 23:0 | i_gain | rw | 0x0 | Integral Gain Value |
| 31:24 | i_shift | rw | 0x0 | Integral Gain Bit Shift |

**i_gain field** Value m of 0-16,777,215 sets the integral multiplier

**i_shift field** Value n of 0-32 sets the integral divisor as 2^-n

**Tx_Data_Width register**

- Absolute Address: 0x43C00038
- Base Offset: 0x38
- Size: 0x4

Set the parallel data width of the parallel-to-serial converter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 7:0 | data_width | rw | 0x8 | Modem input/output data width |

**data_width field** Set the data width of the modem input/output

**Rx_Data_Width register**

- Absolute Address: 0x43C0003C
- Base Offset: 0x3C
- Size: 0x4

Set the parallel data width of the serial-to-parallel converter

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 7:0 | data_width | rw | 0x8 | Modem input/output data width |

**data_width field** Set the data width of the modem input/output

**PRBS_Control register**

- Absolute Address: 0x43C00040
- Base Offset: 0x40
- Size: 0x4

Configures operation of the PRBS Generator and Monitor

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | prbs_sel | rw | 0x0 | PRBS Data Select |
| 1 | prbs_error_insert | w | 0x0 | PRBS Error Insert |
| 2 | prbs_clear | w | 0x0 | PRBS Clear Counters |
| 3 | prbs_manual_sync | w | 0x0 | PRBS Manual Sync |
| 15:4 | prbs_reserved | w | 0x0 | — |
| 31:16 | prbs_sync_threshold | w | 0x0 | PRBS Auto Sync Threshold |

**prbs_sel field** 0 -> Select Normal Tx Data 1 -> Select PRBS Tx Data

**prbs_error_insert field** 0 -> 1 : Insert bit error in Tx data (both Normal and PRBS) 1 -> 0 : Insert bit error in Tx data (both Normal and PRBS)

**prbs_clear field** 0 -> 1 : Clear PRBS Counters 1 -> 0 : Clear PRBS Counters

**prbs_manual_sync field** 0 -> 1 : Synchronize PRBS monitor 1 -> 0 : Synchronize PRBS monitor

**prbs_sync_threshold field** 0 : Auto Sync Disabled N > 0 : Auto sync after N errors

**PRBS_Initial_State register**

- Absolute Address: 0x43C00044
- Base Offset: 0x44
- Size: 0x4

PRBS Initial State

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Seed |

**config_data field** Sets the starting value of the PRBS generator

**PRBS_Polynomial register**

- Absolute Address: 0x43C00048
- Base Offset: 0x48
- Size: 0x4

PRBS Polynomial

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Polynomial |

**config_data field** Bit positions set to '1' indicate polynomial feedback positions

**PRBS_Error_Mask register**

- Absolute Address: 0x43C0004C
- Base Offset: 0x4C
- Size: 0x4

PRBS Error Mask

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | config_data | rw | 0x0 | PRBS Error Mask |

**config_data field** Bit positions set to '1' indicate bits that are inverted when a bit error is inserted

**PRBS_Bit_Count register**

- Absolute Address: 0x43C00050
- Base Offset: 0x50
- Size: 0x4

PRBS Bits Received

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | 0x0 | PRBS Bits Received |

**status_data field** Number of bits received by the PRBS monitor since last BER can be calculated as the ratio of received bits to errored-bits

**PRBS_Error_Count register**

- Absolute Address: 0x43C00054
- Base Offset: 0x54
- Size: 0x4

PRBS Bit Errors

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | 0x0 | PRBS Bit Errors |

**status_data field** Number of errored-bits received by the PRBS monitor since last sync BER can be calculated as the ratio of received bits to errored-bits

**LPF_Accum_F1 register**

- Absolute Address: 0x43C00058
- Base Offset: 0x58
- Size: 0x4

Value of the F1 PI Controller Accumulator

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | 0x0 | PI Controller Accumulator Value |

**status_data field** PI Controller Accumulator Value

**LPF_Accum_F2 register**

- Absolute Address: 0x43C0005C
- Base Offset: 0x5C
- Size: 0x4

Value of the F2 PI Controller Accumulator

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | status_data | r | 0x0 | PI Controller Accumulator Value |

**status_data field** PI Controller Accumulator Value

**axis_xfer_count register**

- Absolute Address: 0x43C00060
- Base Offset: 0x60
- Size: 0x4

Modem status data

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | xfer_count | r | 0x0 | S_AXIS Transfers |

**xfer_count field** Number completed S_AXIS transfers

**Rx_Sample_Discard register**

- Absolute Address: 0x43C00064
- Base Offset: 0x64
- Size: 0x4

Configure samples discard operation for demodulator

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 7:0 | rx_sample_discard | rw | 0x0 | Rx Sample Discard Value |
| 15:8 | rx_nco_discard | rw | 0x0 | Rx NCO Sample Discard Value |

**rx_sample_discard field** Number of Rx samples to discard

**rx_nco_discard field** Number of NCO samples to discard

**LPF_Config_2 register**

- Absolute Address: 0x43C00068
- Base Offset: 0x68
- Size: 0x4

Configures PI Controller I-gain and divisor

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 23:0 | p_gain | rw | 0x0 | Proportional Gain Value |
| 31:24 | p_shift | rw | 0x0 | Proportional Gain Bit Shift |

**p_gain field** Value m of 0-16,777,215 sets the proportional multiplier

**p_shift field** Value n of 0-32 sets the proportional divisor as 2^-n

**f1_nco_adjust register**

- Absolute Address: 0x43C0006C
- Base Offset: 0x6C
- Size: 0x4

Frequency offet applied to the F1 NCO

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data | r | 0x0 | F1 NCO Frequency Adjust |

**data field** Frequency offet applied to the F1 NCO

**f2_nco_adjust register**

- Absolute Address: 0x43C00070
- Base Offset: 0x70
- Size: 0x4

Frequency offet applied to the F2 NCO

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data | r | 0x0 | F2 NCO Frequency Adjust |

**data field** Frequency offet applied to the F2 NCO

**f1_error register**

- Absolute Address: 0x43C00074
- Base Offset: 0x74
- Size: 0x4

Error value of the F1 Costas loop after each active bit period

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data | r | 0x0 | F1 Error Value |

**data field** Error value of the F1 Costas loop after each active bit period

**f2_error register**

- Absolute Address: 0x43C00078
- Base Offset: 0x78
- Size: 0x4

Error value of the F2 Costas loop after each active bit period

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 31:0 | data | r | 0x0 | F2 Error Value |

**data field** Error value of the F2 Costas loop after each active bit period

**Tx_Sync_Ctrl register**

- Absolute Address: 0x43C0007C
- Base Offset: 0x7C
- Size: 0x4

Provides control bits for generation of transmitter synchronization patterns

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 0 | tx_sync_ena | rw | 0x0 | Tx Sync Enable |
| 1 | tx_sync_force | rw | 0x0 | Tx Sync Force |
| 2 | tx_sync_f1 | rw | 0x0 | Tx F1 Sync Enable |
| 3 | tx_sync_f2 | rw | 0x0 | Tx F2 Sync Enable |

**tx_sync_ena field** 0 -> Disable sync transmission 1 -> Enable sync transmission when PTT is asserted

**tx_sync_force field** 0 : Normal operation) 1 : Transmit synchronization pattern)

**tx_sync_f1 field** Enables/Disables transmission of F1 tone for receiver synchronization 0 : F1 tone transmission disabled 1 : F1 tone transmission enabled Both F1 and F2 can be enabled at the same time

**tx_sync_f2 field** Enables/Disables transmission of F2 tone for receiver synchronization 0 : F2 tone transmission disabled 1 : F2 tone transmission enabled Both F1 and F2 can be enabled at the same time

**Tx_Sync_Cnt register**

- Absolute Address: 0x43C00080
- Base Offset: 0x80
- Size: 0x4

Sets the duration of the synchronization tones when enabled

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 23:0 | tx_sync_cnt | rw | 0x0 | Tx sync duration |

**tx_sync_cnt field** Value from 0x00_0000 to 0xFF_FFFF. This value represents the number bit-times the synchronization signal should be sent after PTT is asserted.

**lowpass_ema_alpha1 register**

- Absolute Address: 0x43C00084
- Base Offset: 0x84
- Size: 0x4

Sets the alpha for the EMA

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 17:0 | alpha | rw | 0x0 | EMA alpha |

**alpha field** Value from 0x0_0000 to 0x3_FFFF represent the EMA alpha

**lowpass_ema_alpha2 register**

- Absolute Address: 0x43C00088
- Base Offset: 0x88
- Size: 0x4

Sets the alpha for the EMA

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 17:0 | alpha | rw | 0x0 | EMA alpha |

**alpha field** Value from 0x0_0000 to 0x3_FFFF represent the EMA alpha

**rx_power register**

- Absolute Address: 0x43C0008C
- Base Offset: 0x8C
- Size: 0x4

Receive power computed from I/Q ssamples

| Bits | Identifier | Access | Reset | Name |
|---|---|---|---|---|
| 22:0 | rx_power | r | 0x0 | Receive Power |

**rx_power field** Value that represent the RMS power of the incoming I;