

Review of AC timing for DDR

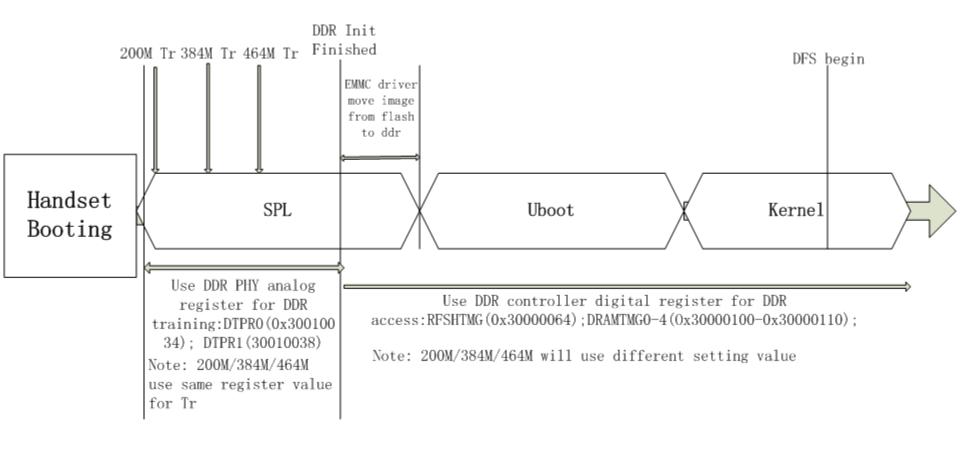


2014/05/21

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Overview





Overview for AC timing Rigester



Totally, 8 rigesters for AC timing ,they are:

0x30000064: RFSHTMG

0x30000100: DRAMTMG0

0x30000104: DRAMTMG1

0x30000108: DRAMTMG2

0x3000010C: DRAMTMG3

0x30000110: DRAMTMG4

0x30010034: DTPR0

0x30010038: DTPR1

DTPR0 and DTPR1 is just used for DDR training when DDR init

The rest RFSHTMG and DRAMTMG0~DRAMTMG4 is used for (SPL after DDR init, Uboot, Kernel/DFS)

Rigester Dump of 200M



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Rigester Dump of 384M



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Rigester Dump of 464M



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VAHB: 300000D0	005B0368 00000101 0000920A 00C20005 hg[Naannh3]		ENAHB:300100C0	00000000 0000000	0 0000000	
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VAHB:30000100	{OF1C2014 0004041F 0407090B 00504000)\$	EFNOPN	ENAHB:30010100	00000000 0000000		
VAHB:30000110	0A020A0A	ESSSNN				
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DDR PHY Analog Rigester DTPR0



- DTPR0=0x36916A6D
- DTPR0[1:0]: tMRD = 1(No use for training)
- DTPR0[4:2]: tRTP = 3 -> 3 tck (200m tck=5ns, 384m tck=2.6ns, 464m tck=2.15ns)
- DTPR0[7:5]: tWTR = 3 -> 3 tck (As ss test, it is too small)
- DTPR0[11:8]: tRP = 12 -> 12 tck
- DTPR0[15:12]: tRCD = 6 -> 6 tck (As ss test, it is too small)
- DTPR0[20:16]: tRAS = 17 -> 17 tck
- DTPR0[24:21]: tRRD = 4 -> 4 tck
- DTPR0[30:25]: tRC = 27 -> 27 tck
- DTPR0[31]: tCCD (only for DDR2 and DDR3)

DDR PHY Analog Rigester DTPR1



- DTPR1=0x193400A0
- DTPR1[1:0]: tAON/tAOFD = 0 (DDR2 only)
- DTPR1[2]: tRTW = 0 -> ddr ctl tRTW (if=1,ddr ctl tRTW+1)
- DTPR1[8:3]: tFAW = 20 -> 20 tck
- DTPR1[10:9]: tMOD (DDR3 only)
- DTPR1[11]: tRTODT (DDR3 only)
- DTPR1[15:12]: reversed
- DTPR1[23:16]: tRFC = 52 -> 52 tck
- DTPR1[26:24]: tDQSCK = 1 -> 1 tck
- DTPR1[29:27]: tDQSCKmax = 3 -> 3 tck
- DTPR1[31:30]: reversed

DDR Controller Digital Rigester



	RFSHTMG	DRAMTMG0	DRAMTMG1	DRAMTMG2	DRAMTMG3	DRAMTMG4
200	0X0018001B	0X0F0D0E09	0X0002020E	0X0407080B	0X00504000	0X05020505
384	0X002E0032	0X0F181B11	0X00040419	0X0407090B	0X00504000	0X08020808
464	0X0038003D	0X0F1C2014	0X0004041F	0Х0407090В	0X00504000	0X0A020A0A

For example:

UMCTL. RFHTMG(0X64) RFSHTMG[8:0]

200m: 0x0018001b 0X1B

• 384m: 0x00230032 0X32

466m: 0x0038003d 0X3D

DDR Controller Digital Rigester - Example



- DDR ctl side tRFC value is according to RFSHTMG[8:0], and the tRFC is below:
- tRFC = RFSHTMG[8:0] x tck
- So tRFC actiming value of 200mhz/384mhz/464mhz is:
- 200m: 0x1B x 5ns = 135 ns
- 384m: 0x32 x 2.6ns = 130 ns
- 466m: 0x3D x 2.15ns = 131 ns

Since there is too many AC timing for DDR controller digital register,
please Refer the Spec for the rest Rigester meaning.



Thank you!

