LDO Sleep Document

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Revision History

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| Revision | Date | Author | Description |
| 0.1 | 2014-06-30 | Kui.Wang | Initial LDO Sleep Work Flow |
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# Introduction

## Request & Purpose

## Definitions & Abbreviations

## Reference

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# Design Overview

## Concept

SPRD智能机芯片的功耗管理可以分为三个层次，第一个层次是各个Sub System组成功耗请求单元；第二个层次是有PMU构成的功耗管理单元；第三个层次是有PMIC构成的功耗管理执行单元。

具体参考文档：



## Function Blocks



## System WorkFlow

有2.2图示可知，功耗管理有三个方面的工作要做，本文档只关注PMU和PMIC如何配置。

PMU的主要作用是对各个SUB SYSTEM进行逻辑组合，进而控制PMIC的行为。

PMIC是对PMU传来的控制信号进行实际的功耗实施者。

LDO Sleep配置函数大体上分为一下几个部分

1、A DIE直接开关电的配置。

2、A DIE在Sleep是的状态(Lowpower or Shutdown)

3、A DIE各个LDOs被PMU控制的Layerout

4、D DIE PMU被各个SUB SYSTEM控制的layerout

5、各XTL/XTLBUF/PLL被各个SUB SYSTEM控制的layerout

6、XTL/XTLBUF/PLL/SUBSYS的上电时序配置。

7、Chip Service Pack的初始化。

### DCDC/LDO work config

正常工作的DCDC/LDO开关配置。以SC2723为例,一下两个寄存器就是配置开机默认是否打开LDO/DCDC的。有些寄存器是需要开机就打开的，sleep的时候会进sleep状态，有些是需要开机的时候是关闭的，用的时候才去打开，不用就关闭，完全由其使用的模块来控制。

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_DCDC\_PD\_RTCCLR,

//BIT\_LDO\_AVDD18\_PD\_RTCCLR |

BIT\_DCDC\_OTP\_PD\_RTCCLR |

//BIT\_DCDC\_WRF\_PD\_RTCCLR |

BIT\_DCDC\_GEN\_PD\_RTCCLR |

BIT\_DCDC\_MEM\_PD\_RTCCLR |

BIT\_DCDC\_ARM\_PD\_RTCCLR |

BIT\_DCDC\_CORE\_PD\_RTCCLR|

BIT\_LDO\_EMMCCORE\_PD\_RTCCLR |

BIT\_LDO\_EMMCIO\_PD\_RTCCLR |

BIT\_LDO\_RF2\_PD\_RTCCLR |

//BIT\_LDO\_RF1\_PD\_RTCCLR |

BIT\_LDO\_RF0\_PD\_RTCCLR |

BIT\_LDO\_VDD25\_PD\_RTCCLR |

BIT\_LDO\_VDD28\_PD\_RTCCLR |

BIT\_LDO\_VDD18\_PD\_RTCCLR |

BIT\_BG\_PD\_RTCCLR |

0

);

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_DCDC\_PD\_RTCSET,

BIT\_LDO\_AVDD18\_PD\_RTCSET |

//BIT\_DCDC\_OTP\_PD\_RTCSET |

BIT\_DCDC\_WRF\_PD\_RTCSET |

//BIT\_DCDC\_GEN\_PD\_RTCSET |

//BIT\_DCDC\_MEM\_PD\_RTCSET |

//BIT\_DCDC\_ARM\_PD\_RTCSET |

//BIT\_DCDC\_CORE\_PD\_RTCSET|

//BIT\_LDO\_EMMCCORE\_PD\_RTCSET |

//BIT\_LDO\_EMMCIO\_PD\_RTCSET |

//BIT\_LDO\_RF2\_PD\_RTCSET |

BIT\_LDO\_RF1\_PD\_RTCSET |

//BIT\_LDO\_RF0\_PD\_RTCSET |

//BIT\_LDO\_VDD25\_PD\_RTCSET |

//BIT\_LDO\_VDD28\_PD\_RTCSET |

//BIT\_LDO\_VDD18\_PD\_RTCSET |

//BIT\_BG\_PD\_RTCSET |

0

);

### DCDC/LDO deep sleep config。

Deep sleep的时候DCDC/LDO的状态控制选择，CTRL0与CTRL1寄存器是用来控制deep sleep的时候是否power down。能否power down首先要清楚DCDC/LDO的用途，看deep sleep的时候是否要开着，具体可以与硬件同事沟通。CTRL0与CTRL1寄存器是用来控制deep sleep的时候是否进入low power模式。设置low power模式要与Adie的同事还有硬件的同事沟通。

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_SLP\_CTRL0,

BIT\_SLP\_IO\_EN |

BIT\_SLP\_DCDC\_OTP\_PD/\_EN |

//BIT\_SLP\_DCDCGEN\_PD\_EN |

BIT\_SLP\_DCDCWPA\_PD\_EN |

//BIT\_SLP\_DCDCWRF\_PD\_EN |

BIT\_SLP\_DCDCARM\_PD\_EN |

BIT\_SLP\_LDOEMMCCORE\_PD\_EN |

BIT\_SLP\_LDOEMMCIO\_PD\_EN |

BIT\_SLP\_LDORF2\_PD\_EN |

//BIT\_SLP\_LDORF1\_PD\_EN |

BIT\_SLP\_LDORF0\_PD\_EN |

BIT\_SLP\_LDOVDD25\_PD\_EN |

//BIT\_SLP\_LDOVDD28\_PD\_EN |

//BIT\_SLP\_LDOVDD18\_PD\_EN |

0

);

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_SLP\_CTRL1,

BIT\_SLP\_LDO\_PD\_EN |

BIT\_SLP\_LDOLPREF\_PD\_EN |

BIT\_SLP\_LDOCLSG\_PD\_EN |

BIT\_SLP\_LDOUSB\_PD\_EN |

BIT\_SLP\_LDOCAMMOT\_PD\_EN |

BIT\_SLP\_LDOCAMIO\_PD\_EN |

BIT\_SLP\_LDOCAMD\_PD\_EN |

BIT\_SLP\_LDOCAMA\_PD\_EN |

BIT\_SLP\_LDOSIM2\_PD\_EN |

//BIT\_SLP\_LDOSIM1\_PD\_EN |

//BIT\_SLP\_LDOSIM0\_PD\_EN |

BIT\_SLP\_LDOSD\_PD\_EN |

BIT\_SLP\_LDOAVDD18\_PD\_EN |

0

);

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_SLP\_CTRL2,

//BIT\_SLP\_DCDC\_BG\_LP\_EN |

//BIT\_SLP\_DCDCCORE\_LP\_EN |

//BIT\_SLP\_DCDCMEM\_LP\_EN |

//BIT\_SLP\_DCDCARM\_LP\_EN |

//BIT\_SLP\_DCDCGEN\_LP\_EN |

//BIT\_SLP\_DCDCWPA\_LP\_EN |

//BIT\_SLP\_DCDCWRF\_LP\_EN |

//BIT\_SLP\_LDOEMMCCORE\_LP\_EN |

//BIT\_SLP\_LDOEMMCIO\_LP\_EN |

//BIT\_SLP\_LDORF2\_LP\_EN |

//BIT\_SLP\_LDORF1\_LP\_EN |

//BIT\_SLP\_LDORF0\_LP\_EN |

0

);

ANA\_REG\_SET(ANA\_REG\_GLB\_LDO\_SLP\_CTRL3,

//BIT\_SLP\_BG\_LP\_EN |

//BIT\_SLP\_LDOVDD25\_LP\_EN |

//BIT\_SLP\_LDOVDD28\_LP\_EN |

//BIT\_SLP\_LDOVDD18\_LP\_EN |

//BIT\_SLP\_LDOCLSG\_LP\_EN |

//BIT\_SLP\_LDOUSB\_LP\_EN |

//BIT\_SLP\_LDOCAMMOT\_LP\_EN |

//BIT\_SLP\_LDOCAMIO\_LP\_EN |

//BIT\_SLP\_LDOCAMD\_LP\_EN |

//BIT\_SLP\_LDOCAMA\_LP\_EN |

//BIT\_SLP\_LDOSIM2\_LP\_EN |

//BIT\_SLP\_LDOSIM1\_LP\_EN |

//BIT\_SLP\_LDOSIM0\_LP\_EN |

//BIT\_SLP\_LDOSD\_LP\_EN |

//BIT\_SLP\_LDOAVDD18\_LP\_EN |

0

);

### XTL Config

XTL信号线的配置，对于LDO/DCDC与哪些信号线相关联是以下几个寄存器控制的（以SC2723为例），EN0~EN3四个寄存器的bit位来关联XTL0，XTL1，EXT\_XTL0,对于的比如GEN0现在对应的XTL0，XTL1，EXT\_XTL0 Bit都置1了，表示GEN0若需要进入sleep则需要XTL0，XTL1，EXT\_XTL0都有sleep信号了。

注意:XTL 信号线绑定了后就无法ＰＤ。

示例：

ANA\_REG\_SET(ANA\_REG\_GLB\_PWR\_XTL\_EN0,

BIT\_LDO\_XTL\_EN |

BIT\_LDO\_GEN0\_EXT\_XTL0\_EN |

BIT\_LDO\_GEN0\_XTL1\_EN |

BIT\_LDO\_GEN0\_XTL0\_EN |

//BIT\_LDO\_GEN1\_EXT\_XTL0\_EN |

//BIT\_LDO\_GEN1\_XTL1\_EN |

//BIT\_LDO\_GEN1\_XTL0\_EN |

BIT\_LDO\_DCXO\_EXT\_XTL0\_EN |

BIT\_LDO\_DCXO\_XTL1\_EN |

BIT\_LDO\_DCXO\_XTL0\_EN |

//BIT\_LDO\_VDD18\_EXT\_XTL0\_EN |

//BIT\_LDO\_VDD18\_XTL1\_EN |

//BIT\_LDO\_VDD18\_XTL0\_EN |

//BIT\_LDO\_VDD28\_EXT\_XTL0\_EN |

//BIT\_LDO\_VDD28\_XTL1\_EN |

//BIT\_LDO\_VDD28\_XTL0\_EN |

0

);

对于XTL0，XTL1，EXT\_XTL0来说，EXT\_XTL0是表示外面的控制信号，XTL0的sleep信号只有ARM7，VCP1，VCP0，CP1,CP0都进deep sleep了XTL0才会有sleep信号。

CHIP\_REG\_SET(REG\_PMU\_APB\_XTL0\_REL\_CFG,

BIT\_XTL0\_ARM7\_SEL |

BIT\_XTL0\_VCP1\_SEL |

BIT\_XTL0\_VCP0\_SEL |

BIT\_XTL0\_CP1\_SEL |

BIT\_XTL0\_CP0\_SEL |

BIT\_XTL0\_AP\_SEL |

0

);

# Data Structure Design

## Data Structure Description

# Interfaces Design

## Public API Description

void init\_ldo\_sleep\_gr(void)

# Verification System

## Function Check List

*必须，模块的各项功能设计验证达标*

### Function Completeness

*模块功能的完备性*

### Performance

*模块性能参数*

### System Stability

*模块稳定性和对系统影响*

### Power Consumption

*对系统功耗影响*

## Function Test Items

*必须，模块的单元测试定义，以内存测试为例*

* Dependency

*依赖于其他那些模块*

DDR/MMU/Cache

* Interface

*基于实现的接口形态*

Posix Libc

* Command

*命令格式*

* Interaction

*测试过程是否需要人为交互，以及如何交互*

NO.

* Auto Test

*机器自动测试和输出支持*

All the test items can be automatic. The final results are in the command output.

* Cases

*标准单元测试样例*

## Integration Test Items

*集成测试环境和耦合验证描述*