

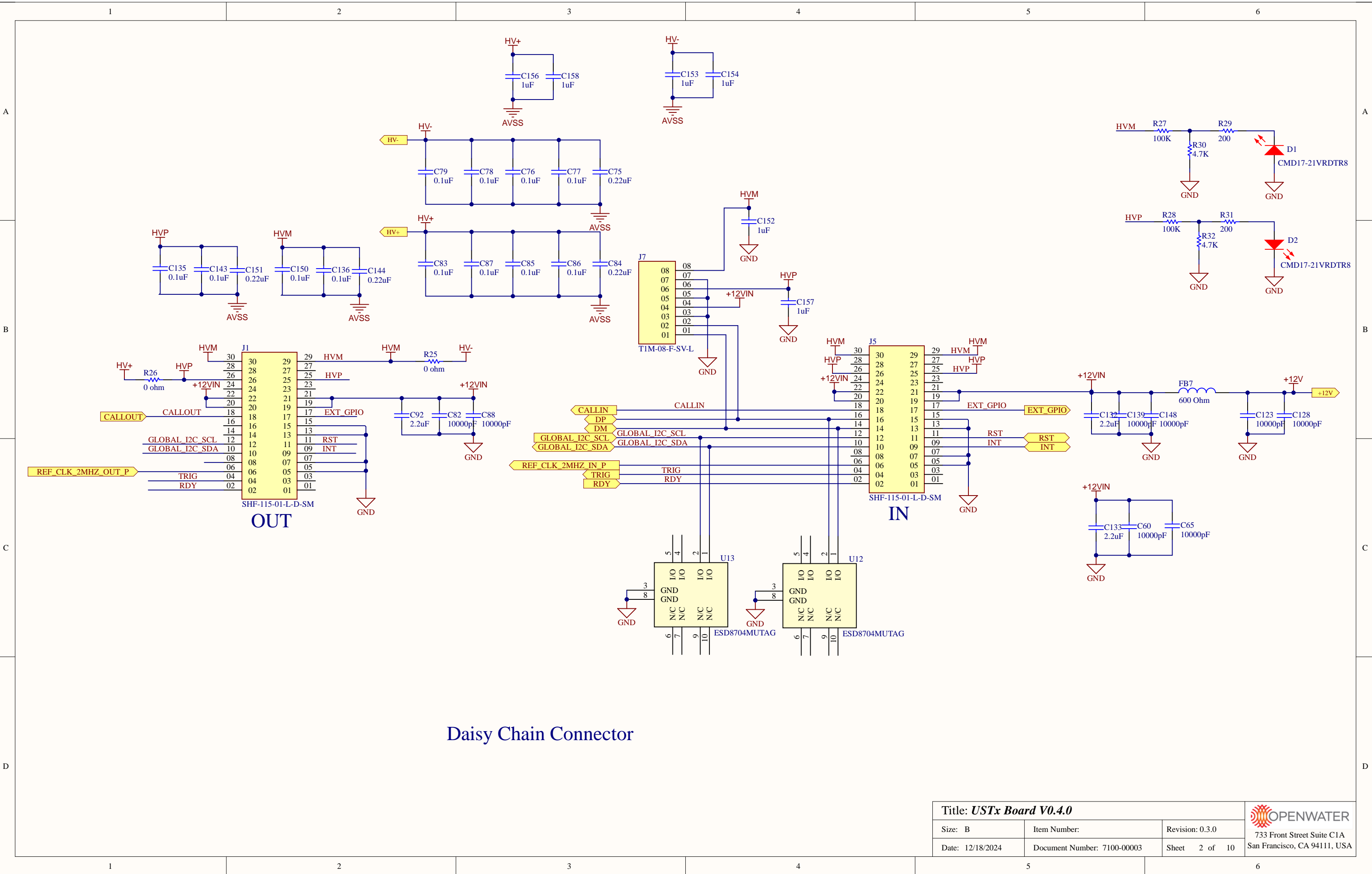


1		2		3		4		5		6	
A	<div>1. Cover</div> <div>2. Power Connector</div> <div>3. Transducer Connector</div> <div>4. RX Connector</div> <div>5. Power Supply</div> <div>6. Clock</div> <div>7. uController</div> <div>8. TX1</div> <div>9. TX2</div>							REVISION	DATE	HISTORY	AUTHOR
								0.4.0	12/20/2024	Initial Design	Henry Tang
B	<div>7100-00003</div> <div>USTx Board V0.4.1</div>										
C											
D											
1		2		3		4		5		6	
								Title: <i>USTx Board V0.4.0</i>		<div> OPENWATER</div> <div>733 Front Street Suite C1A San Francisco, CA 94111, USA</div>	
Size: B				Item Number:		Revision: 0.3.0					
Date: 12/18/2024				Document Number: 7100-00003		Sheet 1 of 10					

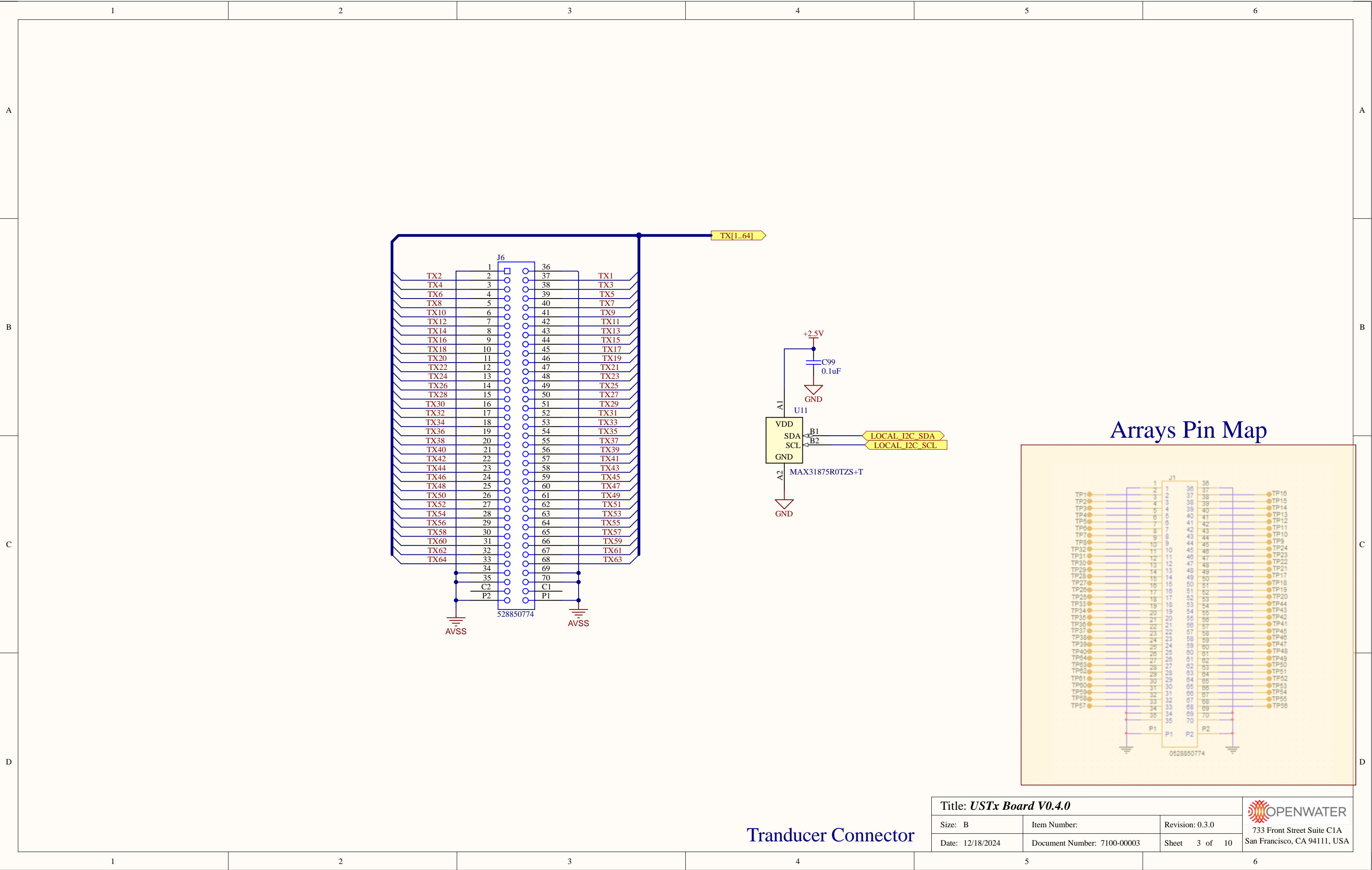
- 1. Cover
- 2. Power Connector
- 3. Transducer Connector
- 4. RX Connector
- 5. Power Supply
- 6. Clock
- 7. uController
- 8. TX1
- 9. TX2

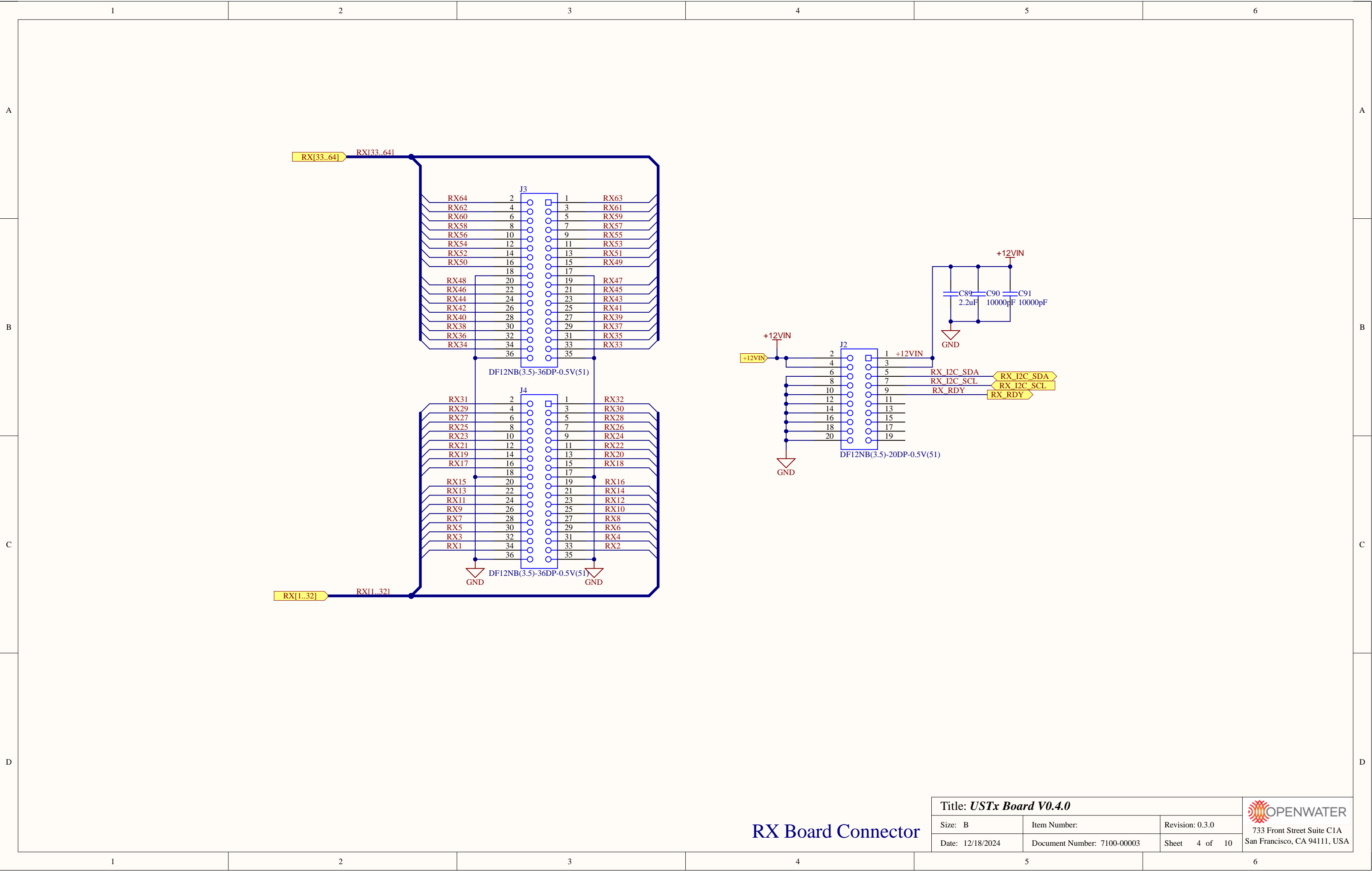
7100-00003
USTx Board V0.4.1

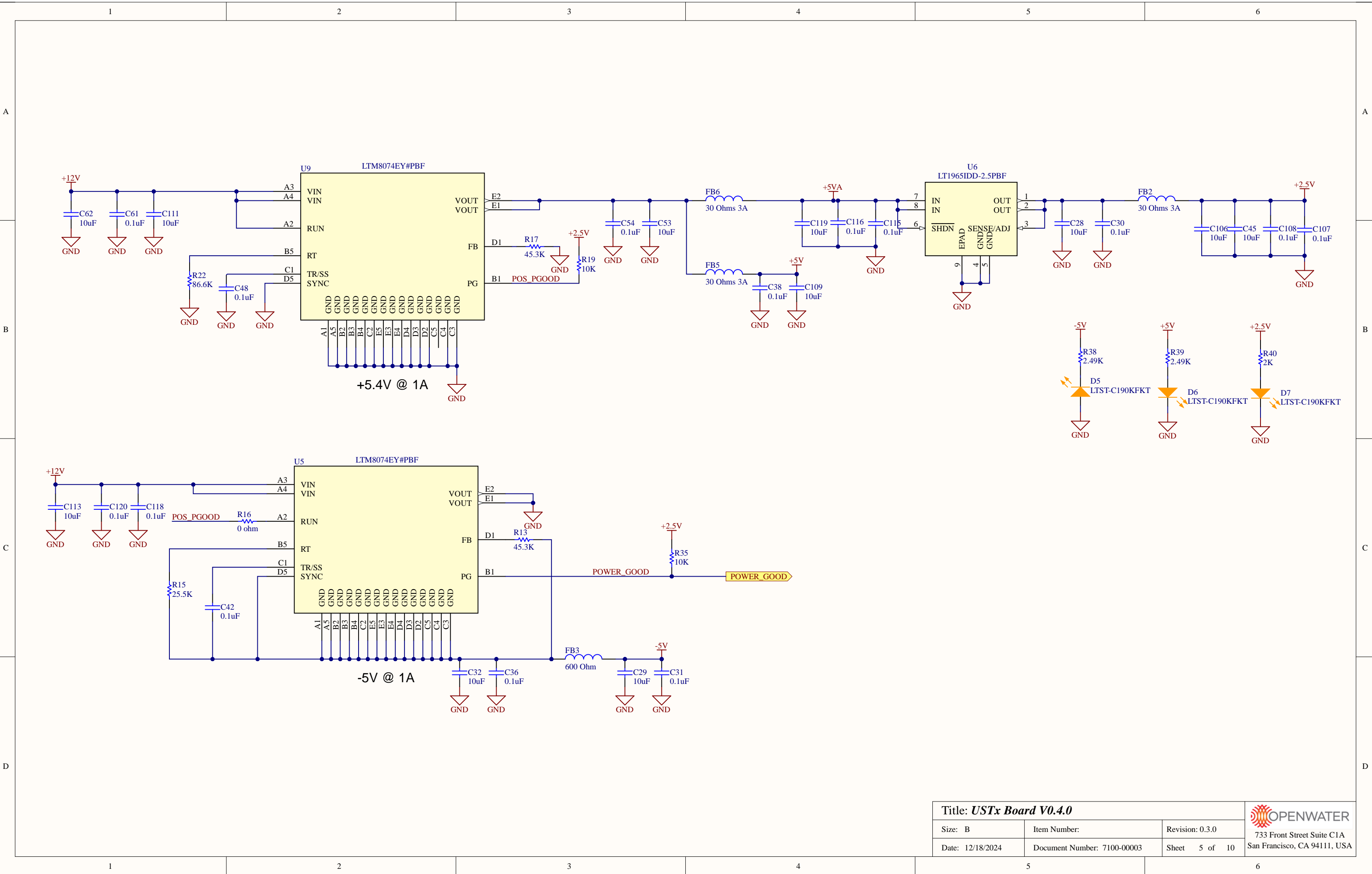
Title: <i>USTx Board V0.4.0</i>					 OPENWATER 733 Front Street Suite C1A San Francisco, CA 94111, USA
Size: B		Item Number:		Revision: 0.3.0	
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Daisy Chain Connector







A

B

C

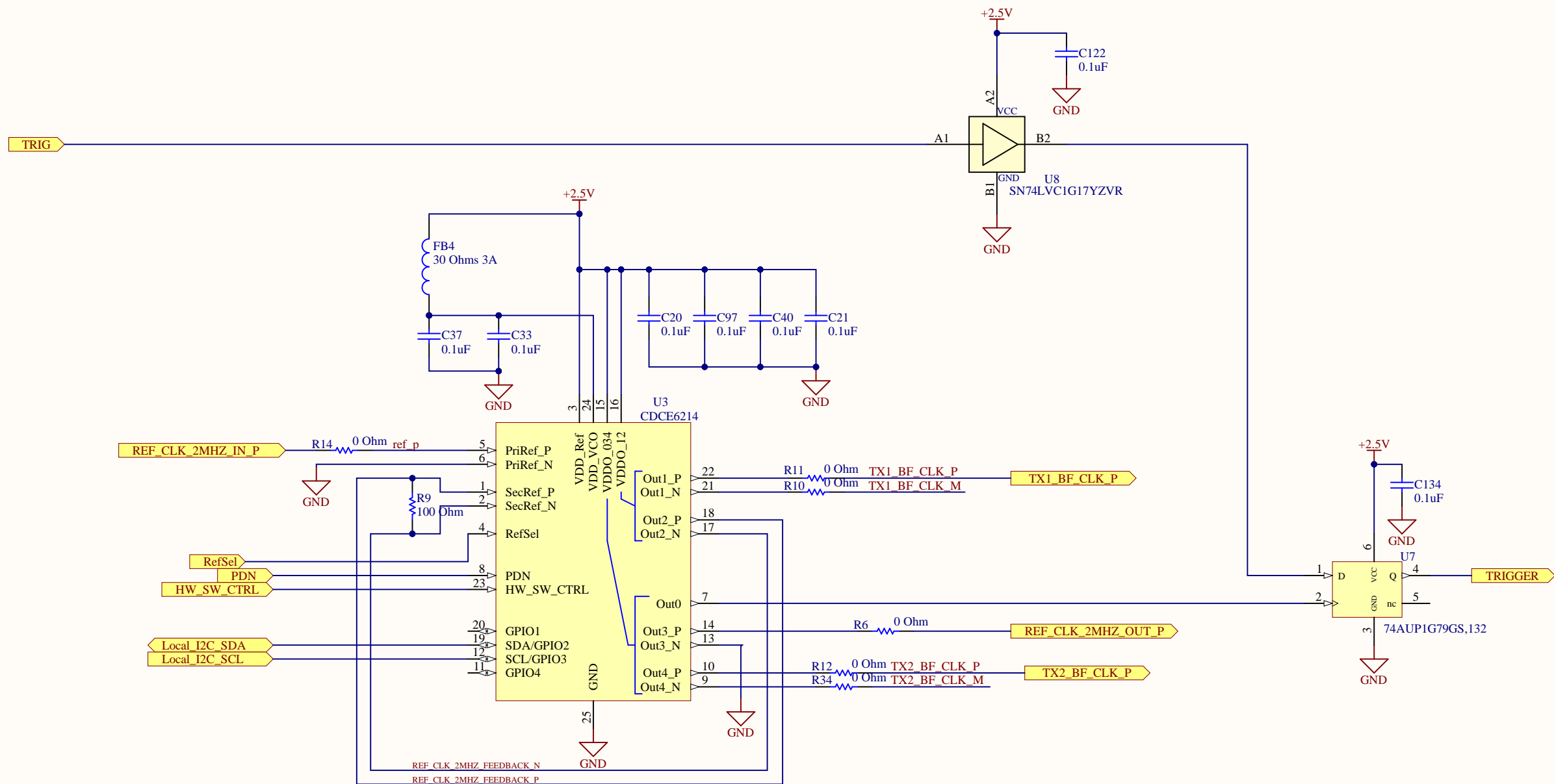
D

A

B

C

D



Configure CDCE6214 for External Zero-Delay PLL

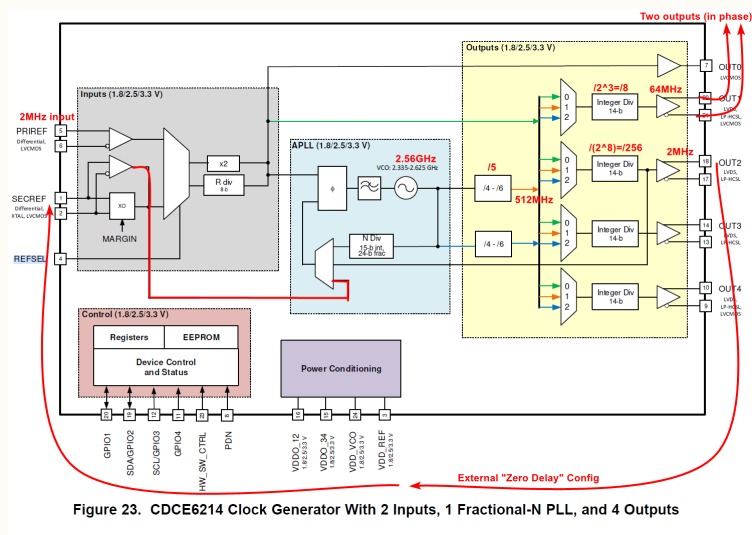


Figure 23. CDCE6214 Clock Generator With 2 Inputs, 1 Fractional-N PLL, and 4 Outputs

TIMING REQUIREMENT FOR ON-CHIP BEAM FORMING MODE

Parameter	Description	Value	Unit
$t_{WUP}^{(4)}$	Minimum time to apply TR_EN* signal before applying TR_BF_SYNC signal	8	μs
$W_{SYNC}^{(4)}$	Sync pulse width	10	20 BF_CLK clock cycles
$t_{SU_SYNC}^{(4)}$	Setup time related to TR_BF_SYNC (Differential) relative to the rising edge of the BF_CLK (Differential) clock	2.14	ns
	Setup time related to TR_BF_SYNC (Single-ended) relative to the rising edge of the BF_CLK (Single-ended) clock	1.27	ns
$t_{H_SYNC}^{(4)}$	Hold time related to TR_BF_SYNC (Differential) relative to the rising edge of the BF_CLK (Differential) clock	1.16	ns
	Hold time related to TR_BF_SYNC (Single-ended) relative to the rising edge of the BF_CLK (Single-ended) clock	1.57	ns
t_{PROP_INT}	From a 50% transition point of BF_CLK rising edge on which TR_BF_SYNC is latched to 1-V deviation at output; see Figure 44	15	ns

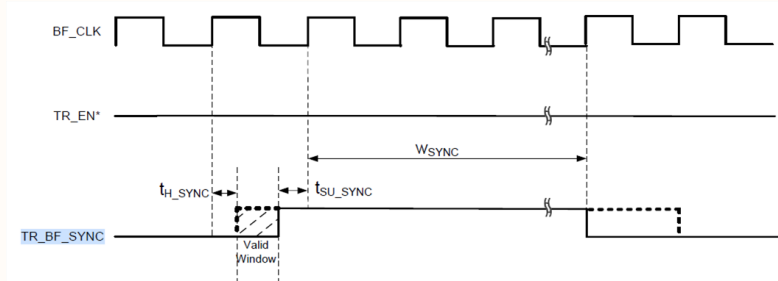


Figure 42. TR_BF_SYNC Timing Requirement for Static Trigger mode

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Revision: 0.3.0

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