Chip Support Library

Release Notes

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Contents

Release Notes

Chip Support Library version 3.3.0.17

Overview

This release of CSL contains peripheral programming (functional and register level) APIs. The list of modules supported in this release is listed in later sections. This set of APIs provides peripheral abstraction that can be used by higher layers of software.

This release includes:

- Compiled library of supported CSL modules for AM574x SOC
- Source
- API reference guide

New and Updated Features

The following is the naming convention for the various CSL prebuilt library files:

Default Directory	Library Name	Description
ti\csl\lib\<soc>\c66	ti.csl.ae66	66 ELF Little Endian Library
ti\csl\lib\<soc>\c66	ti.csl.intc.ae66	66 ELF Interrupt Controller Little Endian
ti\csl\lib\<soc>\armv7	ti.csl.aa15fg	A15 ELF Little Endian Library
ti\csl\lib\<soc>\m4	ti.csl.aem4	M4(IPU) ELF Little Endian Library
ti\csl\lib\<soc>\a53	ti.csl.aa53fg	A53 ELF Little Endian Library
ti\csl\lib\<soc>\a53	ti.csl.init.aa53fg	A53 Startup Library
ti\csl\lib\<soc>\r5f	ti.csl.aer5f	R5F ELF Little Endian Library

ti\csl\lib\<soc>\r5f	ti.csl.init.aer5f	R5F ELF Little Endian Library

Resolved IRs

Release 3.3.0.17 Updates

IR Parent/ Child Number	Severity Level	Description
PRSDK-8074	P3-Medium	csl: c6678 ecc test compilation fails
PRSDK-7682	P3-Medium	j721e: ICSSG instance 0 and 1 macros missing from csl
PRSDK-7524	P3-Medium	CSL: CLEC: Bug in CSL_clecClearEvent
PRSDK-7773	P3-Medium	csl: c66x:scancombined: klocwork warnings to be addressed
PRSDK-7907	P2-High	AM572x GP EVM eth0 is not working at 10Mbps
PRSDK-7436	P3-Medium	CSL csl_AM64_SoC_spec_191112_074644 MSRAM size does not match its alias
PRSDK-4475	P3-Medium	J7ES: Updates need to the clsr_psc.h
PRSDK-8004	P2-High	J7VCL CSL Serdes config update bug fix for Ethernet
PRSDK-7768	P2-High	CSL Serdes for J7ES QSGMII needs to enable RX 2x clock
PRSDK-7203	P3-Medium	CSL SerDes APIs use hard-coded physical address for MMR registers
PRSDK-7274	P2-High	CSL Serdes API needs to check for invalid phytype and refclk
PRSDK-7275	P3-Medium	CSL Serdes APIs needs to update fastsim enable API
PRSDK-7272	P2-High	CSL Serdes enable RX 2x clock for SGMII/QSGMII
PRSDK-7806	P2-High	TIMESYNC_INTRTR0_OUTL_n macros are set to zero
PRSDK-8117	P3-Medium	AM5728: CSL cache API always returns error
PRSDK-5856	P3-Medium	CSL: Arasan source files for mmcsd support - license needs to be fixed
PRSDK-7996	P3-Medium	AM654x CSL: PSILCFG registers for PDMA local to global translator

PRSDK-8136	P3-Medium	AM65xx: NAVSS bit field definitions missing from CSL
PRSDK-8099	P3-Medium	csl: j7200: Remove ICSS references as there are no ICSS instance for j7200
PRSDK-4844	P3-Medium	cslr_cpsw9.h CSL_CPSW9_CPSW_NU_CPSW_NU_ETH Macro Redefinition
PRSDK-7567	P3-Medium	CSL - CPSW9G SGMII CSL-R not aligned with IP spec
PRSDK-5397	P3-Medium	CSL ECC EMIF test hangs at "OCMC FULL ECC Mode" on ARM

Release 3.3.0.16 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-6349	Major	Resolve MISRA-C issues for OSPI, CPTS, FSS, Proxy, PSILCFG, PVU, RingAcc and UDMAP
PRSDK-5915	Major	Incorrect Keystone II Serdes Rx valid signal for PCIE interface using CSL
PRSDK-5346	Major	CSL: AM65X: A53 MSMC ECC examples are added
PRSDK-5000	Major	CSL: AM65x: Fixed the DMSC IRAM Size as per TRM
PRSDK-6204	Major	CSL: Integrate OMAPL1ex platform for ePWM module
PRSDK-5992	Major	CSL: update SYS config for OMAPL13x platform
PRSDK-5100	Major	CSL: AM65x: Update ESM/WDT test case memory map for DDR change

Release 3.3.0.15 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-5742	Major	Resolve divide by zero issue for MMCSD Clock setting

PRSDK-5958	Major	CSL: RTI WWD timer ESM Events specified wrongly
PRSDK-5345	Major	CSL: Added PMU Counter Set APIs
PRSDK-5695	Major	CSL: Support CBA Infrastructure for AM65x R5
PRSDK-5295	Major	CSL: Hyperbuf CSL-FL for AM65x is missing
PRSD-5736	Major	CSL: AM65x MCU R5 RAM Sizes and RAM IDs are incorrectly defined
PRSDK-5749	Major	CSL: Fixes AM65x R5 attributes for OSPI memory

Release 3.3.0.13 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-4478	Major	AM65XX R5F Data and Instruction cache enabled from CSL_init
PRSDK-4050	Major	CSL-OSPI: Support Phy enable
PRSDK-3403	Major	Fix for C++ compilation errors
PRSDK-4698	Major	Enable High speed mode for I2C
PRSDK-4529	Major	CSL UART: new API charGetNonBlocking2() API
PRSDK-4772	Major	CSL OSPI: Fix OSPI indirect mode write issue
PRSDK-4169	Major	CSL Examples: Add sciclient as dependent component for AM65X

Release 3.3.0.12 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-729	Minor	Add L1P/L2 EDC example code for Keystone device
PRSDK-4302	Major	A15 PMU APIs not included in the AM571x/AM572x CSL library
PRSDK-3669	Minor	C++ build failure for PDK LLD components

PRSDK-2274	Major	CSL startup library for AM65xx
PRSDK-2941	Major	Exception Handler Register API
PRSDK-3849	Major	AM65xx : PCIe Driver Baseline Support
PRSDK-2891	Major	CSLR: GPIO Register Macros Definition

Release 3.3.0.11 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-2194	Major	RTOS Installer script to autoset SDK_INSTALL_PATH
PRSDK-3642	Major	Clean up DCAN example code
PRSDK-3742	Major	for' loop for interrupt initialization in 'CSL_armGicInit()' is always executed only once
PRSDK-3308	Major	OMAPL138: MMCSD ARM & DSP tests intermittently pass
PRSDK-3257	Major	EVE support in PDK: enable features from pdk_01_08_00_16 (as in PSDK_VISION 3.1) for AM57xx
PRSDK-4102	Major	misra c issues present in csl
PRSDK-4120	Major	McASP LLD mcaspControlChan() API function w/ cmd argument Mcasp_IOCTL_CNTRL_SET_FORMAT_CHAN introduces channel swap
PDK-2388	Major	Update AMMU HAL to remove unused fields
PDK-2222	Major	Enhancements for semi hosting support on A15
PDK-2389	Major	OPP_PLUS support in PM and CSL for TDA2Ex

Release 3.3.0.10 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-3640	Major	CSLR bug to include correct UPP IP for OMAPL138 and K2G SoCs
PRSDK-3218	Major	Osal baremetal test arm: No response on UART while running with SBL on AM57xx

PRSDK-3562	Major	Update CSL DCAN example to send/receive multiple packets
PRSDK-2489	Major	Fix for C++ build errors on K2G platform
PRSDK-3356	Major	Fixed MISRAC issues
PRSDK-2819	Major	Networking API header files are not compatible with C++
PRSDK-3437	Major	Added DSS PLL CTRL CSL-RL macros for AM574x

Release 3.3.0.9 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-3190	Major	AM574x SoC integration
PRSDK-3205	Major	CSL/FL DCAN Loopback: Frame reception failed on AM3 platform
PRSDK-3134	Major	AM5726: DSP booted by remoteproc stalls Linux boot when CSL unlock/lock MMR_LOCK_2

Release 3.3.0.8 Updates

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-2345	Major	Bare metal CSL A15 interrupt support for K2G HS device
PRSDK-2856	Major	Top level makefile fails on am572x-evm platform
PRSDK-2786	Major	Parity is not enabled even if the UART lld calls UARTLineCharacConfig CSL-FL function
PRSDK-2967	Major	Unable to include csl_cpsw.h in application
PRSDK-2458	Major	Add SOC specific HW attr support for EMAC LLD v0 driver
PRSDK-2015	Major	PWM-FL support extension for AM335x/AM437x/AM57x/K2G

- K2G HS device support for A15 interrupt is added
  - Changed the default start address for the vectors for Keystone devices are assumed to start at beginning of MSMCSRAM (0x0C000000). The size reserved is 0x400 bytes starting from that location.

    The application needs to reserve this location for vectors for these devices when using CSL startup library. If application requires keeping the vectors in a non-default location, it can be done via linker command file by defining *__vector_base__* to desired start address:

    Example: For keystone devices such as K2G, if the vector location desired is say 0xC0E0000, then add below line in the application's linker command file: The vectors would be available from that location.

    __vector_base__= 0xC0E0000;

    Please note to reserve 0x400 from that new address in the linker command file for the vectors.
- Resolved IRs for this release is listed under Resolved IRs section.

Release 3.3.0.7 Updates

- Resolved IRs for this release is as below.

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-2422	Major	PRUSS LLD: provide API to configure PRUSS internal pinmux settings
PRSDK-2450	Major	OMAPL13x bare metal build failure due to missing assembly option '--strip_coff_underscore' for CSL
PRSDK-2448	Major	Adding data memory barrier function to CSL for A15.
PRSDK-2443	Major	Audio format for McASP/EDMA driver for OMAP-L137 is incorrect
PRSDK-2276	Major	PDK: EMAC Driver Support for OMAPL137/OMAPL138 and C6748
PRSDK-2378	Major	K2G PDK: SPI LLD all Frame Format (Polarity, Phase) is not working
PRSDK-1951	Major	CSL: Remove hw_pwmss.h from AM57x soc folder and move to already existing ti/csl/cslr_pwmss.h
PRSDK-2450	Major	OMAPL13x baremetal build failure due to missing assembly option '--strip_coff_underscore' for CSL
PRSDK-1102	Major	TI RTOS SPI: SPI DMA Mode Support for Keystone

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-2020	Major	SPI Interrupt mode operation is not functional on OMAPL13x platform
PRSDK-2366	Major	CSL: Missing EDMA shift/mask definitions for SYNCDIM and STATIC fields
PRSDK-2131	Major	PDK support for DRA72x
PRSDK-1266	Major	UART LLD Rx trigger level user configurable
PDK-1755	Major	M4 SOC defines doesn't define EDMA base address
PRSDK-2187	Major	C6678 CSL CPTS module using the wrong version

Release 3.3.0.6 Updates

- Resolved IRs for this release is as below.

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-1764	Major	Update PCIe CSL Serdes config to match v20.6, VERGH update
PRSDK-1769	Major	Enable INTC support for DRA7XX devices
PRSDK-1518	Major	Control driver support for OMAPL137/OMAPL138 and C6748 added
PRSDK-1805	Major	C++ Compilation support
PRSDK-2022	Major	Fix CSL_MSGMGRQUEUEPROXY_REG macro
PRSDK-998	Major	McSPI RTOS: TCS parameter of McSPI Ip present in McSPI_ChxConf should be exposed in interface
PRSDK-2034	Major	Bug in QSPISetPreScalar CSL function to modify QSPI clock
PRSDK-1716	Major	MMCSD CSL-FL baremetal examples have logical bugs
PRSDK-1974	Major	MMCSD driver support for OMAPL137/OMAPL138 and C6748
PRSDK-563	Major	K2G SPI reads incorrectly when booted in QSPI-96 mode

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-1849	Major	GPIO_read returns incorrect value for AM devices
PRSDK-1901	Major	Fixed CSL_intcCombinedEventEnable() bug to enable a particular event

Release 3.3.0.5 Updates

- Resolved IRs for this release is as below.

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-839	Major	klocwork bug introduced due to version update from 10.2.1 to 11.1.0
PRSDK-781	Major	Klocwork report for IPs : UART, I2C, SPI, McASP and MMCSD
PRSDK-851	Major	Edma example code fails when tcc is above 32
PRSDK-954	Major	CSL: EDMA V1 API EDMA3RequestChannel enabling the wrong interrupt
PRSDK-1074	Major	Memory Barrier implementation in HW_ macros is ineffective when compiling with TI's ARM compiler
PRSDK-1078	Major	Remove unwanted waits in TI RTOS Driver IPs - I2C, UART
PRSDK-1086	Major	K2G I2C LLD Slave mode support
PRSDK-1316	Major	Wrong Regster Macros in K2G GPIO CSL-R
PRSDK-1447	Major	Update V1 version of csl_mdioAux.h with missing functions.
PRSDK-1545	Major	CSL: csl ARM GIC Aux implementation does not work with csl init library
PRSDK-1624	Major	CSL: Add Timer IP to AM3/AM4 CSL library

Release 3.3.0.4 Updates

- Resolved IRs for this release is listed as below.

IR Parent/ Child Number	Severity Level	IR Description

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-1052	Major	Renamed csl_a15init to csl_init
PRSDK-960	Major	Am572x a15 interrupt is triggered only the first time
PRSDK-961	Major	armgic interrupt line 16,17,18,19 do not trigger after csl armgic initialization
PRSDK-966	Major	am57xx m4 interrupt line 48 triggers even after disabling it
PRSDK-948	Major	Enabling CSL-FL for McASP on K2G
PRSDK-1075	Major	CSL A15 interrupt code is wrongly using Intc line no as GIC id
PRSDK-1101	Major	CSL: API to get ARM GIC ID for a given IRQ Input Line
PRSDK-685	Major	PDK ICSS CSL organization/naming does not reflect ICSS IP revision changes
PRSDK-996	Major	TI RTOS: UART - Number of byte read in case of timeout
PRSDK-865	Major	CSL: Baremetal Cache & AMMU routines for Cortex-M4 as a part of CSL

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Release 3.3.0.3 Updates

- CSL bare-metal examples for AM572x and AM571x
- CSL to support i2c, spi, gpio, uart version speficic layers.
- Resolved IRs for this release are listed as below:

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-818	Major	software and the TRM definition of the QSPI word length in the QSPI_SPI_CMD_REG register doesn`t match
PRSDK-539	Major	CSL_a15ReadCoreId returns incorrect results

Release 3.3.0.2 Updates

- K2G merge to Common CSL to support
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00119536	Major	Incorrect PCIE outbound register overlay in Keystone I/II devices CSL code
SDOCM00121249	Major	SEC_MGR register definitions (cslr_sec_mgr.h) in CSL package needs to be removed from the PDK package
SDOCM00120885	Major	Wrong definitions of CSL_CGEM_IDMA1_COUNT_COUNT_SHIFT and CSL_CGEM_IDMA1_COUNT_COUNT_MASK

Release 3.3.0.1 Updates:

- Common CSL to support AM571x, AM572x and KeyStone devices.
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00117947	Major	CSL code accesses DRAEH register in EDMA CC0 and causes memory protection exception on Keystone 1
SDOCM00117869	Major	Keystone II A15 CSL library is not supported
SDOCM00102018	Minor	C6657 CSL CHIP_PIN_CONTROL_0 address is wrong
SDOCM00100228	Major	CSL cache APIs does not include workaround for advisory 6.
SDOCM00097896	Minor	Update CSL cache APIs to support write through functionality
SDOCM00094196	Minor	Problem to enable HW prefetch perf counters with CSL
SDOCM00119865	Major	Update CSL Serdes restore default API for PHY-A
SDOCM00118436	Major	tap offsets are not initialized before passing to CSL_Serdes_DLEV_Patch() in CSL_SerdesLaneEnable

Migration:

- Migration information for CSL from Processor SDK 3.2.0 release
  - Starting CSL Release 3.3.0.6 version,

- Unions and bit field structures in QSPI are removed in the default build to adhere to MISRAC. They are now under macro "ifdef QSPI_H_BACKWARD_COMPATIBLE_CHG" in file src\ip\qspi\V1\ qspi.h. The driver does not define this macro by default.

- Migration information for CSL from BIOS-MCSDK 2.1.2 release
  - SOC_C6657 needs to be defined for including CSL header files for C6657 PDK
  - SOC_C6678 needs to be defined for including CSL header files for C6678 PDK
  - Top level cslr_pcie*.h needs to be changed to include cslr_pcie.h
  - cslr_sgmii.h, csl_sgmii.h renamed to cslr_cpsgmii.h and csl_cpsgmii.h respectively.
  - following files are not supported from the top level CSL folder (ti/csl)
    - csl_mpuAux.h
    - csl_memprot.h
    - csl_memprotAux.h
    - csl_pllcAux.h
    - csl_cp_tracer.h
    - cslr_cpsw_3gf.h and cslr_cpsw_3gfss_s.h
    - csl_cpsw_3gf.h, csl_cpsw_3gfAux.h, csl_cpsw_3gfssAux.h, csl_cpsw_3gfss_s.h
  - Top level csl_cpsw_3gfAux.h files are substituted with csl_cpswAux.h and csl_cpsw_3gfssAux.h files are substituted with csl_cpswAux.h
  - Top level csl(r)_cpsw_3gf*.h files are substituted with csl(r)_cpsw.h and csl(r)_cpsw_ss_s.h files respectively and also all the definitions regarding 3gf are renamed as below.
    - Rename CSL_CPSW_3GF_XXXXXX to CSL_CPSW_XXXXXX
- Migration information for CSL from MCSDK 3.1.4 release
  - Renamed “ti/csl/device” folder to “ti/csl/soc” – hence any include header files as “ti/csl/device/k2?/src/xxxx.h” needs to be changed to “ti/csl/soc/k2?/src/xxxx.h”
  - Top level include files for “bcp” are moved under “ti/csl/src/ip/bcp/V0” folder, except for cslr_bcp.h
  - Top level include files for “iqn2” are moved under “ti/csl/src/ip/bcp/V0” folder, except for cslr_iqn2.h

- Top level include files for “rac” are moved under “ti/csl/src/ip/rac/V0” folder, except for csl_rac.h
- Top level include files for “tac2” are moved under “ti/csl/src/ip/tac2/V0” folder, except for csl_tac2.h
- Top level include files for “aif2” are moved under “ti/csl/src/ip/aif2/V0” folder, except for csl_aif2.h and cslr_aif2.h
- Deprecated top level cslr_cpsw_5gf*.h files which was there for backwards compatibility and also all the definitions regarding 5gf are renamed as below.
    - Rename CSL_CPSW_5GF_XXXXXX to CSL_CPSW_XXXXXX
- Top level cslr_pcie*.h needs to be changed to include cslr_pcie.h
- Removed support for wiz8b8sb header files.

- Migration information for CSL from Processor SDK 2.0.0 release
    - None

Release 3.3.0.0 Updates:

- First Release to support AM571x and AM572x SOCs
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00114000	Major	Updated csl serdes flow for all serdes K2 peripherals

Known Issues / Limitations

The release has undergone limited testing on simulator. Current Known issues at the time of release include:

IR Parent/ Child Number	Severity Level	IR Description

Licensing

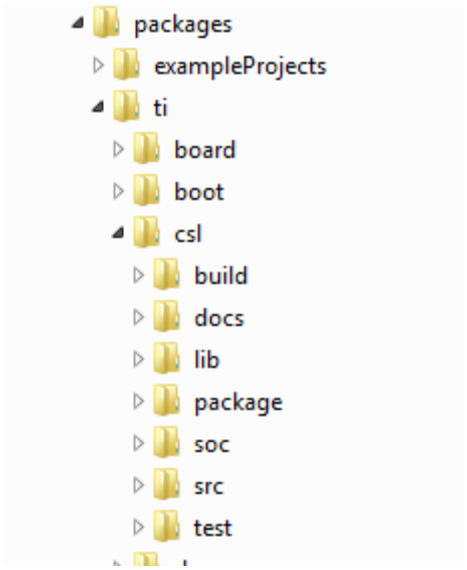
BSD Licensing

Delivery Package

Package is delivered as full source release in tar format.

Directory Structure

Following is the directory structure after CSL tar package is extracted.



Instruction for RTSC getLibs

In order to retrieve CSL library for a device using getLibs following line would be required in RTSC configuration file.

```
/* Load and use the CSL package */
var Csl = xdc.loadPackage('ti.csl.device.am572x.c66');
```

Replace k2k with the appropriate device name for the library being included

Customer Documentation List

Table 1 lists the documents that are accessible through the **/docs** folder on the product installation CD or in the delivery package.

Table 1 Product Documentation included with this Release

Document #	Document Title	File Name
1	API documentation (generated by Doxygen)	csl/docs/csldocs.chm