OptTrot

Circuit synthesis

Kim, Hyunseong

GIST

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Part I

Time evolution over Pauli Frame

Introduction

Quantum circuit

Some basic properties of quantum circuit.

- Each line is spin 1/2 system.

$$|\psi\rangle = \cos(\theta/2)\,|\uparrow\rangle + e^{i\phi}\sin(\theta/2)\,|\downarrow\rangle$$

- Usually, the arrow notations are represented with binary zero-one notation.

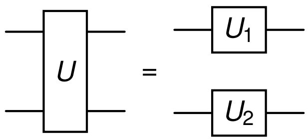
$$|\uparrow\rangle \to |0\rangle\,, |\downarrow\rangle \to |1\rangle$$

- Time direction: From left to right, $|\psi\rangle\ \text{—}\boxed{U}\text{—}\ |\phi\rangle \ \leftrightarrow |\phi\rangle = U\,|\psi\rangle$.
- Each gate represents n qubit operator = 2^n size unitary matrix.

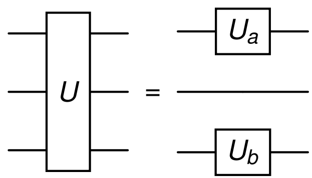
$$U = \begin{bmatrix} c_0 + c_3 & c_1 - ic_2 \\ c_1 + ic_2 & c_0 - c_3 \end{bmatrix}$$

- It represents a quantum algorithm, and sometimes we call it as a quantum *program*.

We can convert the circuit as tensor or matrix formula.

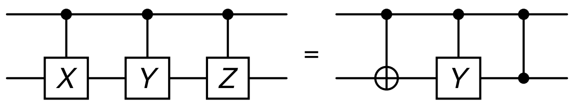


$\leftrightarrow U = U_1 \otimes U_2.$

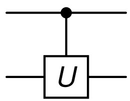


$\leftrightarrow U = U_a \otimes I \otimes U_b,$

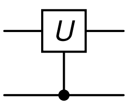
Controlled gate: A gate applying a specific operator on *controlled* qubit by the state of *control* qubit. It is an unseparable 2-qubit gate.
Example: CX(CNOT), CY, CZ gates.



General case: Controlled-U gate



$$= |0\rangle\langle 0| \otimes I + |1\rangle\langle 1| \otimes U = \begin{bmatrix} I & O \\ O & U \end{bmatrix}$$

Warning 

$$\neq \begin{bmatrix} U & O \\ O & I \end{bmatrix}$$

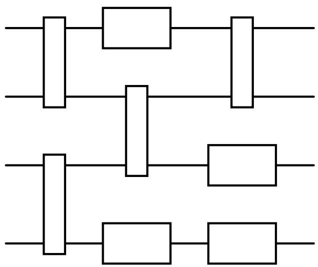
Theorem 1

Solovay-Kaitaev Theorem

Any n qubit unitary matrix could be approximated with combination of 1 and 2 qubits gates.

$$||U - U_{1,2}|| < \epsilon \tag{1}$$

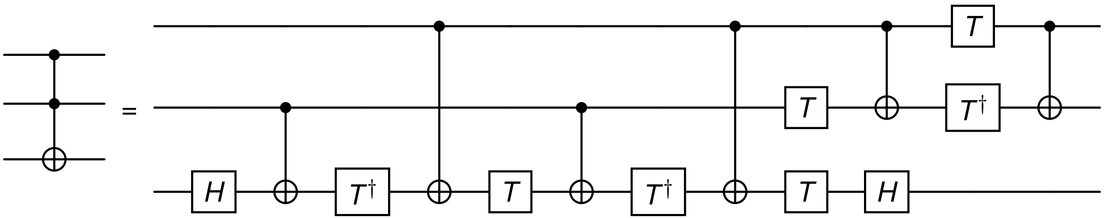
where $\epsilon > 0$ *and* $U_{1,2} =$



Universal gate set:

- $\{CNOT, H, S, T\}$ is universal.

Example: Toffoli gate



Complexity: A measure of resource to be used in calculation. Usually, we count a number of operation in a specific task.
In quantum circuit, number of gates is proportion to operation complexity. By the set of universal gates, the complexity could be different.
Example in $\{CNOT, H, S, T\}$ set.

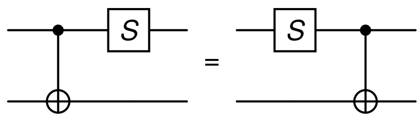
- Reducing specific gate: T and $CNOT$ gates are hard to implement and yield huge error comparing to other gates.
- Reducing overall steps in circuit:

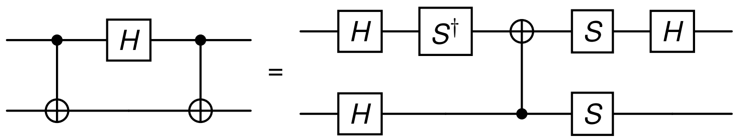
Circuit Optimization

Basic optimization method

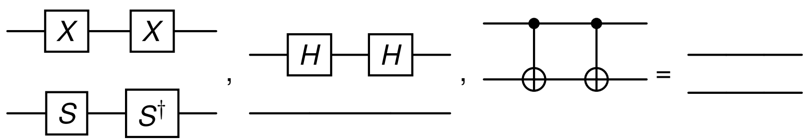
Assume that we have a given circuit representation of U.

1. By the type of the gate, we can modify the order and location of the gates. Therefore, there are equivalent representation of single U with different complexity.





2. All quantum gates are unitary operators, $U^{\dagger} = U^{-1}$, we can eliminate $U^{\dagger}U$ pairs.



TROTTERIZATION

On gate model computation, an implementation of quantum dynamics is a mimicking a time-propagator operator U corresponding to a system hamiltonian H.

$$|\psi(0)\rangle \to U \to \psi(t)\rangle$$

The propagator U is determined by Schrödinger equation.

$$i\hbar|\psi\rangle = H|\psi\rangle, \; |\psi(t)\rangle = e^{-iH/\hbar t}|\psi(0)\rangle$$

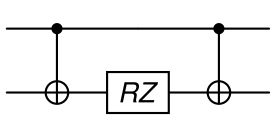
Trotterization

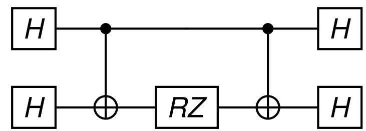
Trotterization circuit

Standard method to implement time evolution is a Trotterization

$$\lim_{n\to\infty}(e^{A/n}e^{B/n})^n = e^{A+B} \tag{2}$$

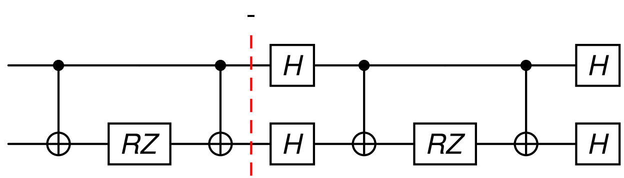
1. Construct a single Pauli element evolution gate.

$\exp(-itZ \otimes Z) =$ 

, $\exp(-itX \otimes X) =$ 

2. Combine the circuit by the Hamiltonian

$$H = ZZ + XX \tag{3}$$

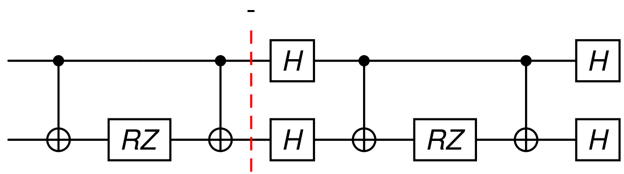
$\exp(-itH) \approx$ 

Trotterization

Reducing method

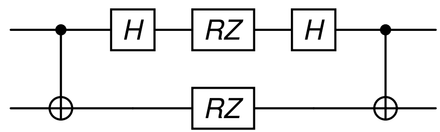
Problem: Simply concatenating the single terms requires too many gates.

$\exp(-itH) \approx$



Question: What hamiltonian would be a corresponding hamiltonian of the next circuit?

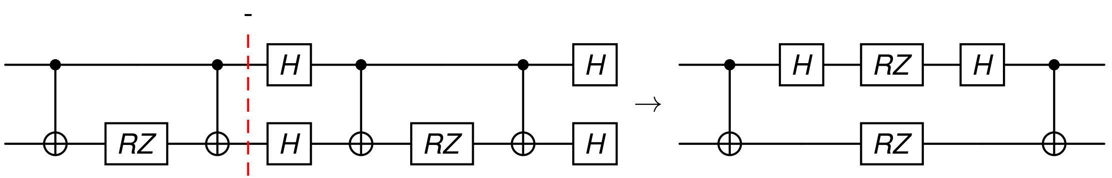
$\exp(-itH) \approx$



$$H = ZZ + P_{unkonwn}$$

PAULI FRAME

Answer: $H = ZZ + XX$
We can decrease the circuit depth for the given time-evolution.

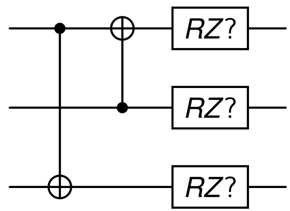


Key properties: ZZ and XX are *commuting* to each other. If $H = ZZ + ZX$ then the above optimization is impossible.

Pauli Frame

To construct the such optimization, we must know **what Pauli term** contributes to each wire on circuit, when we apply a Rotation gate on it.

$$\exp(-iH_{unknown}t) \approx$$



Pauli Frame is a representation of the Pauli elements on circuit. See details on Schmitz et al., 2023.

Graph Optimization Perspective for Low-Depth Trotter-Suzuki Decomposition

Albert T. Schmitz[*]
Intel Labs, Intel Corporation, Hillsboro, Oregon 97124, USA
Department of Physics and Center for Theory of Quantum Matter,
University of Colorado, Boulder, Colorado 80309, USA

Nicolas P. D. Sawaya
Intel Labs, Intel Corporation, Santa Clara, California 95054, USA

Sonika Johri[†] and A.Y. Matsuura
Intel Labs, Intel Corporation, Hillsboro, Oregon 97124, USA

(Dated: May 30, 2023)

Pauli Frame

Definition 4.1

Pauli Frame

For N qubit system, Pauli Frame is a collection of $2N$ number of generalized Pauli elements,
$B = (\{s_i\}_{i=1}^N, \{\tilde{s}_i\}_{i=1}^N), \forall i, s_i, \tilde{s}_i \in \mathcal{P}$*, satisfying the next conditions.*

1. $[s_i, s_j] = 0 \, \forall i, j \in [N]$
2. $[s_i, \tilde{s}_i] \neq 0 \, \forall i \in [N]$
3. $[s_i, \tilde{s}_j] = 0 \, \forall i \neq j$

$$B = \begin{bmatrix} s_1 & , & \tilde{s}_1 \\ s_2 & , & \tilde{s}_2 \\ \vdots & , & \vdots \\ s_N & , & \tilde{s}_N \end{bmatrix}$$

Pauli Frame

Gate actions on the frame

$$B = \begin{bmatrix} IIZ & , & IIX \\ IZI & , & IXI \\ ZII & , & XII \end{bmatrix}$$

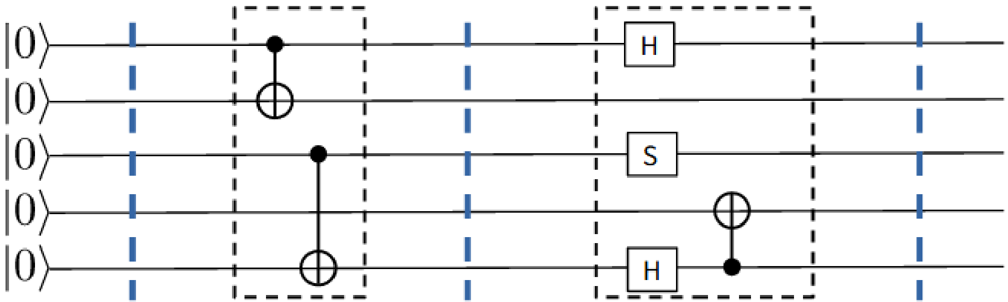
1. Hadamard gate(H): $s_i \leftrightarrow \tilde{s}_i$
2. Phase gate(S):$\tilde{s}_i = s_i + \tilde{s}_i$
3. CX gate: $s_j = s_i + s_j, \tilde{s}_i = \tilde{s}_i + \tilde{s}_j$

Example: $B \rightarrow_{(CX_{1,2})} B'$

$$B' = \begin{bmatrix} IIZ & , & \mathbf{IXX} \\ \mathbf{IZZ} & , & IXI \\ ZII & , & XII \end{bmatrix}$$

Pauli Frame

Using a Pauli Frame we can chase the Pauli element we can rotate on the circuit by applying RZ gate.



$$
\begin{pmatrix} Z_1 & X_1 \\ Z_2 & X_2 \\ Z_3 & X_3 \\ Z_4 & X_4 \\ Z_5 & X_5 \end{pmatrix}
\qquad
\begin{pmatrix} Z_1 & X_1X_2 \\ Z_1Z_2 & X_2 \\ Z_3 & X_3X_5 \\ Z_4 & X_4 \\ Z_3Z_5 & X_5 \end{pmatrix}
\qquad
\begin{pmatrix} X_1X_2 & Z_1 \\ Z_1Z_2 & X_2 \\ Z_3 & Y_3X_5 \\ Z_4X_5 & X_4 \\ X_5 & Z_3X_4Z_5 \end{pmatrix}
$$

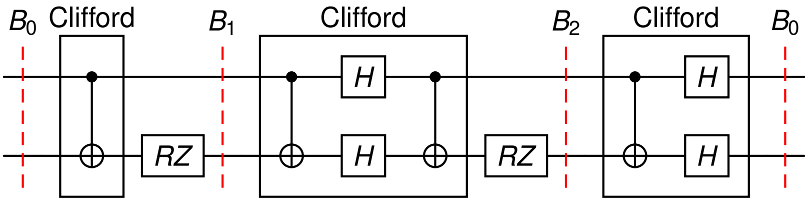
Figure. Example of Pauli term chasing on circuit by Clifford gate application.

Clifford transformation over frame

Clifford gates $[CX, H, S]$ preserve the structure of Pauli Frame.

$$B_i \rightarrow_{clifford} B_j$$

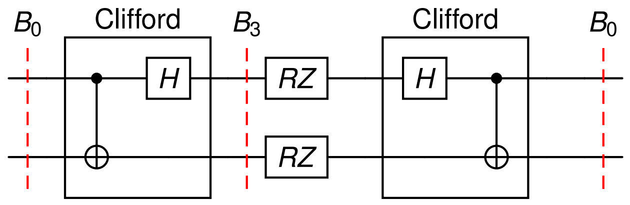
Examples: $\exp(-it(ZZ + XX))$ time evolution gate



$$\begin{bmatrix} IZ & , & IX \\ ZI & , & XI \end{bmatrix} \rightarrow \begin{bmatrix} IZ & , & XX \\ \mathbf{ZZ} & , & XI \end{bmatrix} \rightarrow \begin{bmatrix} IX & , & ZZ \\ \mathbf{XX} & , & ZI \end{bmatrix} \rightarrow \begin{bmatrix} IZ & , & IX \\ ZI & , & XI \end{bmatrix}$$

We can make any Pauli frame on N qubit system using Clifford gate set.

Pauli Frame



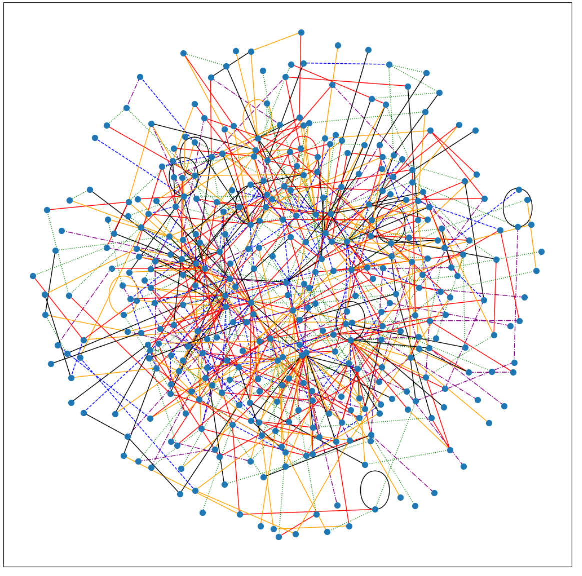
$$\begin{bmatrix} IZ & , & IX \\ ZI & , & XI \end{bmatrix} \to \begin{bmatrix} \mathbf{XX} & , & IZ \\ \mathbf{ZZ} & , & XI \end{bmatrix} \to \begin{bmatrix} IZ & , & IX \\ ZI & , & XI \end{bmatrix}$$

Pauli Frame

That is, optimization of Trotter circuit is equivalent to finding an optimial **path** defined with Pauli frames and corresponding **Clifford gates**. In original paper, Schmitz et al., 2023 concluded that

1. Path finding problem is a Classic NP hard problem (Traveling Purchaser Problem).
2. There is no method to derive the Clifford gate connecting two arbitrary frames, B_1, B_2.

$$B_1 \rightarrow_{???} B_2$$

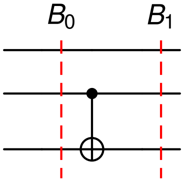


Part II

CIRCUIT SYNTHESIS

IZ FAMILIES

CX gate makes product of two Pauli elements on stabilizer of the frame.



$$\begin{bmatrix} IIZ & IIX \\ IZI & IXI \\ ZII & XII \end{bmatrix} \rightarrow_{2,3CX} \begin{bmatrix} IIZ & IIX \\ IZI & XII \cdot IXI \\ IZI \cdot ZII & XII \end{bmatrix}$$

Symplectic Representation of Pauli element

Usually, we manipulate Pauli element as tensor product of Pauli matrices.

$$P = IXZYI = I \otimes X \otimes Z \otimes Y \otimes I$$

We can represent them into a product of X, I or Z, I produced elements without considering phase.

$$YXIY = XXIX \cdot ZIIZ$$

Then we can make a bijective transformation between Pauli elements and 2 binary vectors tuple.

$$P = (-i)^f \hat{X}^{\vec{x}} \cdot \hat{Z}^{\vec{z}}$$

$$P \leftrightarrow (\vec{x}, \vec{z})$$

This is called by *symplectic representation* of Pauli elements.

Symplectic Representation of Pauli element

IZ family Pauli element is Pauli elements generated by tensor products of I, Z.
Example: $IIIIZ, ZIZIZIZ, ZZZZI$.
Simplectic representation of IZ family, $(\vec{x}, \vec{z})$.

$$IIIZ = ([0,0,0,0],[0,0,0,1]), IZIZ = ([0,0,0,0],[0,1,0,1])$$

Product: $IIIZ \cdot IZIZ = IZII$

$$[0,0,0,1]^\wedge[0,1,0,1] = [0,1,0,0]$$

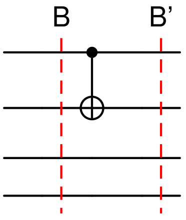
$^\wedge$ is a bitwise XOR operation.

FRAME AND AN ELEMENT

We want to apply $\exp(-itIIZZ)$ gate on circuit when the given circuit state was, B with Pauli frame representation.

$$B = \begin{bmatrix} ZZZI \\ ZZIZ \\ ZIZZ \\ IZZZ \end{bmatrix} \rightarrow B' = \begin{bmatrix} \cdot \\ \mathbf{IIZZ} \\ \vdots \end{bmatrix}$$

The circuit is simple, in here we will reconstruct the circuit with algorithmically.



Now, change the representation as binary vector

$$B = \begin{bmatrix} ZZZI \\ ZZIZ \\ ZIZZ \\ IZZZ \end{bmatrix} = \begin{bmatrix} 1110 \\ 1101 \\ 1011 \\ 0111 \end{bmatrix} = \begin{bmatrix} \vec{w}_1 \\ \vec{w}_2 \\ \vec{w}_3 \\ \vec{w}_4 \end{bmatrix} \tag{4}$$

With the binary represent, the CX combination of i, j-th wires is identical to generate XOR of two w_is, $w_i \oplus w_j$. XOR is commutative so that, the problem becomes the next statement.

Definition 3.1

Find the minimum size subset $\{w_k\} \subset B$ whose XOR products is P where,

$$P = \oplus_k \vec{w}_k$$

More simply, it is equivalent with finding a binary vector $\vec{x} \in \{0, 1\}^N$ of

$$P = \oplus_{i=1}^{N} x_i \& \vec{w}_i \tag{5}$$

Frame and an element

Let, $v = [1, 1, 0, 0]^T$, it is a symplectic representation of $Z_1 Z_2$, and $x = [x_1, x_2, x_3, x_4]^T, x_i \in \{0, 1\}$.

$$Mx = v \tag{6}$$

$$M = \left[\begin{array}{c|c|c|c} w_1 & w_2 & w_3 & w_4 \end{array} \right] \tag{7}$$

$$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \tag{8}$$

How can we use gauss elimination: $(\mathbb{Z}/2\mathbb{Z}, \wedge, \&)$ form a modulo 2 field. Therefore, $w_i \oplus w_j$ is a linear combination over $(\mathbb{Z}/2\mathbb{Z})^4$.

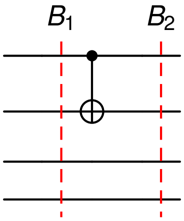
Frame and an element

With Gauss elimination method, Reduced row echelon form would be obtained.

$$\left[M \mid v\right] \rightarrow \left[\begin{array}{cccc|c} 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{array}\right] \tag{9}$$

1. $w_1 \oplus w_2 = 0$
2. $w_2 \oplus w_3 = 1$
3. $w_3 = 0$
4. $w_4 = 0$

Thus, we get $x = [1, 1, 0, 0]$, and it means $[0, 1, 1, 1] \oplus [1, 0, 1, 1] = [1, 1, 0, 0]$
It means that CX over 1st and 2nd yields $Z1Z2 = IIZZ$ Pauli element on the frame. The process reached the same point we had predicted at first.



Frame and frame

From the above method when two frames was given, B_1, B_2, we can construct $\oplus_i x_i \& w_i$ representation for all $v_i \in B_2$.

$$B_1 = \begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ w_4 \end{bmatrix}, B_2 = \begin{bmatrix} v_1 & = & w_1 \oplus w_2 \\ v_2 & = & w_2 \oplus w_4 \\ v_3 & = & w_1 \oplus w_2 \oplus w_4 \\ v_4 & = & w_2 \oplus w_3 \end{bmatrix}$$

Rewrite the addition as more convenience form $+$.

$$\begin{bmatrix} v_1 & = & w_1 + w_2 \\ v_2 & = & w_2 + w_4 \\ v_3 & = & w_1 + w_2 + w_4 \\ v_4 & = & w_2 + w_3 \end{bmatrix}$$

Frame and frame

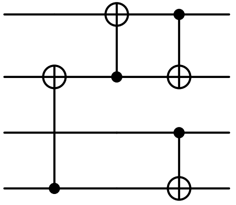
$$\begin{bmatrix} IIIZ \\ IIZI \\ IZII \\ ZIII \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix} = \begin{bmatrix} ZIZZ \\ IIIZ \\ IZII \\ ZZII \end{bmatrix}$$

LU/UL decomposition: Decomposition of the given matrix into lower triangular and upper triangular.

L, U non-zero terms indicate elementary row operators.

Frame and frame

$$\begin{bmatrix}1&1&0&0\\1&0&1&1\\0&1&0&0\\0&0&0&1\end{bmatrix} = L \cdot U = \begin{bmatrix}1&0&0&0\\1&1&0&0\\0&0&1&0\\0&0&1&1\end{bmatrix} \cdot \begin{bmatrix}1&1&0&1\\0&1&0&1\\0&0&0&0\\0&0&0&1\end{bmatrix}$$



The circuit is a reversible linear quantum circuit, we can adopt various optimization algorithmsPatel et al., 2008.

Frame and frame

General case: What about general Pauli elements? We cannot use the method for general Hamiltonian elements, since there are some elements anti-commuting to the other.
For example, if frames are connected by the next stabilizers,

$$ZXZX, YXYX, YZYZ, XXXX, \ldots$$

They are mutually commuting. In that case, we can use the above method we applied to IZ family.

Theorem 2

Let N qubit system and the N fold Pauli group be a $\mathcal{P}$. If the union of stabilizers of two Pauli frames, B_1, B_2, were mutually commuting subset of $\mathcal{P}$. The Clifford gate connecting the two frame only consist of CX gates.

References I

Patel, K. N., Markov, I. L., & Hayes, J. P. (2008).**Optimal synthesis of linear reversible circuits.** *Quantum Info. Comput.*, *8*(3), 282–294.

Schmitz, A. T., Sawaya, N. P. D., Johri, S., & Matsuura, A. Y. (2023, May). **Graph Optimization Perspective for Low-Depth Trotter-Suzuki Decomposition [arXiv:2103.08602 [cond-mat, physics:math-ph, physics:physics, physics:quant-ph]].**