FAQ for selecting bits in 12bit 10bit and 8bit application.

Question:. The line sensor DR 4K X 7 has A/D conversion of 13bits, Which bits should be used for 12 bit operation?

> If you connect only 12 bit's, we recommend you use the 12 LSB's. The sensor provides on chip logic, to prevent "wrap around error" for the 13th bit. If you set bit 1 in register 5 to high (enable_saturation) the sensor output will be clipped to 4095 in case the AD result is larger than 4095. (please refer to page 26 of the ASIC SPEC spec sheet)

Question:. How can "End of Range" register be used for configuring the ADC resolution. Can we configure sensor for 8 bits resolution, 10 bit or 11 bit resolution?

> Yes, you can configure the sensor to give out only 8 bit's. It will not necessarily have any advantage to do so, but you can. In order to read out one line of data from the sensor, you use the same time the ADC takes to compute 10 bit's when in normal speed, and 11bit's when using on chip clock division of 2, thus reducing the ADC conversion range below 10 bit's will not result in higher maximum line rate, but it is still possible.

The AD conversion range, i.e. the last AD code generated, is programmed over register 9. The last code given out is "register content" * 32 + 4. So to get no code higher than 1023, you should program the register with 0x1Fh. To get no code higher than 255 you should write 07 in the register.

When considering only 8 LSB's the sensor will have a high digital gain, unless the ADC conversion step (Regsiter 3) is adjusted to a value 4x higher than for 10 bit conversion. But in terms of noise, dynamic range, or maximum line rate, the effect of limiting the ADC range to 8bit or considering only the bits 2-9 while working in 10bit configuration is very much the same.

In case you would want to work in 10 bit mode only, you should also connect the 10 LSB's and configure the ADC end range register to avoid digital over flow. When using the offset subtraction, you can still work with 11bit before on chip offset subtraction so that you get full 10bit output, but you would have to adjust the ADC end range yourself in accordance with the subtracted value to prevent "wrap around" data error.

Example: Assume the average dark image before enabling on chip offset subtraction would be 45DN, the lowest pixel before dark level offset subtraction would be 38DN. After saving the dark level reference and enabling offset subtraction, the highest possible ADC code would be for the pixel with the lowest dark reference value the (in our example for the pixel with 36DN dark reference) "ADC END RANGE register" * 32 + 4 - 38. This value has to be lower than 1023 otherwise a digital wrap around error may occur. Therefore the ADC END RANGE register could in this case be programmed to 0x21h.

When using programmable logic, such as CPLD's or FPGA's to receive the data, the digital saturation can more easily be prevented by capturing the 11th bit and implementing a saturation logic to 1023 in FPGA or CPLD.

In case you need only 8 bit, easiest is to work similar to 10 bit mode, but ignoring the 2 LSB's.

Recommended connection schemes:

Sensor Bits	**b12 (MSB)**	**b11**	**b10**	**b9**	**b8**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0 (LSB)**
13 bit operation	MSB												LSB
12 bit * operation	NC	MSB											LSB
10 bit ** operation	NC	NC	NC**	MSB									LSB
8 bit ** operation	NC	NC	NC**	MSB							LSB	NC	NC

* Enable Register 1 bit 5 (12 bit saturation) to avoid digital wrap around error when exceeding output value of 4095. (signal will saturate at 4095DN)

** configure ADC_END range register (Register 9) such as to avoid output codes exceeding 1023DN. Default write hex 0x1F to Register 9. (Slightly higher values may be possible in combination whit on chip offset subtraction.) Alternatively connect bit b10 and implement saturation logic to 10 bit.