3TB4
Prelab 3
March 2, 2018
Chris Adams - 001403187

Question 1:

8 kHz = 8000 Hz = 8000 samples/sec = 8 samples/ms
Student number last two numbers: 87

87ms * 8 samples/ms
=696 samples

Question 3: Mux

```
module multiplexer(input [15:0] a, input [15:0] b, input [15:0] c, input [1:0] sel, output reg [15:0] r);

//declare 3 16-bit buses
wire [15:0] bus_2_d [2:0];

//bus one connects to 16 bit input a
assign bus_2_d[0] = a;

//bus two connects to 16 bit input b
assign bus_2_d[1] = b;

//bus three connects to 16 bit input c
assign bus_2_d[2] = c;

//always block implements a multiplexer that selects between 3
always @(*)
begin
case (sel)
2'b00: r = bus_2_d[0];
2'b01: r = bus_2_d[1];
2'b10: r = bus_2_d[2];
endcase
end
endmodule
```

Question 4: fir

```
module fir(input numTaps, input [15:0] d, output reg[15:0] out, clock);
    reg[15:0]coeffs[numTapsaps-1:0];
    reg[15:0]taps[numTapsaps-1:0];
    always @(posedge clock)
        begin
            for (i=0;i<numTapsaps-1;i=i+1)
                begin
                    taps[i+1] <= taps[i];
                end
     taps[0] = d;
        out = 0;
        for (i=0;i<numTaps;i=i+1)
            begin
                q = q + taps[i]*coeffs[i];
            end
        end
endmodule
```

Question 5: echo

```
module echo(input clk, input [15:0] sampleIn, output [15:0] sampleOut);

    wire[15:0] delay, divdelay, feedback;
    assign feedback = sampleOut;
    assign divdelay = {delay[15], delay[15], delay[15:2]};

    always @(posedge clk)
    begin
        sampleOut = divdelay + sampleIn;
    end
Endmodule
```

Question 6: subsystem

```
module dsp_subsystem (input sample_clock,  input reset, input [1:0] selector, input [15:0] input_sample, output
[15:0] output_sample);

    //assign output_sample = input_sample;
    echo(input_sample,output_c,sample_clock);
    fir(input_sample,output_b, 65, sample_clock);
    multiplexer(input_sample,output_b,output_c,sel,output_sample);

endmodule
```