3TB4 Postlab

March 23 2018

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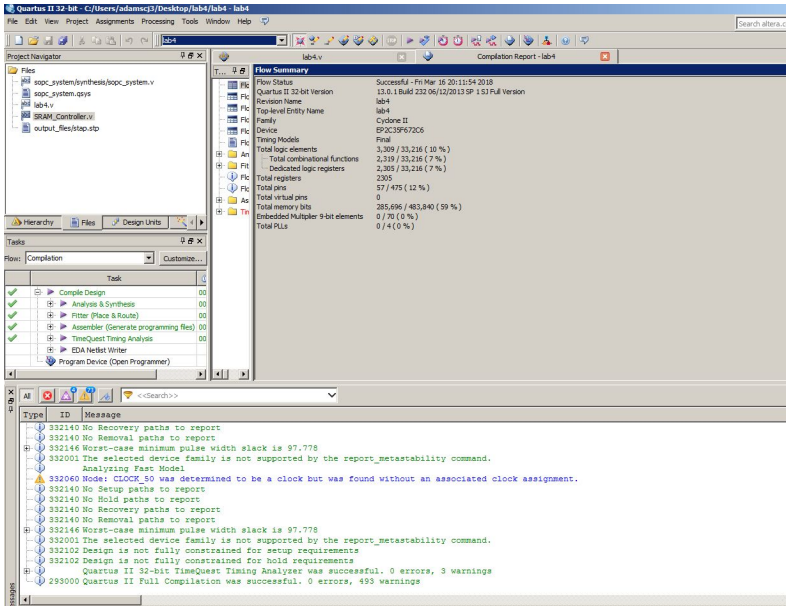
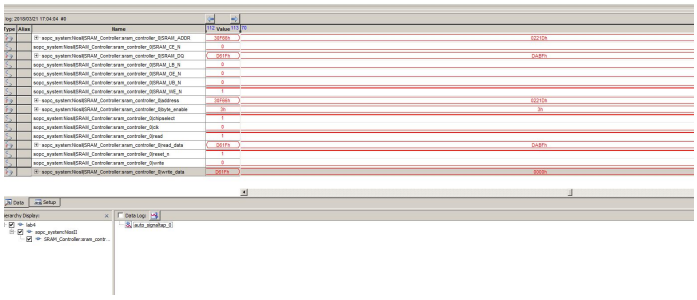
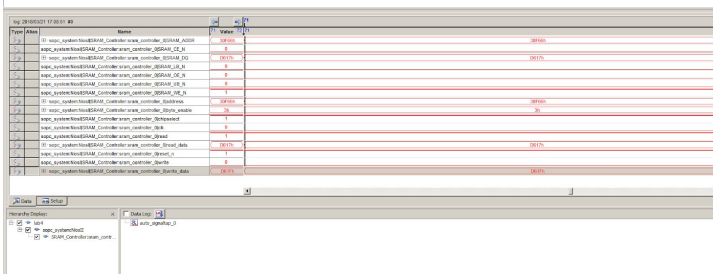
Images:

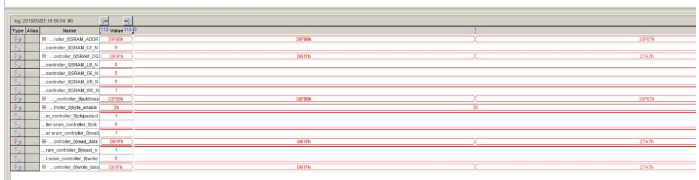
Compilation Report:

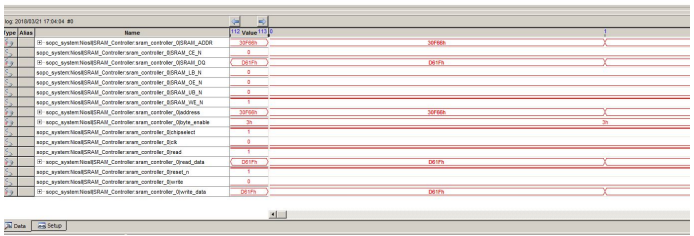


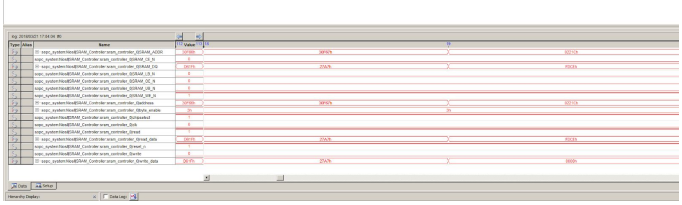
Read/Write Ints:



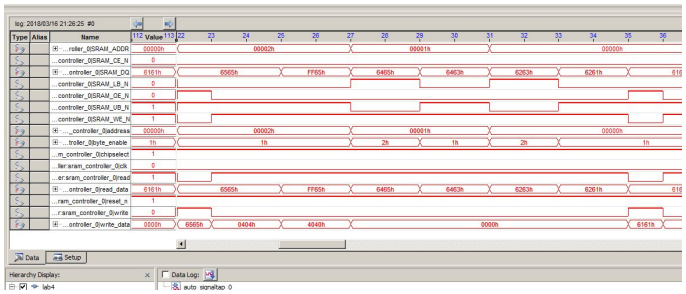


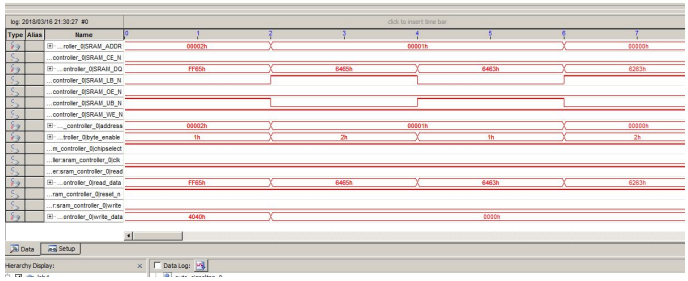


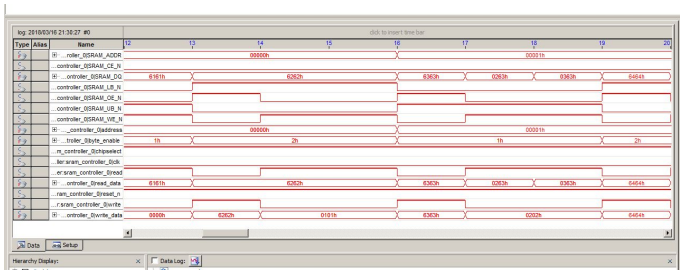


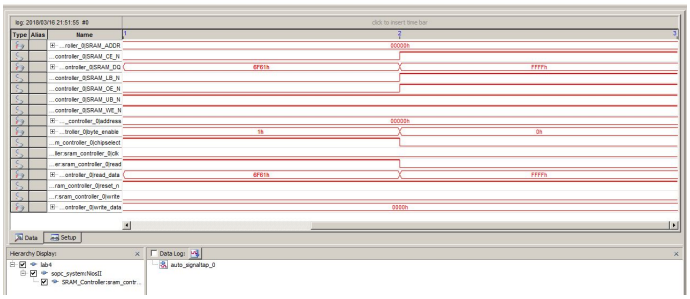


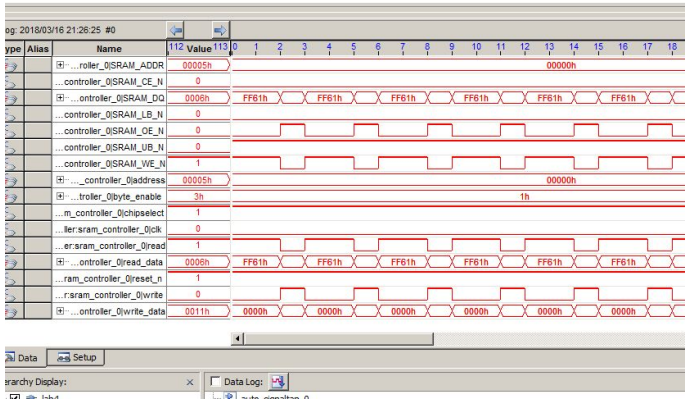
Read/Write Chars:



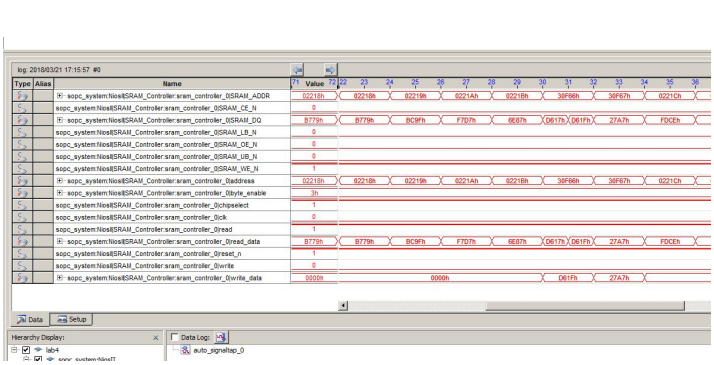


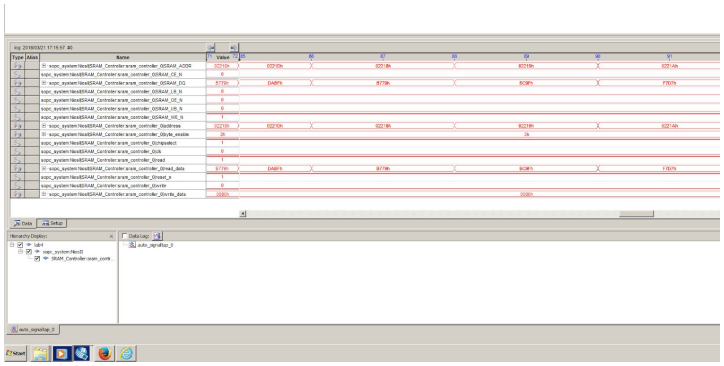


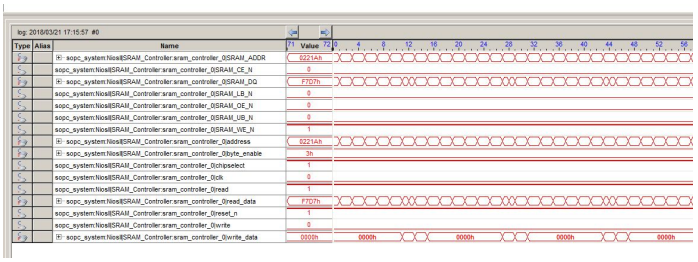


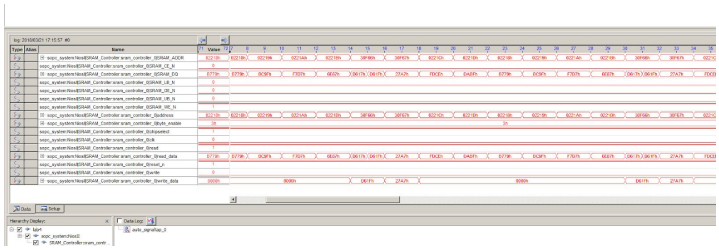


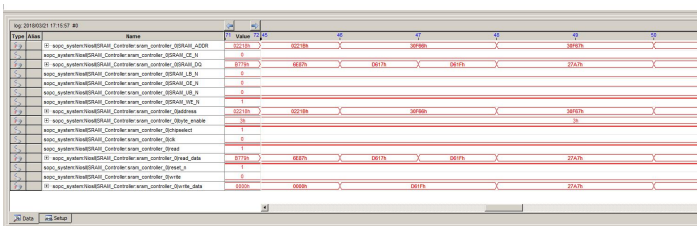
Read/Write Shorts:

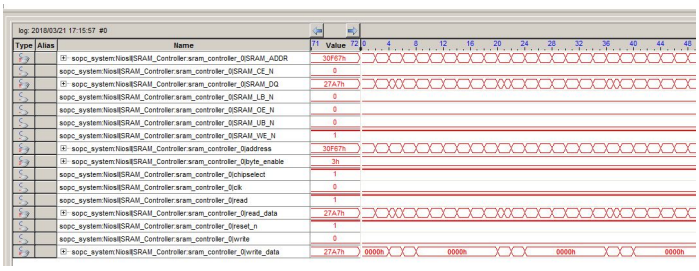












Question One:

It appears that writing takes less clock cycles than reading on the screenshots provided in this report. This is due to the fact that reading may need wait states in between the master and the slave. Due to these wait states that master is waiting until the slave is ready to proceed.

The SRAM_DQ shows values such as 0x0505 where you would expect 0x0005. This happens because the values may be placed in the upper or lower byte during storing.

SRAM_ADDR is responsible for showing the start address of the instruction. If you have two values such as 5 and 6 that both require less than a byte of space for storage they can be placed in the same address space. They are then distinguished from one another using byte enable signals.

Question Two:

What steps does the Avalon interconnect take to write a 32-bit integer into the 16-bit SRAM memory

Question Three:

1. Total number of logic elements used by your circuit = 3 309
2. Total number of memory bits used by your circuit = 285 696
3. Total number of pins = 57
4. The maximum number of logic elements that can fit in the FPGA = 33 216

Question Four:

Given that the SOPC system we designed in the lab required 3309 logic elements and the FPGA we used has a maximum number of 33216 logic elements available, 10 of our SOPC system could fit onto an FPGA.

Question Five:

Given that the SOPC system we designed in the lab required 285696 memory bits and the FPGA we used has a maximum number of 483840 memory bits available, 1 of our SOPC system could fit onto an FPGA.

Question Six:

Given that the SOPC system we designed in the lab required 57 pins and the FPGA we used has a maximum number of 475 pins, 8 of our SOPC system could fit onto an FPGA.