Mechtron 3TB4: Embedded Systems Design II
Assignment 3

Due: Friday March 16, 2018, in the class

Q.1 [20] You are using 16 bits to represent real numbers in the range $-120 \leq x < 120$.

a) (2 marks each)

(i) What Q format should you use? Justify your answer.

(ii) What is the largest positive number this Q format can represent? (Sanity check - this better be greater than or equal to 120!)

(iii) What is the smallest positive number this Q format can represent?

(iv) What is the largest negative value this Q format can represent?

b) Convert 0.25 and -0.75 to Q0.4 format fixed point representation (total bits used = 5).[4]

c) Write Verilog code for a module that takes two 16 bit inputs in your Q15 format and produces a number in the same Q format after multiplication of the two numbers. [4]

d) The following numbers represent fractions in Q15 format. What are their values in decimal numbers? [2+2]
1110_0000_0000_0000
0011_0000_0000_0000

Q.2 Explain what is wrong (at least two things) with the following section of Verilog code: [10]

```
module(input x, y,z, output a, b,c);
always @(*)
begin
  case ({x,y,z})
  3'b111:
   begin
   a = 1'b0;
   b=1'b1;
   c=x;
   end

 3'b101:
  begin
  a=1'b0;
  b=y;
  c=z;
  end
```

```
default:
  begin
  a=1'b0;
  b=b;
  end
 endcase
end
endmodule
```

Q.3 [10] What will be the result of synthesizing the following Verilog code: (Draw the resulting circuit, if any)?

```
module xyz (input a, input b, output reg out);

 always @(*)
  begin
   case ({b, a})
    2'b11: out = 1'b0;
    default: out = 1'b1;
  endcase
 end

always @(*)
  begin
   out = 1'b1;
    if (a == 1 && b == 1)
       out = 1'b0;
  end

endmodule
```

Q.4 [10]

1. The coefficients of an FIR are:
   b0, ... b4 = 0.025761, - 0.246666, 0.507790, - 0.246666, 0.025761
   You want to implement this filter on an 8 bit processor using a fixed point approx- imation. If all of the coefficients are to fit in 8 bit values, what Q format should you use to represent them and what are the coefficient values in your chosen Q format? [2+6]
2. What is anti-aliasing filter? Why is it necessary to employ it before sampling? [2]

Q.5 [10] Given the FPGA configuration shown in figure 1, determine the function it is implementing. If there are any problems with the circuit in the figure, clearly indicate where the problem is and show the functions implemented by individual LUT's. (show all your work!)

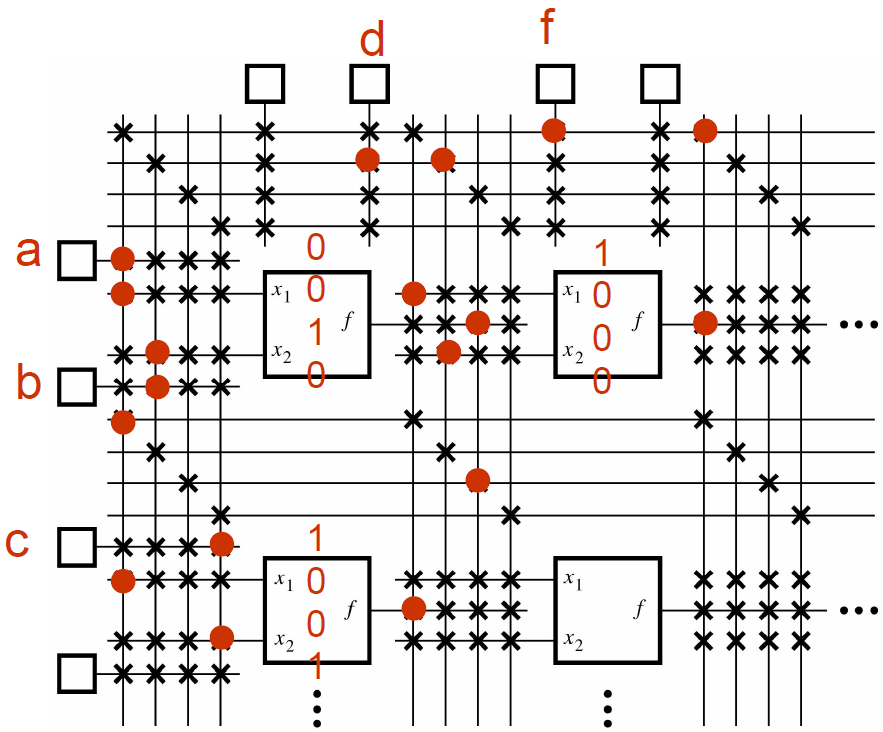

Figure 1: