OPL2500

ULTRA-LOW POWER 2.4GHZ WI-FI + BLUETOOTH SMART SOC

DataSheet

OPULINKS

OPL2500-DataSheet-NDA | Version 1.2

REVISION HISTORY

Date	Version	Contents Updated
2021/08/04	1.1	• Initial Release
2022/07/20	1.2	• Content rehash

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1. GENERAL DESCRIPTION

The OPL2500 SoC features a fully integrated 2.4GHz radio transceiver and baseband processor for Wi-Fi 802.11b/g/n/ax and Bluetooth® Smart applications. The SoC can be used as a standalone application-specific communication processor or as a wireless data link in hosted MCU systems where ultra-low power is critical. The OPL2500 supports flexible memory architecture for storing profiles, stacks and custom application codes, and can be updated using Over-The-Air (OTA) technology. Qualified Bluetooth Smart protocol stack and Wi-Fi TCP/IP stack are stored in a dedicated ROM. The OPL2500 is equipped with dual processors, ARM® Cortex®-M0 and M3, for handling different processes. All software runs on the ARM® Cortex®-M0 processor while more intensive application-specific activities run on the ARM® Cortex®-M3 processor. The OPL2500 can be connected to an external MCU through SPI, I2C or UART interfaces and sensors or other devices through GPIOs. The transceiver interfaces directly to the antenna and is fully compliant with the Wi-Fi 802.11b/g/n/ax and Bluetooth 5.2 BLE standards. With integrated antenna switch, RF balun, power amplifier (PA) and low noise amplifier (LNA), OPL2500 allows Wi-Fi and Bluetooth Smart applications with minimal PCB design area and external component requirement.

2. FEATURES

The OPL2500 complies with ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

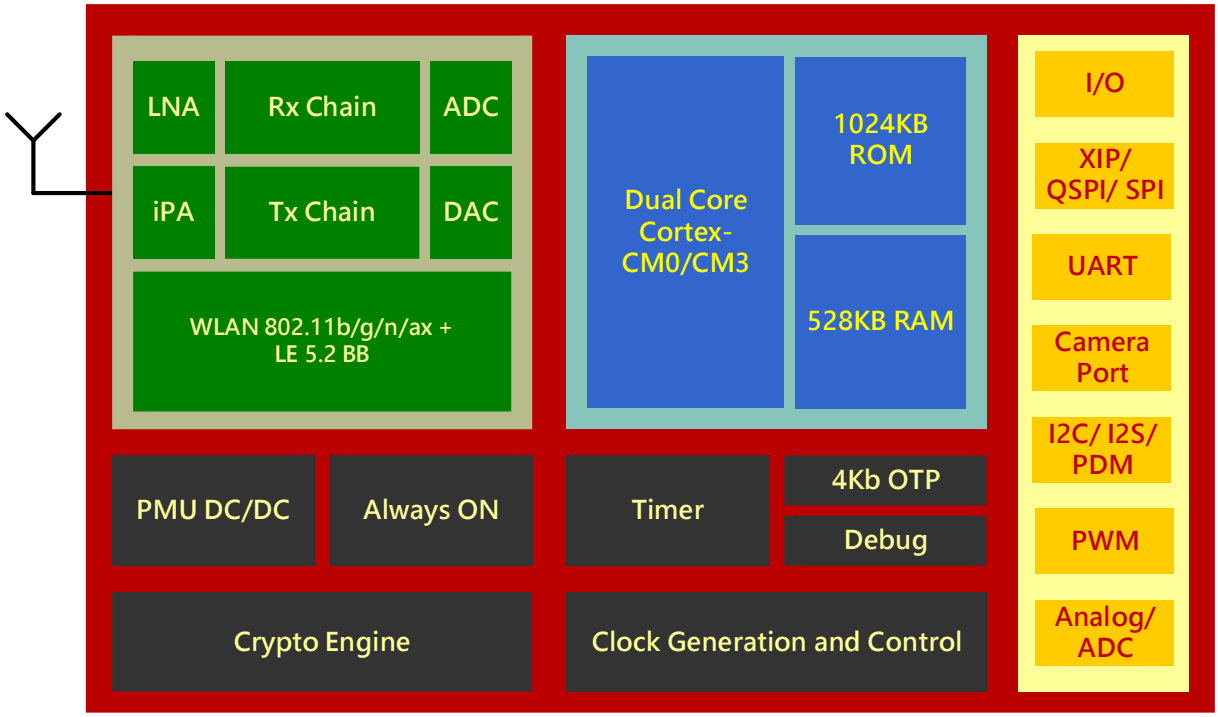
- Processors
  - ARM® Cortex®-M3 Application Processor
  - ARM® Cortex®-M0 Link Controller
- Wi-Fi
  - 802.11 b/g/n/ax up to 86Mbps PHY data rate
  - Support TWT
  - WPA/WPA2/WPA3 security supports
  - Automatic beacon scanning and discovery
  - Built-in TCP/IP stacks
  - Integrated dual power amplifiers: low (0dBm), high (+17dBm) †

    † Optional internal T/R switch by-pass mode available to increase to +19dBm
- Bluetooth Smart
  - Compliant with Bluetooth 5.2 BLE specifications w/ 2Mbps rate capability
  - Supports Master and Slave Modes
  - Built-in BLE stack
  - Support LE mesh
  - 0 to 10 dBm transmit output power
  - -92 dBm receiver sensitivity
  - Adaptive Frequency Hopping (AFH)
  - All GATT-based profiles
  - Max. 8 concurrent BLE connections
- HW Crypto Engine
  - AES-128/192/256 bits Encryption
  - P-256 ECDH (Elliptic Curve Diffie-Hellman) Key Generation
  - SHA2
  - TRNG
- Power Management
  - Integrated Buck DC-DC converter
  - Supports coin (typ. 3.0 V) or two stacked alkaline (each typ. 1.5 V) battery cells

- General Purpose, Capture and Sleep timers
- Digital Interfaces
  - Up to 37 general purpose I/Os
  - Two UARTs with hardware flow control with speed up to 3Mbps
  - Three SPI+™ interfaces
  - Support XIP
  - I2C bus with data rate of 100 kbps/400 kbps
  - I2S
  - A camera port supporting Omnivision™ camera OV2640 or compatible models.
- Analog Interfaces
  - 10-bit Auxiliary ADC inputs up to 16 channels
  - Six pins with 16mA driving capability
  - Six PWMs
- Package
  - 48-pin QFN, 6 mm x 6 mm

3. BLOCK DIAGRAM

Figure 1: OPL2500 Block Diagram

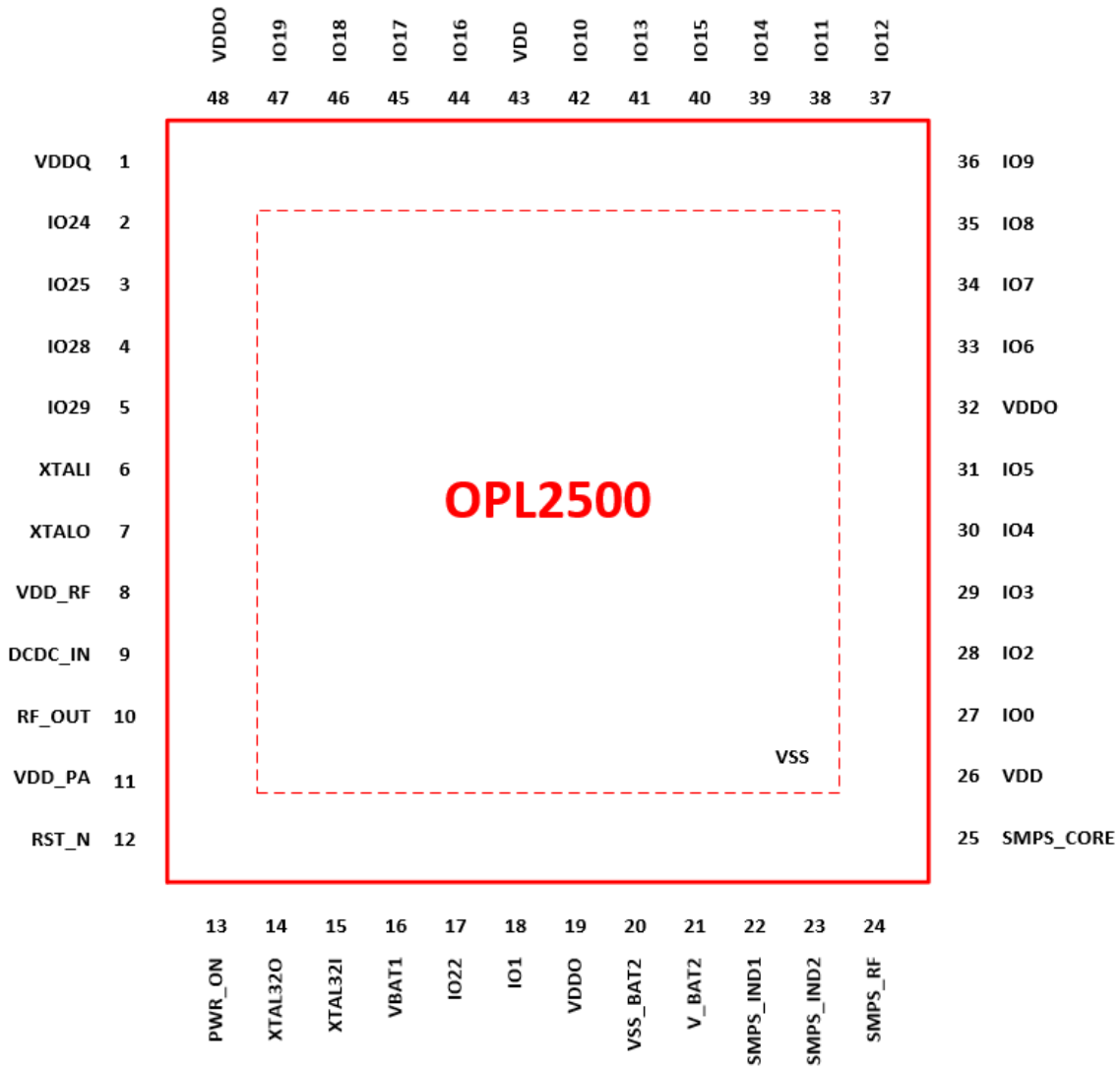


4. PIN DEFINITIONS

4.1. Pin Layout

Figure 2 lists the pin-out assignments for the 48-pin QFN package.

Figure 2: OPL2500 Pin Layout



4.2. Pin Description

The table below provides IO pin functional description.

Table 1: OPL2500 Pin Description (48-pin package)

Pin Name	Type	Location	Pull-up/Pull Down	Function Description
VDDQ	P	1		Power supply for internal OTP memory for programming mode
IO24	IO	2	Up	General Purpose Input/Output
IO25	IO	3	Up	General Purpose Input/Output
IO28	IO	4	Up	General Purpose Input/Output
IO29	IO	5	Up	General Purpose Input/Output
XTALI	I	6		Crystal reference input pin
XTALO	O	7		Crystal reference output pin
VDD_RF	P	8		Main RF LDO output
DCDC_IN	P	9		Power supply input for RF LDOs
RF_OUT	IO	10		RF input/output with on-chip T/R switch
VDD_PA	P	11		PA power supply input
RST_N	I	12		Reset input signal
PWR_ON	I	13		Power on signal
XTAL32O	O	14		32K crystal output
XTAL32I	I	15		32K crystal input
VBAT	P	16		Main power supply input
IO22	IO	17	Up	General Purpose Input/Output
IO1	IO	18	Up	General Purpose Input/Output
VDDO	P	19		Power supply for digital IO pad
VSS_BAT2	P	20		Main power supply ground for the power management unit

Pin Name	Type	Location	Pull-up/Pull Down	Function Description
V_BAT2	P	21		Main power supply for the power management unit
SMPS_IND1	P	22		DC-DC power converter inductor pin
SMPS_IND2	P	23		DC-DC power converter inductor pin
SMPS_RF	P	24		DC-DC converter output for RF radio
SMPS_CORE	P	25		DC-DC converter output for digital core supply
VDD	P	26		Power supply for digital core
IO0	IO	27	Up	General Purpose Input/Output
IO2	IO	28	Up	General Purpose Input/Output
IO3	IO	29	Down	General Purpose Input/Output
IO4	IO	30	Up	General Purpose Input/Output
IO5	IO	31	Up	General Purpose Input/Output
VDDO	P	32		Power supply for digital IO pad
IO6	IO	33	Down	General Purpose Input/Output
IO7	IO	34	Up	General Purpose Input/Output
IO8	IO	35	Up	General Purpose Input/Output
IO9	IO	36	Up	General Purpose Input/Output
IO12	IO	37	Up	General Purpose Input/Output
IO11	IO	38	Up	General Purpose Input/Output
IO14	IO	39	Up	General Purpose Input/Output
IO15	IO	40	Up	General Purpose Input/Output
IO13	IO	41	Down	General Purpose Input/Output
IO10	IO	42	Up	General Purpose Input/Output
VDD	P	43		Power supply for digital core
IO16	IO	44	Down	General Purpose Input/Output
IO17	IO	45	Down	General Purpose Input/Output

Pin Name	Type	Location	Pull-up/Pull Down	Function Description
IO18	IO	46	Up	General Purpose Input/Output
IO19	IO	47	Up	General Purpose Input/Output
VDDO	P	48		Power supply for digital IO pad

† Multi-function pins. Please refer to the Pin Multiplexing Table below for the multi-functions provided.

Table 2: OPL2500 Pin Multiplexing Table (48-pin package)

Pin	Loc.	Signal Name	Signal Dir.	Signal Description
IO0	27	APS_DBG_UART_TX	O	APS debug UART transmit output
IO1	18	UART1_RX	I	UART1 receive data input
		UART0_RX	I	UART0 receive data input
IO2	28	APS_DBG_UART_RX	I	APS debug UART receive input
IO3	29	AUX3	I	AUX ADC input channel 3
		I2S_SDO0	O	I2S serial data output
IO4	30	AUX4	I	AUX ADC input channel 4
		I2S_SDI0	I	I2S serial data input
		SCL	O	I2C clock output
IO5	31	UART1_TX	O	UART1 transmit data output
		UART0_TX	O	UART0 transmit data output
		SDA	IO	I2C bi-directional data
IO6	33	PDM_CLK	O	PDM interface clock output
		AUX6	I	AUX ADC input channel 6
		SPI1_CLK	O	SPI1 clock out
IO7	34	MSQ_UART_TX	O	MSQ debug UART transmit output
		PDM_RXD	I	PDM receive data input
		AUX7	I	AUX ADC input channel 7
		SPI1_IO1	O/IO	SPI1 serial output/quad IO
IO8	35	MSQ_UART_RX	I	MSQ debug UART receive input
		SCL	O	I2C clock out
		AUX8	I	AUX ADC input channel 8
		SPI1_IO0	I/IO	SPI1 serial input/quad IO
IO9	36	SDA	IO	I2C bi-directional data
		AUX9	I	AUX ADC input channel 9
		SPI1_CS2	O	SPI1 chip select 2 output
IO10	42	SPI0_IO2	IO	SPI0 quad data IO2

Pin	Loc.	Signal Name	Signal Dir.	Signal Description
IO11	38	SPI0_IO3	IO	SPI0 quad data IO3
IO12	37	SPI0_CS0	O	SPI0 chip select 0 output
IO13	41	SPI0_CLK	O	SPI0 clock out
IO14	39	SPI0_IO0	IO	SPI0 quad data IO0
IO15	40	SPI0_IO1	IO	SPI0 quad data IO1
IO16	44	MSQ_SWCLK	I	MSQ serial wire debug clock input
		SCL	O	I2C clock out
		I2S_SDO0	O	I2S serial data output
		PWM3	O	PWM channel 3
IO17	45	MSQ_SWDIO	IO	MSQ serial wire debug bi-directional data
		SDA	IO	I2C data
		I2S_SDI0	I	I2S serial data input
		PWM2	O	PWM channel 2
		SPI3_MOSI	O	SPI3 master data out
IO18	46	APS_SWDIO	IO	APS serial wire debug bi-directional data
		SCL	O	I2C clock out
		I2S_SCLK	O	I2S serial clock out
		PWM1	O	PWM channel 1
IO19	47	APS_SWCLK	I	APS serial wire debug clock input
		SDA	IO	I2C bi-directional data
		I2S_WS_OUT	O	I2S word select output
		PWM0	O	PWM channel 0
IO22	17	UART1_TX	O	UART1 transmit data output
		UART0_TX	O	UART0 transmit data output
		PWM2	O	PWM channel 2
		PDM_CLK	O	PDM clock out
IO24	2	SPI2_CLK	I	SPI2 slave clock input

Pin	Loc.	Signal Name	Signal Dir.	Signal Description
		I2S_SCLK	O	I2S serial clock out
		PDM_CLK	O	PDM clock out
		PWM4	O	PWM channel 4
IO25	3	SPI2_CS	I	SPI slave chip select input
		I2S_WS_OUT	O	I2S word select output
		PDM_RXD	I	PDM receive data input
		PWM5	O	PWM channel 5
IO28	4	SPI2_MISO	O	SPI slave data out (TXD)
		UART0_TX	O	UART0 transmit data output
IO29	5	SPI2_MOSI	I	SPI slave data input (RXD)
		UART0_RX	I	UART0 receive data input

For detailed configuration, please refer to the application note.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU and Memory

5.1.1. CPU

The OPL2500 implements two low-power ARM® 32-bit Cortex-M0/M3 microprocessors with the following features:

- 3-stage pipeline to support clock frequencies up to 176 MHz
- 16/32-bit Instruction set for high code-density
- 32 interrupt vectors from 64 interrupt sources

Main CPU interfaces include:

- Cortex-M0/M3 RAM/ROM Interface for instruction and data
- Cortex-M0/M3 AHB/APB Interface for fast peripheral access
- Interrupt with external and internal sources
- SWD (Serial Wire Debug) interface for code debugging

5.1.2. Flash

The OPL2500 supports up to 8 x 16 MB of external QSPI Flash with hardware encryption based on AES to protect developer's programs and data. OPL2500 is packaged with an 8Mb QSPI flash.

The OPL2500 can access external QSPI Flash through a high speed, quad-line SPI interface with the following features:

- Up to 16MB of external Flash are memory mapped into the CPU code space, with 8-, 16- and 32-bit accesses supported for code execution
- Up to 8MB of external Flash/SRAM are memory mapped into the CPU data space, with 8-, 16- and 32-bit accesses supported for data read on Flash/SRAM and data write on SRAM

5.2. Timers

5.2.1. 32-bit Timer

There are two general-purpose timers embedded in the OPL2500.

The timers include the following features:

- A 32-bit time-base counter
- Count down time-base counter
- Halt and resume of time-base counter
- Interrupt held until cleared
- Software-controlled instant reload
- Interrupt generation

5.2.2. Watch Dog Timer

The OPL2500 supports two watchdog timers: one in Cortex-M0 and the other with Cortex-M3. These watchdog timers are provided for recovery from runaway process. The watchdog timers are based on a 32-bit down-counter that is loaded with pre-defined value.

If the interrupt is not cleared by the time the counter reaches zero, the watchdog module asserts the reset signal.

The OPL2500 watchdog timers have the following features:

- Two system watchdogs for M3, M0, each can be configured or disabled separately
- Programmable timeout period for each
- 32-bit counter

5.3. Radio

The OPL2500 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- Bias and regulators
- Balun and transmit-receive switch†

† Optional internal T/R switch by-pass mode available

- Integrated dual mode Power Amplifier (PA)

5.4. Wi-Fi Media Access Controller (MAC)

MAC controls the transmission and reception of 802.11 frames. The OPL2500 implements a unique soft-MAC architecture where timing-critical tasks are handled automatically in hardware MAC engine, while tasks such as scheduling, frame parsing, etc. are performed by the low-power Cortex M0 core. On the transmit side, the layer 2 LLC driver prepares the frame data and deposits them in the transmit queues. The MAC engine starts the transmission when the channel access procedure is completed. On the receive side, frame data from the physical layer are sorted by this MAC engine according to receive frame types and sent to the upper layer for further processing when needed. In cases where acknowledgement is required after reception of a frame, MAC can be configured to enable automatic acknowledgement.

Supported features include:

- 802.11b/g/n/ax features
- MPDU aggregation/de-aggregation
- Block acknowledgement
- Station (STA) mode
- Infrastructure mode
- Passive & active scanning
- RTC/CTS, NAV, IFS, TSF
- Power save mode
- MIB statistics

5.5. Wi-Fi Physical Layer (PHY)

PHY interacts with the 2.4GHz radio and the MAC engine. It processes data from MAC for better adapted to the channel condition, and for achieving better bandwidth efficiency. On the receive side, PHY is responsible for recovering and decoding the receive data with the inherent channel impairments.

Supported features include:

- 802.11b/g/n/ax
  - Support Legacy, Mixed (Long and Short GI), Green Field and HE formats
  - Data rate up to 86Mbps
- Automatic Gain Control (AGC)
  - Channel quality statistics, include frequency / timing offset and RSSI

5.5.1. Wi-Fi Firmware

The OPL2500 Wi-Fi Firmware provides the following functions:

- Infrastructure BSS Station mode support
- WPA/WPA2-Personal/WPA3-Personal
- Open interface for various upper layer authentication schemes over EAP such as TLS, PEAP, LEAP
- Clock/Power gating combined with 802.11-compliant power management to dynamically adapt to current connection condition for minimal power consumption
- Adaptive rate fallback algorithm to set the optimal transmission rate and transmit power based on actual Signal Noise Ratio (SNR), packet loss information, etc.
- Facilitates automatic retransmission and ACK response with the MAC

5.6. Bluetooth Low Energy

The OPL2500 integrates Bluetooth Low Energy (LE) link controller and Bluetooth baseband which executes low-level link routines, such as modulation/ demodulation, packet processing, bit stream processing, frequency hopping, etc.

5.6.1. Bluetooth Low Energy Radio and Baseband

The OPL2500 LE Radio and Baseband support the following features:

- Support 1Mbps, 2Mbps and Long Range (125Kbps or 500Kbps) rates
- Up to 10dBm of output power with over 30dB dynamic control range
- High performance NZIF receiver sensitivity with over 98dB dynamic range
- Bluetooth Link Controller
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening, and transmit pulse shaping
- AFH
- Power management for low power applications

- SMP with 128-bit and 256-bit AES

5.6.2. HCI Interface

OPL2500 provides control to external host through the UART HCI interface.

5.6.3. Bluetooth Stack

The Bluetooth stack of the OPL2500 is compliant with the Bluetooth v5.2 BLE specifications.

5.6.4. Bluetooth Link Controller

The link controller supports up to eight LE links. Supported features include:

- Advertising
- Multiple connections
- Asynchronous data reception and transmission
- Adaptive frequency hopping and channel assessment
- Connection parameter update
- Data length extension
- Link layer encryption
- LE Ping

5.7. Network Stack Support

The OPL2500 has all necessary network stacks embedded, including:

- TCP/UDP/IPv4/IPv6
- ICMP/ARP
- IGMP
- DNS client / DHCP client / HTTP client
- TLS
- SNTP/TFTP
- Socket interface

5.8. DMA Controller

OPL2500 provides two DMA controllers with a total of five channels. The DMA source/destination can be memory or peripheral; the latter includes UART, SPI and I2C. Furthermore, both single-block transfers, and multi-block transfers using linked list and linked list pointers are supported.

6. INTERFACES

The OPL2500 provides various control interfaces for easy access to chip features from customer applications.

6.1. General Purpose Input/Output (GPIO)

Up to thirty-seven (37) general purpose IO pins are provided for various peripherals and input or output functions.

6.2. Peripheral Interfaces

Functions supported in this module include UART, Serial Peripheral Interface (SPI), I2C, I2S, camera interface, and Pulse Width Modulation (PWM).

6.2.1. UART

The UART transport supports baud rates of 115200, 460800, 921600, 1.5M, and 3M bits per second. Hardware based auto-baud rate detection is supported when the crystal frequency other than the default 20MHz is used. Besides, hardware flow control through RTS & CTS is also supported.

6.2.1.1. Timing Specifications

Table 3 shows the UART AC characteristics followed by timing diagram in Figure 6.

Table 3: UART Timing Specifications

Symbol	Parameter	Min	Max	Unit
t1	Delay time, UART_CTS_N low to UART_TXD valid		21	Baud rate cycles
t2	Setup time, UART_CTS_N high before midpoint of stop		11	ns
t3	Delay time, midpoint of stop bit to UART_RTS_N high		2	Baud rate cycles

Figure 3: UART Timing Diagram

6.2.2. Serial Peripheral Interface (SPI)

Four SPI modules are supported in OPL2500 with three of them operate in master mode at a maximum frequency of 100MHz and one operates in slave mode. Each master SPI has six interface signals, of which up to four can be used for data transfer enabling higher throughput. In addition, one of the three master-SPI modules has execute-in-place (XIP) capability. The slave-SPI has four interface signals, of which two are used for data transfer. The OPL2500 DMA controller can be used to transfer data to/from any of the four SPI modules. SPI0 is used to interface to an external flash for firmware/application code download. Furthermore, the Master-SPI supports single-bit, dual-bit and quad-bit modes.

6.2.2.1. External Serial Flash

In one usage case, firmware boot code determines if valid code and system configuration are stored in the serial flash before loading them to internal SRAM for execution. If there is no valid

signature in the serial flash, code download from an external host to the serial flash can occur if the UART interface is detected and correct escape sequence received from it. Also, the chip internal ROM will contain valid code so that the external serial flash will only contain customer application code and maybe system static and dynamic configuration information.

The OPL2500 provides native support for flash devices including but not limited to the following:

- Atmel®: AT25BCM512B
- MXIC®: MX25V512ZUI-20G
- MXIC®: MX25V8035F
- GIGA-DEVICE®: GD25Q80C
- WINBOND®: W25Q80DV
- Puya P25Q80SH-SSH-1R

6.2.3. I2C

The two-wire I2C serial interface consists of a serial data line (SDA) and a serial clock (SCL) supporting both master mode and slave mode.

6.2.3.1. Features

The I2C supports the following features:

- Speed supported are: Standard mode up to 100 kbps and Fast mode of 400 kbps
- 7- or 10-bit addressing

6.2.3.2. Definition of Bits in First Byte

Table 4: Definition of Bits in First Byte

Slave Address	R/W Bit	Description
0000 000	0	General Call Address to store data in the receive buffer and to issue a General Call interrupt.
0000 000	1	START byte.
0000 001	X	CBUS address.
0000 010	X	Reserved.

Slave Address	R/W Bit	Description
0000 011	X	Reserved.
0000 1xx	X	High-speed master code.
1111 1xx	X	Reserved.
1111 0xx	X	10-bit slave addressing.

6.2.4. AUXADC

The OPL2500 contains a 10-bit ADC supporting 16 analog channels – these channels share IO pins with digital GPIOs. Taking ADC sample is controlled by internal firmware driver with the setting of the start conversion signal and with the subsequent reading of the ADC output sample when conversion is completed. Furthermore, auto sampling of channels by hardware are also supported; the channels to be scanned can be controlled by either firmware or by a predefined fixed order. Beyond the 16 analog channels, the ADC can also measure internal chip internal sources such as VBAT, temperature sensor, band gap, etc.

6.2.5. Pulse Width Modulation (PWM)

There are six PWM channels supported in the OPL2500, each with 10 bits to support 1/1000 resolution. PWM clock sources include the main crystal, 32k crystal, or the 32k RC clock. There are two operation modes: regular PWM and LED flashing. The latter contains the following states:

- Dull state:
  with the lowest brightness
- Ramp up state:
  going from the lowest to the highest brightness
- Bright state:

the highest brightness state with a programmable duration

- Ramp down state:
  going from the highest to the lowest brightness

6.2.6. I2S

The I2S module is a serial audio interface with two channels; one each for transmitter and receiver . It is compatible with the Philips I2S serial protocol with both master and slave modes of operation and with data resolutions of 12, 16, 20, 24 and 32 bits.

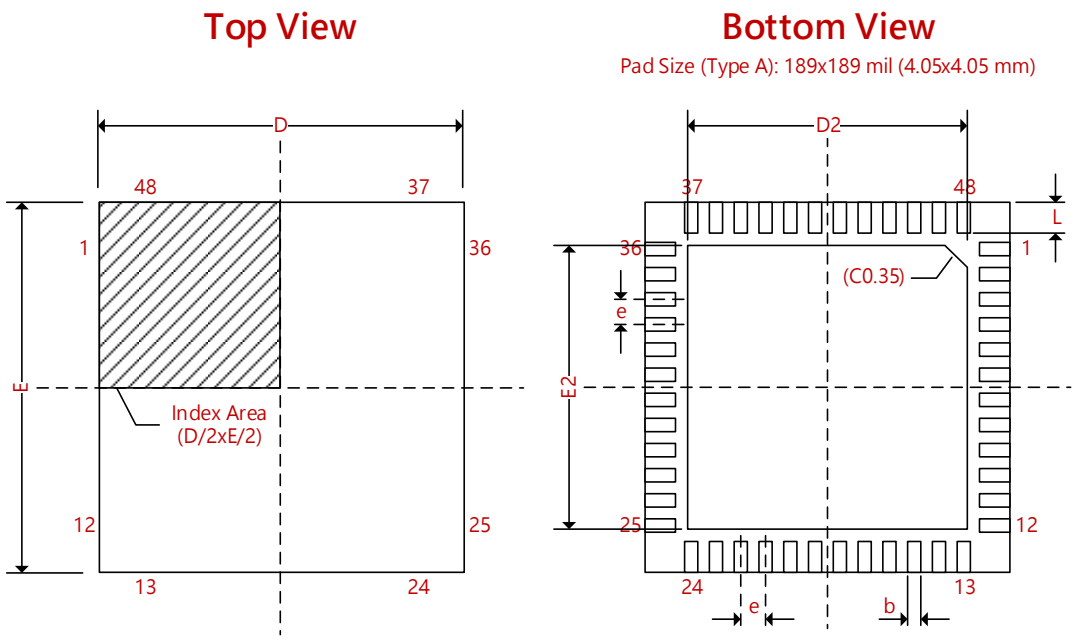
7. SECURITY

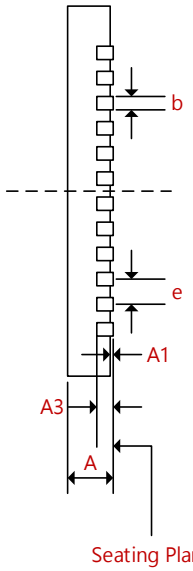
Industry leading hardware-based security accelerator is included in the OPL2500. The supported features include the following:

- Software API support:
  - AES-CCM Encryption/Decryption
  - AES-ECB Encryption/Decryption
  - AES CMAC
  - HMAC-SHA1
  - SHA-1/SHA-224/SHA-256
  - TRNG (True random number generation)
  - ECDH Key Pair Generation
  - ECDH Shared-secret (DH Key) Generation
- Wi-Fi security support:
  - 802.11i-2007
  - WPA-PSK (TKIP) / WPA2-PSK (AES) / Mix Mode
- LE security support:
  - Security manager
  - Improved privacy with low power consumption (LE Privacy 1.2 and Secure Connections)
  - P256 Key Pair (ECDH Key Pair)

8. PACKAGE INFORMATION

Figure 4: OPL2500 QFN48 Packaging Drawing





Symbol	Package Type		
	TQFN		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
L	0.30	0.40	0.50
e	0.40 BSC.		

		Exposed Pad Dimension		
Type A	Pad Size	D2/E2		
	189x189	Min	Nom	Max
	(4.05x4.05)	3.95	4.05	4.15

9. ORDERING INFORMATION

Part Number	Package	Description	Ambient Operating Temperature
OPL2500A0	6x6mm QFN	2.4GHz single band Wi-Fi 802.11b/g/n/ax+LE 5.2	-30 to 70°C

CONTACT

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