

Kinetic inductance Traveling-wave amplification
through Three-wave mixing with amorphous
Tungsten Silicide

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Abstract

Superconducting circuits are a promising platform for quantum computers due to their anharmonic oscillators, which can be fabricated and measured using well-established protocols. However, one major challenge in creating a good quantum computer is the readout signal, which is often weak and accompanied by a high level of noise. To overcome this challenge, we have developed a Three-Wave Mixing Kinetic Inductance Traveling-Wave Amplifier that utilizes the special characteristics of tungsten silicide in a superconducting state.

Our amplifier operates in a three-wave mixing fashion, significantly reducing the power of the microwave pump tone and associated parasitic heating compared to conventional four-wave mixing amplifiers. This allows for improved efficiency and performance. The amplifier utilizes tungsten silicide (WSi) as a waveguide with Kinetic inductance traits and incorporates aluminum fingers for capacitance, creating a 50Ω artificial transmission line with a controlled amplification bandwidth. The use of WSi allows for a smaller amplifier area while still achieving a theoretically predicted gain of 16dB across a 5GHz bandwidth.

In this thesis, we present a theoretical model and experimental characterization of our Three-Wave Mixing Kinetic Inductance Traveling-Wave Amplifier. Our model, based on [12, 50], demonstrates the potential for this amplifier to improve readout signals in quantum computers, addressing a major challenge in the field.

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Chapter 1

Introduction

The 21st century is an exciting time for the field of experimental quantum physics. The collaboration between academia and industry has led to a rapid advancement in our understanding of quantum systems and the development of new technologies and products. One of the most promising areas of research is the development of quantum computers using superconducting qubits and amplifiers.

In this thesis, we will take a closer look at superconducting amplifiers and their potential to improve the efficiency and capabilities of superconducting qubits in quantum computing. One of the key components of superconducting amplifiers is the superconducting kinetic inductance, which plays a crucial role in the amplifier's performance. The nonlinear properties of superconducting kinetic inductance are particularly important in making the amplifier more efficient and effective. Through a review of existing literature and original research, we aim to gain a deeper understanding of the properties and characteristics of superconducting amplifiers and their potential applications in this field. Additionally, we will present the theory and outcomes of an amplifier that we have built in our lab. Our goal is to contribute to the ongoing efforts to advance quantum computing and further explore the potential of superconducting amplifiers. The following chapters delve into the introduction of quantum computation and its particular emphasis on amplifiers based on nonlinear kinetic inductance. Their advantages and future prospects are explored. Chapter 2 provides a comprehensive background on the fundamental theories and knowledge necessary to understand the rest of the thesis. In Chapter 3, we apply the theories developed in Chapter 2 to the design of our amplifier. This includes a discussion on the design methodology, the simulations performed to evaluate its benefits, limitations, and characteristics. Chapter 4 describes the equipment, instruments, and techniques used in the fabrication and measurement of the amplifier. A step-by-step description of the fabrication process and the results obtained from these techniques are also presented in this chapter. Finally, in Chapter 5, we present the results of measuring the amplifier and analyze their significance, as well as discuss potential applications.

1.1 Superconducting Supremacy in Quantum Information

In the four decades since Richard Feynman proposed using quantum computers for simulating physics[21], the field has grown to encompass a wide range of applications, including cryptography [41], synchronization[18], and quantum sensing[49, 52]. Among the various subfields of quantum technology, the universal quantum computer stands out as a particularly powerful tool superior to the strongest classical computers for particular problems of interest[17]. However, realizing a functional quantum computer requires reliable qubits and quantum gates, high gain signals, low losses, and small noise interference similar to how classical computers rely on classical logic gates and bits.

Finding suitable qubits poses a significant challenge, as not all quantum systems are reliable or suitable for this purpose. While quantum mechanics governs our physical world, humans are accustomed to the principles of classical physics, as the vast number of degrees of freedom in open quantum systems can quickly destroy quantum behavior. Therefore, reliability in quantum computation depends on isolating the qubits, which is not always easy to achieve while also ensuring they remain controllable for gate operations. Additionally, qubits must also have the ability for fast readout of their state.

1.1.1 Qubit Candidates

Qubits, or two-level systems (TLS) that exhibit quantum mechanical behavior, can come in various forms. However, certain candidates stand out due to their advantages.

Trapped ions, for example, can be used as qubits by utilizing the electronic orbital levels of atoms as the states of the qubit, by virtue of the anharmonicity of these levels [6]. This system has a long lifespan, but the small size of the ions can make operation difficult. Additionally, gaseous ions must be controlled by high-power lasers in ultra-high vacuum to avoid scattering with the air and the coupling to trapped ions can be challenging [53].

Another potential qubit candidate is the nitrogen-vacancy (NV) center in diamond. When a carbon atom is replaced with a nitrogen atom and a nearby site is depleted of its carbon atom, the nitrogen atom's valence electron spin functions as a TLS. NV centers can operate at room temperature, but the limited couplings available and the natural network determined by the surrounding carbon atoms can be a disadvantage.

Finally, superconducting qubits are essentially anharmonic LC resonators that utilize the nonlinear inductance of Josephson junctions as the source of anharmonicity. These qubits have several benefits such as controllable design and operation, long lifetimes, and the capability of isolating the systems. However, the major disadvantage of superconducting qubits is that they require cryogenic temperatures for operation, which can be difficult to maintain in non-specialized labs.

1.1.2 Advances in Superconducting Qubits: Current Applications and Future Potential

Superconducting (SC) qubits have been the subject of intense research for nearly two decades. The physics of SC qubits has been extensively studied, resulting in the development of new versions that offer improved control, tunability, reduced noise, and longer coherence times.

Despite the fact that full-scale universal quantum computers are not yet available, SC qubits are already being employed or researched in various contexts by major commercial enterprises such as Google and IBM. In fact, as of this writing, anyone can run simple algorithms online using a few SC qubits, free of charge.

One of the major advantages of SC qubits is that they do not require installation in personal homes or research institutions. Instead, they can be concentrated at a common institute and operated remotely at the international or national level. This also addresses the issue of temperature control, which is a significant challenge in the development of quantum computers.

1.1.3 Optimizing the Performance of Superconducting Qubits: The Role of the Operating Environment

The environment in which SC qubits operate plays a crucial role in determining their performance and capabilities. In addition to serving as a unit for quantum information storage and manipulation, SC qubits also have the potential to generate single photons.

To fully utilize the potential of SC qubits, they must be supported by a range of structures and equipment, both on the SC chip itself and at the macroscopic level. This includes other SC devices such as readout resonators and flux bias lines, as well as electronic equipment and packaging for physically mounting the qubits in the refrigerator.

It's also worth mentioning that the amplifier plays a vital role in this environment, as it amplifies the signals coming from the SC qubit, which is important for the operation and control of the qubits. Amplifiers also help to improve the efficiency and capabilities of superconducting qubits, making it an essential component of the overall environment.

In short, the strength of SC qubits is only fully realized when considered in conjunction with the supporting structures and equipment that make up the environment in which they operate.

1.1.4 Amplifiers based on nonlinear kinetic inductance

low-noise broadband amplifiers are critical for a variety of applications such as the multiplexed readout of astronomical detectors [14, 32, 62] and superconducting qubits, the manipulation of mechanical resonators coupled to microwave cavities [54], and the study of nonclassical states of microwave light [10, 19]. These experiments often use high electron mobility transistor (HEMT) amplifiers, which typically have a noise temperature of 2–5 K in the 4–8 GHz range [2]. This noise is 10–40 times above the standard quantum limit, the fundamental limit imposed by quantum mechanics [11].

Over the past decade, there has been rapid development of quantum-limited microwave amplifiers, including particularly Josephson parametric amplifiers (JPAs) [5, 9, 29]. JPAs use the dissipationless nonlinearity of Josephson junctions in a parametric process to achieve gain. Both narrowband JPAs, based on junction-embedded resonant architectures, and broadband JPAs, based on junction-embedded transmission lines, have been developed and have demonstrated near quantum-limited noise performance [42, 48]. However, the $\sim 10 \mu\text{A}$ critical current of the junctions limits the dynamic range of these devices and excludes them from some important applications, such as the multiplexed readout of thousands of qubits or detectors. In addition, fabricating a large number (> 1000) of junctions with the high yield is a nontrivial task.

Recently, another type of a broadband parametric amplifier based on the nonlinear kinetic inductance of NbTiN transmission lines has been proposed[1, 7, 12, 30, 43, 56]. These devices are simple to fabricate, requiring only one lithography step (patterning of the NbTiN film). Due to the 1mA critical currents of the films, the amplifier saturation power is 5–6 orders of magnitude higher than JPAs, making them promising for readout of a large array of detectors or qubits. In contrast with reflection-type resonant JPAs, the travelingwave architecture of the NbTiN amplifier eliminates the need for a circulator, enabling on-chip integration with a detector or qubit. In previous work, NbTiN amplifiers were realized as long coplanar waveguide (CPW) transmission lines, with > 20 dB gain over several GHz bandwidth. Despite the excellent gain performance, the CPW amplifier has a few drawbacks. To achieve ≥ 15 dB gain, a CPW over 2 m long is used, which can result in a low fabrication yield.

In this work, we adopt the chip structure that was previously proposed by Chaudhuri et al. [12] and Malnou et al. [43]. However, we make an improvement by replacing NbTiN with WSi as the main waveguide and Aluminum as the fingers instead of NbTiN. This alteration leads to an increased capacitance provided by the Aluminum and improved kinetic inductance behavior due to the unique characteristics of WSi. This results in the maintenance of the favorable performance attributes of the NbTiN amplifier, while significantly reducing the size of the chip from $2 \times 2 \text{ cm}^2$ as reported in [43] to $6.25 \times 6.25 \text{ mm}^2$.

Chapter 2

Background

2.1 Superconductivity and Critical current

This section aims to provide a comprehensive overview of the fundamental concepts of superconductivity that are relevant to our experiments. The discussion begins with an introduction to the theoretical foundations of superconductivity and then proceeds to elaborate on the behavior of the critical current, specifically in the context of WSi. To achieve this goal, we rely on key sources, including the works of [55, 57, 58]. The section also delves into the electromagnetic phenomenology and the London equations, which play a vital role in understanding the behavior of superconductors.

2.1.1 Electromagnetic phenomenology and London equations

The fundamental electromagnetic properties that define a superconductor at a temperature lower than the critical temperature T_C include perfect DC conductivity and perfect diamagnetism, also known as the Meissner effect. This effect is characterized by the expulsion of magnetic fields in the material, except for a thin external layer of thickness λ - the penetration depth. This layer is typically around $\lambda \approx 500\text{\AA}$ in thickness.

As superconductors must produce currents to screen magnetic fields, there exists a critical field strength H_C beyond which it becomes energetically unfavorable to expel the field, resulting in the material returning to its normal state. The energy required to cancel the critical field is the difference between the free energies of the normal and superconducting states, which can be represented by the equation:

$$\frac{\mu_0 H_C T^2}{2} = f_n(T) - f_s(T) \quad (2.1)$$

Where f_n and f_s are the Helmholtz free energies per unit volume of the normal and superconducting states.

In 1935 [39], the London brothers proposed a phenomenological theory that accounts for these properties. According to their theory, superconductivity is established by super electrons, whose fractional density n_s/n is zero above T_C and approaches 1 when $T = 0$. The dynamics of the supercurrent \vec{J}_s of the superelectrons are governed by the London equations, which are:

$$\frac{\partial}{\partial} \left(\Lambda \vec{J}_c \right) = \vec{E} \quad (2.2)$$

and

$$\vec{\nabla} \times \left(\Lambda \vec{J}_c \right) = -\vec{B} \quad (2.3)$$

Where Λ is the London parameter, defined as:

$$\Lambda \equiv \frac{m_e}{n_s e^2}. \quad (2.4)$$

Equation 2.2 implies perfect conductivity, as it describes the free acceleration of the superelectrons by the electric field. Equation 2.3 when combined with Ampere's law, yields:

$$\vec{\nabla}^2 \vec{B} = \frac{\vec{B}}{\lambda_L^2}, \quad (2.5)$$

Where $\lambda_L \equiv \sqrt{\Lambda/\mu_0}$ represents the exponential decay of the magnetic field with a characteristic length of λ_L , as observed in the Meissner effect. This length is known as the London penetration depth. It is crucial to note that the superconducting kinetic inductance plays a crucial role in this theory, as it determines the nonlinear properties of the superconductor, which are vital to making the amplifier more efficient.

2.1.2 Ginzburg-Landau theory

The Ginzburg-Landau (GL) theory, developed in the 1950s, is a phenomenological theory that can account for phenomena not explained by the London theory. It can handle cases where the superelectron density is not spatially uniform, and it has a natural connection to the microscopic theory.

The GL theory is an extension of Landau's theory of second-order phase transitions. It assumes the existence of a complex order parameter $\Psi(\vec{r})$, which is spatially dependent and whose magnitude squared is related to the superelectron density: $\Psi^* \Psi \equiv n_s$. Since Ψ is spatially dependent, the free energy F needs to be expanded in gradients of Ψ as well. Additionally, when magnetic fields are included, F should be gauge-invariant and real.

Minimizing the free energy expansion with respect to Ψ^* and the vector potential \vec{A} yields the Ginzburg-Landau equations:

$$\frac{1}{2m} \left(-i\hbar \vec{\nabla} - 2e\vec{A} \right)^2 \Psi + (\alpha + \beta \Psi^* \Psi) \Psi = 0 \quad (2.6)$$

and

$$\vec{J}_s = \frac{-i\hbar e}{m} \left(\Psi^* \vec{\nabla} \Psi - \Psi \vec{\nabla} \Psi^* \right) - \frac{4e^2}{m} \vec{A} \Psi^* \Psi, \quad (2.7)$$

where $\alpha(T) \propto (T - T_C)$ and $\frac{\beta}{2} = const > 0$ are the coefficients of the first and second order terms in $\Psi^* \Psi$ in the expansion of F .

In the absence of magnetic fields, just above T_C , if there is a place with a small non-zero Ψ , we will get from Equation 2.6 (by neglecting $\Psi^* \Psi$)

$$\vec{\nabla}^2 \Psi = \frac{\Psi}{\xi_{GL}^2} \quad (2.8)$$

with

$$\xi_{GL} \equiv \sqrt{\frac{\hbar^2}{2m|\alpha|}}, \quad (2.9)$$

which implies that Ψ decays exponentially to its equilibrium value (zero above T_C) with a characteristic length ξ_{GL} . This length is known as the Ginzburg-Landau coherence length.

If the superconducting sample is larger than the penetration length, the magnetic field inside it will vanish. This implies that the free energy will be minimized if $\vec{\nabla}\Psi = 0$, which yields using Equation 2.6: $\Psi^*\Psi = \frac{-\alpha}{\beta}$. Substituting this value in Equation 2.7 and applying curl on both sides gives an equation with the same form as Equation 2.3. Thus we will get an expression for the Ginzburg-Landau penetration depth

$$\lambda_{GL} = \sqrt{\frac{m\beta}{4e^2\mu_0|\alpha|}}. \quad (2.10)$$

An important point to note is that λ_{GL} is typically much smaller than λ_L , and as a result, the GL theory is able to account for phenomena that occur on a much smaller scale than those described by the London theory.

2.1.3 BCS theory

The Bardeen-Cooper-Schrieffer (BCS) theory of superconductivity, proposed in 1957 [3, 13], provides a successful explanation for conventional low-temperature superconductivity. The theory posits that in the presence of a weak attractive force, the formation of bound pairs with opposite spin and orbital momentum, $(\vec{k}\uparrow - \vec{k}\downarrow)$, is energetically favorable. The attractive interaction between the two negatively-charged electrons is assumed to be due to an electron-phonon-electron interaction.

The BCS ground state at $T = 0$ is given by the following wave function:

$$|BCS\rangle \equiv \prod_{\vec{k}} \left(u_{\vec{k}} + v_{\vec{k}} c_{\vec{k}\uparrow}^\dagger c_{\vec{k}\downarrow}^\dagger \right) |0\rangle \quad (2.11)$$

where $|0\rangle$ is the vacuum state, $c_{\vec{k}\sigma}^\dagger$ is the Fermionic creation operator of a particle with spin σ and orbital angular momentum \vec{k} , and $|u_{\vec{k}}|^2 + |v_{\vec{k}}|^2 = 1$. The state is characterized by an undetermined number of particles N , but with a definite phase. The probability of the pair $(\vec{k}\uparrow - \vec{k}\downarrow)$ being occupied (unoccupied) is $|v_{\vec{k}}|^2$ ($|u_{\vec{k}}|^2$).

The Hamiltonian that describes the interactions of this state is the pairing Hamiltonian:

$$H \equiv \sum_{\vec{k}\sigma} \epsilon_{\vec{k}} c_{\vec{k}\sigma}^\dagger c_{\vec{k}\sigma} + \sum_{\vec{k}\vec{l}} V_{\vec{k}\vec{l}} c_{\vec{k}\uparrow}^\dagger c_{-\vec{k}\downarrow}^\dagger c_{\vec{l}\uparrow} c_{-\vec{l}\downarrow} - \mu \hat{N}, \quad (2.12)$$

where $\epsilon_{\vec{k}}$ is the single-particle energy, $V_{\vec{k}\vec{l}}$ is the (attractive) interaction matrix element for scattering of $(\vec{l}\uparrow - \vec{l}\downarrow)$ to $(\vec{k}\uparrow - \vec{k}\downarrow)$, μ is the chemical potential, and \hat{N} is the (total) particle number operator.

By minimizing the expectation value of $|BCS\rangle$ with respect to this Hamiltonian, the values of the parameters $v_{\vec{k}}, u_{\vec{k}}$ can be calculated, which allows for the determination of the condensation energy, or the energetic gain of the system being in

the superconducting state $|BCS\rangle$ rather than in the normal state. Under the assumption of a simple weak attractive potential and weak coupling, the condensation energy is given by:

$$\langle E \rangle_s - \langle E \rangle_n = -\frac{1}{2}g_0\Delta^2, \quad (2.13)$$

where g_0 is the density of states at the Fermi level (for a definite spin) and Δ is the energy gap. This energy gap is a measure of the size of the region around the Fermi energy in which pairs are occupied, with a binding energy of Δ .

It should be noted that the BCS theory is based on the assumption of weak coupling between the electrons and the phonons, which is true for conventional superconductors such as aluminum and WSi the materials we use on our chip and highly relevant for our study. However, for high-temperature superconductors, the electron-phonon coupling is much stronger, and the BCS theory is not able to fully explain the properties of these materials. Alternative theories, such as the theory of strong-coupling superconductivity and the theory of d-wave superconductivity have been proposed to explain the properties of high-temperature superconductors.

Despite its limitations, the BCS theory remains an important and widely used framework in the study of superconductivity. It has been used to calculate various properties of superconductors such as the critical temperature, the energy gap, and the critical magnetic field. The theory has also been applied to other areas of physics such as nuclear physics and condensed matter physics, where the concept of pairing of particles plays a crucial role.

To sum up, the BCS theory is a successful theory in the realm of conventional low-temperature superconductors. This theory is founded on the concept of a feeble attractive force between electrons, resulting in the creation of bound pairs having inverse spin and orbital momentum. This theory is exceedingly applicable in calculating the diverse properties of superconductors, particularly in the context of Aluminum and WSi, which has significant benefits for experimental physics. It has also been expanded to other domains of physics. Nonetheless, it is crucial to note that this theory is only relevant to conventional superconductors and that alternative theories are required to clarify the features of other categories of superconductors.

2.1.4 Critical current of superconductors

The critical current, also known as the depairing current, is a fundamental concept in the field of superconductivity. It is defined as the maximum current density that a superconductor can carry without losing its superconducting properties. The critical current density, J_c , is a material-dependent parameter that is sensitive to various factors such as temperature, magnetic field, and the microstructure of the material[16].

The critical current density can be calculated using the Ginzburg-Landau (GL) theory, which describes the behavior of superconductors in the vicinity of the critical temperature. According to this theory, the critical current density is proportional to the square of the order parameter Ψ , which represents the amplitude of the superconducting condensate as follows

$$J_c \propto |\Psi|^2 \quad (2.14)$$

The critical current density can also be measured experimentally using various techniques such as the four-probe method [40], the transport method, and the critical

state model. These methods allow for the determination of the critical current density under different conditions such as varying temperature, magnetic field, and microstructure.

The critical current density is an important parameter in the design and optimization of superconducting devices such as superconducting quantum interference devices (SQUIDs), superconducting microwave resonators, and superconducting transmission lines. In these devices, the critical current density sets a limit on the maximum current that can be carried, which can ultimately affect the performance of the device.

Critical current Of SC microstrip WSi circuit

In our lab, previously experimented and measured [25], by cooling down the devices made from strips of WSi which contain different areas, to a temperature of 30 mK, which means that we cannot rely solely on the GL theory to calculate the critical current of their devices. Instead, we focus on tungsten silicide (WSi) which has a large kinetic inductance due to its smaller cross-sectional area A (as discussed in Chapter 2.3.2). To determine the critical current of WSi, our lab , conducted measurements using DC current on six different test-wires in two different cooldown sessions. The results are shown in Figure 2.1.

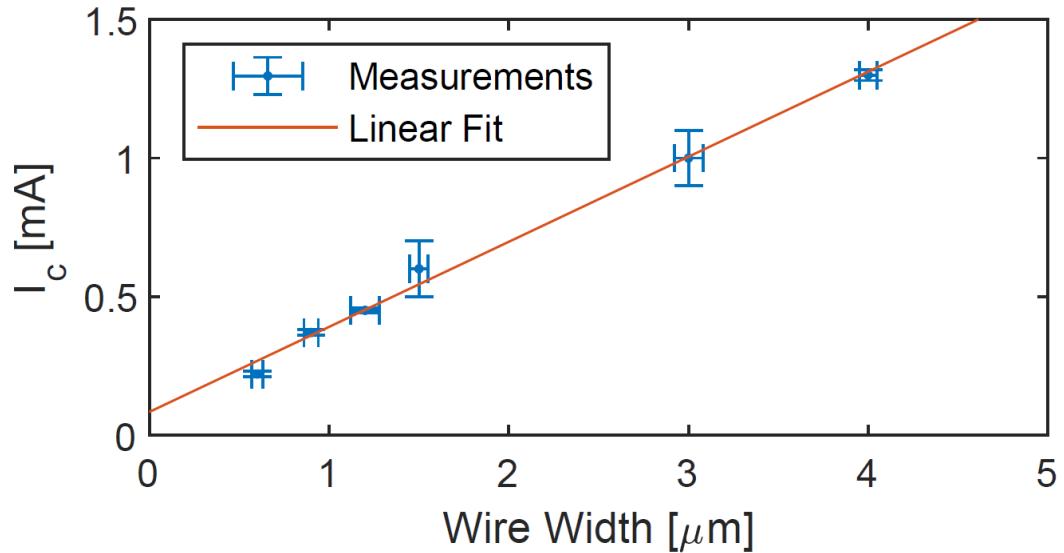


Figure 2.1: Critical current vs. width (proportional to cross section) of $\sim 11 - 13\text{nm}$ thick WSi wires. This graph was created from six different test-wires measured with DC current in two different cooldown-sessions. The Figure was taken from [25]

Changing the x-axis to the wire area using the constant wire height to be 12 nm the linear equation of I_c vs wire cross-section area A , using Figure 2.1 data, is:

$$I_c = \eta A \quad (2.15)$$

while $\eta = 2.792e10[A/\text{m}^2]$ a formula that will serve us on Chapter 3.2.

2.2 Classical Electrodynamics

This section delves into a key aspect of classical electrodynamics that is relevant to our discussion of superconductivity. While superconductivity is primarily a quantum phenomenon, its applications and experiments often incorporate classical elements, particularly in the design and construction of large-scale features. Therefore, it is essential to review the classical underpinnings of electrodynamics and their implications for superconductivity in practice.

2.2.1 Elements of Transmission Line Theory

The propagation of current and voltage in transmission lines can be described using the Telegrapher's equations. These equations take into account the important parameters of inductance per unit length (L_l), capacitance per unit length (C_l), resistance (R) and conductance (G) which may be frequency dependent.

$$\frac{\partial V(x, t)}{\partial x} = -L_l \frac{\partial I(x, t)}{\partial t} - RI(x, t) \quad (2.16)$$

$$\frac{\partial I(x, t)}{\partial x} = -C_l \frac{\partial V(x, t)}{\partial t} - GV(x, t) \quad (2.17)$$

When loss is neglected, the equations can be simplified to:

$$\partial_x V(x, t) = -L_l \partial_t I(x, t) \quad (2.18)$$

$$\partial_x I(x, t) = -C_l \partial_t V(x, t) \quad (2.19)$$

This formulation leads to a wave equation with the phase velocity $v_{ph} = 1/\sqrt{L_l C_l}$. Using the phasor ansatz $V = V e^{-i\omega t}$, the solutions to the equations are:

$$V(z) = V_0^+ e^{ikx} + V_0^- e^{-ikx} \quad (2.20)$$

$$I(z) = \frac{V_0^+}{Z_L} e^{ikx} - \frac{V_0^-}{Z_L} V_0^- e^{-ikx} \quad (2.21)$$

where $k = \omega/v_{ph}$ is the wave number and ω is the frequency in units of Hz. The characteristic impedance $Z = \sqrt{L_l/C_l}$ plays an important role in the propagation of waves in a medium. When the impedance changes throughout the transmission line, reflections arise according to the reflection coefficient:

$$\mathbb{R} = \frac{Z_L - Z_{ext}}{Z_L + Z_{ext}} \quad (2.22)$$

It is highly desirable to avoid reflections in quantum circuits, for this reason the load impedance Z_L is usually matched to 50Ω , the standard of the impedance Z_{ext} of commercial electronics, in order to keep the reflection coefficient zero.

In certain cases, Z is varied periodically (so-called dispersion engineering) in the context of wave-mixing dynamics [20] with the purpose of compressing higher order harmonics of the pump, enhancing the amplifier's efficiency. generations of our amplifier presented in Chap. 5, included broadenings of the transmission every few hundred μm for this purpose, leading to band gaps in the transmission spectra.

In summary, The Telegrapher's equations are used to describe the propagation of current and voltage in transmission lines, taking into account the important parameters of inductance, capacitance, resistance, and conductance. The characteristic impedance plays an important role in the propagation of waves in a medium and can be varied periodically to enhance the amplifier's efficiency.

2.2.2 The Transmission (ABCD) Matrix

Many microwave networks consist of a cascade connection of two or more two-port networks. This section follows closely [50]. In this case it is convenient to define a 2×2 transmission, or ABCD matrix, for each two-port network. We will see that the ABCD matrix of the cascade connection of two or more two-port networks can be easily found by multiplying the ABCD matrices of the individual two-ports.

The ABCD matrix is defined for a two-port network in terms of the total voltages and currents as shown in Figure 2.2a and the following:

$$\begin{aligned} V_1 &= AV_2 + BI_2, \\ I_1 &= CV_2 + DI_2, \end{aligned}$$

or in matrix form as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.23)$$

It is important to note from Figure 2.2a that a change in the sign convention of I_2 has been made from the definitions, which had I_2 as the current flowing into port 2. The convention that I_2 flows out of port 2 will be used when dealing with ABCD matrices so that in a cascade network I_2 will be the same current that flows into the adjacent network, as shown in Figure 2.2b. Then the left-hand side of Equation 2.23 represents the voltage and current at port 1 of the network, while the column on the right-hand side of Equation 2.23 represents the voltage and current at port 2.

In the cascade connection of two two-port networks shown in Figure 2.2b we have that

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.24a)$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} \quad (2.24b)$$

Substituting Equation 2.24b into Equation 2.24a gives

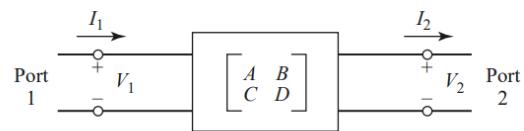
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} \quad (2.25)$$

which shows that the ABCD matrix of the cascade connection of the two networks is equal to the product of the ABCD matrices representing the individual two-ports. Note that the order of multiplication of the matrix must be the same as the order in which the networks are arranged since matrix multiplication is not, in general, commutative.

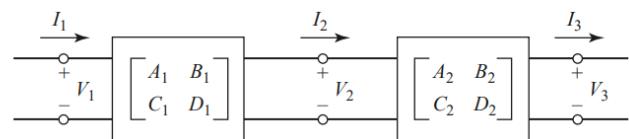
The usefulness of the ABCD matrix representation lies in the fact that a library of ABCD matrices for elementary two-port networks can be built up, and applied in building block fashion to more complicated microwave networks, like we will do later on in Chapter 3.2.1 that consist of cascades of these simpler two-ports.

The special case of a two-port microwave network occurs so frequently in practice and also in our calculations and experiments which can represent the signals that came from each port and go out to each port. In our experiments we insert a signal in port one and measure the signal comes out from port 2 this representation is defined as S_{21} and can be calculated by: [50]

$$S_{21} = 2/(A + B/Z_0 + CZ_0 + D) \quad (2.26)$$



(a)



(b)

Figure 2.2: (a) A two-port network (b) a cascade connection of two-port networks. Those Figures was taken from [50]

2.3 Kinetic Inductance

In this section, we will delve into the fascinating phenomena of kinetic inductance. Specifically, we will focus on the properties and behavior of kinetic inductance in WSi, which are the materials used in the construction of our chip. Kinetic inductance is a relatively new and exciting area of research, and we will explore the underlying physics and the implications of this phenomenon for our chip design.

2.3.1 Kinetic Inductance in Superconductors

In electrodynamics, inductance is a measure of the ability of a conductor to oppose changes in current flow. It can be thought of as electromagnetic inertia, analogous to the concept of mass in mechanics. When a voltage is applied to a conductor, a current will flow, and the proportionality between the voltage and the rate of change of current is known as the inductance. This quantity is often described in terms of the magnetic field created around the conductor (as described by Maxwell's equations).

However, inducing a current in a conductor not only creates a magnetic field with associated energy, but also requires the acceleration of charged particles, which requires additional kinetic energy. To understand this effect, consider a superconductor with cross-sectional area A and length l . The density of Cooper pairs in the superconductor, n_s , is equal to half the density of electrons, n_e . The total kinetic energy of the Cooper pairs, E_k , can be expressed as the kinetic energy of a single pair multiplied by the number of pairs:

$$E_k = \frac{1}{2}(2m_e)v_s^2 \cdot \frac{n_e}{2}Al \quad (2.27)$$

where m_e is the mass of a single electron, and v_s is the velocity of the Cooper pairs.

The current in the superconductor is given by $I = qn_sAv_s = 2e \cdot \frac{n_e}{2}Av_s = en_eAv_s$, where $q = 2e$ is the charge of a Cooper pair and e is the elementary charge. Using this expression for the current and the definition of kinetic inductance,

$$L_{kin} = \frac{1}{2} \frac{m_e l}{n_s e^2 A} = \frac{\mu_0 \lambda_L^2}{A} l, \quad (2.28)$$

where λ_L is the London penetration depth discussed in chapter 2.1.1 , we can rewrite the expression for the total kinetic energy as

$$E_k = \frac{1}{2} L_{kin} I^2. \quad (2.29)$$

The geometric inductance, L_g , is usually orders of magnitude larger than the kinetic inductance, L_{kin} , and the kinetic energy can therefore be neglected. However, in certain superconductors where the velocity of the Cooper pairs is relatively high compared to other materials (and the value of $n_s A$ is correspondingly low), the kinetic inductance can become significant. The ratio of kinetic inductance to the total inductance,

$$\alpha = \frac{L_{kin}}{L_g + L_{kin}}, \quad (2.30)$$

is an important parameter in the study of kinetic inductance materials and will be discussed further in the context of nonlinear wave-mixing.

In the case of very thin films, where the thickness of the kinetic inductance material is a few nanometers and much smaller than the London penetration depth, the value of α can be accurately approximated by the simple expression given in Equation (2.30). However, in other cases it may be necessary to consider additional factors such as the surface inductance and a geometrical factor G that can be calculated using numerical models. But in this work we will limit ourselves to case of very thin films, where the thickness of the kinetic inductance material is a few $nm < \lambda_L/50$. In this regime, α indeed reduces to Equation 2.30 (given that the factor G is close to unity) [22].

2.3.2 Nonlinear Kinetic Inductance in Tungsten Silicide

Tungsten silicide, W_xSi_{1-x} , is a high-kinetic inductance material that has received relatively little attention in the literature. As an amorphous material, the proportion of tungsten to silicon in the alloy can significantly affect the London penetration depth, λ_L , and therefore the kinetic inductance, L_{kin} . In our fabrication process, we have achieved values of α , the ratio of kinetic inductance to total inductance, close to unity, indicating that $L_{kin} \gg L_g$.

However, the kinetic inductance of tungsten silicide also exhibits nonlinear behavior. The inductance per unit length, $L_{kin,l} = \frac{L_{kin}}{l}$, can be expressed as: [22, 30]

$$L_{kin,l} = \frac{\mu_0 \lambda_L^2}{A} \left(1 + \left(\frac{I}{I_*} \right)^2 \right) \equiv L_0 \left(1 + \left(\frac{I}{I_*} \right)^2 \right) \quad (2.31)$$

where I_* is the characteristic current scale of nonlinearity, which is of the order of the critical current, I_c , and will be discussed further in a later section. For typical values of $\lambda_L \approx 0.5 - 1\mu m$ in tungsten silicide transmission lines that are a few micrometers wide and approximately 10 nanometers thick, $L_{kin,l}$ can reach values of 15-60 μH [61].

2.4 Coplanar waveguides

The theory of coplanar waveguides (CPW) is a fundamental concept in the field of microwave engineering. CPW consists of a metallic planar strip placed on a dielectric substrate, with two metallic planes on both sides separated by a gap, as shown in Figure 2.3 . The planar geometry of CPW makes it ideal for fabrication, enabling the creation of scalable devices.

One of the key properties of CPW is the ability to support transverse electromagnetic (TEM) waves, which are characterized by the absence of longitudinal electromagnetic fields. TEM waves have the important property of being independent of frequency, unlike non-TEM waves which have a cut-off frequency below which the wave is exponentially attenuated [50]. Conformal mapping is a powerful tool for solving the 2D static problem of TEM waves in complex geometries [50].

Superconducting CPW, placed on a dielectric substrate, can only support quasi-TEM modes due to the presence of longitudinal electromagnetic fields [60]. However, conformal mapping can still be applied to determine the geometric inductance per unit length, given by [59]

$$L_l = \frac{\mu_0}{4} \frac{K(k_2)}{K(k_1)} \quad (2.32)$$

and capacitance per unit length

$$C_l = 4\epsilon_0 \epsilon_{eff} \frac{K(k_1)}{K(k_2)}, \quad (2.33)$$

where K is the complete elliptic integral of the first kind, k_1 and k_2 are the arguments (see Figure 2.3)

$$k_1 \equiv \frac{w}{w + 2s} \quad (2.34)$$

$$k_2 = \sqrt{1 - k_1^2} \quad (2.35)$$

and ϵ_{eff} is the effective dielectric constant which in general is needed to be calculated numerically [28] but in practice can be approximated as the average of the dielectric constants of the substrate and the air $\epsilon_{eff} \approx (\epsilon_r + 1)/2$ [60].

In addition to the regular geometric inductance, superconductors have another contribution to the inductance from the kinetic energy of the electrons, known as kinetic inductance. This can become non-negligible under certain conditions (see section 2.3).

The properties of CPW and superconducting CPW make them useful in a variety of applications, such as high-frequency signal transmission, microwave filtering, and resonators. As we will discuss in later sections, the characteristics of aluminum make them particularly suitable for use in CPW and superconducting CPW applications.

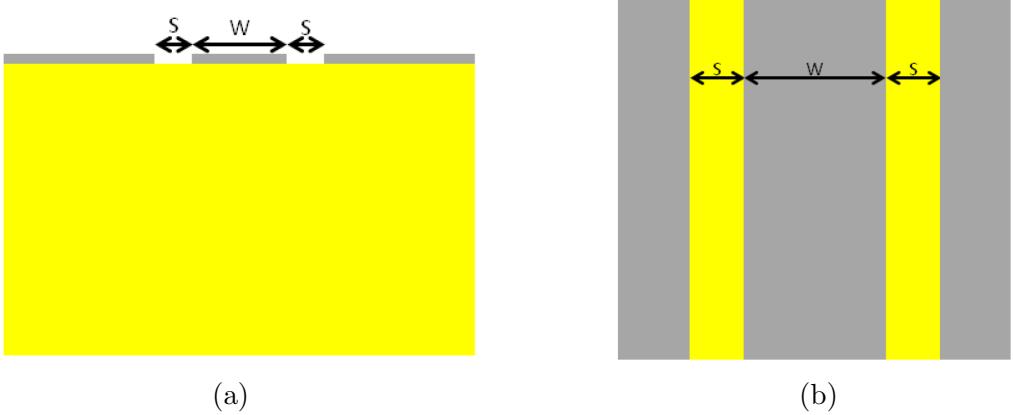


Figure 2.3: A schematic view of a CPW.(a) Side view. (b) Top view. Those Figures was taken from [38]

2.5 Three-wave mixing kinetic inductance traveling-wave amplifier Theory

In this section, we will explore the theory behind kinetic inductance traveling-wave (KIT) amplifiers and specifically, the phenomenon of three-wave mixing (most of the theory is based on [43]). KIT amplifiers utilize the nonlinear kinetic inductance of a superconducting line to generate parametric interactions between pump, signal, and idler photons. This process, known as three-wave mixing (TWM), involves a single pump photon converting into both a signal and idler photon, whereas four-wave mixing (4WM) converts two pump photons in this fashion.

First, as the pump frequency is far detuned from the amplification band, it is easily filtered, which is often necessary to avoid saturating the following amplifier. Second, it reduces the rf pump power because energy is extracted from dc power to convert pump photons, which avoids undesirable heating effects from the strong rf pump, including those happening in the packaging. One of the key advantages of using KIT amplifiers is their ability to generate exponential gain through phase matching. When a KIT amplifier is biased with a DC current I_d , its inductance per unit length, L , can be described by the equation [56]:

$$L = L_d[1 + \epsilon I + \xi I^2 + O(I^3)] \quad (2.36)$$

where I is the RF current, L_d is the amplifier's inductance under DC bias at zero RF currents, $\epsilon = 2I_d/(I_*^2 + I_d^2)$, and $\xi = 1/(I_*^2 + I_d^2)$. The parameter I_* determines the scale of the nonlinearity, which is discussed in more detail in chapter 2.3.2. The term ϵI allows for three-wave mixing, while ξI^2 permits four-wave mixing.

For a pump frequency ω_p , the signal at ω_s and idler at ω_i such that $\omega_p = \omega_s + \omega_i$, the 3WM phase matching condition for exponential gain can be described by the following equation (see chapter 2.5.1):

$$\Delta_k = -\frac{\xi I_{p0}^2}{8}(k_p - 2k_s - 2k_i) \quad (2.37)$$

Here $\Delta_k = k_p - ks - ki$, where k_p, k_s, k_i are the pump, signal, idler wavenumbers, and I_{p0} is the RF pump amplitude at the KIT amplifier's input. In a nondispersive

transmission line, $\Delta k = 0$, and thus Equation 2.37 can naturally be fulfilled over a very wide frequency range in KIT amplifiers, where $I_{p0} \ll I_*$.

However, it is important to note that while desirable within the amplification bandwidth, parametric conversion processes outside of that bandwidth can lead to pump depletion and degradation of the amplifier's power handling, as well as an increase in amplifier-added noise. Thus, in order to optimize performance and avoid these undesirable effects, it is necessary to carefully control the frequency range over which three-wave mixing occurs.

2.5.1 Coupled-mode theory of a dc-biased KIT Amplifier

The phase-matching condition for exponential gain, Equation 2.37, is obtained by solving the CMEs while pumping in a 3WM fashion, i.e., such that $\omega_p = \omega_s + \omega_i$, and in the presence of 3WM and 4WM terms; see Equation 2.36. The CMEs relate the current amplitudes $I_j, j \in \{p, s, i\}$ at the frequencies $\omega_j, j \in \{p, s, i\}$ they are obtained by injecting Equation 2.36 into telegrapher's equations in a lossless transmission line (see chapter 2.2.1), and by operating the harmonic balance (HB) with only these three frequencies we obtain

$$v_p^2 \frac{\partial^2 I}{\partial x^2} - \frac{\partial^2 I}{\partial t^2} = \frac{\partial}{\partial t^2} \left(\frac{1}{2} \epsilon I^2 + \frac{1}{3} \xi I^3 \right) \quad (2.38)$$

with $v_p = 1/\sqrt{CL_d}$ the phase velocity. To solve Equation 2.38, we perform the HB. We assume that the current in the transmission line is a sum of three terms at three different frequencies,

$$I = \frac{1}{2} [I_p(x)e^{i(k_p x - \omega_p t)} + I_s(x)e^{i(k_s x - \omega_s t)} + I_i(x)e^{i(k_i x - \omega_i t)} + \text{c.c.}] \quad (2.39)$$

and we then keep only the mixing terms from Equation 2.38 that emerge at these frequencies. This approach is valid in our case, because the phase-matching bandwidth is limited by dispersion engineering, and thus mostly these three frequencies are able to mix together. Under the slow-varying envelope approximation, $|d^2 I_j/dx^2| \ll |k_j dI_j/dx|$ for $j \in \{p, s, i\}$, the left-hand side of Equation 2.38 yields

$$v_p^2 \frac{\partial^2 I}{\partial x^2} - \frac{\partial^2 I}{\partial t^2} = v_p^2 \sum_{j=p,s,i} ik_j \frac{dI_j}{dx} e^{ik_j x - \omega_j t} + \text{c.c.} \quad (2.40)$$

Using $\omega_p = \omega_s + \omega_i$, we collect terms at $\omega_j, j \in \{p, s, i\}$, on the right-hand side (rhs) and form the CMEs

$$\frac{dI_p}{dx} = \frac{ik_p \epsilon}{4} I_s I_i e^{-i\Delta_k x} + \frac{ik_p \xi}{8} I_p (|I_p|^2 + 2|I_s|^2 + 2|I_i|^2), \quad (2.41a)$$

$$\frac{dI_s}{dx} = \frac{ik_s \epsilon}{4} I_p I_i^* e^{i\Delta_k x} + \frac{ik_s \xi}{8} I_s (2|I_p|^2 + |I_s|^2 + 2|I_i|^2), \quad (2.41b)$$

$$\frac{dI_i}{dx} = \frac{ik_i \epsilon}{4} I_p I_s^* e^{i\Delta_k x} + \frac{ik_i \xi}{8} I_i (2|I_p|^2 + 2|I_s|^2 + |I_i|^2), \quad (2.41c)$$

with $\Delta_k = k_p - k_s - k_i$. The phase-matching condition, Equation 2.37, is found for a strong pump, where $\{|I_s|, |I_i|\} \ll |I_p|$. Assuming that the pump is undepleted,

$|I_p(x)| = I_{p0}$ Equation 2.41 can be rewritten as

$$\frac{dI_p}{dx} = \frac{ik_p\xi}{4} I_p I_{p0}^2, \quad (2.42a)$$

$$\frac{dI_s}{dx} = \frac{ik_s\epsilon}{4} I_p I_i^* e^{i\Delta_k x} + \frac{ik_s\xi}{4} I_s I_{p0}^2, \quad (2.42b)$$

$$\frac{dI_i}{dx} = \frac{ik_i\epsilon}{4} I_p I_s^* e^{i\Delta_k x} + \frac{ik_i\xi}{4} I_i I_{p0}^2, \quad (2.42c)$$

which results in $I_p(x) = I_{p0} \exp(i\xi k_p I_{p0}^2 x / 8)$. Signal and idler amplitudes are then searched with the form $I_j(x) = \tilde{I}_j \exp(i\xi k_j I_{p0}^2 x / 4)$, $j \in \{s, i\}$ Equations 2.42 then yield

$$\frac{d\tilde{I}_s}{dx} = \frac{ik_s\epsilon}{4} I_{p0} \tilde{I}_i^* e^{i\Delta_\beta x} \quad (2.43a)$$

$$\frac{d\tilde{I}_i}{dx} = \frac{ik_i\epsilon}{4} I_{p0} \tilde{I}_s^* e^{i\Delta_\beta x} \quad (2.43b)$$

with $\Delta_\beta = \Delta_k + (\xi I_{p0}/8)(k_p - 2k_s - 2k_i)$. The system of equations 2.43 has known solutions [8]. In particular, when phase matching is achieved, i.e., $\Delta_\beta = 0$ we obtain

$$\tilde{I}_s = \cosh(g_3 x) \tilde{I}_{s0}, \quad (2.44a)$$

$$\tilde{I}_i = i \sqrt{\frac{k_i}{k_s}} \sinh(g_3 x) \tilde{I}_{s0}, \quad (2.44b)$$

with $g_3 = (\epsilon I_{p0}/4) \sqrt{k_i k_s}$ and with initial conditions $I_s(0) = I_{s0}$ and $I_i(0) = 0$. The signal power gain

$$G_s(x) = \left| \frac{I_s(x)}{I_{s0}} \right|^2 \quad (2.45)$$

is then exponential with x : $G_s = \cosh^2(g_3 x)$

Chapter 3

Design and Simulation

3.1 Design

In this section, we will look into the design process of our superconducting KIT amplifier. The foundation of our design is built upon the concepts and principles outlined in [12, 43]. However, in order to optimize the design, we made several modifications to the original design presented in the literature. These modifications aimed to improve the use of space and increase the gain results, while also reducing the overall size of the chip. In particular, we chose to use tungsten silicide (WSi) as our primary waveguide material, taking advantage of its high kinetic inductance properties, as discussed in chapter 2.3.2 and a second layer of aluminum for capacitance. In the following sections, we will elaborate on the specific design modifications we made and the reasoning behind them.

3.1.1 Basic structure

In our design, we use an artificial transmission line made of WSi (tungsten silicide) that is fabricated to be $h = 15 \text{ nm}$ hight and $w = 6 \mu\text{m}$ thick. This serves as the gain medium in our system. The artificial transmission line, also known as a lumped-element transmission line, utilizes lumped-element inductors and Aluminum (Al) capacitors. As seen in Figure 3.1, the basic structure of the KIT consists of a series of CPW sections, or cells. Each cell has an inductance L_d that is flanked by two interdigitated capacitor (IDC) fingers that form the capacitance to ground C , such that $Z_0 = \sqrt{L_d/C} = 50\Omega$. The value of L_d is calculated to be $L_d = 66.67\text{pH}$ using the method outlined in chapter 2.3.2 and [27]. The Aluminum fingers are $152\mu\text{m}$ long and are used to create a capacitance of $C = 26.67\text{fF}$, which is calculated using the method outlined in chapter 2.4. The inductance of the Aluminum fingers, L_f , is calculated to be $L_f = 30.48\text{pH}$ using the same method. The equivalent electrical circuit of this structure can be seen in Figure 3.2.

The WSi is fabricated to be 15 nm hight and 6 nm thick in order to achieve the best amplification parameters while maintaining an impedance of 50Ω in our simulations. The Aluminum, on the other hand, is fabricated to be 100 nm hight. This is to ensure that it is a few times thicker than its penetration depth of around $6\mu\text{m}$ at temperatures of 30 mK [4], while still being small enough for fabrication purposes.

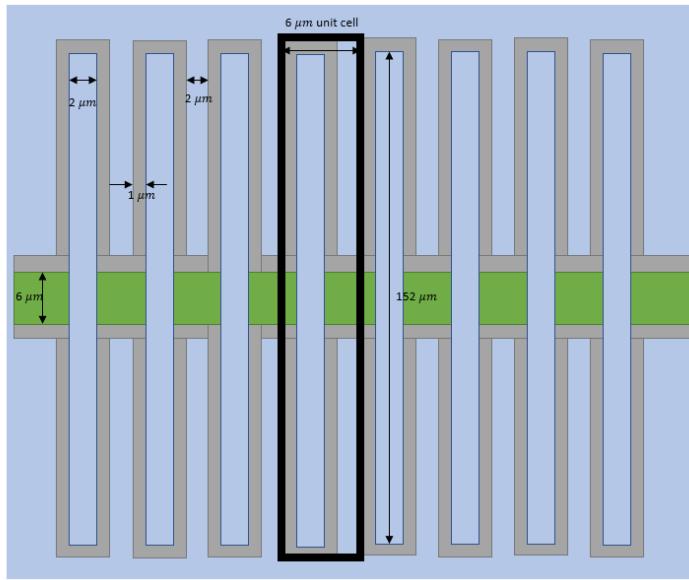


Figure 3.1: Schematic of the KIT amplifier artificial transmission line, The Green line is the first layer WSI $6\mu m$ width, to it we connect fingers aluminum (pale blue) with $2\mu m$ with and $152\mu m$ long, $2\mu m$ separates between two aluminum fingers neighbors. The gray area is silicon with high resistivity with a width of $1\mu m$ that is separated from the background aluminum and serves as ground, which gives us a unit cell of $6\mu m$ (black)

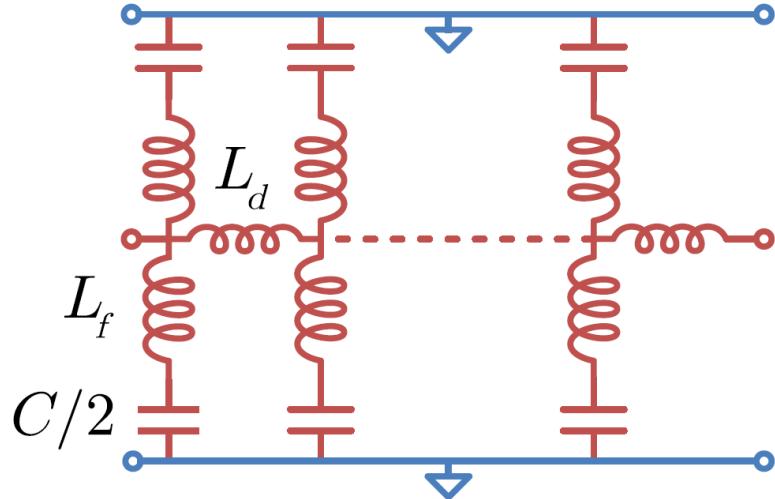


Figure 3.2: Equivalent electrical circuit, each cell consists of a series inductance L_d and two resonators with inductance L_f and capacitance to ground $C/2$. This picture was taken from [43]

3.1.2 Fine details structure

In order to achieve phase matching over a desired bandwidth, we have incorporated a periodic design in our system. This design feature increases the line impedance

on short sections, creating a resonance in the line's phase response (and a stopband in the line's amplitude response) at a frequency ω_l that is controlled by the loading periodicity. The periodicity is composed of 5 small fingers of $140\mu m$ followed by 21 long ones, as can be seen in Figure 3.3. The capacitance of the small finger, C_s , is calculated to be $C_s = 24.61fF$ and the inductance of the small finger, L_s , is calculated to be $L_s = 28.13pH$. This design feature is inspired by the works of [12, 43].

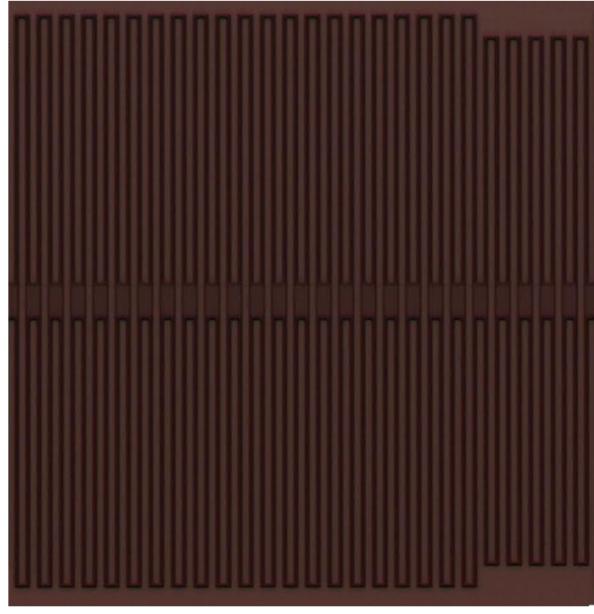


Figure 3.3: Period of 21 long fingers followed by 5 short ones.

3.1.3 Big picture Design

As previously mentioned, our goal was to utilize a space of $6.25 \times 6.25mm^2$ in the most efficient way possible. To achieve this, we have designed a structure that comprises multiple stripes of WSI, each measuring $565\mu m$ in length, and periodic fingers. Each strip contains 36 periods, as detailed in chapter 3.1.2. Each period contains $N_f = 26$ fingers, resulting in a total of 936 fingers per strip. The strips are spaced $80\mu m$ apart, allowing us to fit 27 strips on a single chip. The strips are connected using coplanar waveguide (CPW) technology, as shown in Figure 3.4. We have set the CPW to have $s = 5\mu m$ and $w = 8\mu m$, which gives us the desired impedance of $Z = 50\Omega$ which is also calculated with the methods from chapter 2.4. This relationship of $w/s = 8/5$ is what gives us the 50Ω impedance.

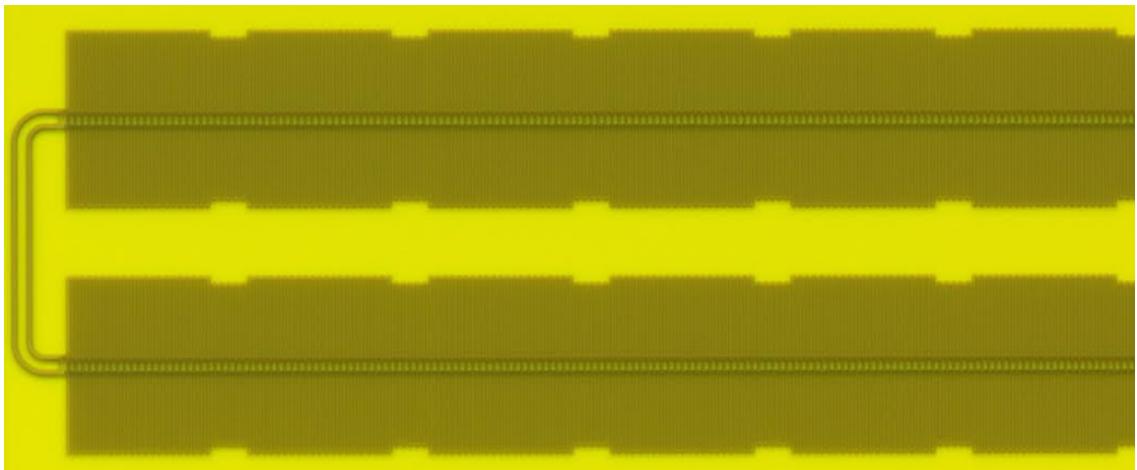


Figure 3.4: Two lines connected by CPW .

A key feature of our design is the inclusion of two Lunchers (Figure 3.5). These Lunchers serve as the means for inputting and outputting current to and from the chip. These connectors are relatively large-scale features, each measuring around $400 \times 340\mu m^2$. To accommodate these connectors, we had to shorten 5 of the strips to $4090\mu m$. This results in 5 small lines with 26 periods instead of 36, and which gives us 676 fingers for the small strip, and for conclusion we have 22 long strips and 5 short strips which gives us total of $N_c = 23,972$ fingers. The connections to and from the connectors are also made using CPW technology, as described earlier in this chapter.

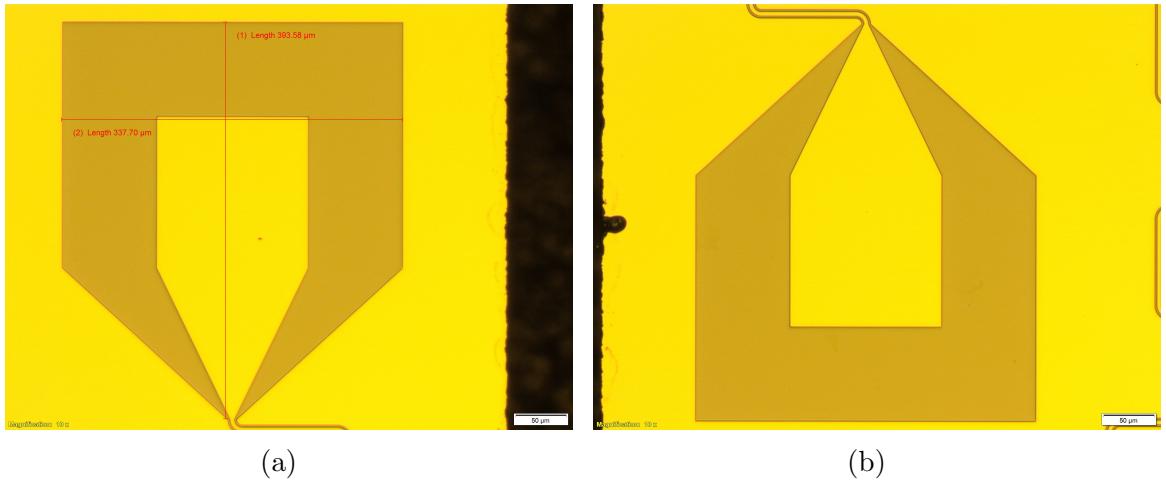


Figure 3.5: (a) A connector with measured size of approximately $400 \times 340\mu m^2$. (b) A connector

3.2 Simulation

In this chapter, we present the simulation results of the design presented in chapter 3.1. Our goal is to evaluate the performance of the design before its fabrication and measurement. Through simulations, we aim to verify the theory and determine the optimal parameters for our device.

To begin, we will simulate the wavenumber k as a function of frequency, using the equations will derive here and derived in the background chapter. This will allow us to ensure that the phase-matching condition is met and that the device operates within the desired frequency range of $4 - 8\text{GHz}$, the frequency spectrum of the signal.

Next, we will determine the optimal pump frequency that will give us the highest gain in the desired frequency range. This is crucial for the overall performance of the device.

Lastly, we will simulate the gain as a function of frequency, which will give us an idea of the overall performance of the device and its ability to amplify the signal.

Overall, the simulation results will provide valuable insight into the performance of our design and guide us in making any necessary adjustments before its fabrication and measurement.

3.2.1 wavenumber as a function of the frequency

The calculation of the wavenumber k as a function of frequency for the KIT amplifier is an important aspect of understanding the amplification gain of the device. In this section, we will use the $ABCD$ matrices of the Kit amplifier cells to calculate k as per the method outlined in Chapter 2.5.

We first construct the matrix of an unloaded cell, as shown in Fig. 3.2. The $ABCD$ matrix of the cell is given by [43]

$$T_{c_l} = \begin{pmatrix} 1 & iL_d\omega \\ \frac{i2C\omega}{2-L_fC\omega^2} & 1 - \frac{2L_dC\omega^2}{2-L_fC\omega^2}, \end{pmatrix} \quad (3.1)$$

where L_d and C are the inductance and capacitance of the longer finger, respectively. Similarly, the $ABCD$ matrix of the shorter finger is given by,

$$T_{c_s} = \begin{pmatrix} 1 & iL_d\omega \\ \frac{i2C_s\omega}{2-L_sC_s\omega^2} & 1 - \frac{2L_dC_s\omega^2}{2-L_sC_s\omega^2}, \end{pmatrix} \quad (3.2)$$

where L_s and C_s are the inductance and capacitance of the shorter finger, respectively.

To construct the $ABCD$ matrix of a period containing 21 long fingers and 5 short ones, we use the following equation:

$$T_p = T_{c_l}^{21} \cdot T_{c_s}^5, \quad (3.3)$$

The $ABCD$ matrix of the entire chip can be calculated by powering T_p by the number of periods in the chip, $N_p = N_c/N_f = 922$. This gives us the KIT amplifier $ABCD$ matrix, $T_k = T_p^{N_p}$.

To compute the dispersion relations, we then compute the KIT amplifier S_{21} scattering parameter from Equation 2.26. The wavenumber k can then be calculated using :

$$k = -\text{unwrap}[\arg(S_{21})]/N_c \quad (3.4)$$

Figure 3.6a shows the full spectrum graph of the calculated wavenumber k as a function of frequency for the KIT amplifier. Figure 3.6b provides a closer look at the spectrum of 14.35 – 14.58 GHz, where the nonlinearity of the wavenumber occurs. This nonlinearity is an outcome of the different lengths of the fingers in a period and helps to fulfill Equation 2.37.

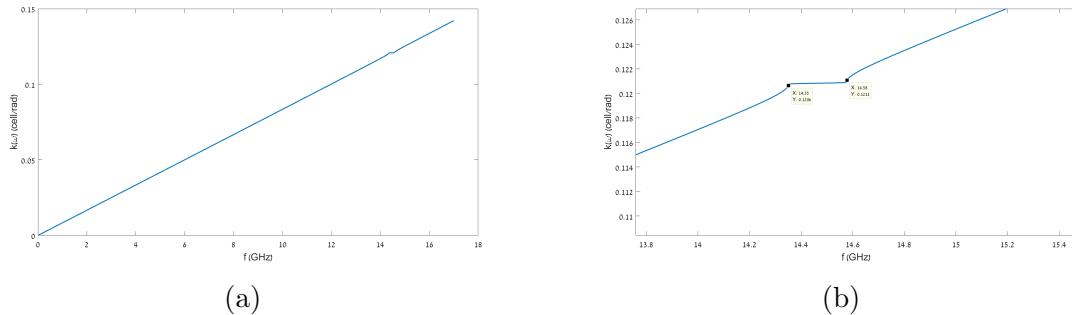


Figure 3.6: The wavenumber k is calculated as a function of frequency for the KIT amplifier (a) Full spectrum graph, (b) Closer look at the spectrum of 14.35 – 14.58 GHz where the nonlinearity of the wavenumber accrues

3.2.2 Gain as function the frequency

The gain of a system can be calculated by using coupled mode theory, as discussed in chapter 2.5.1. The simulations use Equations 2.41 and the wavenumber calculated in Chapter 3.2.2.

A key parameter in the calculation is I_* , which is first presented in Chapter 2.3.2. I_* can be evaluated using the critical current of the WSi, which can be calculated using Equation 2.15. For a WSi with a thickness of $15nm$ and a width of $6\mu m$, the critical current is $I_c = 2.518mA$. The relationship between I_* and I_c is given by $I_* = 2.69I_c = 6.759mA$.

Defining the DC current I_d is an important task, as it affects the values of ξ and ϵ , and therefore the gain. However, there is a restriction on the value of I_d , as it must be less than the critical current in order to maintain the superconducting state. In this case, we choose $I_d = I_*/4 = 1.69mA$. The initial conditions for the pump, signal, and idler currents are $I_{p0} = I/60 = 0.113mA$, $I_{s0} = I_{p0}/100 = 1.13\mu A$, and $I_{i0} = 0$, respectively.

To find the ideal ω_p that will give the ideal gain spectrum, we solve the two equations 2.37 and $\omega_p = \omega_i + \omega_s$. However, this leaves a degree of freedom in the system, which can be resolved by introducing another constraint. One such constraint is $|\omega_i - \omega_s| = \text{constant}$. This constraint creates resonances at two frequencies, resulting in maximum gain at $(\omega_p \pm \text{constant})/2$. For example, when $|\omega_i - \omega_s| = 8GHz$, $\omega_p = 14.49GHz$, and the maximum gain is around the frequencies of $3.3GHz$ and $11.3GHz$ with a maximum gain of $7.85dB$, as shown in Figure 3.7.

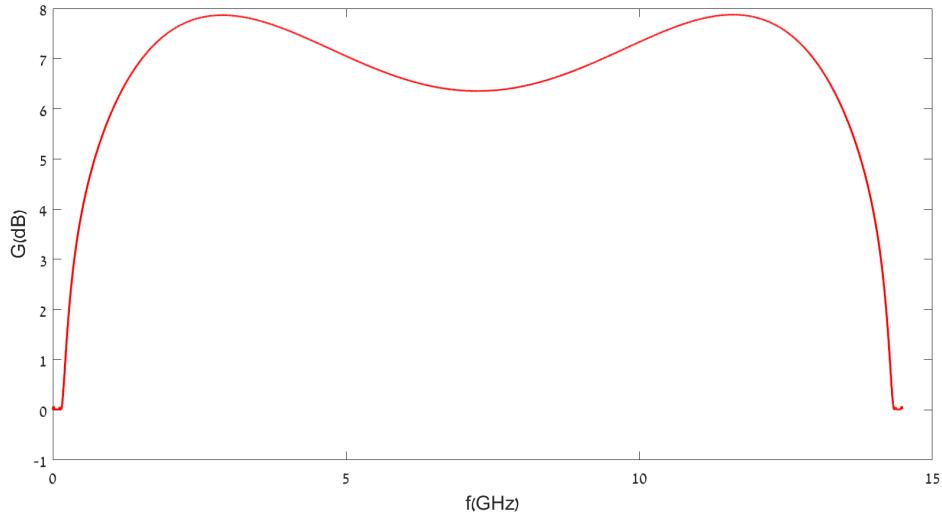


Figure 3.7: Gain as function of the frequency for the constraint $|\omega_i - \omega_s| = 8GHz$, $\omega_p = 14.49GHz$

To create the maximum gain possible, as well as the most symmetrical and wide bandwidth around the maximum gain, we choose the constraint $\omega_i = \omega_s$ which breaks the symmetry and gives us one maximum . This results in $\omega_p = 14.5241GHz$, and the maximum gain at 7.262 GHz with 18.64 dB amplification and a desired bandwidth of at least 16dB amplification at frequencies of (4 – 8)GHz, as shown in Figure 3.8. It is noteworthy that the values of ω_p obtained in this section fall within the nonlinear range depicted in Figure 3.6b, highlighting the importance of the nonlinearity resulting from the variation in finger lengths.

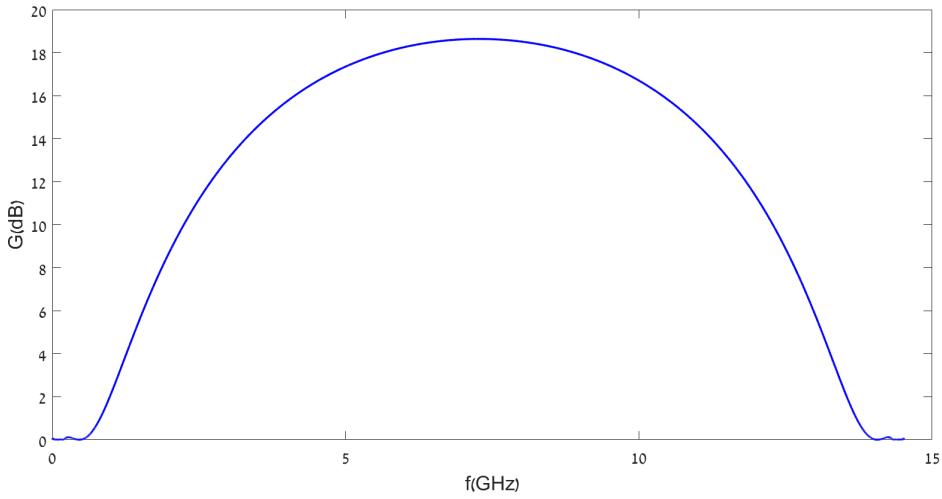


Figure 3.8: Gain as function of the frequency for the constraint $\omega_i = \omega_s$, $\omega_p = 14.5241GHz$

3.2.3 Parametric sweep

To more thoroughly analyze the characteristics of the simulation and to gain deeper insights into the results, we will create a series of graphs that examine the effect of various parameters on the Gain profile, while keeping the other basic parameters constant, as demonstrated in Figure 3.8.

Variations of ω_p

We will now examine the impact of varying the parameter ω_p on the gain profile. Running simulations with different values of ω_p from 14.483GHz to 14.563GHz, with an increment of 10 MHz each time, gives us Figure 3.9. This figure shows that the best gain spectrum and maximum amplification is achieved at $\omega_p = 14.523\text{GHz}$. As the pump frequency increases, the maximum gain decreases, but its frequency remains constant, and the width of the amplification spectrum narrows. Conversely, when the frequency is decreased from 14.523GHz, the maximum gain also decreases and its frequency shifts, resulting in two maximum frequencies with a wider gain amplification spectrum.

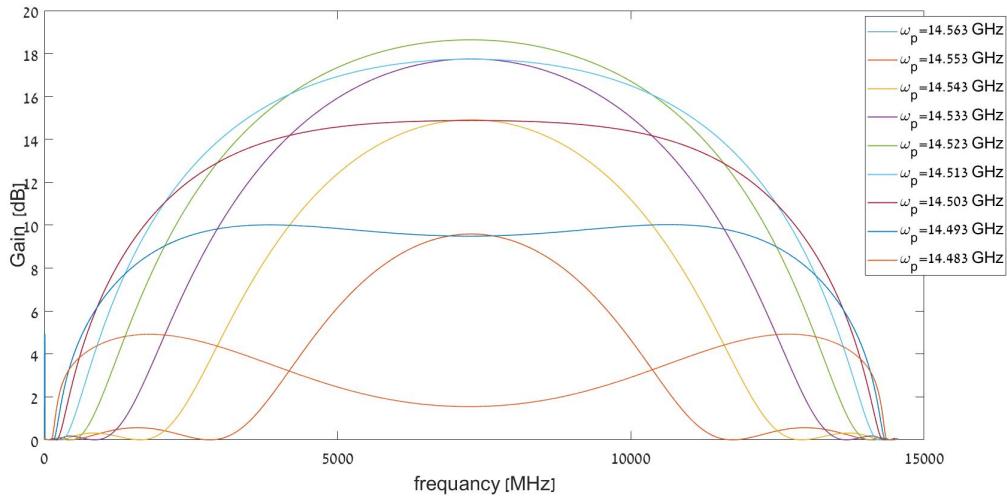


Figure 3.9: Gain as a function of frequency For various values of ω_p

Effects of DC Current on Gain Spectrum

When examining the effects of DC current on the gain spectrum, it is crucial to note that increasing the DC current will not provide meaningful results. This is because as the DC current approaches I_c , the chip will cease to be in a superconducting state, thus rendering any amplification observed in simulations irrelevant in practice.

In Figure 3.10, we present the gain for different DC currents, ranging from 0.1mA to 1.7mA with increments of 0.2mA, as well as an additional 1.8mA to show that the gain improves when the superconducting state is not broken. The figure clearly demonstrates the significant impact of the DC current on the creation of gain, and that the higher the DC current, the higher the gain. This highlights the importance of having a higher I_c and the benefits of using the resonance construction we employed, as opposed to JPAs and comparing NbTiN to WSI.

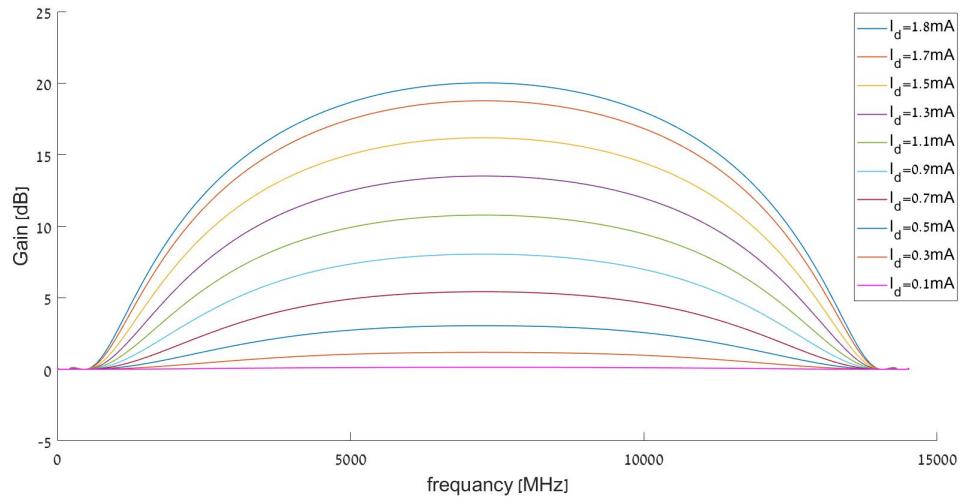


Figure 3.10: Gain as a function frequency for various dc current

It is worth noting that for zero DC current, no amplification occurs, and the signal can be considered as the incoming signal when there is a perfect impedance match, a characteristic that will be used for comparison in our experiments.

Chapter 4

Clean room fabrication, processes and experimental setup

In this chapter, we will cover the technical aspects of building the KIT Amplifier. We will examine the methods and machinery used during the fabrication process, highlighting their pros and cons, and discussing the reasons and situations in which each one was used. We will also provide a thorough explanation of the various steps involved in the fabrication process, from the initial design to the final assembly of the KIT Amplifier. Additionally, we will explore the critical role of a clean room environment in the fabrication process and the protocols and procedures that were followed to maintain a high level of cleanliness and precision during the fabrication process.

4.1 Clean room and experiment processes and machines

The clean room is an essential environment for the fabrication of microelectronic devices. It is a controlled environment that allows for the preparation and processing of wafers using various techniques and instruments. In this section, I will focus on the processes and machines that I have operated, explain their uses in the clean room, and how they work.

4.1.1 resist

In microfabrication processes, a resist is a material that is selectively removed to create patterns on a substrate. There are two main types of resists: positive and negative. Positive resists are those that are removed where the pattern is to be created, while negative resists are those that remain after patterning. This means that a positive resist forms a pattern in the shape of the desired features, while a negative resist forms a pattern in the shape of the spaces between the features.

There are several examples of positive resists that are commonly used in electron-beam lithography and laser-writing. One example is polymethylmethacrylate (PMMA), which is often used in electron-beam lithography due to its high resolution and sensitivity. Another example is AZ 1505, which is a positive photoresist used in laser-writing. Negative resists, on the other hand, are typically used in situations where

the patterns to be created have high aspect ratios or fine features, as they can be more easily removed from the spaces between the features. Examples of negative resists include AZnlof 2020, which is a negative photoresist used in laser-writing, and ma-N 2403, which is a negative resist used in electron-beam lithography.

The selection of resist material in microfabrication is influenced by a variety of factors, including the desired pattern and the specific requirements of the process. Positive resists are often favored for their ease of use and straightforward process flow, while negative resists offer the advantage of higher resolution and more complex patterning capabilities. Additionally, the density of features to be created also plays a role in the choice of resist. For small, densely packed patterns where most of the resist is to wear off, negative resists may be the preferred option, while positive resists may be more suitable for larger patterns where most of the resist is to stay. However, it is worth noting that other considerations may also come into play when making this decision.

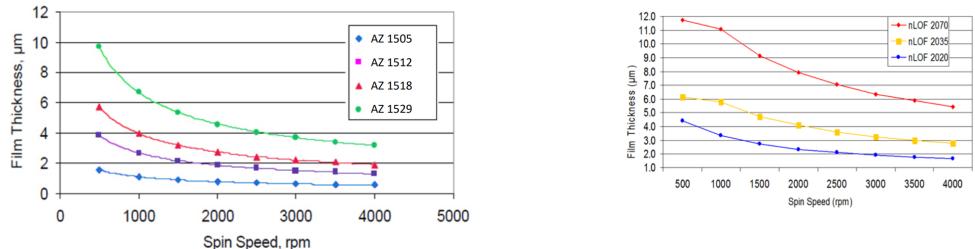
Resists are commonly used in the lift-off process, which is a technique for removing layers of material from a substrate. In this process, a patterned resist is used to define the areas where the material is to be removed. The material is then deposited on top of the resist, and the entire structure is immersed in a solvent that dissolves the resist. This leaves the material only in the areas where the resist was not present, forming a pattern on the substrate.

Resists are mainly used in wet etching, which is a chemical process used to remove material from a substrate. In wet etching, a patterned resist is used to protect certain areas of the substrate from the etchant, which selectively removes the unprotected material. The resist is then removed, leaving a patterned surface on the substrate.

Both the lift-off and wet etching processes require the use of resists to create precise patterns on the substrate. The choice of resist depends on the materials being used and the specific requirements of the process. Positive resists are often preferred for lift-off, as they can be easily dissolved in a solvent, while negative resists are often preferred for wet etching, as they can withstand the etching process and protect the desired areas of the substrate.

4.1.2 Spinner

A spinner is a tool used to apply a thin, uniform layer of resist onto a wafer. This process is essential for achieving the desired thickness of the resist layer, as shown in Figures 4.1 (a) and 4.1 (b). Figure 4.1(a) illustrates the relationship between spin speed and film thickness for various types of positive resist, while Figure 4.1(b) shows the same relationship for negative resists. By controlling the spin speed and selecting the appropriate resist type, we can accurately and consistently apply the resist layer to the wafer.



(a) relationship between spin speed and film thickness of positive resist[44] (b) relationship between spin speed and film thickness of negative resist[46]

Figure 4.1: Film thickness as a function of spin speed for different types of resist.

4.1.3 Laser Writer

The laser writer that we use in the clean room is the LW405B model, which has a laser wavelength of 405 nm. We operate the laser writer using the Clewin program, which allows us to specify the desired patterns on the resist. The practical resolution of the laser writer is 1 micrometer, which means that it can create patterns with a minimum feature size of 1 micrometer.

A laser writer is an essential tool in the clean room, as it allows us to pattern the resist on the wafer with high precision and accuracy. By carefully controlling the laser exposure, we can create complex and detailed patterns on the resist, which can be used to create the desired features on the wafer.

The LW405B model is a versatile and reliable laser writer that can be used for a variety of applications. Its compact size and advanced features make it an ideal choice for microelectronic device fabrication, and it has proven to be a valuable tool in our clean room.

4.1.4 Electron-beam lithography

Electron-beam lithography which we use is ELS-G100, which is a microfabrication instrument that uses a beam of highly focused electrons to draw patterns on a surface covered with a thin film of resist. The resist is then used as a mask for etching or Lift off, creating patterns on the underlying substrate.

Electron-beam lithography has several advantages over other lithography techniques, such as photolithography. It has a higher resolution, since the electron beam has a smaller wavelength than light and can therefore create smaller features. It also has a larger depth of focus, meaning it can print patterns on surfaces with uneven topography. Additionally, electron-beam lithography can print patterns with very high aspect ratios, or the ratio of the feature's height to its width.

However, electron-beam lithography also has some disadvantages. It is a slow process, as the beam must be scanned over the entire surface to create the pattern. It is also expensive, due to the cost of the equipment and the need for high vacuum conditions. In addition, it is not suitable for mass production, as it is a labor-intensive process.

Despite these drawbacks, electron-beam lithography is a valuable tool in the microfabrication industry, especially for creating patterns with high resolution and

aspect ratios. It is commonly used in the production of microelectromechanical systems (MEMS), nanoelectromechanical systems (NEMS), and other micro- and nanoscale devices.



Figure 4.2: Elionix E-Beam Lithography System ELS-G100. [31]

4.1.5 Optical Profilometer

The Optical Profilometer is a device used to measure the surface profile of a sample with high precision. It works by shining a laser light on the sample and measuring the reflection of the light to determine the height profile of the surface. The principle of operation is based on the optical triangulation method.

An optical profilometer can measure surface roughness, step height, and other physical characteristics of a sample with high accuracy and resolution. In our study, we utilized an Optical Profilometer to measure the surface profile of the samples after each fabrication step.

The Optical Profilometer we used in our study is shown in Figure 4.3. It consists of a laser source, a microscope lens, a camera, and a computer. The laser light is projected onto the sample, and the reflection is captured by the camera. The software then processes the image and calculates the height profile of the surface.

By using the Optical Profilometer, we were able to obtain accurate measurements of the surface profile of our samples and ensure the quality of our fabrication process. The results of the measurements were used to evaluate the success of each fabrication step and make improvements where necessary.

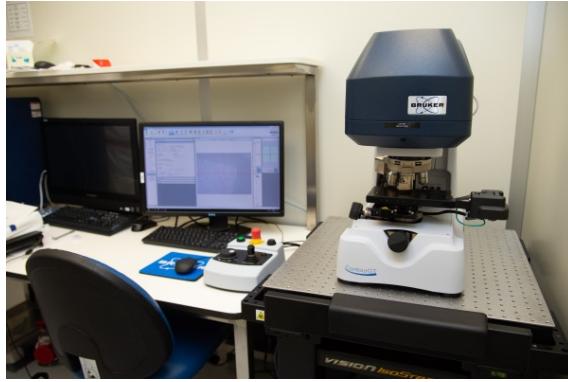


Figure 4.3: Optical Profilometer used in the study. This picture taken from [36]

4.1.6 wet etch

The main characteristic of the etching process is its ability to selectively dissolve specific materials. Different materials require different etchants in order to be dissolved, and the correct etchant must be carefully chosen to ensure that only the intended material is attacked. This selective nature of etching is important because it allows for the creation of patterns on a chip with multiple layers of different materials.

One disadvantage of chemical etching is that it is isotropic, meaning that it etches in all directions equally. In cases where the thickness of the material is similar to the transverse dimensions of the area being etched (such as the width of the traces on a chip), the final patterned film will have sloping walls.

When using the wet etching process, we first deposit the desired material onto the wafer using sputtering. We then apply a layer of resist to protect the areas that we do not want to etch. The areas where the resist is removed will be exposed to the etchant and will be dissolved, while the areas that are protected by the resist will remain intact. By carefully planning and designing the patterns on the chip, we can use the wet etching process to create the desired features on the wafer.

Prior to the wet etch process, it is essential to hard bake the wafer with the features to improve the adhesion of the resist and enhance pattern stability. As shown in Figure 4.4 [46], the hard bake stability for large pads in AZ nLOF 2070 for $7.0\mu m$ film thickness is displayed at different temperatures.

4.1.7 Lift Off

It is also possible to prepare a resist mask before material deposition, and not subsequently. After the device is covered by a uniform film the wafer is placed for hours in solvents such as acetone and/or n-methyl-2-pyrrolidone, commonly known as NMP. These solutions attack not the material, but the resist. This patterning method is therefore negative; where resist has been removed, the material remains after the process.

In many cases lift-off is preferable over etching for various reasons. First, unlike wet and dry-etch, no apparent harm is done to the material, which is typically harder to remove than resist. Second, when alignment between consecutive layers are required at the exposure level, and the film to be deposited is opaque (e.g. $100nm$ Al), it can be easier to see through a resist mask to find the features of the underlying layer. Since liftoff involves patterning of resist before applying the metal,

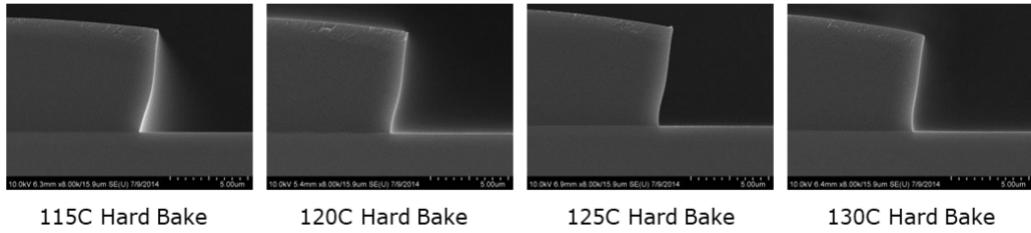


Figure 4.4: Hard bake stability for large pads in AZ nLOF™ 2070 (7.0 μm film thickness) [23]

the alignment process is far less challenging. And third, eventually the device must be stripped of the resist mask, even after etching processes, and lift-off patterning practically turns this otherwise auxiliary cleaning step into a central part of the fabrication scheme

Despite its clear advantages lift-off can be difficult, and in the development of new fabrication recipes, it often fails for various reasons:

- The adhesion between evaporated film and the underlying surface is insufficient; e.g. A does not stick to B. In this case, sonication can sometimes removes material residues. For certain substrates the adhesion is improved by a short ion milling sequence prior to evaporation.
- During the evaporation process, the resist is heated radically by the gaseous material during deposition. Of course, baking of resist is a standard step in many processes; softbake is mandatory before lithography exposure to get rid of solvent residues and improve the resist's adhesion to the substrate. Prior to wet-etch, the resist is also hardbaked after development to harden the resist, making it robust. But when intended for lift-off, this is obviously counter-productive. The resist must only endure evaporation, and hardening makes adhesion stronger and the removal becomes even hard. This problem can be overcome by cooling the wafer during the evaporation.
- If the exposed areas (i.e. the regions where material is to stay) are too small, the material to be "lifted" draws along the material that landed on the surface at the exposed areas. This problem can be overcome with a double layer of resists. For optical lithography, one uses LOR (lift-off-resists) and for electronic lithography a so-called "co-polymer".

4.1.8 The EDC Spin Processor

The EDC Spin Processor is a machine that is used to clean wafers in the microfabrication industry. One of the key features of this machine is its use of the pirana solvent for cleaning.

Pirana is a blend of chemicals that is specifically designed for cleaning silicon wafers in the microfabrication industry. It is a mixture of isopropyl alcohol (IPA), hydrogen peroxide (H₂O₂), and deionized water. This combination of chemicals is effective in removing contaminants such as organic and inorganic residues, as well as particles from the wafer surface. However, it is important to note that pirana may not be suitable for all materials used in the fabrication process as it can potentially harm metals and other materials.

The EDC Spin Processor uses the pirana solvent in a spin-rinse-dry process. The wafer is placed in the machine and is spun at high speeds to evenly distribute the solvent over the surface. The solvent is then rinsed off with deionized water, and the wafer is dried using a nitrogen gas purge. This process is repeated several times to ensure that the wafer is thoroughly cleaned.

The EDC Spin Processor is a highly efficient and effective machine for cleaning wafers. Its use of the pirana solvent allows for the removal of a wide range of contaminants, ensuring a clean and pristine surface for the next steps in the microfabrication process. However, it is important to consider the potential impact on other materials used in the fabrication process before using pirana. Alternative cleaning methods should be considered if necessary.



Figure 4.5: EDC Spinner used in the study.[35]

4.1.9 Angstrom Quantum Series Evaporator

The deposition of aluminum and titanium in the fabrication process of microelectronic devices is performed using an evaporator system. Our system, the Angstrom Quantum Series Evaporator, is a two-chamber system consisting of a bottom chamber for the deposition materials and an e-beam source, and a top chamber for the samples and processing. The two chambers are separated by a gate valve. The base pressure in the bottom chamber is 3×10^{-9} Torr, while the base pressure in the top chamber is 5×10^{-8} Torr.

The evaporation process works by heating the material to be deposited, typically in the form of a metal wire or filament, to a high temperature in the bottom chamber. The metal atoms then become vaporized and are transported to the top chamber where the samples are placed. The vaporized metal atoms then condense on the surface of the samples, forming a thin metal film.

The Angstrom Quantum Series Evaporator provides precise control over the thickness and uniformity of the deposited metal films, as well as the ability to deposit multiple materials in a single deposition process. This makes it an essential tool in the fabrication of microelectronic devices with precise metal film requirements.



Figure 4.6: Angstrom Quantum Series Evaporator [33]

4.1.10 Plasma Asher

A Plasma Asher, uses a plasma discharge to remove contaminants from the surface of the wafers. The process is known as plasma cleaning or plasma etching. A vacuum chamber is used to evacuate the air and create a low-pressure environment. Then, high-frequency electric fields are applied to a gas, typically argon or oxygen, which causes the gas molecules to break down into ions and free electrons. This plasma state is also known as a "fourth state of matter."

The ions and electrons in the plasma interact with the surface of the wafer, breaking down and removing contaminants such as dust, oil, and organic molecules. The process is highly effective at removing even tightly-bound contaminants, making it ideal for semiconductor applications.

Overall, vacuum plasma cleaning using an ashler device is a powerful and effective

method for removing contaminants from silicon wafers, and plays a critical role in ensuring the performance and reliability of the final devices.



Figure 4.7: Plasma asher used in the study. [24]

4.1.11 Sonication

Sonication is a common technique used in the clean room for cleaning and removing contaminants from various surfaces, including wafers. The process involves using high-frequency sound waves to agitate a liquid, creating small bubbles that collapse and create tiny high-pressure jets. These jets can remove particles and contaminants from surfaces, making sonication an effective method for cleaning wafers. The sonication process should be performed in a sonication bath, which is a specialized equipment designed to generate the high-frequency sound waves needed for sonication.

It is important to note that sonication can cause mechanical damage to the wafer if not performed correctly. Therefore, it is important to use the correct sonication parameters and to monitor the wafer during the process to ensure that the wafer is not damaged. Additionally, the sonication bath should be cleaned and maintained regularly to ensure that it is working properly.

Overall, sonication is an effective technique for removing resist from wafers in the clean room, but it is important to use the correct equipment, parameters, and safety precautions to ensure that the wafer is not damaged and that the process is performed safely.

4.1.12 Dicing System

The Dicing System is a machine used to cut wafers into individual chips. In our study, we utilized a Dicing System to cut our wafers into the desired dimensions for further testing and analysis.

The Dicing System we used was capable of handling wafers up to 200mm in diameter and 1mm in thickness. It consists of a mechanical saw and a motor that rotates the wafer during the cutting process. The cutting process is guided by a laser that provides high precision and accuracy in determining the cutting path. Additionally, the process is aided by the pressure of water that is applied to the blade during the cutting process. This helps to cool the blade and reduce the risk of damage to the wafer.

The parameters of the Dicing System include the cutting speed, blade thickness, blade gap, and pressure applied during the cutting process. These parameters were carefully optimized to ensure smooth and accurate cuts without causing any damage to the samples.

Figure 4.9 shows the Dicing System used in our study. It is an efficient machine that can handle large wafers and produce high-quality cuts.



Figure 4.8: Dicing System used in the study.[34]

4.1.13 Wire Bonding

Wire bonding is a process used to electrically connect a device to its surrounding environment. In the case of the KS wedge bonder, aluminum wires and ribbons are bonded using ultrasonic bonding.

The ultrasonic bonding process uses high frequency mechanical vibrations, or ultrasonic waves, to generate heat through friction at the bonding interface. This heat melts the aluminum wire or ribbon, allowing it to flow and form a metallurgical bond with the bond pad. The ultrasonic waves are generated by an actuator and are transferred to the bonding tool, which applies pressure to the wire or ribbon and the bond pad. The combination of heat and pressure results in a strong, permanent bond.

The KS wedge bonder is capable of ultrasonically bonding round aluminum wires with diameters ranging from 25 to 500 microns and aluminum ribbons with cross-sections ranging from 500 x 100 to 2000 x 300 microns.

The ultrasonic bonding process is ideal for bonding aluminum wires and ribbons because it is a fast and efficient method that does not require the use of a filler material or additional heat sources. This results in a clean and reliable bond that is well suited for a variety of applications, including microelectronics and electronics packaging.



Figure 4.9: Wire Bonder Wedge K&S. This picture taken from [37]

4.1.14 The Dilution Refrigerator

The cooling of superconducting radiofrequency (SC RF) circuits to temperatures close to absolute zero is essential to perform experiments in this field. At these temperatures, where $kT \ll \hbar\omega$, thermal noise is greatly reduced, enabling more precise measurements and improved performance of the circuits.

To reach such temperatures, specialized cooling equipment known as Dilution Refrigerators are required. In this work, we used an Oxford Vericold DR-200 model to cool our SC RF circuits.

The Dilution Refrigerator is composed of multiple stages, each kept at a different temperature, ranging from $70K$ to $20mK$. The division of the stages is due to the different physical cooling methods employed at each stage, which effectively limit heat radiation to the base plate.

The operation of the Dilution Refrigerator involves a number of physical processes that can be broadly classified into three cooling steps. Firstly, temperatures in the single-Kelvin scale are achieved through thermal contact with a 4He bath at approximately $4K$. The second step involves cooling the temperature to below $1K$ by means of a Joules-Thompson cycle, which is an endothermic process resulting from the adiabatic expansion of a mixture of 3He and 4He isotopes. Finally, below $\sim 0.9K$, the mixture spontaneously separates into two phases: a 3He -rich phase and a dilute phase. In the mixing chamber, 3He is pumped through the phase boundary into the dilute phase, which leaves the former rich phase in a thermally unstable intermediate phase. The restoration of the two stable phases occurs when 3He crosses the phase boundary back again, which is an endothermic process and the source of the cooling power[51]. The mixing chamber is located on the coldest and lowest plate of the refrigerator, with boxes mounted below or on its vertical extension to increase space for cooling multiple devices simultaneously.

The Dilution Refrigerator is enclosed by multiple thermal isolation cans, and the outer vacuum chamber (OVC) is evacuated to $\sim 10^{-6}$ torr. To protect the

refrigerator and the devices inside from external magnetic fields, three μ -Metal cans are utilized.

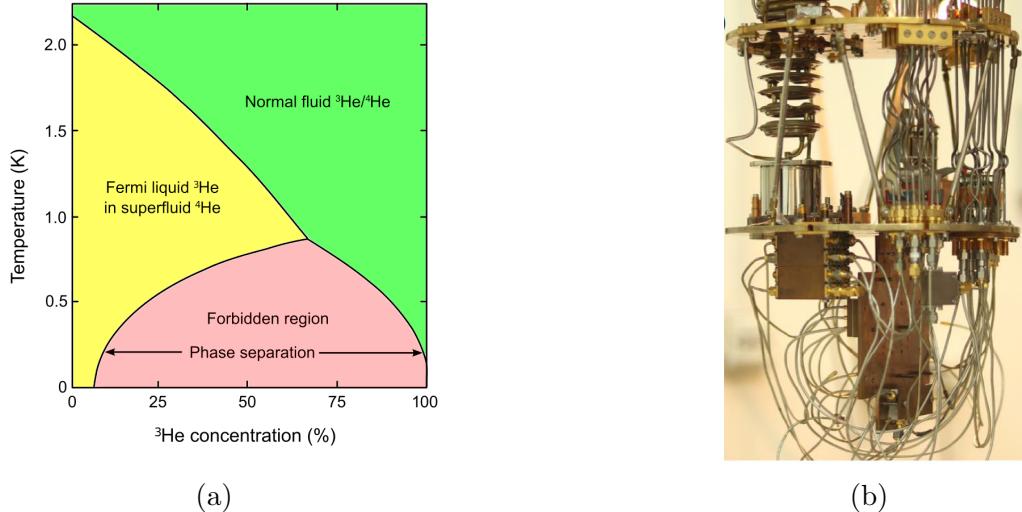


Figure 4.10: (a) Helium mixture phase diagram showing the ^3He -rich region in green, and the diluted region in yellow. The second cooling stage (from $\sim 0.9\text{K}$ to $20m\text{K}$) exploits the unstable state of the intermediate "forbidden" region (pink). Image from Wikipedia (under Wikipedia Commons License), reproduced from [51]. (b) Photography showing our refrigerator's two coldest stages with numerous SMA cables. To the left, the mixing chamber (metallic grey box) is visible).

4.2 Building the amplifier

Building the amplifier involved a lot of trial and error, and it required a thorough understanding of the processes and machines involved in the fabrication of microelectronic devices. In this section, I will describe the process of building the amplifier, the tools and instruments that I used, and the steps I took to find the most effective way of working through each stage of the process.

The amplifier is a critical component in many electronic systems, and it requires careful design and precise fabrication in order to function properly. The process of building the amplifier involved several steps, including spin coating, lithography, etching, liftoff and more. Each of these steps required the use of specialized tools and instruments, and I had to learn how to operate them in order to achieve the desired results.

4.2.1 cleaning

The successful fabrication of microelectronic devices relies heavily on maintaining a clean and controlled environment. The presence of even the smallest particle of dust can cause damage to the delicate features on the wafer, hence it is of utmost importance to maintain a high level of cleanliness throughout the fabrication process. This can be achieved through the implementation of consistent protocols, attention to detail, and the willingness to make adjustments when necessary.

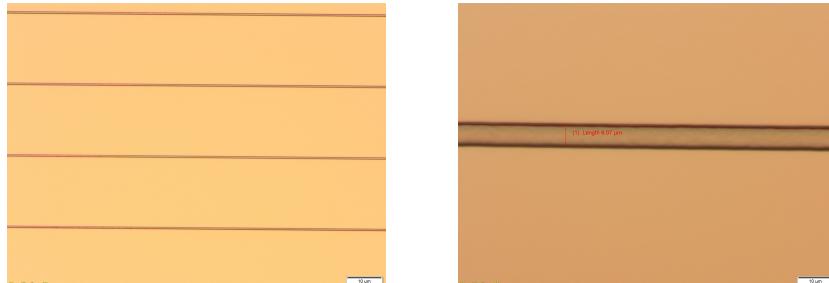
To ensure the cleanliness of the wafer, our lab employs the use of the EDC Spin Processor discussed in chapter 4.7, Plasma Asher discussed in chapter 4.1.10. Additionally, the use of solvents such as isopropanol, ethanol, acetone, NMP and water is crucial in removing contaminants from the wafer. These solvents are highly effective and should be used whenever possible. Using these solvents with sonication process can highly increase their efficiency as well. However, it is important to note that during the fabrication process, it is inevitable for some dirt to adhere to the wafer. Therefore, utilizing these solvents in the appropriate manner and at the correct temperatures can minimize contamination. One potential drawback of using these liquids is that they can be absorbed by the wafer, which may require additional steps to evaporate them. To address this issue, our lab has implemented dedicated steps to ensure that the wafer is properly cleaned and dried.

4.2.2 First layer WSI

The fabrication process for creating WSI strips begins with a high-resistance silicon wafer, which is cleaned using an EDC spinner hood that employs plasma to remove contaminants. The wafer is then sputter coated with WSI, aiming for a thickness of 15 nm. The new layer of WSI is then cleaned using isopropanol, followed by heating the wafer on a 200-degree plate for 20 minutes to evaporate any remaining liquid.

To create the WSI strips as described in chapter 3.2.3, we utilize the wet etch process, which dissolves the WSI everywhere there is no resist. As the features are small in comparison to the size of the chip, we use a negative resist, AZnlof 2020. The features are written using a laser writer with lens 4, 100% filter D-step 3, and gain 9. Additionally, alignment marks are created to aid in aligning the new layer of aluminum to the WSI layer.

After writing the features, the wafer is soft baked for 1 minute and 15 seconds at 110 degrees. The resist is then developed in AZ 726 developer. With a negative resist, it is easy to determine when development is complete, as most of the resist is supposed to wear off, which takes around 25 seconds. The resulting features can be seen in Figure 4.11.



(a) The wafer under $\times 5$ microscope magnification

(b) The wafer under $\times 20$ microscope magnification

Figure 4.11: WSI resist features after lithography

The next step in our process is to hard-bake the wafer at 120 degrees Celsius for 3 minutes prior to the wet etch. We will then use a tungsten etchant to etch the wafer. Heating the etchant to 60 degrees Celsius will achieve an etch rate of 250 \AA/s , which means that the etching should take around 60 seconds. After the etching is complete, we are left with the desired WSI strips, but the resist is also still present on the wafer. In order to remove the resist, we dissolve the wafer in N-Methyl-2-pyrrolidone (NMP) solvent for three hours. The NMP should be heated to a temperature of 70-80 degrees Celsius to ensure effective removal of the resist. At the end of the three hours, sonication for 5-10 minutes in the hot NMP and additional sonication in Isopropanol will aid in cleaning the wafer from the resist. If there is still some resist present after this process, 10 minutes in the Plasma cleaner should remove the resist once and for all. The result can be seen in Figure 4.12. Finally we want to ensure the height of the WSI so we measure it at the Optical Profilometer.

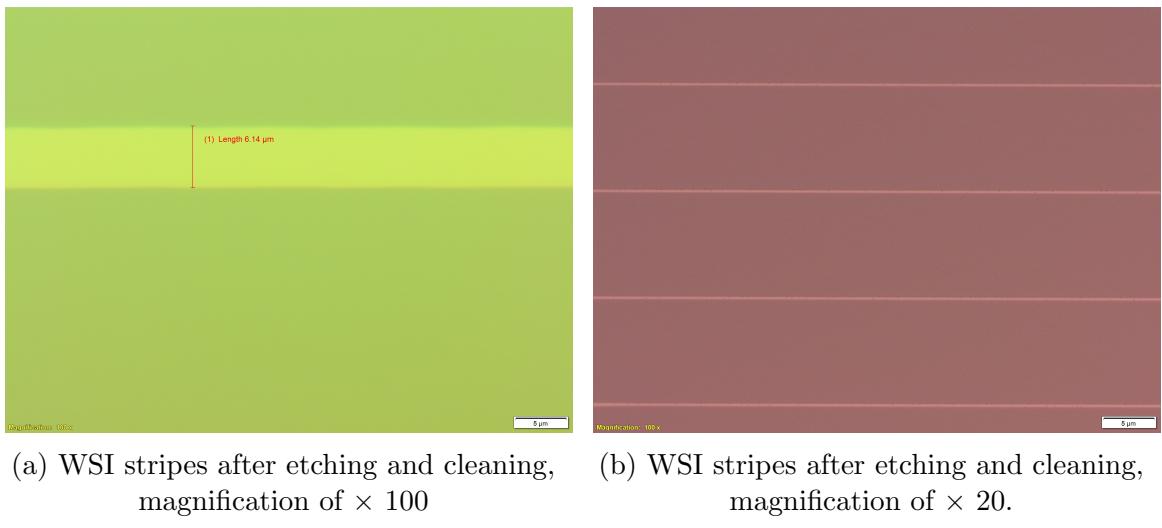


Figure 4.12: WSI stripes after etching and cleaning

4.2.3 Second layer Aluminum

The second layer of the amplifier was challenging to fabricate, as we had to explore different methods and overcome several errors. The methods that failed are documented in the appendix. The final solution we found is the Lift-Off method.

We first cleaned the wafer using Oxygen Plasma in the Plasma Asher for 10 minutes. Then, we used negative resist ma-N 2403 which we spun at 3500 rounds per second and an acceleration of 2 for 30 seconds, resulting in a film thickness of about 300 nm [47]. This film is 3 times thicker than the aluminum thickness which is the ideal ratio for lift off process. After spinning, the wafer was subjected to a soft bake on a 90 degree hot plate for 4 minutes.

The features were created using a precise E-beam writer, and we used alignment marks to ensure the best possible alignment between the two layers. The features were developed in Developer AZ 726 for 23 seconds. The results are shown in Figure 4.13.

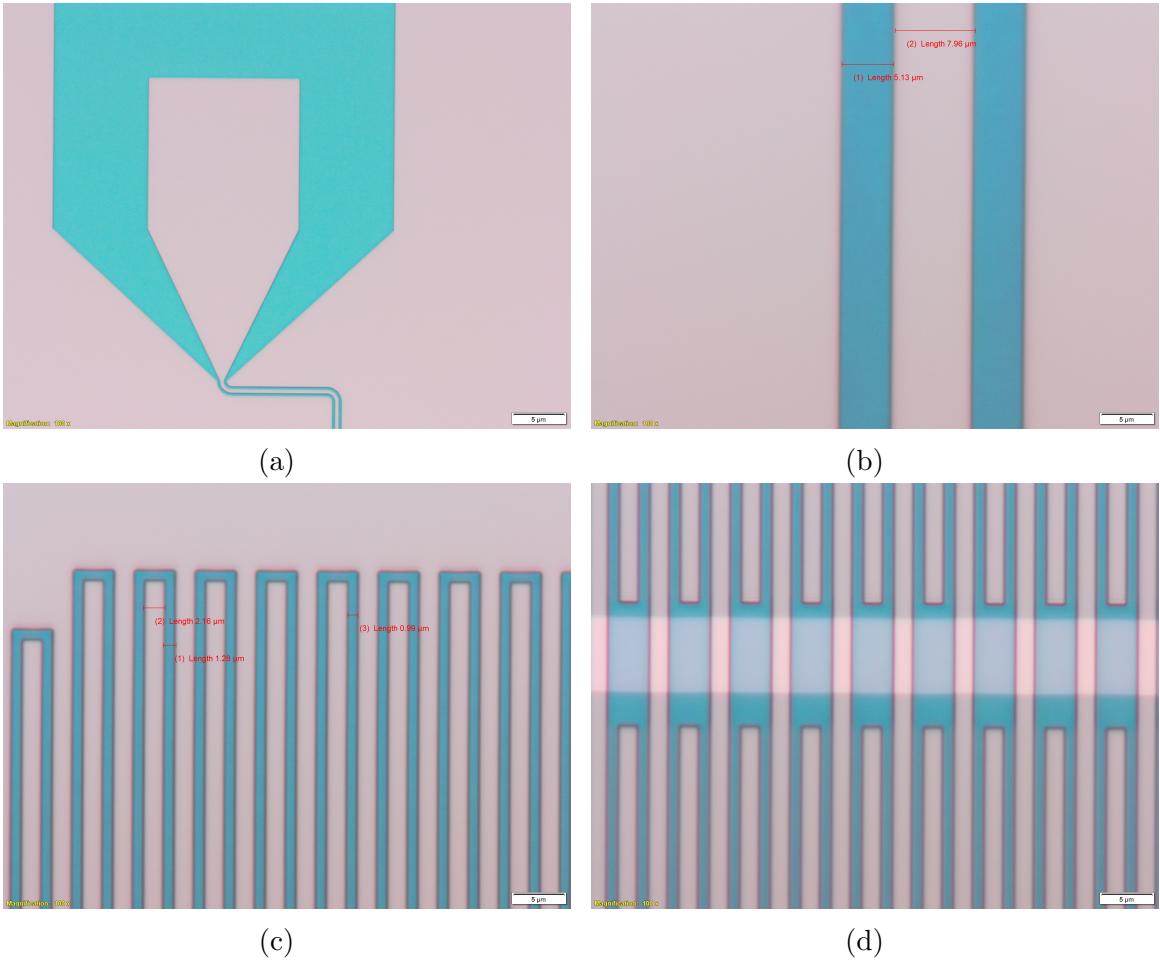
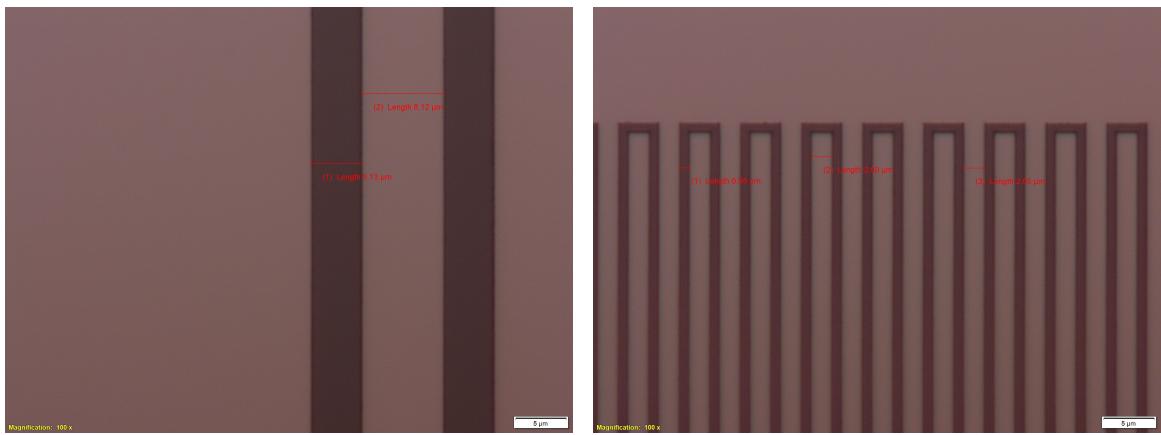


Figure 4.13: ma-2043 resist after writing with E-beam and development: (a) A connector (b) a CPW in the desired magnitude (c) The fingers in the desired magnitude (d) The fingers aligned with the WSI strip.

Next, we deposit a 100 nm layer of aluminum using the Angstrom Quantum Series Evaporator. The subsequent liftoff process involves immersing the wafer in hot acetone for three hours, ensuring sufficient acetone is used to prevent evaporation, which occurs at a temperature of 40 degrees Celsius. Following this, the wafer undergoes sonication for 10 minutes in hot acetone and is then transferred to isopropanol for another 10 minutes of sonication. In some cases, additional sonication with hot acetone and isopropanol may be necessary to fully remove the metal layer. It is important to be mindful during the sonication process to ensure that the features of the wafer are not damaged. The outcome of this process can be seen in Figures 4.14, 3.5, 3.4, and 3.3.

Before the dicing process, it is crucial to cover the wafer with a thick resist in order to protect the features from being damaged from the dicing. For this purpose, we use the resist AZ 4562, which has a thickness of $8.77\mu m$ after spinning at 2000rps for 30 seconds with an acceleration of 4 seconds [45]. The dicing process is then carried out, and the chips are cleaned from the resist using acetone and isopropanol. Finally, the chips are wire bonded to the PCB using the Wire Bonder Wedge KS. The final chip can be seen in Figure 4.15



(b) The fingers in the desired magnitude

Figure 4.14: The KIT amplifier features after lift-off.(a) CPW in the desired magnitude (b) The fingers in the desired magnitude

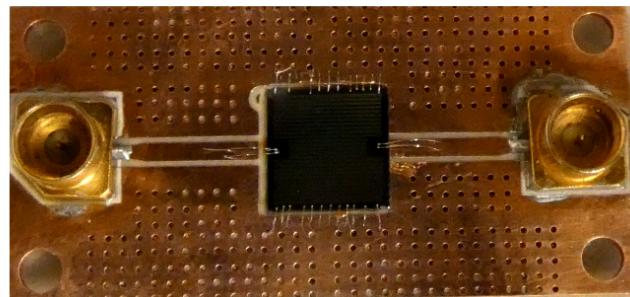


Figure 4.15: Final chip

Chapter 5

Results

In this chapter, we present the results of our experiments, which involved connecting the chip to a Dilution Refrigerator, cooling it down to 3mK, and applying a signal pump and DC current. The aim of these experiments was to observe the effects and compare them with the theoretical and simulated results discussed in Chapter 3.1. Unfortunately, the chip was scratched during the process, which resulted in a disturbance of the resonance features and damaged the desired 50Ω resistance. Due to limited time, we were unable to create a new chip. Despite this setback, we still went ahead with measuring the chip, with the hope of observing some amplification and potential for a perfectly built chip.

5.1 Critical current

In this section, we will present the results of the critical current experiment, which is the first and most fundamental aspect of the chip's behavior. The experiment was conducted by incrementing the current from 0 to 2 mA in steps of 0.1 mA and measuring the power of the outgoing signal S_{21} over the frequency spectrum from 2 to 10 GHz. Prior to measurement, the signal underwent Attenuation of approximately -50 to -60 dBm to protect the refrigerator temperature.

Figure 5.1 shows the results of the experiment, where the signal power ranges from -60 dBm to -140 dBm. It can be observed that even with zero current, there are certain frequencies where no signal is transferred. This could be due to damage to the chip or impedance mismatch with the 50Ω standard. Further experimentation on a new chip un damaged chip could help to determine the exact cause. Additionally, the figure reveals a clear Attenuation in the signal power around 1.6 mA, which suggests proximity to the critical current, I_c . As calculated in Chapter 3.1, I_c is estimated to be around 2.5 mA, and in Figure 5.3 we can see that this value indeed destroys the signal for all frequencies. Any deviation from this critical current could be attributed to fabrication mismatches in the width of $6\mu m$ and height of $15nm$, which may vary by up to 10%, leading to a potential variance in the area of $\sim 14\%$ and thus the critical current. moreover, there is an error estimation in the formula created in Chapter 2.1.4 which comes from the same uncertainty of dimensions in the fabrication which add to the shift from the calculations, A fact that will affect I_* as it is dependent linearly on I_c .

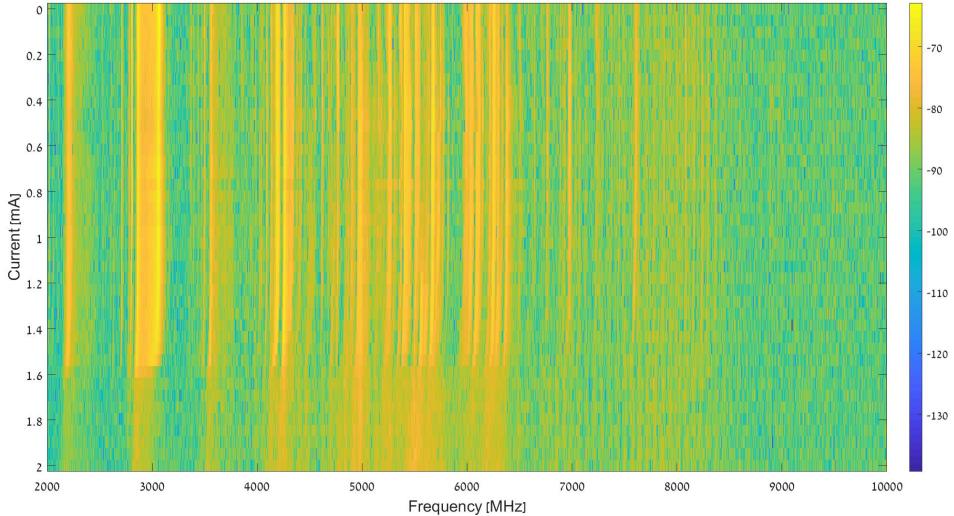


Figure 5.1: Power of S_{21} for different frequencies and currents.

5.2 Amplification results

Obtaining clear amplification from the chip was a challenging task, and the majority of the frequency spectrum did not exhibit much change with the implementation of the pump and DC current. The reasons for these results are difficult to fully identify, but further experimentation with an undamaged chip could provide more insight. Another reason for these results may be ground, we suspect that connecting the chip to the ground wasn't good enough, and more complex methods using better material to connect the ground and make more connections may help.

Despite these challenges, a small portion of the spectrum did show signs of amplification. In this section, we will study this frequency range and perform relevant experiments, comparing them to the simulations presented in Chapter 3.1.

Our focus will be on the frequency range around 3 GHz with a band span of 400 MHz, where we were able to achieve amplification. Figure 5.2 shows the S_{21} signal output without the pump or DC current and will serve as our reference point.

5.2.1 Experiment on the Effect of DC Current on Gain Spectrum

In the relevant spectrum discussed earlier, we applied a 6 GHz pump signal with a power of 20 dBm and varied the system current from 0 to 1.6 mA in increments of 0.2 mA. We also added a current of 2.5 mA to observe the effects of superconductivity breakdown. The results were divided by the results without current and frequency and expressed in dB (all our results will be presented in this manner). The results can be seen in Figure 5.3.

We can observe that the DC current has a positive effect on a significant portion of the spectrum, with the gain increasing as the current increases. We see a peak gain of 10 dB at the frequencies 2860 and 3040 and a relatively stable amplification around 4 dB in the frequency range of 2950-3050. This suggests that these frequencies have suffered the least damage among the frequencies in the spectrum. Our

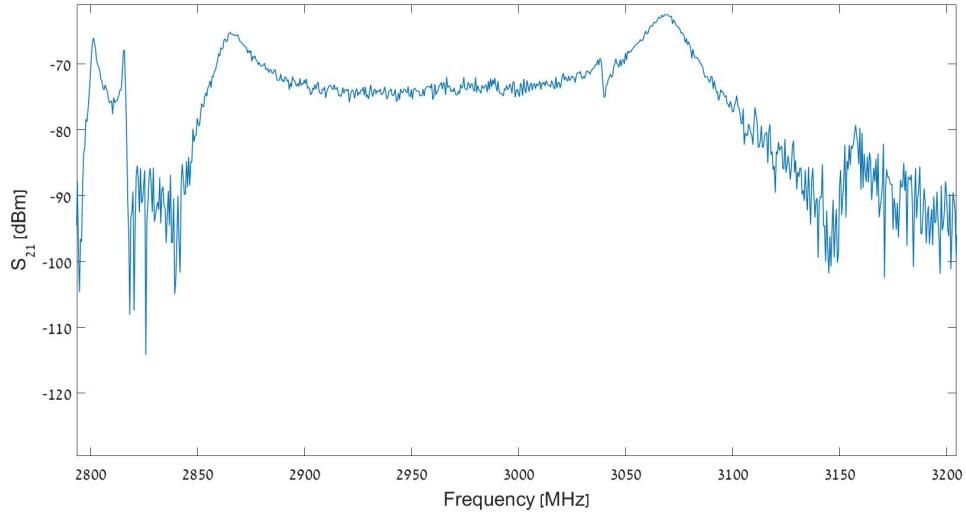


Figure 5.2: Spectrum of S_{21} without pump and DC current.

experiment clearly shows that amplification occurs and that 3WM plays a role, providing evidence that an amplifier can be implemented using the methods presented in this thesis.

5.2.2 Experiment on the Effect of ω_p Frequency on Gain Spectrum

In this experiment, we aimed to evaluate the influence of the pump frequency, ω_p , on the gain spectrum. The DC current was kept fixed at 1.4 mA and the pump power was set to 20 dBm. We varied the pump frequency from 5090 MHz to 6040 MHz in 10 MHz increments and recorded the corresponding gain at each frequency. The results are illustrated in Figure 5.4 and show that although there are minor variations in the gain across the different pump frequencies, the overall results are similar to each other. This is likely due to not fulfilling the condition specified in Equation 2.37 with the experiment parameters.

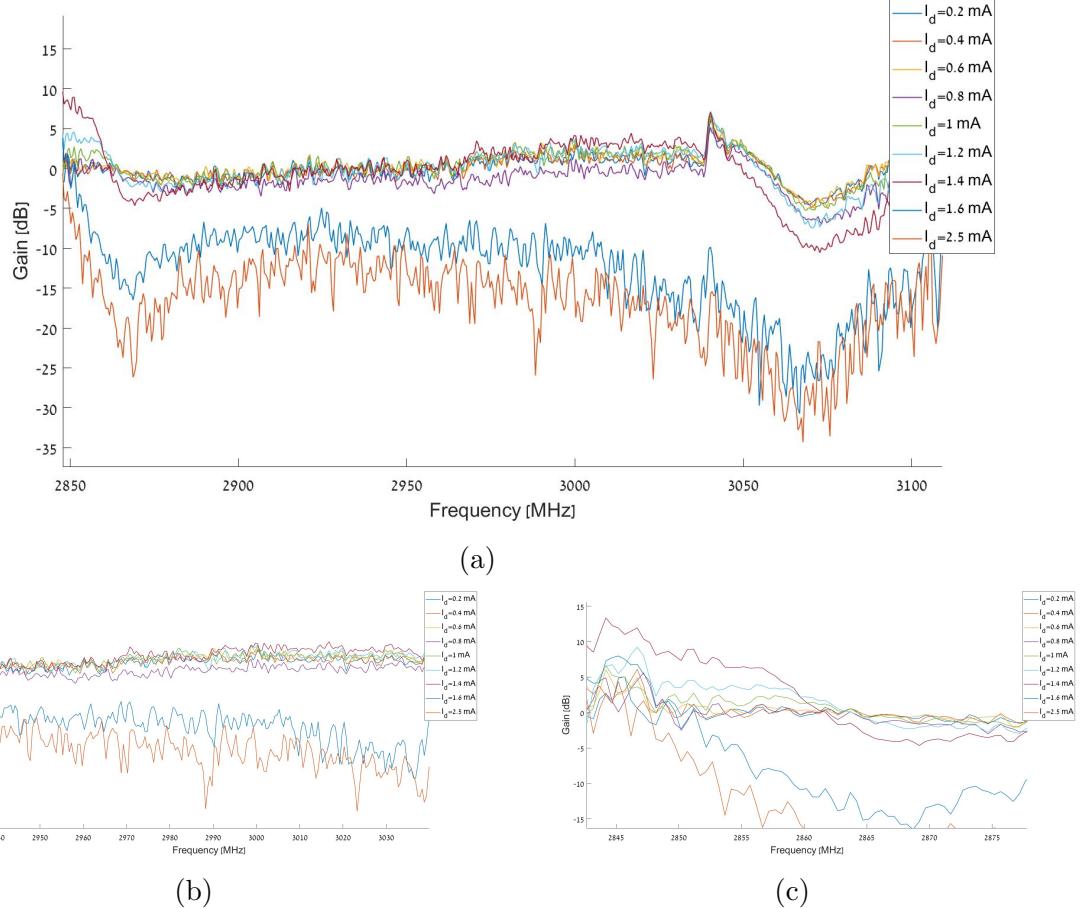


Figure 5.3: The amplification Gain as a function of the frequency for different values of the current (a) The graph shows the gain as a function of frequency over a range of 2850-3150 MHz (b) The graph shows the gain as a function of frequency over a focused range of 2940-3040 MHz. (c) The graph shows the gain as a function of frequency over a focused range of 2840-2880 MHz

5.2.3 Comparison of 3-wave Mixing and 4-wave Mixing

In our final experiment, we compared the effects of 3-wave mixing (3WM) and 4-wave mixing (4WM) [15, 26]. To achieve this, we recorded the amplification results of a pump frequency of 6020 MHz with DC current values of 1.4 mA and 0.8 mA. Additionally, we generated 4WM by implementing a pump frequency of 3010 MHz, which uses two photons instead of one for the amplification effect. The results of this experiment are presented in Figure 5.5, where it can be observed that the majority of the amplified frequencies show stronger results for 3WM, as expected. However, it should be noted that the DC current has a significant impact on the outcome, with lower DC currents potentially altering the results. This experiment highlights the advantages of 3WM over 4WM, although these differences are not significant across the entire frequency spectrum.

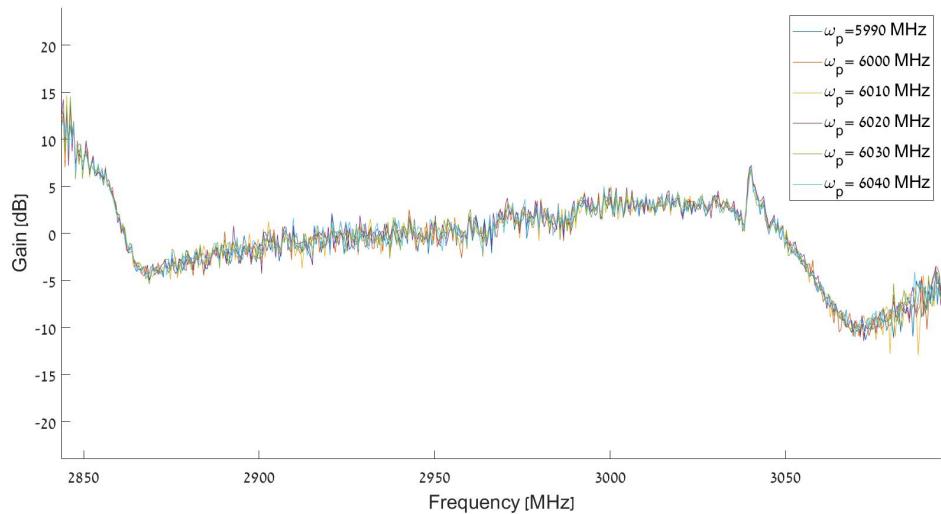


Figure 5.4: The amplification gain as a function of frequency for different values of pump frequency.

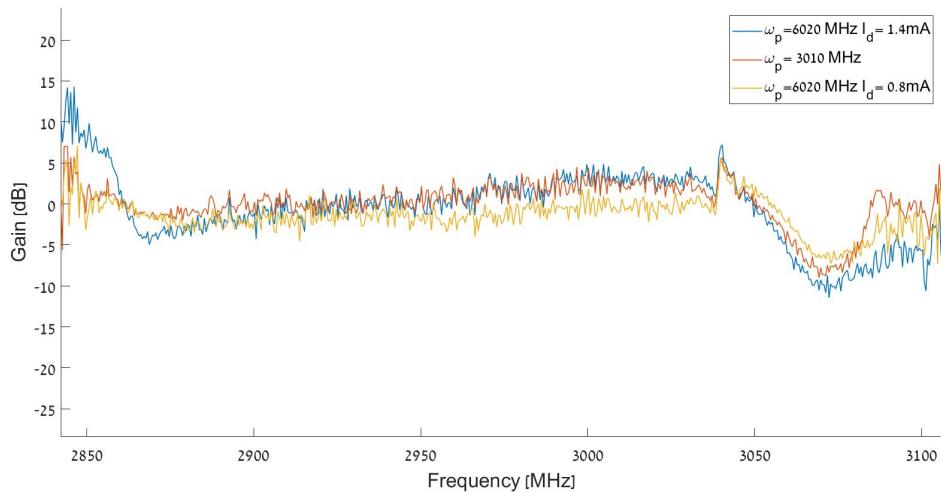


Figure 5.5: The amplification gain as a function of frequency for 4WM and 3WM with $I_d = 1.4$ mA and 0.8 mA.

Summary and outlook

In this thesis, we have presented the theory and implementation of a dc-biased Kinetic Inductance Transistor (KIT) Amplifier. We have covered the fundamental aspects of superconductivity and kinetic inductance, as well as the theory of 3-wave mixing and coplanar waveguide design. We have used these concepts to design and simulate a $6.25 \times 6.25 \text{ mm}^2$ amplifier, achieving in theory 18 dB amplification and a spectrum of 4 GHz with more than 16 dB amplification.

The methodology for building the amplifier was thoroughly discussed, including the work environment in a clean room and the systematic steps involved in the process, such as cleaning, E-beam lithography, lift-off, wet etching, and more. This highlights the importance of precision and carefulness in creating a chip of this nature, as well as the significance of using the right tools and the most accurate methods of work.

After building the amplifier, we cooled and measured it, observing amplification and DC current sensitivity, as well as a superconducting Critical current. Although the amplifier was slightly damaged, the results show potential for further trials. These trials include the creation of an undamaged amplifier and a series of experiments comparing the results to the theoretical and simulated outcomes presented in this thesis. We plan to scan a broader range of amplifier dimensions in order to achieve impedance matching and a broadband amplification with intrinsic loss.

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