Design of a CMOS OTA in BiCMOS8HP Technology

Authors:

Or Fachima
Arsen Arutyunov

Date: 12/01/2025

Introduction

This report presents the design and simulation of a CMOS Operational Transconductance Amplifier (OTA) using the BiCMOS8HP technology. The primary objective is to achieve a high-performance OTA that meets specific requirements for gain, bandwidth, phase margin, and power efficiency. The design process involves careful selection of components, circuit optimization, and detailed simulation to ensure compliance with the desired specifications. Through this work, various aspects of analog circuit design are explored, including stability analysis, noise performance, and transient behavior.

Circuit Design and Schematic

Device Parameters

The table below summarizes the key parameters for the transistors and other components used in the design:

Device	**Length (L)**	**Width (W)**	g_m **(uS)**	g_{ds} **(uS)**
M1	0.4μm	12μm	910.2	14.48
M2	0.4μm	12μm	910.2	14.48
M3	3.6μm	120μm	437.4	7.555
M4	3.6μm	120μm	437.4	7.555
M5	0.7μm	2.8μm	531.3	28.35
M6	0.2μm	28.8μm	1542	32.17
M7	3.1μm	10.2μm	605.5	21.02
M8	0.7μm	0.3μm	52.13	3.612
Cc		1.1pF		
R0		147.1kΩ		
R3		7kΩ		

Table 1: Summary of device parameters in the OTA design.

Schematics

The following figures illustrate the OTA schematics with operating currents and voltages:

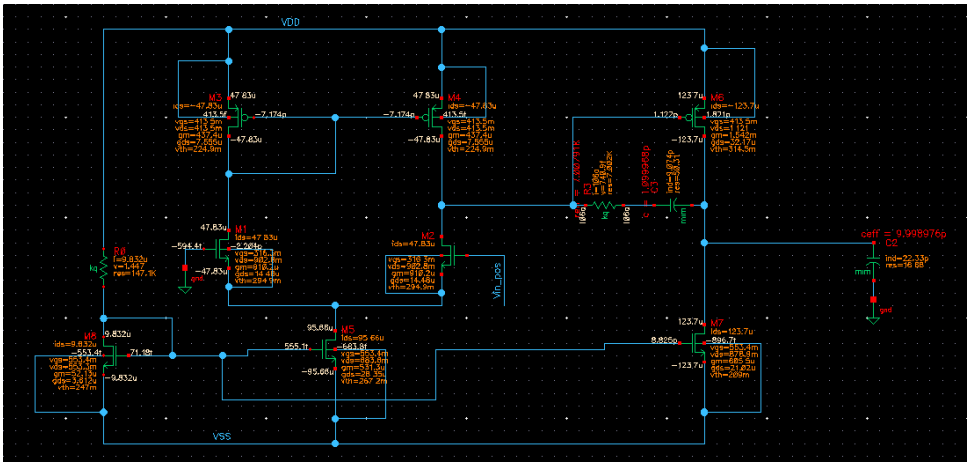


Figure 1: OTA schematic with currents.

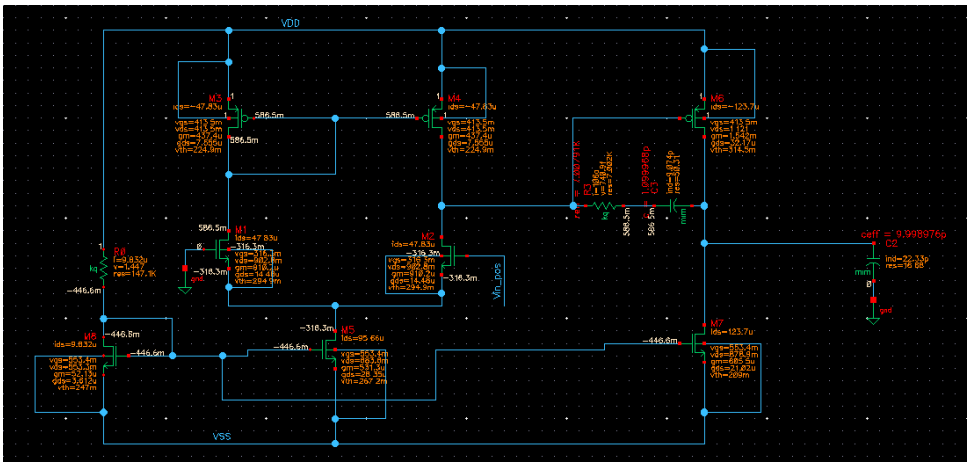


Figure 2: OTA schematic with operating voltages.

Simulation Results

DC Analysis

Power Calculation

The power consumption was analyzed based on the voltage and current sources. The calculation is shown below:

$$P = V \cdot I = 2 \cdot 229.2\mu = 458.4\mu\text{Watt}$$

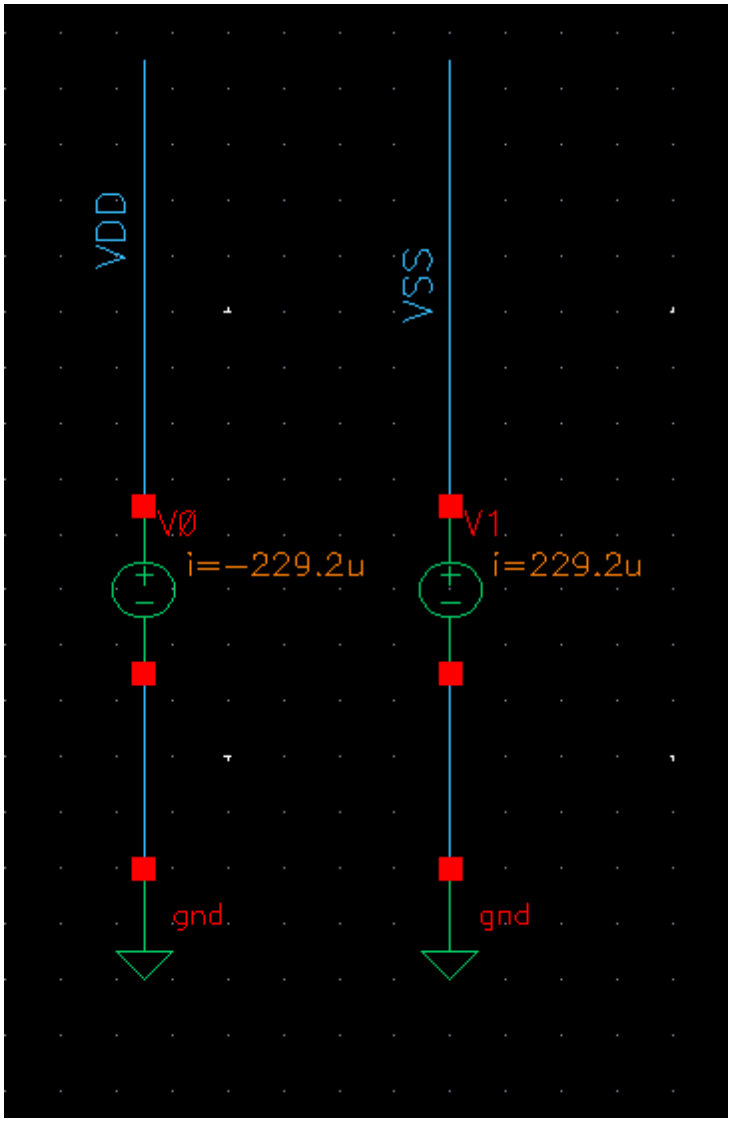


Figure 3: Power calculation based on DC voltage and current sources.

AC Analysis

Frequency and Phase Response

The gain and phase response are shown in the same plot. The achieved gain is 61.49 dB with a bandwidth of 90.6 kHz. The unity gain frequency was 50.46 MHz, and the phase at this frequency (from the AC simulation) is -130 degrees.

It is important to note that the unity gain frequency is lower than the GBW. This behavior arises because the system is not a purely single-pole system. While it was possible to achieve a perfect separation of poles, we opted for a trade-off to reduce power consumption. The gain-bandwidth product (GBW) was calculated as follows:

$$\text{GBW} = \text{Gain} \cdot \text{BW} = 10^{\frac{61.49}{20}} \cdot 90.6\text{kHz} = 107.55\text{MHz}$$

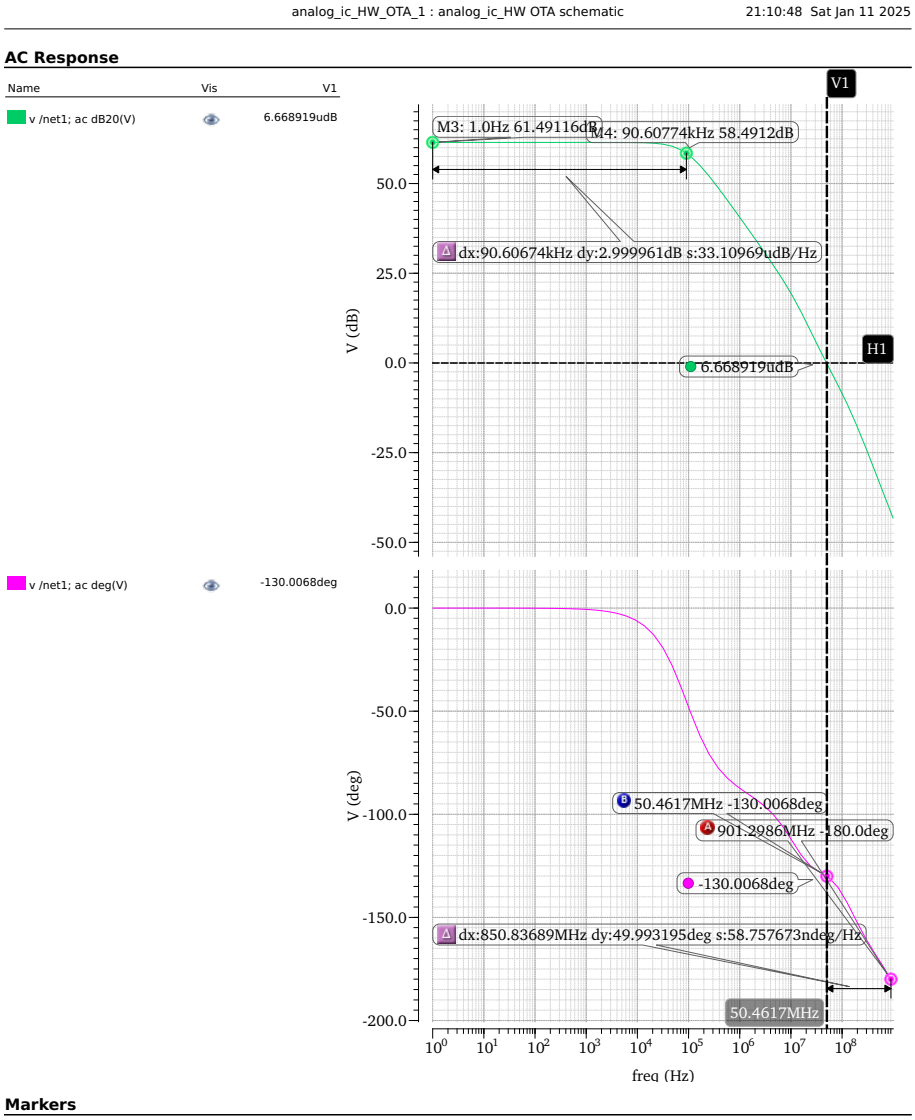


Figure 4: AC simulation results showing gain and phase response.

CMRR Results

To efficiently compute the CMRR, a test bench was created to calculate both the differential and common-mode gains. The test bench is shown in the figure below:

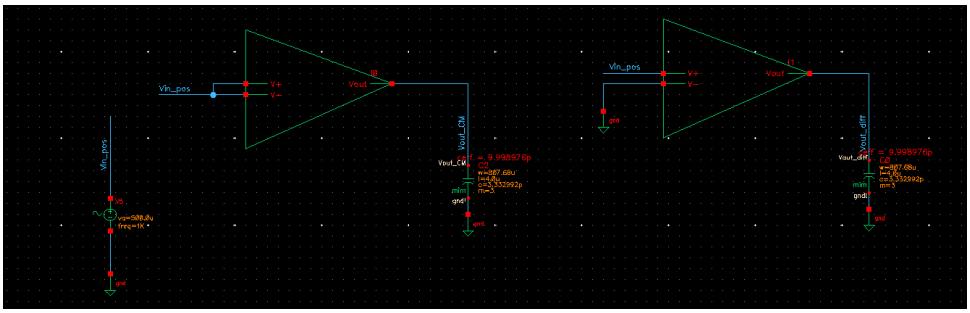


Figure 5: Test bench for calculating differential and common-mode gains.

The CMRR was calculated using the formula:

$$\text{CMRR} = 20 \cdot \log_{10} \left(\frac{A_{\text{diff}}}{A_{\text{cm}}} \right)$$

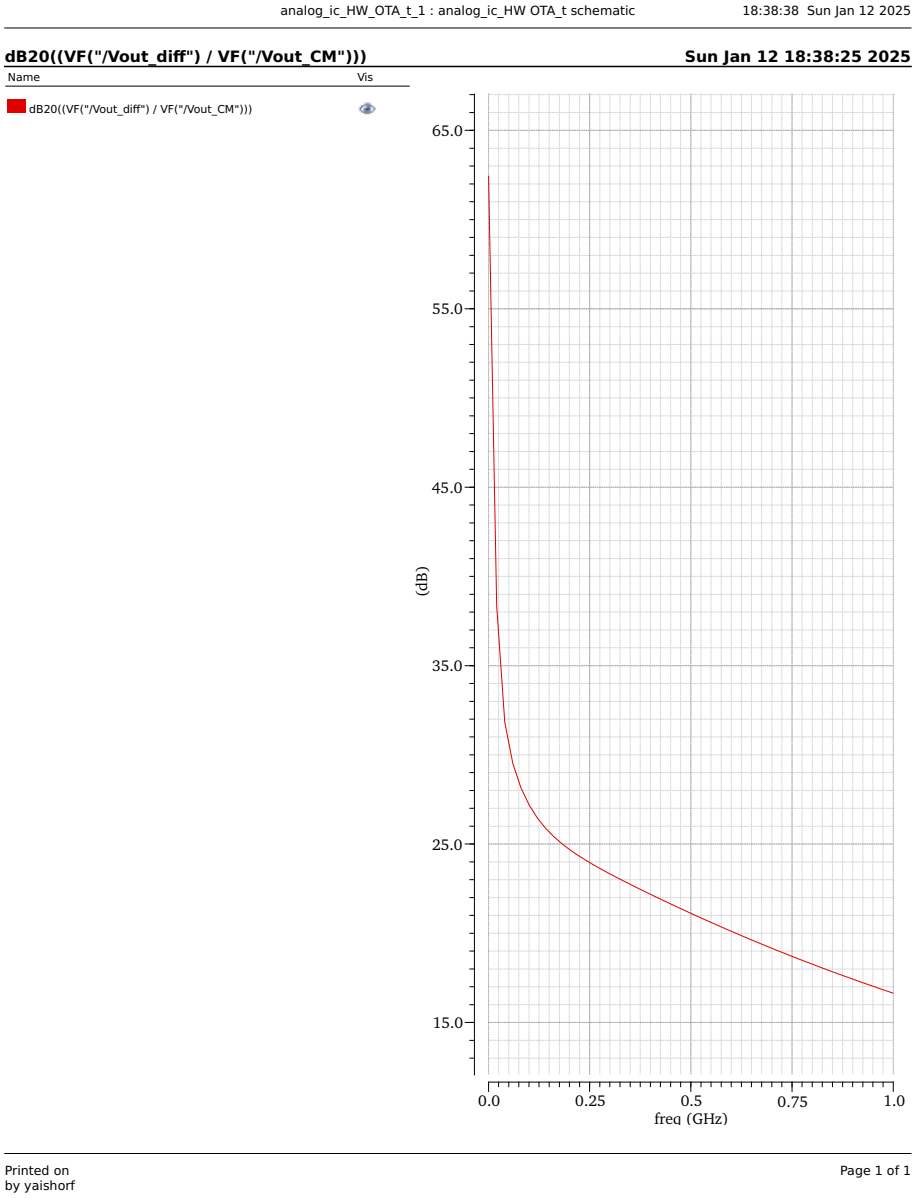


Figure 6: CMRR results showing the calculated values.

The following figure shows a comparison of the common-mode and differential gains:

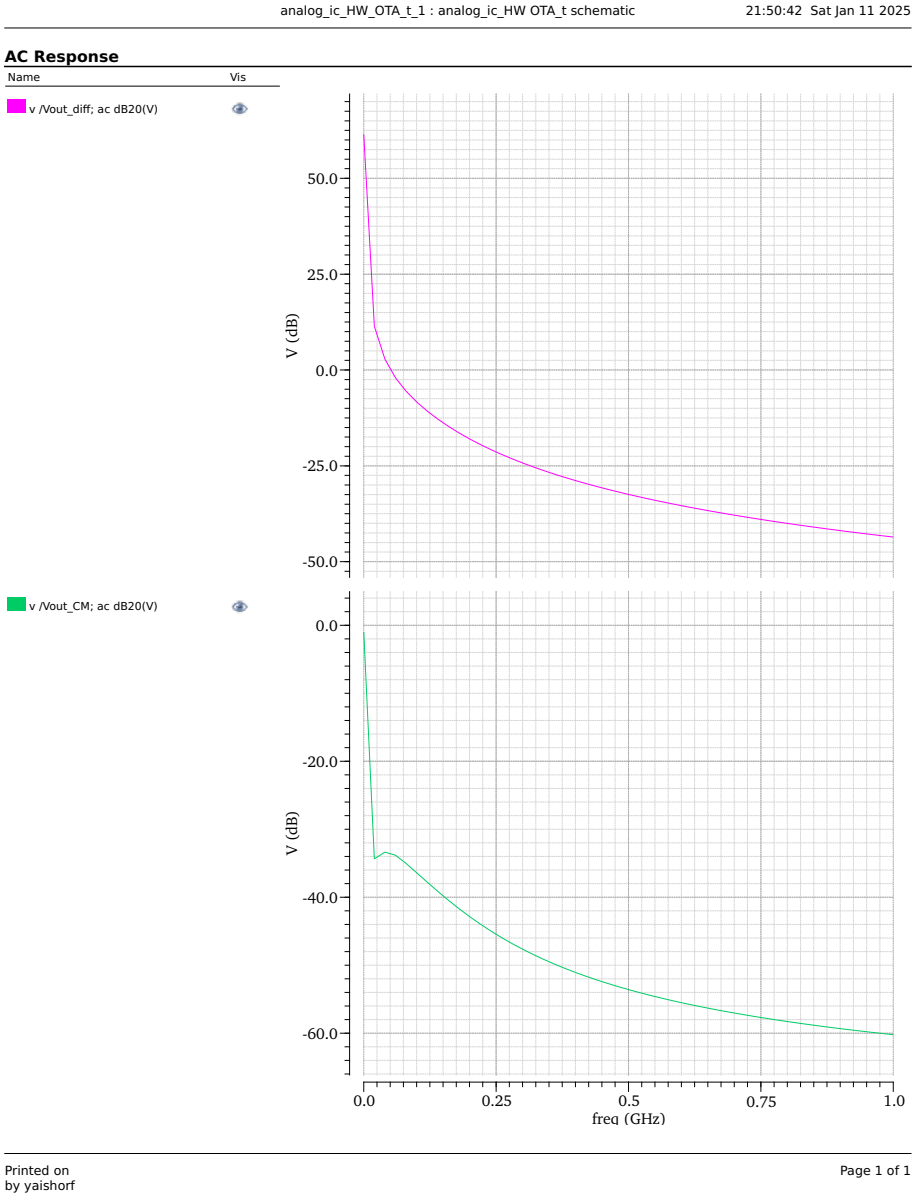


Figure 7: Common-mode versus differential gain plots.

It is evident that the circuit rejects the common-mode signal efficiently and predominantly amplifies the differential signal.

Input and Output Impedance

The input and output impedance of the circuit were analyzed using the results shown in the following figures:

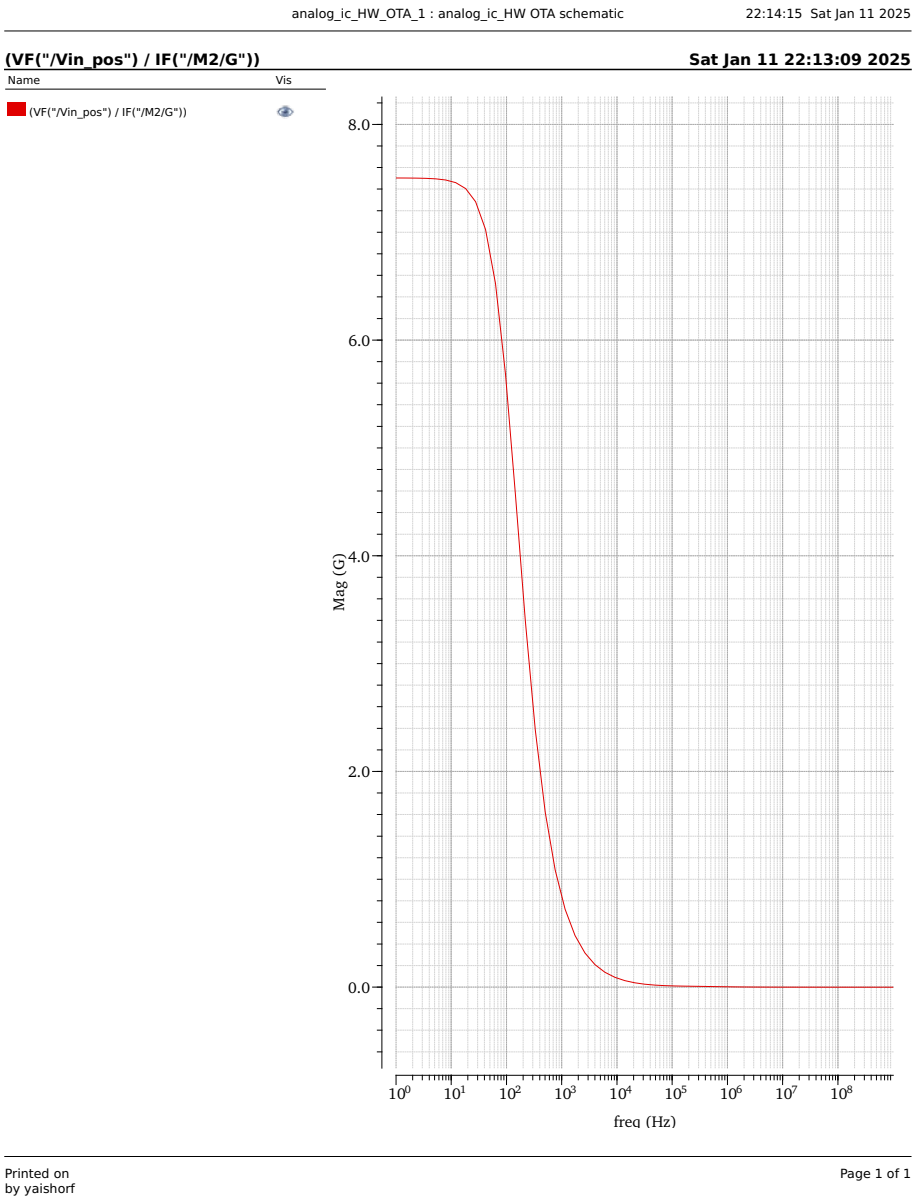


Figure 8: Input impedance analysis showing a high value of approximately 8GΩ for low frequencies, typical for OTA gate input.

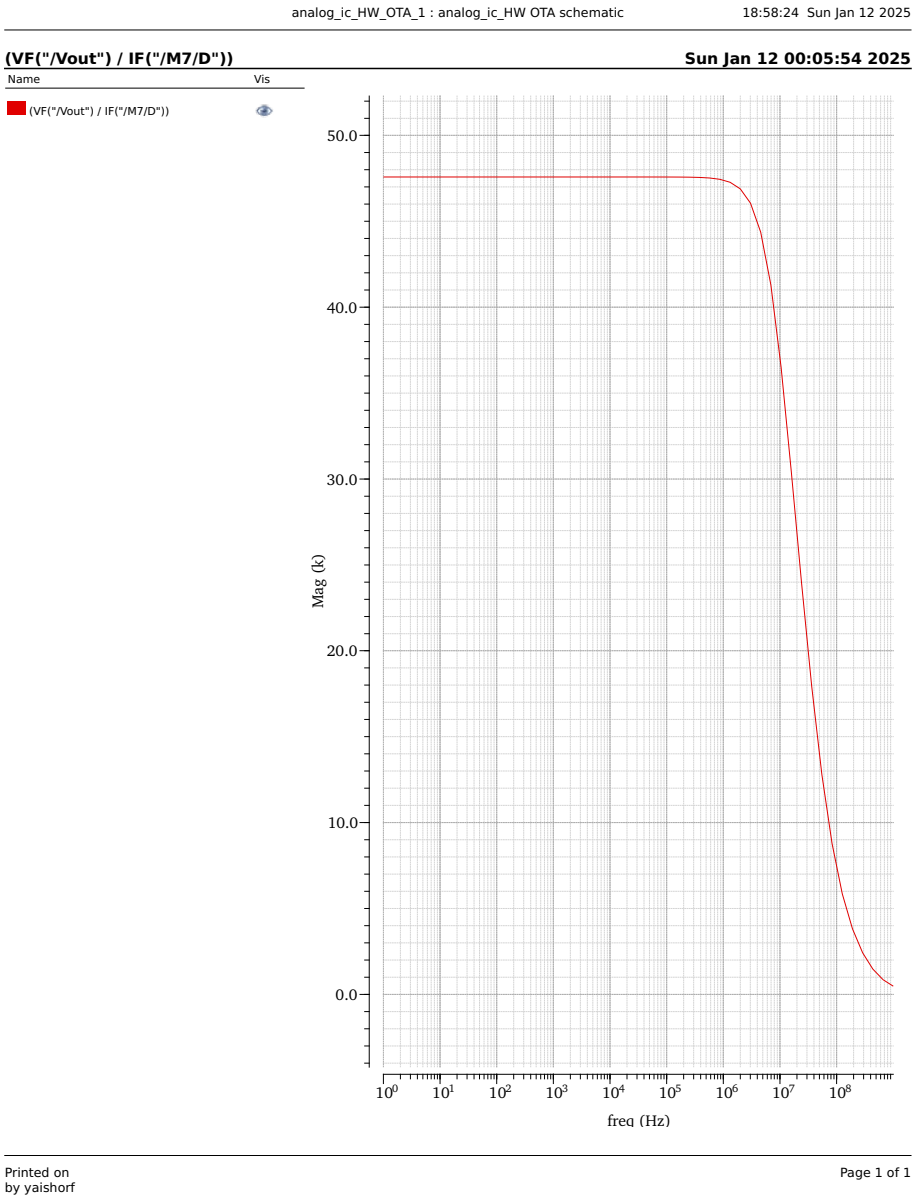


Figure 9: Output impedance analysis showing a value of approximately 47.5kΩ.

Transient Analysis

For the transient analysis, a sinusoidal input signal with an amplitude of 0.5 mV and a frequency of 1 kHz was applied. The output signal was observed to be symmetric with an approximate amplitude of 540 mV. A slight asymmetry of 4 mV was noted. The following figures show the output signal and its zero-centered version for clarity:

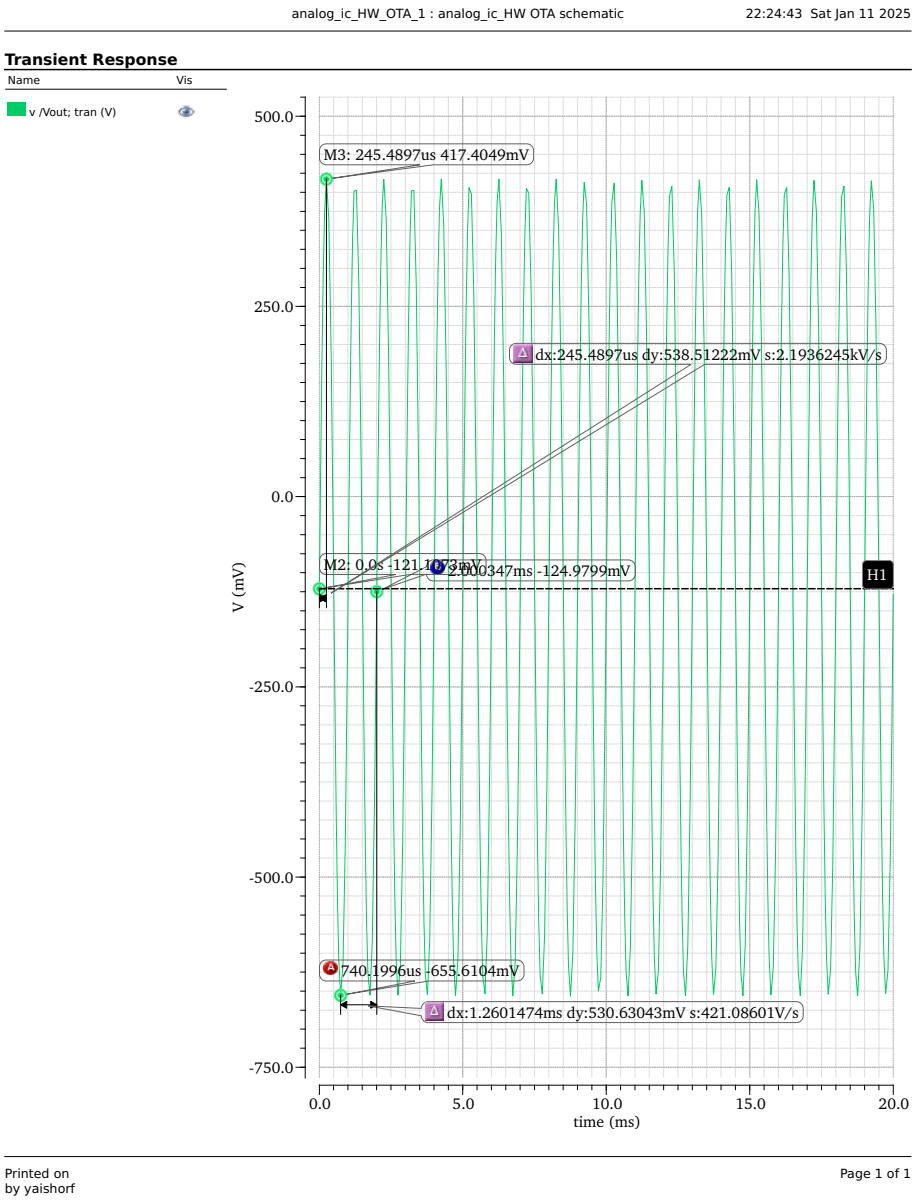


Figure 10: Output signal for a sinusoidal input of 0.5 mV amplitude at 1 kHz.

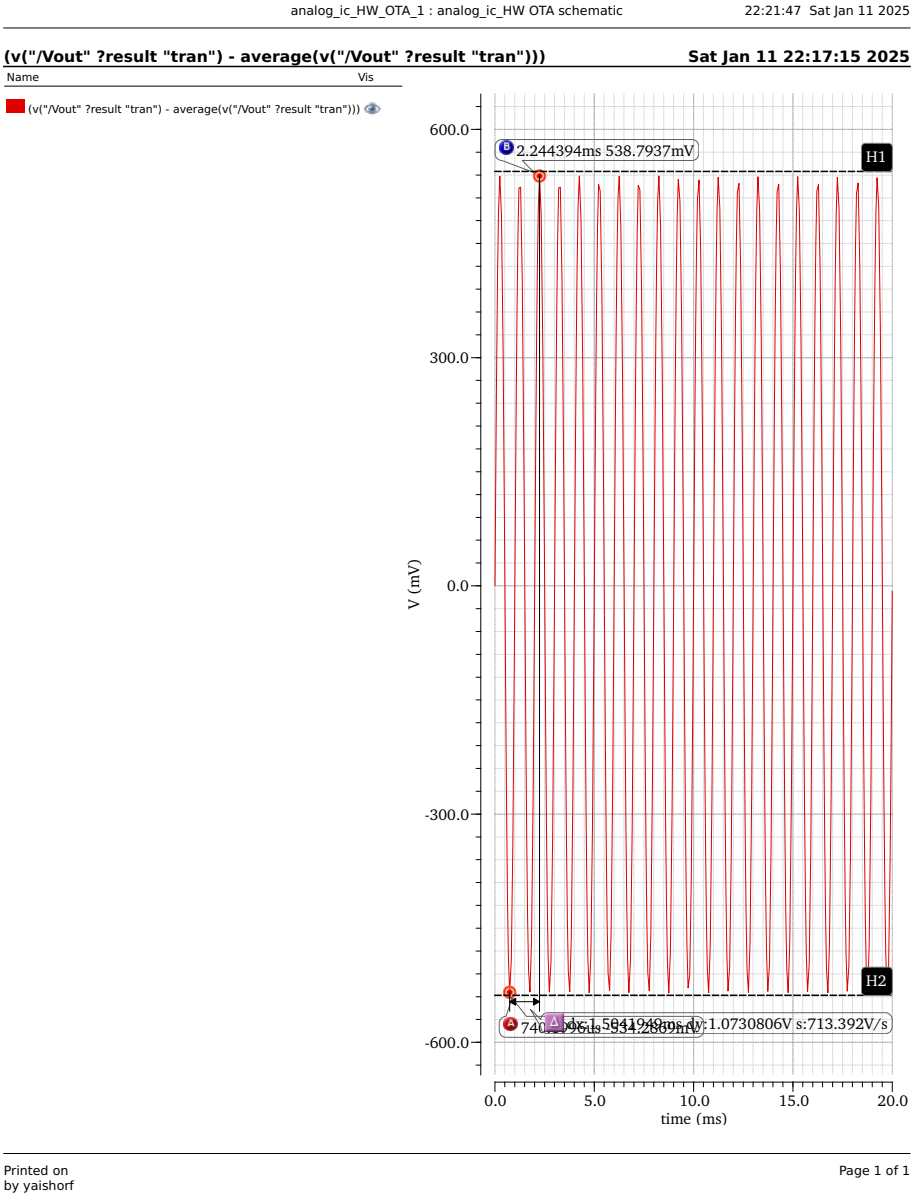


Figure 11: Zero-centered version of the output signal for better visualization.

Slew Rate (SR)

To measure the SR, a pulse signal with an amplitude of 1 V was applied to evaluate the speed at the output. Using the simulator's calculator, the measured value was:

$$\text{SR} = 81\,\text{V/µs}.$$

This was also measured analytically by calculating the derivative of V_{out} over time. The analytical result aligns well with the theoretical relationship:

$$\text{Slew Rate} = \frac{I_5}{C_c} = \frac{95\,\mu\text{A}}{1.1\,\text{pF}} \approx 86.3\,\text{V/µs}.$$

The following figures illustrate the results from both methods:

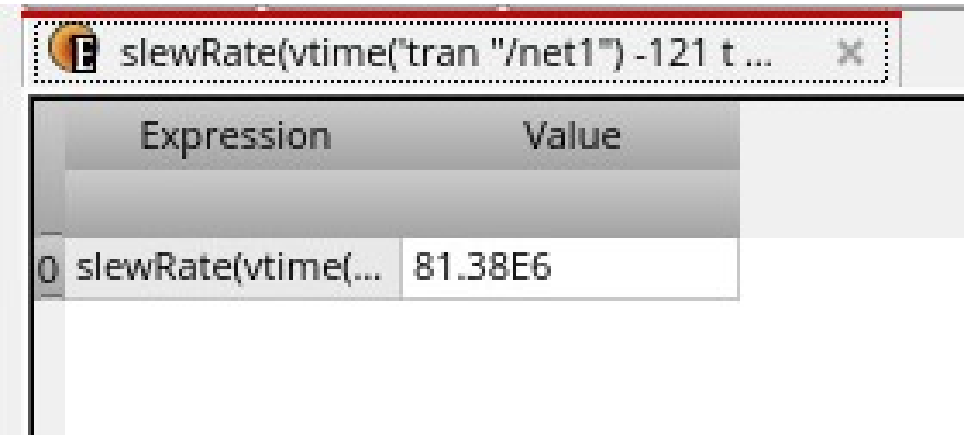


Figure 12: Slew rate measurement using the simulator's calculator.

This was also measured analytically by calculating the derivative of Vout over time.

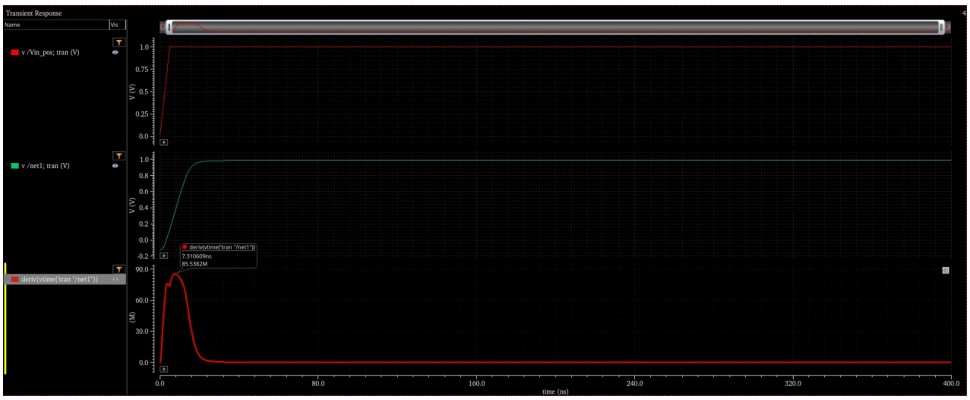
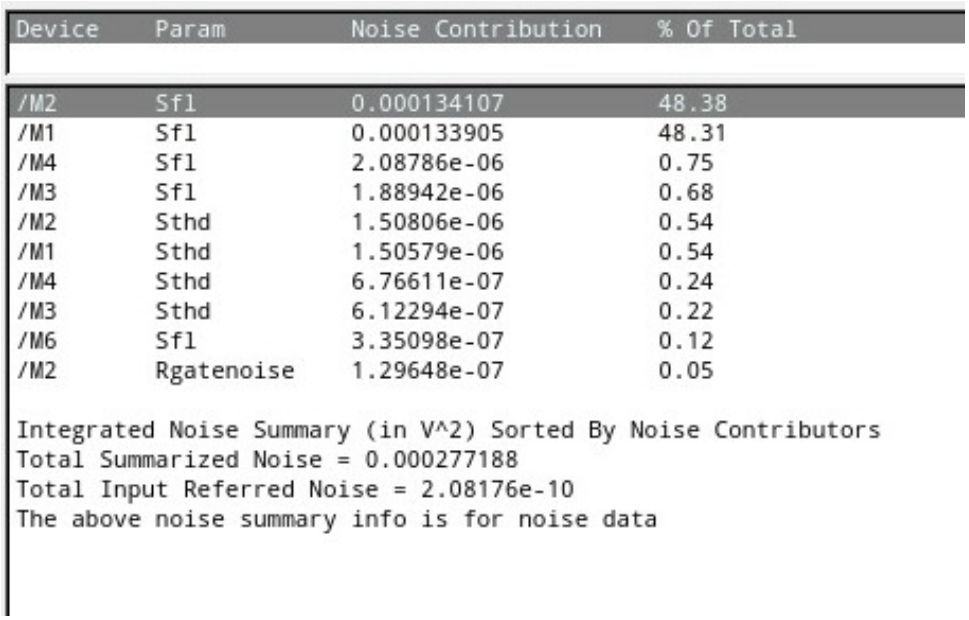


Figure 13: Measurement of the slew rate based on the derivative of V_{out} over time.

Noise Analysis

The noise analysis was conducted to evaluate the output voltage and current noise. It can be observed that the output voltage noise increases approximately by the gain (about 1000) relative to the input voltage noise. This behavior is expected and aligns with the amplifier's gain characteristics.

Additionally, the total integrated noise over the bandwidth was calculated using the simulator's calculator with the integration limits set to match the bandwidth. The integrated noise is shown in the figure below:



Device	Param	Noise Contribution	% Of Total
/M2	Sfl	0.000134107	48.38
/M1	Sfl	0.000133905	48.31
/M4	Sfl	2.08786e-06	0.75
/M3	Sfl	1.88942e-06	0.68
/M2	Sthd	1.50806e-06	0.54
/M1	Sthd	1.50579e-06	0.54
/M4	Sthd	6.76611e-07	0.24
/M3	Sthd	6.12294e-07	0.22
/M6	Sfl	3.35098e-07	0.12
/M2	Rgatenoise	1.29648e-07	0.05

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 0.000277188
Total Input Referred Noise = 2.08176e-10
The above noise summary info is for noise data

Figure 14: Total integrated noise over the bandwidth.

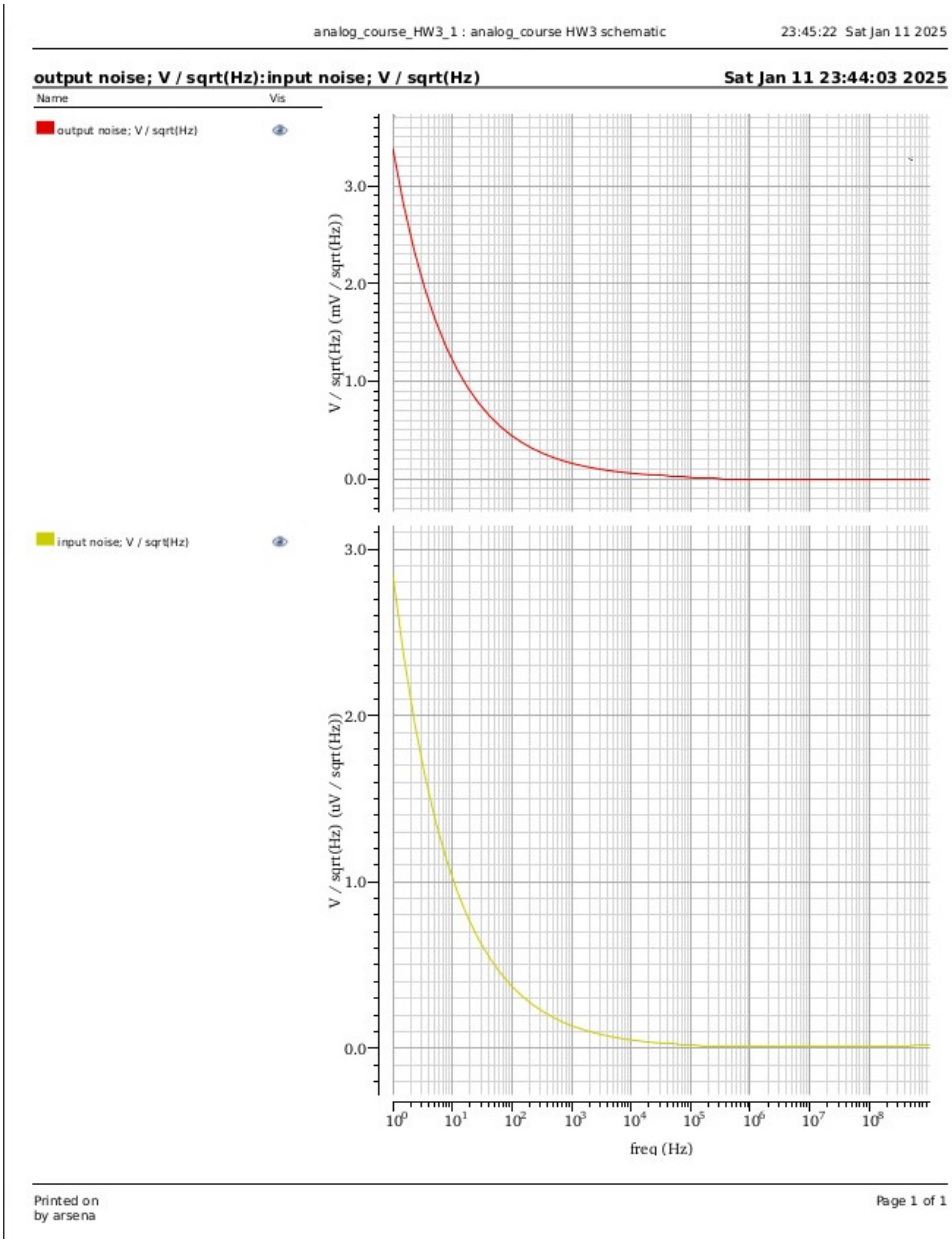


Figure 15: Output voltage noise simulation result.

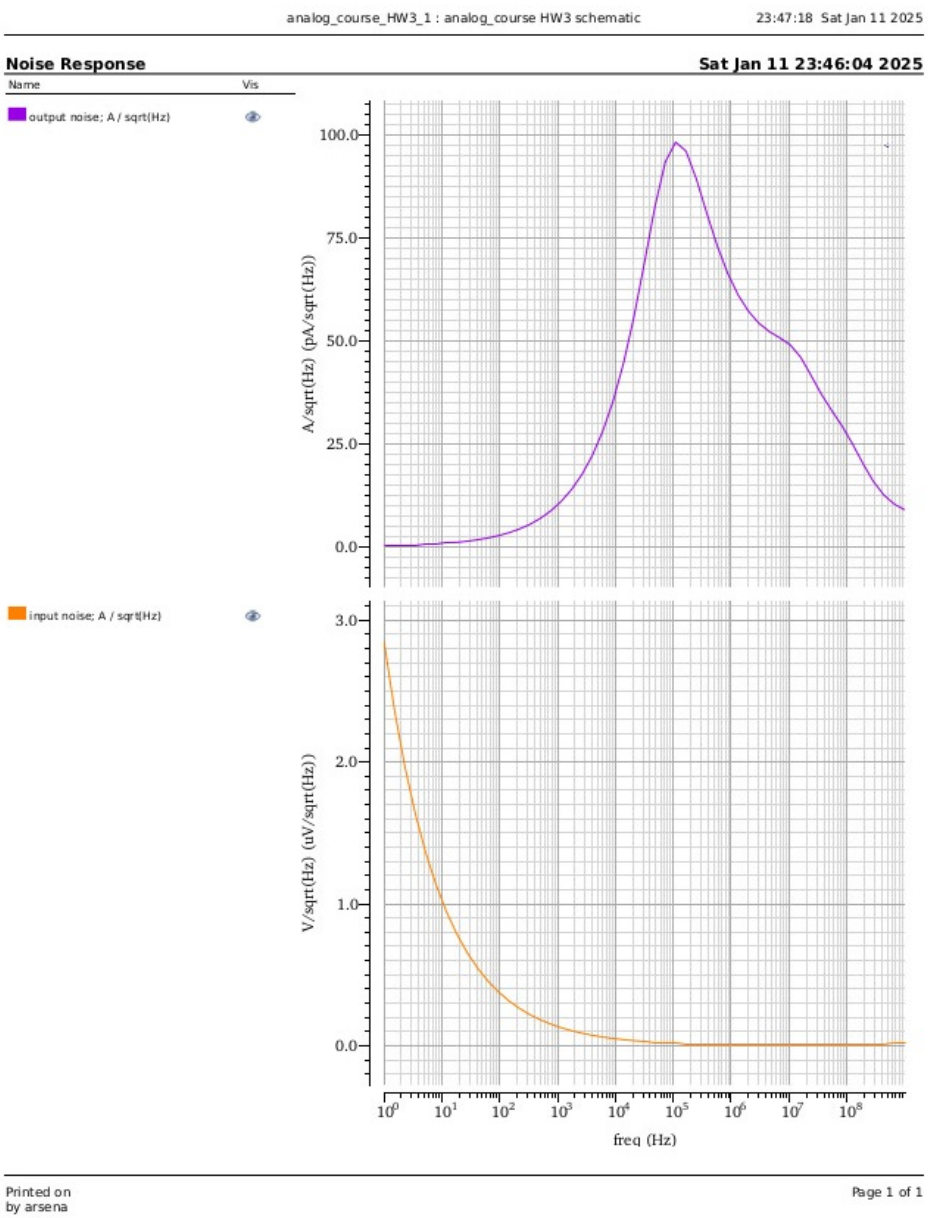
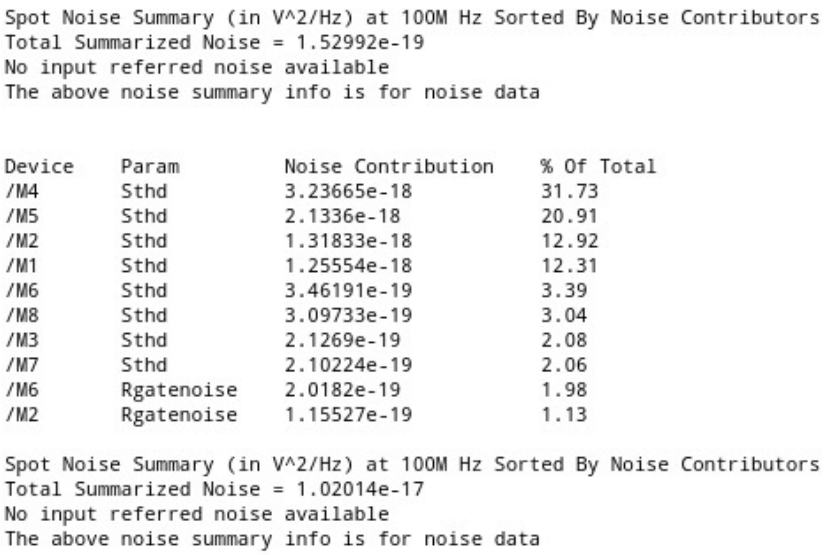


Figure 16: Output current noise simulation results.

Additionally, the top 10 noise contributors at 100MHz were analyzed and summarized in the following figure:



Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.52992e-19
No input referred noise available
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/M4	Sthd	3.23665e-18	31.73
/M5	Sthd	2.1336e-18	20.91
/M2	Sthd	1.31833e-18	12.92
/M1	Sthd	1.25554e-18	12.31
/M6	Sthd	3.46191e-19	3.39
/M8	Sthd	3.09733e-19	3.04
/M3	Sthd	2.1269e-19	2.08
/M7	Sthd	2.10224e-19	2.06
/M6	Rgatenoise	2.0182e-19	1.98
/M2	Rgatenoise	1.15527e-19	1.13

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.02014e-17
No input referred noise available
The above noise summary info is for noise data

Figure 17: Top 10 noise contributors in the OTA design.

It is noteworthy that M4 ranks as the highest contributor to the noise, which aligns with its size and role in the circuit. Interestingly, M3, despite having the same size as M4, contributes significantly less noise, highlighting differences in their operational conditions and roles in the circuit.

Stability Analysis

To achieve accurate results, a stability simulation was performed. The results were as follows:

- Gain Margin (GM): 46 dB
- Phase Margin (PM): 49.07 degrees

The following figure illustrates the stability plot from the simulation:

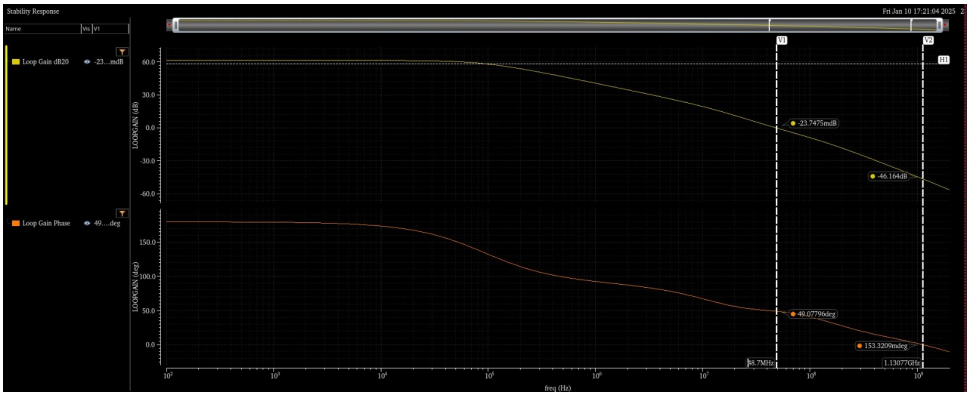


Figure 18: Stability simulation results showing gain and phase margins.

Discussion and Observations

When we started the task, we initially followed the equations strictly to achieve the desired ratios. This approach led to excessively large transistor sizes and significant current consumption. The turning point in the task came when we decided to focus on the principles rather than the exact numerical results. This shift allowed us to design a circuit that, in our opinion, is far more optimal compared to the initial design.

We will now summarize the steps and considerations taken during the design process, categorized by the components involved:

M8: M8 was designed to provide a stable bias voltage for the current mirrors and the input stage. Its sizing was optimized to minimize its impact on the overall power consumption.

M5: M5 serves as the current source for the first stage. While it is not the sole factor affecting g_{m1}, it plays a significant role in limiting its values. Furthermore, M5 strongly impacts the gain of the first stage due to the reduction of R_{out4} as the current increases. The sizing of M5 was adjusted to balance the trade-off between gain and current consumption. See Figure **??**.

M1 and M2: To achieve the desired g_{m1} for a GBW greater than 100 MHz, we carefully sized M1 and M2. We initially determined the current through these transistors and then adjusted their lengths and widths to achieve a g_{m1} of approximately 3.14 m. This value, along with a compensation capacitor of half the load capacitance ($C_c = 0.5C_L$), enabled us to reach the GBW target. However, to reduce parasitic capacitances, we opted for a g_{m1} value reduced by a factor of 3 and compensated for it with a smaller C_c. Finally, as the gain was slightly below the desired level, we fine-tuned the widths of M1 and M2 to minimize V_{ov}, ensuring the required gain. See Figure **??**.

M3 and M4: To ensure proper gain in the second stage while maintaining reasonable transistor sizes, we adjusted the lengths and widths of M3 and M4. A key consideration was reducing the V_{ov} of M6 by slightly decreasing the length of M4. This optimization ensured the required V_{ov} for M6 in order to increase the gain . See Figures **??**.

M6 and M7: Initially, M6 and M7 were sized very large to ensure the desired pole splitting and phase margin. However, this resulted in high power consumption and excessive transistor sizes. To optimize this stage, we introduced a compensation resistor (R_3) and fine-tuned the compensation capacitor (C_c), which allowed us to reduce the sizes of M6 and M7 significantly while maintaining a PM above 45 degrees. Additionally, the channel length of M7 was increased to improve the output resistance and ensure the desired gain. Finally, W_6 was adjusted to achieve a symmetric output swing.

Compensation Capacitor and Resistor: The compensation components were critical for optimizing the GBW and PM. Initially, we set C_c to half the load capacitance and R_3 to zero. This setup resulted in a low GBW and high PM. By carefully tuning C_c and R_3, we observed a significant improvement in GBW, which increased from below 100 MHz to 110 MHz, and a stable PM above 45 degrees. Furthermore, the optimized C_c and R_3 reduced the influence of the zero introduced by R_3, allowing for smaller g_m values in M6 and M7, thereby reducing power consumption. See Figures **??** and **??**.

This systematic optimization process allowed us to achieve the desired specifications while minimizing power consumption and maintaining performance within the required parameters.

Summary of Achieved Results

The table below summarizes the required specifications and the achieved results for the CMOS OTA design. The measured output swing was found to be $-0.884\,\mathrm{V}$ to $0.884\,\mathrm{V}$, as illustrated in Figure **??**.

Parameter	**Required**	**Achieved**
Gain (A_0)	60 dB	61.49 dB
Gain Bandwidth (GBW)	100 MHz	107.5 MHz
Phase Margin (PM)	$>45°$	49°
Unity Gain Frequency	Not specified	50.4 MHz
Power Consumption	Not specified	458 µW
Dynamic Range	Not specified	-0.884 V to 0.884 V

Table 2: Summary of required specifications and achieved results.

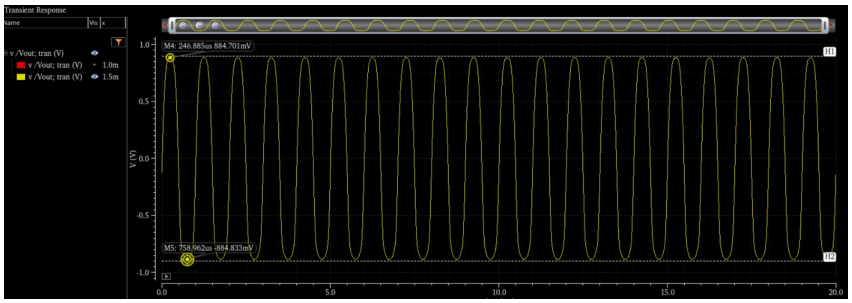


Figure 19: Measured output swing of the CMOS OTA.

Figures

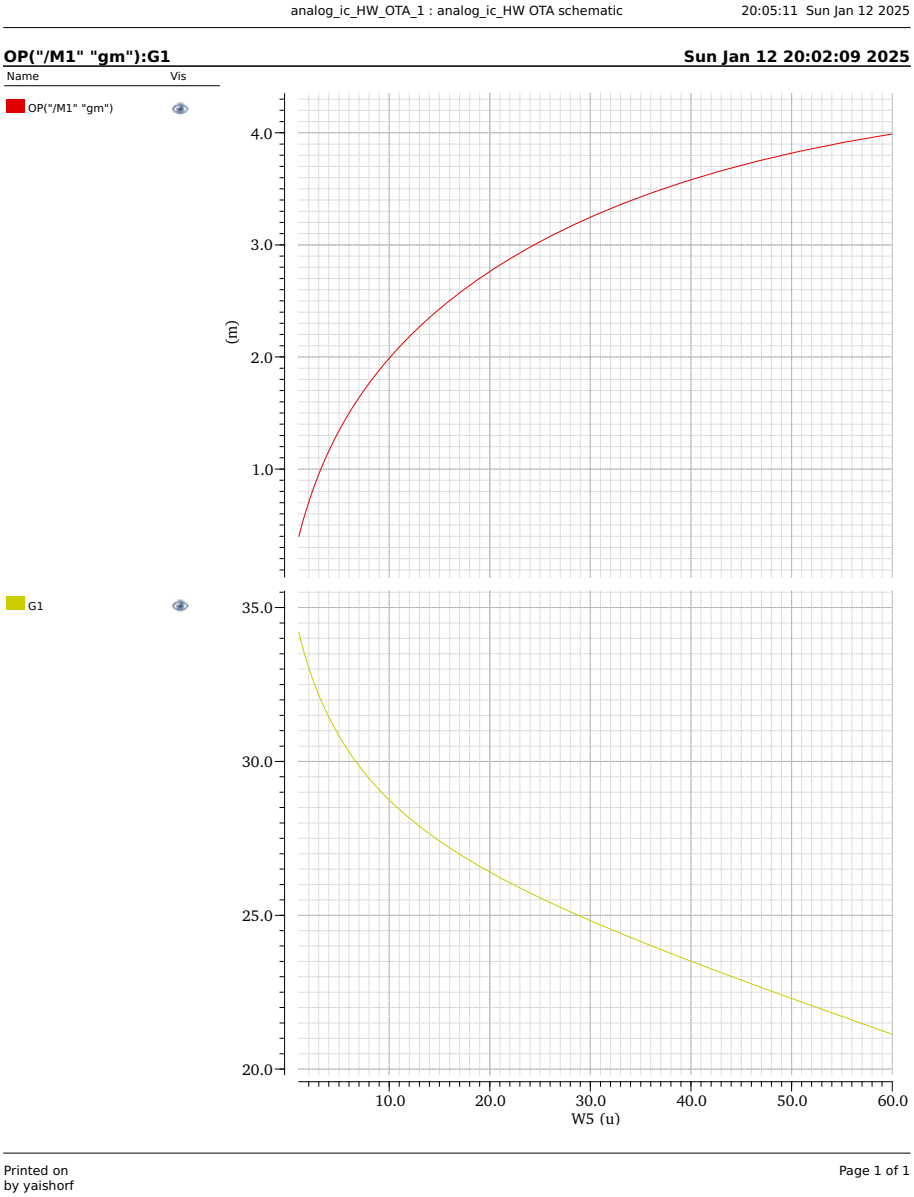


Figure 20: The impact of W_5 on g_{m1} and stage gain.

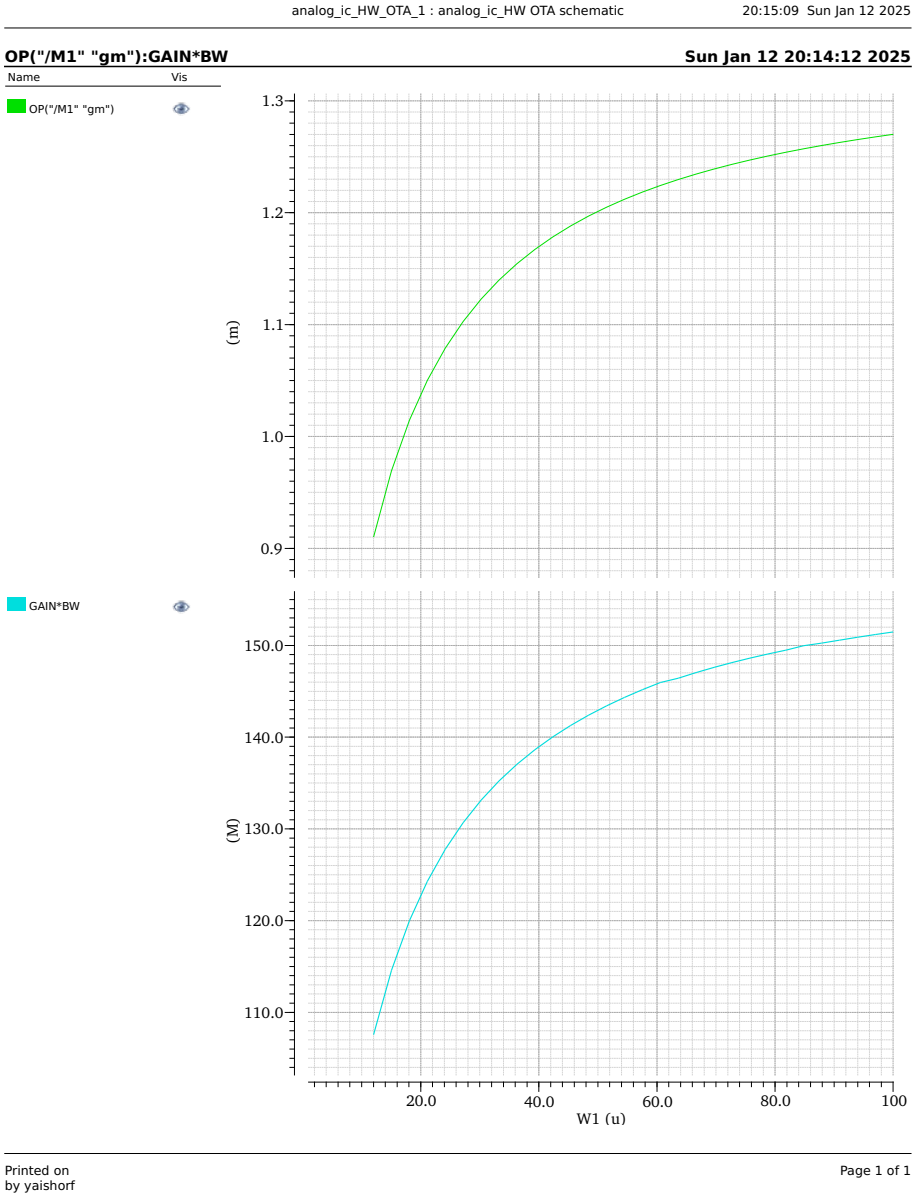


Figure 21: The relationship between g_{m1} and GBW as a function of W_1.

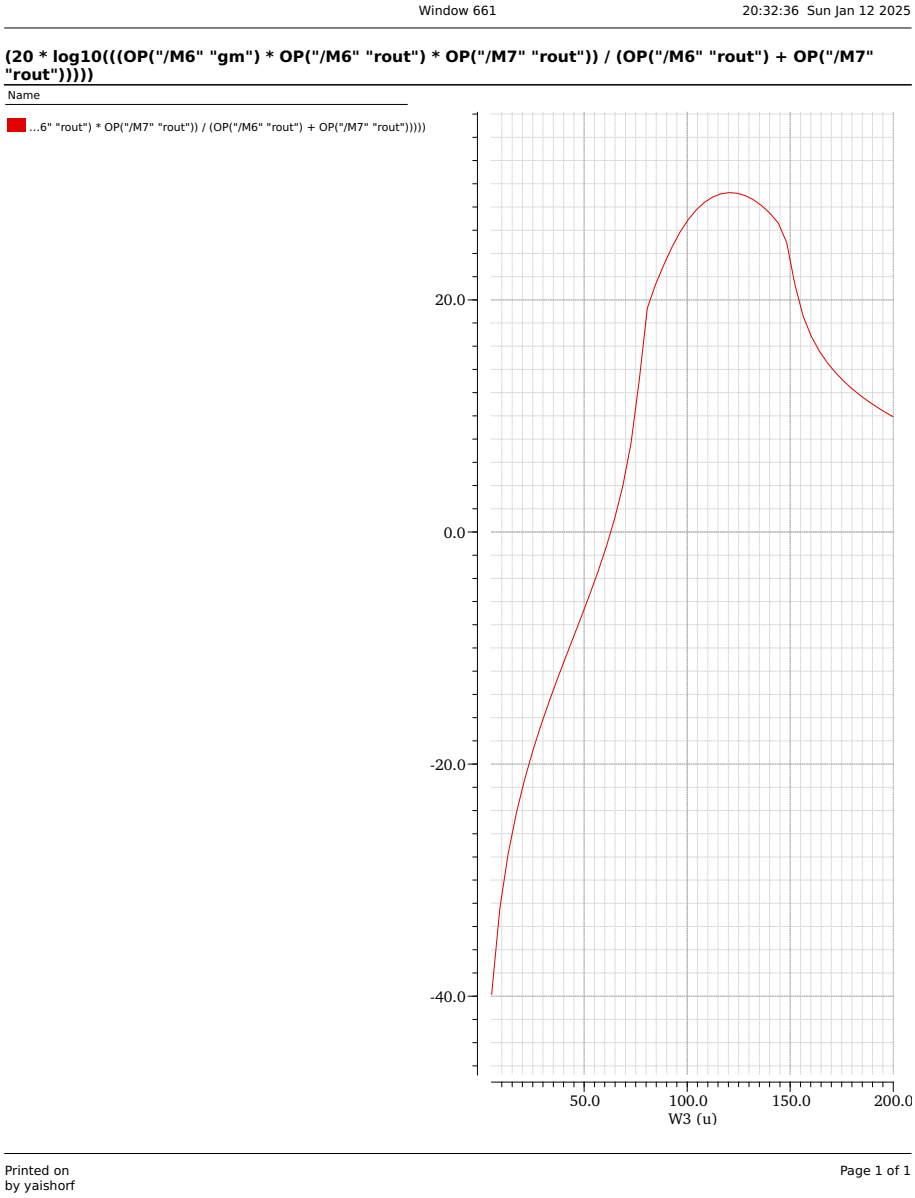


Figure 22: The gain of the second stage versus W_4.

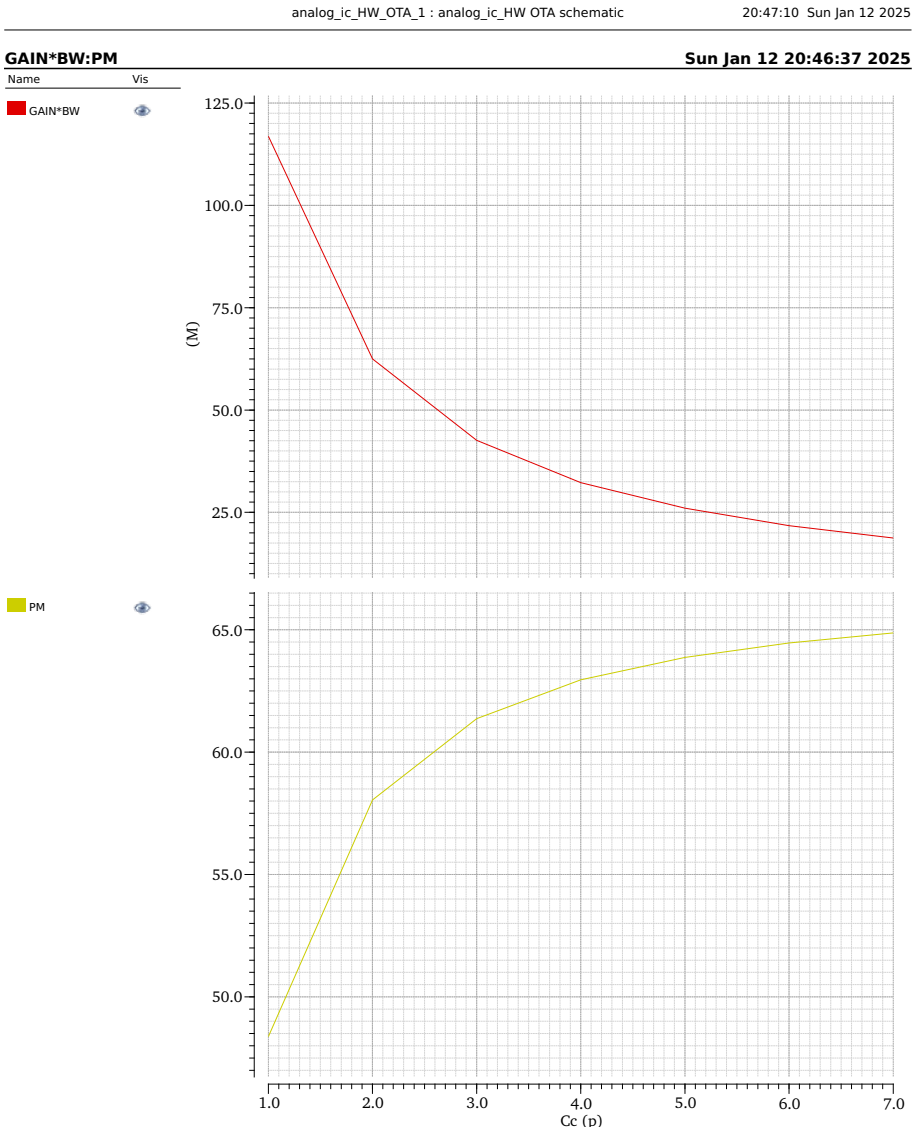


Figure 23: GBW and PM as functions of C_c.

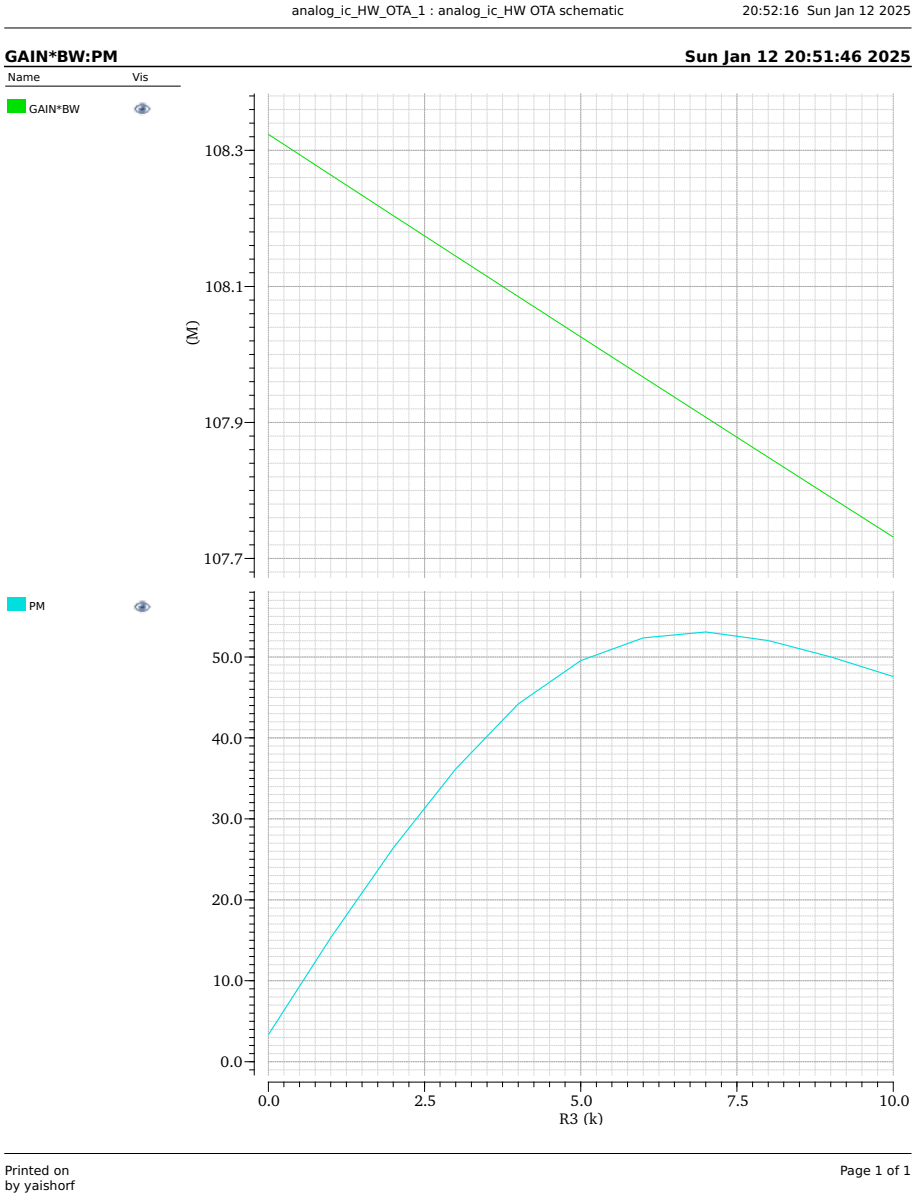


Figure 24: Effect of R_3 on GBW and PM.