# Final Project Report: 4-bit ALU Design

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**Abstract**

This report presents the design and implementation of a 4-bit Arithmetic Logic Unit (ALU) using Cadence Virtuoso and the gpdk045/gsclib045 technology. The ALU supports arithmetic operations, including addition and subtraction, and adheres to predefined area, timing, and voltage constraints.

## 1 Introduction

The objective of this project is to design and implement a **4-bit Arithmetic Logic Unit (ALU)** using **Cadence Virtuoso** and the **gpdk045/gsclib045** standard cell technology. The ALU performs arithmetic operations, including addition and subtraction, while adhering to predefined constraints such as **area limitations, timing requirements, and voltage levels**.

A key aspect of this project was the implementation of a **Knowles adder**, selected based on the project requirements. The Knowles adder was chosen due to its efficient parallel prefix structure, which balances speed and power consumption while maintaining reasonable layout complexity. The ALU design follows a structured approach where the addition result is stored in an internal register before subtraction is performed.

The design process was divided into two main phases:

1. **Planning Stage:**
   - Estimating the required standard cells.
   - Defining the floor plan.
   - Evaluating area constraints.
2. **Implementation Stage:**
   - Designing the **Knowles adder** and the subtractor.
   - Performing **detailed layout optimizations** in Virtuoso.
   - Validating correctness through **simulations, DRC, and LVS verification**.
   - Measuring **maximum clock frequency** under different voltage conditions.

The project was carried out in the **Virtuoso library** located at:

`/project/gpdk45/users/yaishorf/ws/final_project`

The following **cells contain the implementations**:

- **TB** – Testbench for functional validation.
- **KNOWLES_ADDER2** – Knowles adder implementation.
- **KNOWLES_SUBBER1** – Subtractor implementation.

By following these structured steps, we ensured compliance with the **maximum allowable area, rise/fall time constraints, and timing requirements** as outlined in the project guidelines.

# Note

After numerous manual measurements, it became apparent that manually verifying each requirement was neither practical nor reliable. Therefore, I developed comprehensive **SKILL scripts** to systematically verify all design requirements. These scripts can be found in:

- `/project/gpdk45/users/yaishorf/ws/final_project/scripts`

Their generated reports are available in:

- `/project/gpdk45/users/yaishorf/ws/final_project/reports/`

While space limitations prevent including all these detailed measurements in this report, I would be glad to elaborate on the verification methodology and results during the project examination.

# 2 Design Specifications

- **Inputs and Outputs**: A[3:0], B[3:0], C[3:0], Y[4:0].
- **Operations**:
  - Addition: $X = A + B$
  - Subtraction: $Y = X - C$
- **Encoding**: Two's complement representation.
- **Technology**: gpdk045/gsclib045.
- **Voltage Supply**: 1.2V.
- **Area Constraints**: Limited to 150% of total cell area.
- **Timing Constraints**: Rise/Fall time must not exceed 50ps.

# 3 Schematic Representations

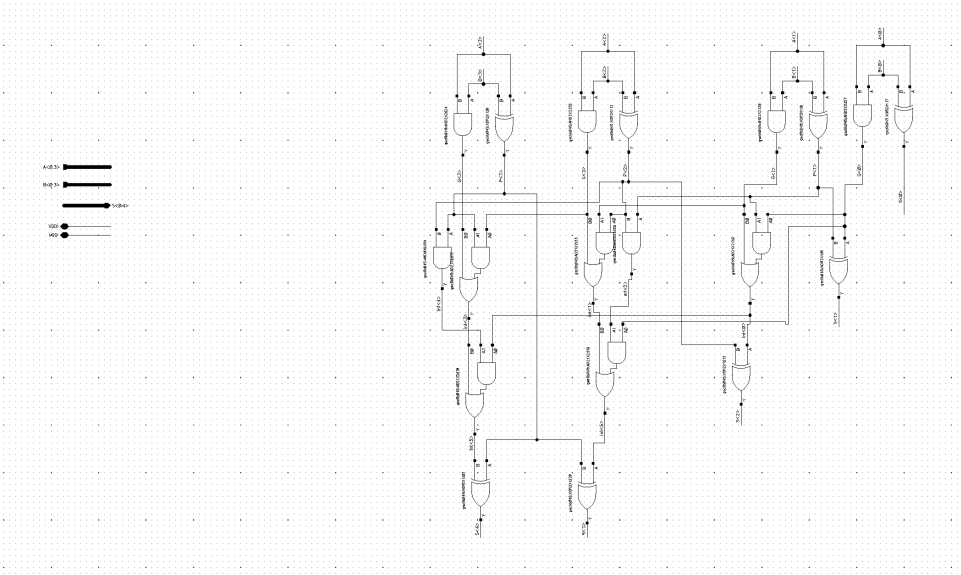

Figure 1: Schematic of the ADD operation.

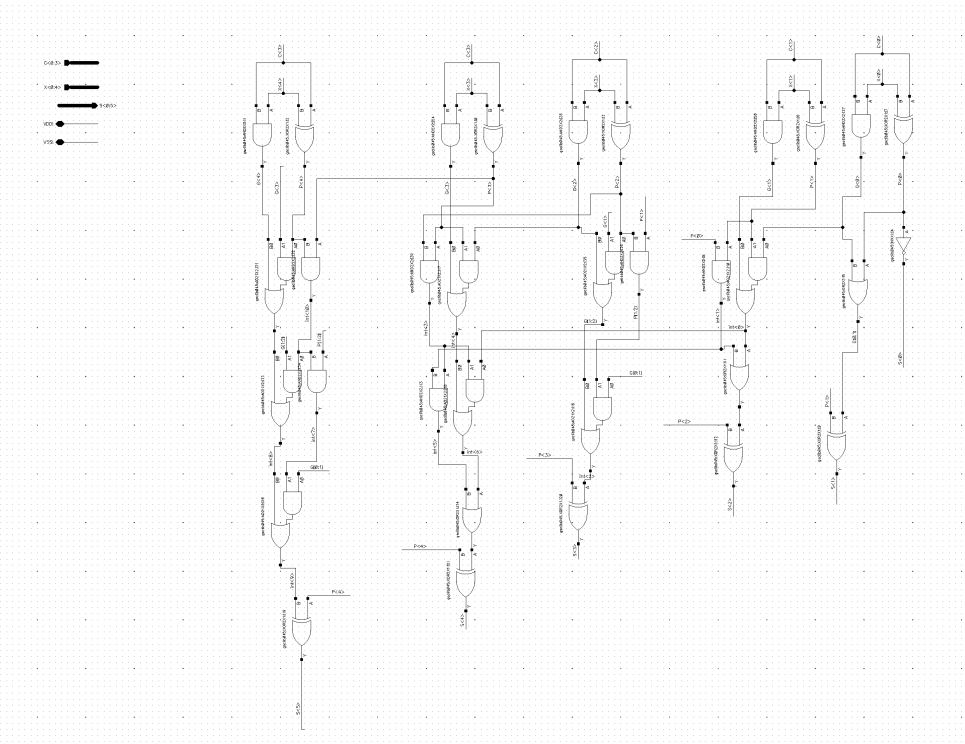

Figure 2: Schematic of the SUB operation.

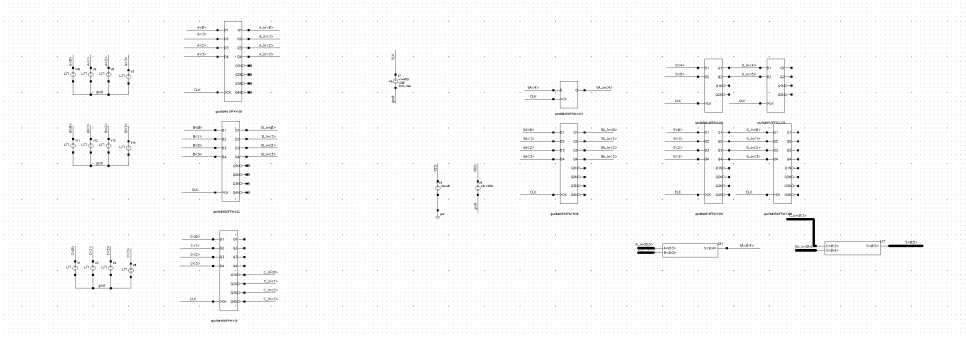

Figure 3: Testbench schematic for verification.

### 3.0.1 Library Cells Used in the Design

To design the circuit, we utilized standard cells from the **gsclib045** library. The following cells were used in different components:

- **Adder:**
  - 8 `XORX1`
  - 6 `ANDX2`
  - 5 `AOX1`
- **Subtractor:**
  - 10 `XORX1`
  - 8 `ANDX2`
  - 8 `AOX1`
  - 2 `ORX1`
  - 1 `INX1`
- **Testbench (Sequential Elements):**
  - 5 `DFF4`
  - 1 `DFF1`
  - 1 `DFF2`

The use of these cells was determined based on functional requirements, power efficiency, and area constraints. The selection of flip-flops in the testbench ensured proper clocking and sequential

# 4 Signal Notation

To avoid conflicts with library cells in the simulation, the following signal conventions were used:

- <signal_name>_in : Represents a flip-flop output.
- SA : Replaces X, the output of the adder.
- S : Replaces Y, the output of the subtractor.

# 5 Implementation of the Subtractor

The subtractor was implemented similarly to the adder, but with key modifications:

- It uses the NOT of input C to perform subtraction.
- Modifications were made to support a default condition of $Cin = 1$.
- The implementation relies on the fundamental identity: $-X = \sim X + 1$.

# 6 Build the Layout

In the final implementation, we deviated slightly from the original floor plan to reduce wire lengths. It is difficult to determine whether this was the optimal decision, as layout optimization always involves trade-offs. Manual cell placement proved to be more challenging than expected, even with a relatively small number of cells. Every improvement in one wire segment often resulted in an increased wire length in another part of the design.

Throughout the process, we aimed to maintain the following design principles:

- As much as possible, we kept **M2** routing vertical and **M3** routing horizontal. **M1** was barely used.
- Additional vias were inserted wherever feasible to reduce resistance.
- We tried to maintain direct wiring with minimal detours.

The following figures illustrate the final layout configuration:

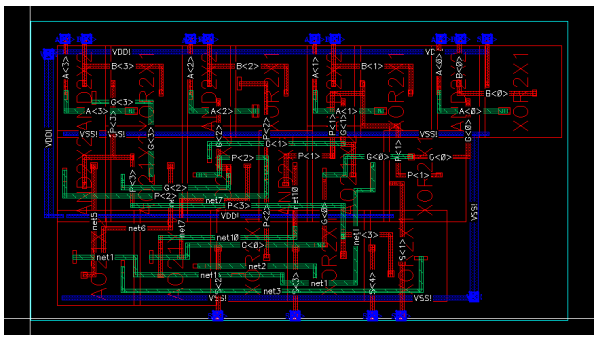

Figure 4: Final Layout (View 1)

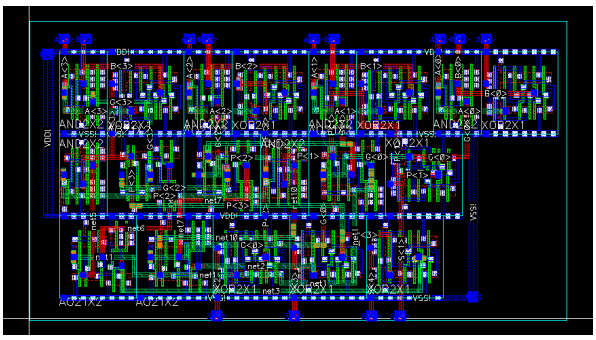

Figure 5: Final Layout (View 2)

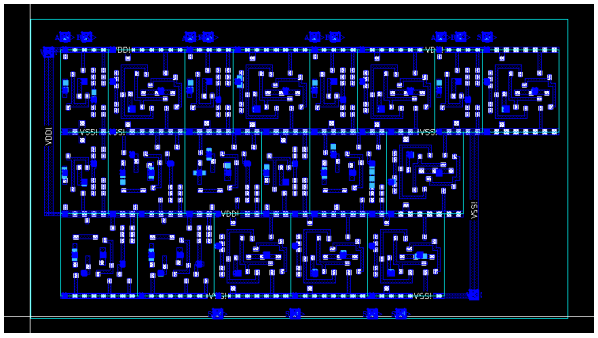

Figure 6: Layout Metal Layer 1 (M1)

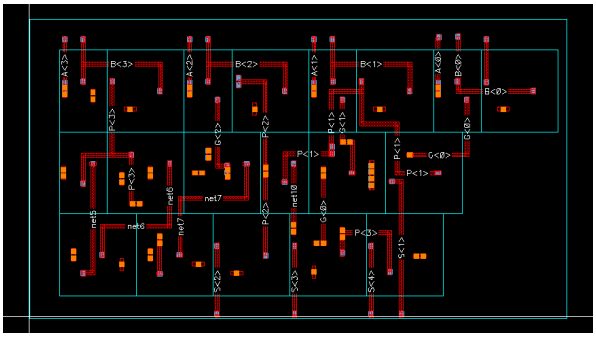

Figure 7: Layout Metal Layer 2 (M2)

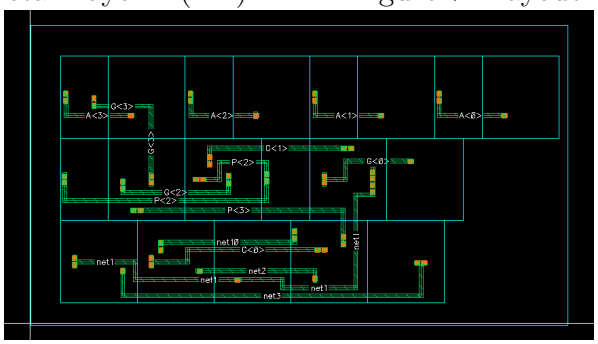

Figure 8: Layout Metal Layer 3 (M3)

## 6.1 Cell Area Requirement Validation

To validate compliance with the area constraint, we performed a detailed calculation of the total cell area.

From our previous analysis, the individual cell areas were computed as follows:

$$\text{XOR2X1 Area} = 1.9 \times 1.72 = 3.268\,\mu m^2$$

$$\text{AND2X2 Area} = 1.9 \times 1.12 = 2.128\,\mu m^2$$

$$\text{AO21X2 Area} = 1.99 \times 1.605 = 3.195\,\mu m^2$$

Given the number of instances used:

$$\text{Total XOR Area} = 8 \times 3.268 = 26.144\,\mu m^2$$

$$\text{Total AND Area} = 6 \times 2.128 = 12.768\,\mu m^2$$

$$\text{Total AOI Area} = 5 \times 3.195 = 15.975\,\mu m^2$$

**Summing all contributions:**

$$\text{Total Standard Cell Area} = 26.144 + 12.768 + 15.975 = 54.88\,\mu m^2$$

According to the design constraint, the layout must not exceed **150% of the standard cell area**:

$$\text{Max Allowed Area} = 1.5 \times 54.88 = 82.32\,\mu m^2$$

The final measured layout area was **56.29 $m^2$**, confirming that the design meets the area constraint.

Additionally, the average wire density was measured as **7%** of the total layout area, indicating minimal routing congestion.

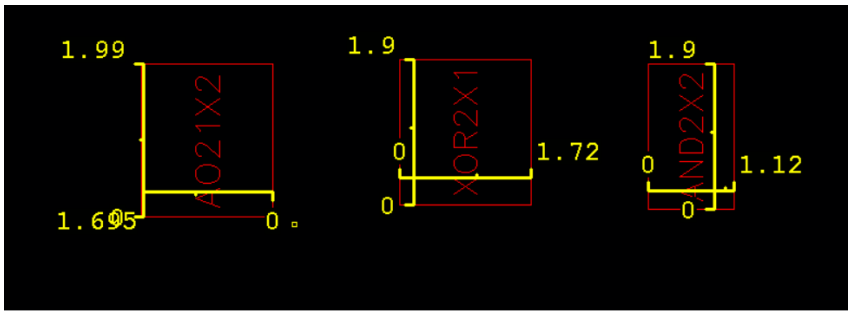


Figure 9: Cell Area Calculation

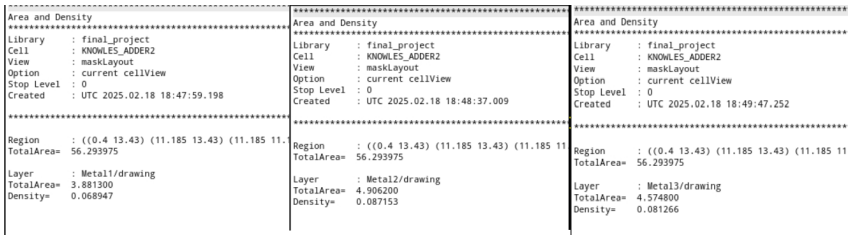


Figure 10: Final Total Layout Area

# 7 Verification Process

To ensure circuit correctness, the verification was conducted in the following stages:

- Initial asynchronous simulation using Logisim.
- Formal verification in the simulator.
- Manual verification using a custom script, which automated circuit validation and facilitated clock frequency testing.

Initially, I considered verifying all 4096 possible input combinations exhaustively. However, the simulator became unresponsive after approximately 100 cycles, making full verification impractical. To address this, I adopted a more feasible approach by generating random input values, ensuring a broad coverage of cases. This method, commonly used in verification processes, increased the likelihood of detecting corner cases while maintaining simulation efficiency.

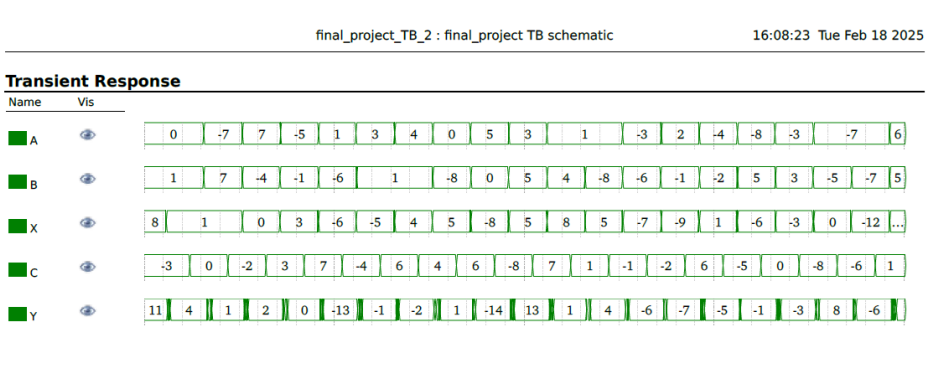


Figure 11: Waveform truth table from the simulation.

| Clock Cycle | A | B | X | X.Q | (A+B)_prev = X.Q | Status |
|---|---|---|---|---|---|---|
| 1 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 1 | 0 0 0 0 1 | 0 = 1 | SA_in Error |
| 2 | 1 0 0 1 | 0 1 1 1 | 0 0 0 0 0 | 0 0 0 0 1 | 1 = 1 | OK |
| 3 | 0 1 1 1 | 1 1 0 0 | 0 0 0 1 1 | 0 0 0 0 0 | 0 = 0 | OK |
| 4 | 1 0 1 1 | 1 1 1 1 | 1 1 0 1 0 | 0 0 0 1 1 | 3 = 3 | OK |
| 5 | 0 0 0 1 | 1 0 1 0 | 1 1 0 1 1 | 1 1 0 1 0 | -6 = -6 | OK |
| 6 | 0 0 1 1 | 0 0 0 1 | 0 0 1 0 0 | 1 1 0 1 1 | -5 = -5 | OK |
| 7 | 0 1 0 0 | 0 0 0 1 | 0 0 1 0 1 | 0 0 1 0 0 | 4 = 4 | OK |
| 8 | 0 0 0 0 | 1 0 0 0 | 1 1 0 0 0 | 0 0 1 0 1 | 5 = 5 | OK |
| 9 | 0 1 0 1 | 0 0 0 0 | 0 0 1 0 1 | 1 1 0 0 0 | -8 = -8 | OK |
| 10 | 0 0 1 1 | 0 1 0 1 | 0 1 0 0 0 | 0 0 1 0 1 | 5 = 5 | OK |
| 11 | 0 0 0 1 | 0 1 0 0 | 0 0 1 0 1 | 0 1 0 0 0 | 8 = 8 | OK |
| 12 | 0 0 0 1 | 1 0 0 0 | 1 1 0 0 1 | 0 0 1 0 1 | 5 = 5 | OK |
| 13 | 1 1 0 1 | 1 0 1 0 | 1 0 1 1 1 | 1 1 0 0 1 | -7 = -7 | OK |
| 14 | 0 0 1 0 | 1 1 1 1 | 0 0 0 0 1 | 1 0 1 1 1 | -9 = -9 | OK |
| 15 | 1 1 0 0 | 1 1 1 0 | 1 1 0 1 0 | 0 0 0 0 1 | 1 = 1 | OK |
| 16 | 1 0 0 0 | 0 1 0 1 | 1 1 1 0 1 | 1 1 0 1 0 | -6 = -6 | OK |
| 17 | 1 1 0 1 | 0 0 1 1 | 0 0 0 0 0 | 1 1 1 0 1 | -3 = -3 | OK |
| 18 | 1 0 0 1 | 1 0 1 1 | 1 0 1 0 0 | 0 0 0 0 0 | 0 = 0 | OK |
| 19 | 1 0 0 1 | 1 0 0 1 | 1 0 0 1 0 | 1 0 1 0 0 | -12 = -12 | OK |
| 20 | 0 1 1 0 | 0 1 0 1 | 0 1 0 1 1 | 1 0 0 1 0 | -14 = -14 | OK |

Figure 12: Truth table verification for addition.

| Clock Cycle | C | X | Y | Y.Q | (C-X)_prev = Y.Q | Status |
|---|---|---|---|---|---|---|
| 1 | 1 1 0 1 | 0 0 0 0 1 | 0 0 0 1 0 0 | 0 0 1 0 1 1 | 0 = 11 | S_in Error |
| 2 | 0 0 0 0 | 0 0 0 0 1 | 0 0 0 0 0 1 | 0 0 0 1 0 0 | 4 = 4 | OK |
| 3 | 1 1 1 0 | 0 0 0 0 0 | 0 0 0 0 1 0 | 0 0 0 0 0 1 | 1 = 1 | OK |
| 4 | 0 0 1 1 | 0 0 0 1 1 | 0 0 0 0 0 0 | 0 0 0 0 1 0 | 2 = 2 | OK |
| 5 | 0 1 1 1 | 1 1 0 1 0 | 1 1 0 0 1 1 | 0 0 0 0 0 0 | 0 = 0 | OK |
| 6 | 1 1 0 0 | 1 1 0 1 1 | 1 1 1 1 1 1 | 1 1 0 0 1 1 | -13 = -13 | OK |
| 7 | 0 1 1 0 | 0 0 1 0 0 | 1 1 1 1 1 0 | 1 1 1 1 1 1 | -1 = -1 | OK |
| 8 | 0 1 0 0 | 0 0 1 0 1 | 0 0 0 0 0 1 | 1 1 1 1 1 0 | -2 = -2 | OK |
| 9 | 0 1 1 0 | 1 1 0 0 0 | 1 1 0 0 1 0 | 0 0 0 0 0 1 | 1 = 1 | OK |
| 10 | 1 0 0 0 | 0 0 1 0 1 | 0 0 1 1 0 1 | 1 1 0 0 1 0 | -14 = -14 | OK |
| 11 | 0 1 1 1 | 0 1 0 0 0 | 0 0 0 0 0 1 | 0 0 1 1 0 1 | 13 = 13 | OK |
| 12 | 0 0 0 1 | 0 0 1 0 1 | 0 0 0 1 0 0 | 0 0 0 0 0 1 | 1 = 1 | OK |
| 13 | 1 1 1 1 | 1 1 0 0 1 | 1 1 1 0 1 0 | 0 0 0 1 0 0 | 4 = 4 | OK |
| 14 | 1 1 1 0 | 1 0 1 1 1 | 1 1 1 0 0 1 | 1 1 1 0 1 0 | -6 = -6 | OK |
| 15 | 0 1 1 0 | 0 0 0 0 1 | 1 1 1 0 1 1 | 1 1 1 0 0 1 | -7 = -7 | OK |
| 16 | 1 0 1 1 | 1 1 0 1 0 | 1 1 1 1 1 1 | 1 1 1 0 1 1 | -5 = -5 | OK |
| 17 | 0 0 0 0 | 1 1 1 0 1 | 1 1 1 1 0 1 | 1 1 1 1 1 1 | -1 = -1 | OK |
| 18 | 1 0 0 0 | 0 0 0 0 0 | 0 0 1 0 0 0 | 1 1 1 1 0 1 | -3 = -3 | OK |
| 19 | 1 0 1 0 | 1 0 1 0 0 | 1 1 1 0 1 0 | 0 0 1 0 0 0 | 8 = 8 | OK |
| 20 | 0 0 0 1 | 1 0 0 1 0 | 1 1 0 0 0 1 | 1 1 1 0 1 0 | -6 = -6 | OK |

Figure 13: Truth table verification for subtraction.

## 7.1 Design Rule Check (DRC) and Layout Versus Schematic (LVS) Validation

To ensure the correctness of the final layout, we successfully performed both **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** verification. The DRC confirmed that all layout rules were followed, ensuring manufacturability, while the LVS verified that the netlist extracted from the layout matched the intended schematic.

Additionally, the extraction process was completed successfully, allowing for post-layout simulations to validate circuit performance.

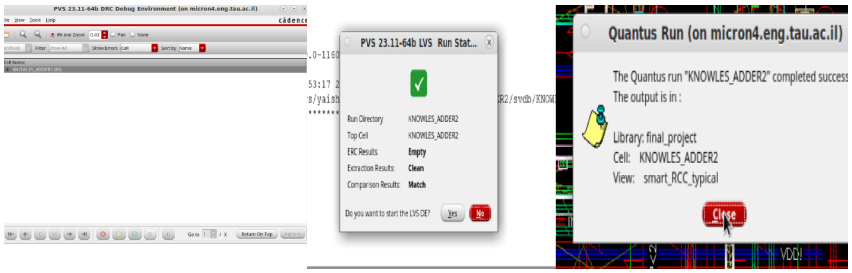


Figure 14: Proof of successful DRC, LVS, and extraction completion

# 8 Maximum Clock Frequency

## 8.1 FF Timing Analysis

To estimate the maximum clock frequency accurately, it was necessary to analyze the parameters of the FFs from the standard library. Unfortunately, there were no FFs with more than 4-bit width, leading to the following structure:

- X was stored using a 4-bit FF and an additional single-bit FF.
- Y was stored using a 4-bit FF and an additional 2-bit FF.

Each component was simulated under different voltage levels to obtain reliable reference values, acknowledging that these values are non-deterministic and may vary due to multiple factors. For simplicity, it was assumed that the delay is similar across all FF outputs. Below are the extracted timing values:

| $t_{FF}$ (ps) | 4-bit | 2-bit | 1-bit |
|---|---|---|---|
| Setup (1.2V/0.9V) | 13/32 | 15/36 | 21/44 |
| Hold (ps) | Around 8 | | |
| $t_{CQ}$ (ps) (1.2V/0.9V) | 62.2/123 | 52/104 | 45/90 |

Table 1: FF Timing Characteristics with ALU as Load

Key observations:

- The simulations per component were crucial for accurate estimation.
- The drastic effect of VDD on device speed is evident.
- The clock-to-q ($t_{CQ}$) values are significantly high and not negligible, contrary to initial expectations.

## 8.2 Simulation Results

To further analyze the timing characteristics, the following waveform comparisons were generated:

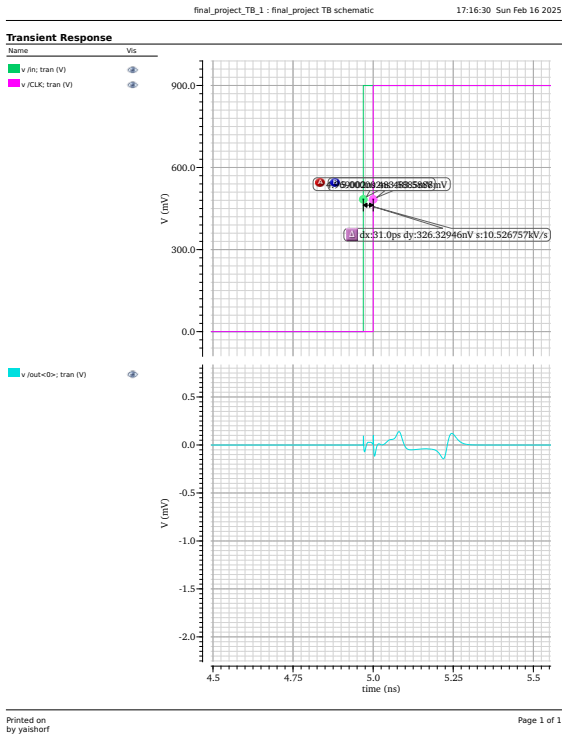


Figure 15: Setup time at 0.9V - 31ps.

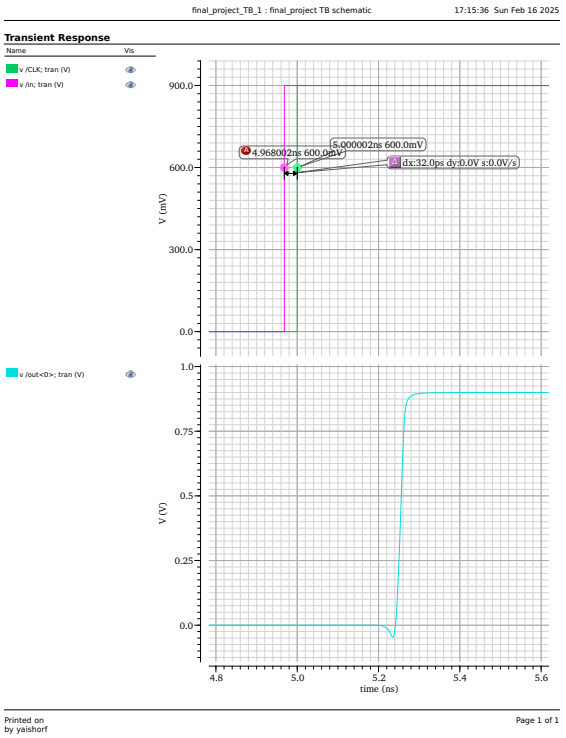


Figure 16: Setup time at 0.9V - 32ps.

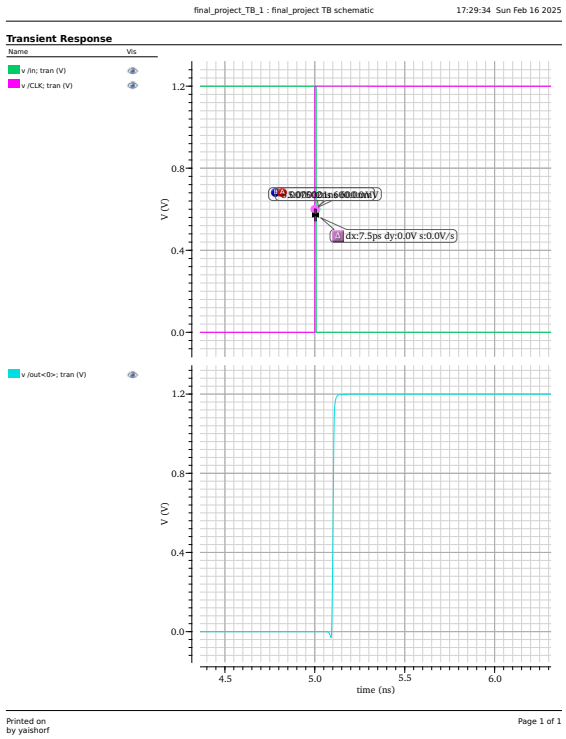


Figure 17: Hold time at 1.2V - 7.5ps.

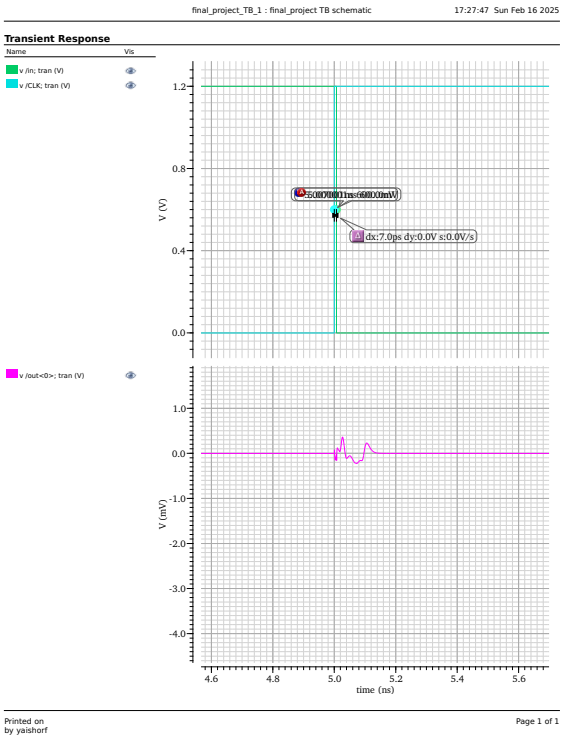


Figure 18: Hold time at 1.2V - 7ps.

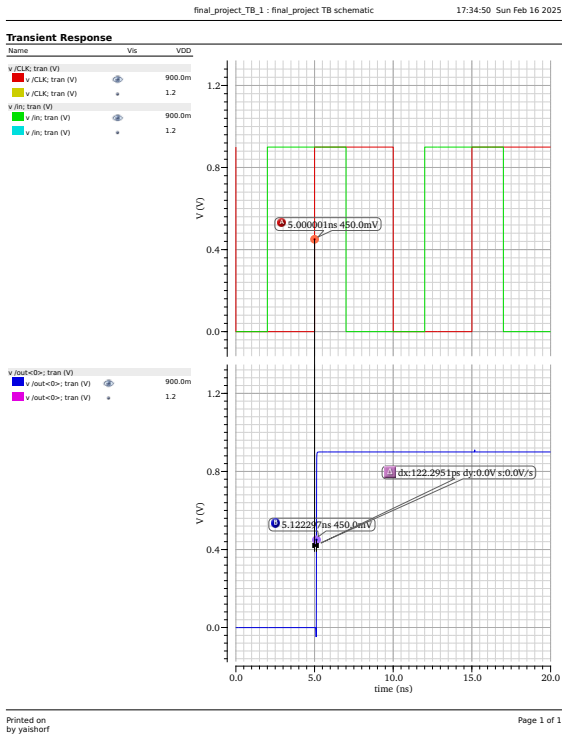


Figure 19: Clock-to-Q delay at 0.9V - 122.3ps.

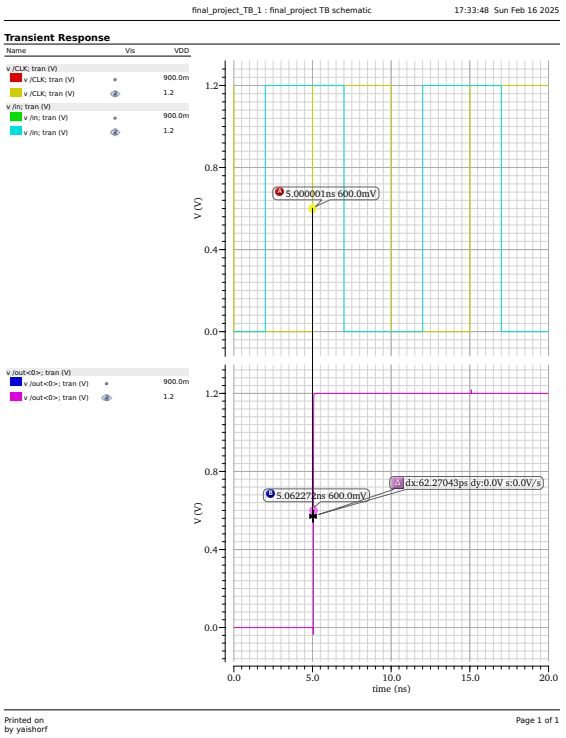


Figure 20: Clock-to-Q delay at 1.2V - 62.2ps.

## 8.3 Finding the Critical Path

To meet the setup and hold constraints, it was necessary to identify the critical path in both the adder and subtractor. This involved determining the minimum and maximum logical paths among all REG-to-REG paths in the different components.

Additionally, timing values for both the adder and subtractor were extracted at two supply voltages, both before and after layout extraction. Due to the complexity of analyzing these paths manually, a custom script was developed using the SKILL programming language to automate the extraction of delays for all paths.

To ensure accuracy, FALSE PATH constraints were applied to exclude logically irrelevant connections. Specifically, input bits beyond a certain index do not impact lower-index output bits (e.g., $A[3]$ does not influence $X[0]$), and such paths were omitted from the analysis. The following tables summarize the analysis conducted for all different scenarios:

Table 2: Delays for the ADDER

| Start Point | End Point | Before Extraction (0.9V/1.2V) | After Extraction (0.9V/1.2V |
|---|---|---|---|
| A_in<0> | SA<0> | 87.0/43.0 | 157.8/75.4 |
| A_in<0> | SA<1> | 122.3/58.9 | 254.2/121.5 |
| B_in<0> | SA<1> | 138.3/67.6 | 281.2/130.9 |
| A_in<1> | SA<1> | 167.9/84.3 | 279.2/138.0 |
| B_in<1> | SA<1> | 121.3/57.5 | 253.1/125.9 |
| A_in<0> | SA<2> | 133.2/63.6 | 259.2/126.1 |
| B_in<1> | SA<2> | 131.2/62.2 | 254.8/123.4 |
| B_in<2> | SA<2> | 131.2/62.2 | 254.1/123.0 |
| A_in<0> | SA<3> | 140.2/66.9 | 271.8/132.2 |
| B_in<1> | SA<3> | 147.3/70.5 | 292.8/140.3 |
| B_in<2> | SA<3> | 138.2/65.5 | 266.7/129.1 |
| A_in<3> | SA<3> | 156.0/75.6 | 303.2/146.3 |
| A_in<0> | SA<4> | 152.3/73.0 | 297.4/145.0 |
| B_in<0> | SA<4> | 191.6/90.4 | 382.6/181.4 |
| B_in<1> | SA<4> | 157.3/76.4 | 325.7/156.7 |
| A_in<2> | SA<4> | 218.1/101.6 | 465.3/219.2 |
| B_in<2> | SA<4> | 150.3/71.6 | 292.3/141.9 |
| A_in<3> | SA<4> | 169.8/82.5 | 334.3/162.0 |
| B_in<0> | SA<2> | -/- | 406.4/197.4 |
| A_in<1> | SA<2> | -/- | 384.8/183.0 |
| A_in<2> | SA<2> | -/- | 332.7/160.5 |
| B_in<0> | SA<3> | -/- | 268.9/128.6 |

Table 3: Delays for the SUBSTRACTOR

| Start Point | End Point | 0.9V (pS) | 1.2V (pS) |
|---|---|---|---|
| C_in<0> | S<0> | 110.5 | - |
| SA_in<0> | S<0> | 82.8 | 39.3 |
| C_in<0> | S<1> | 125.7 | - |
| SA_in<0> | S<1> | 162.2 | 80.1 |
| C_in<1> | S<1> | 145.7 | - |
| C_in<0> | S<2> | 151.9 | - |
| C_in<2> | S<2> | 145.9 | - |
| SA_in<0> | S<2> | - | 114.2 |
| C_in<0> | S<3> | 145.3 | - |
| C_in<2> | S<3> | 145.2 | - |
| C_in<3> | S<3> | 141.7 | - |
| SA_in<0> | S<3> | - | 73.8 |
| SA_in<3> | S<3> | - | 57.8 |
| C_in<0> | S<4> | 146.1 | 70.4 |
| C_in<2> | S<4> | 146.0 | 70.4 |
| C_in<3> | S<4> | 142.5 | 68.0 |
| C_in<0> | S<5> | 158.2 | 76.5 |
| C_in<2> | S<5> | 158.2 | 76.5 |
| C_in<3> | S<5> | 154.6 | 74.1 |

Table 4: Maximum and Minimum Delays Summary

| Component | Condition | Voltage | Min Delay (pS) | Max Delay (pS) | Min Path | Max Path |
|---|---|---|---|---|---|---|
| ADDER | Before EX | 0.9V | 87.0 | 336.9 | A_in<0> → SA<0> | B_in<0> → SA<4> |
| | | 1.2V | 43.0 | 150.8 | A_in<0> → SA<0> | B_in<0> → SA<4> |
| | After EX | 0.9V | 157.8 | 598.8 | A_in<0> → SA<0> | B_in<0> → SA<4> |
| | | 1.2V | 75.4 | 279.4 | A_in<0> → SA<0> | B_in<0> → SA<4> |
| SUBSTRACTOR | - | 0.9V | 82.8 | 162.2 | SA_in<0> → S<0> | SA_in<0> → S<1> |
| | | 1.2V | 39.3 | 114.2 | SA_in<0> → S<0> | SA_in<0> → S<2> |

1. **Extraction Impact:**
   - The delays after extraction are approximately doubled compared to before extraction in the ADDER
   - The critical path (B_in<0> → SA<4>) remains consistent before and after extraction
2. **Voltage Impact:**
   - At 1.2V, delays are consistently shorter than at 0.9V by approximately 50%
   - This voltage effect is observed in both ADDER and SUBSTRACTOR
3. **Component Analysis:**
   - ADDER delays after extraction are significantly larger due to the extraction process
   - SUBSTRACTOR delays cannot be directly compared with ADDER as it hasn't undergone extraction
   - A fair comparison would require extraction data for both components
4. **Critical Paths:**
   - ADDER maintains the same critical paths (both min and max) across all conditions
   - SUBSTRACTOR shows different maximum critical paths at different voltages, while maintaining the same minimum critical path
5. **Expected vs. Actual Results:**
   - Most paths behaved as expected, with longer paths showing maximum delays and shorter paths showing minimum delays
   - However, some paths exhibited higher delays than anticipated based on their path length
   - This suggests that factors beyond path length, such as load capacitance and gate complexity, significantly influence the delay

### 8.3.1 Critical Path Delay Verification

To further validate the critical path delays, timing analysis was conducted using waveform diagrams. The analysis includes both the **minimum delay path** and the **maximum delay path** for both the adder and subtractor circuits. The verification was performed at two supply voltages (1.2V and 0.9V) before and after extraction.

The following figures illustrate the measured signal delays:

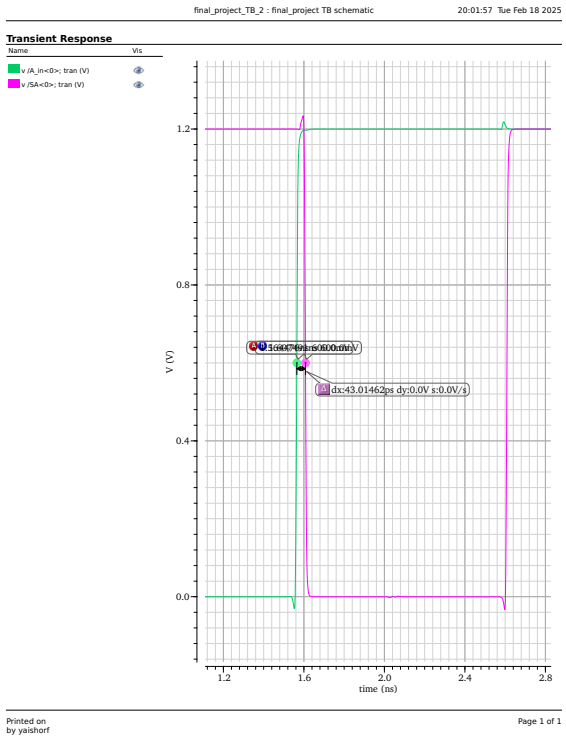


Figure 21: Minimum delay path - Adder @ 1.2V

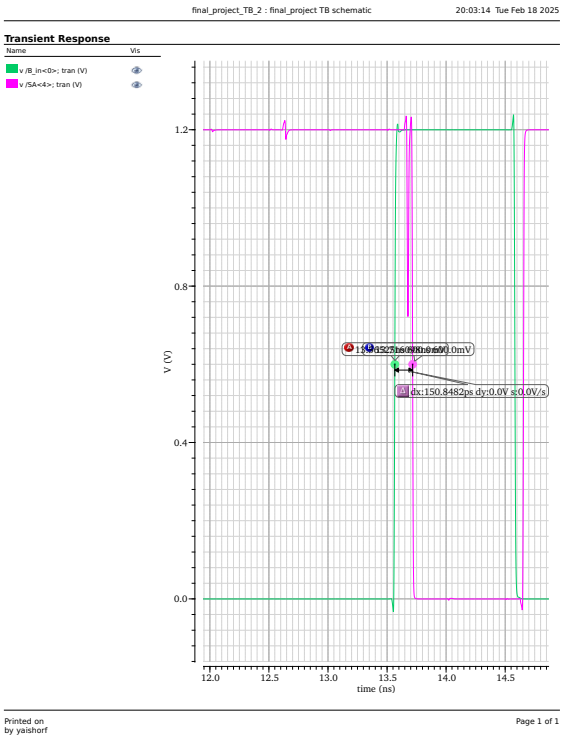


Figure 22: Maximum delay path - Adder @ 1.2V

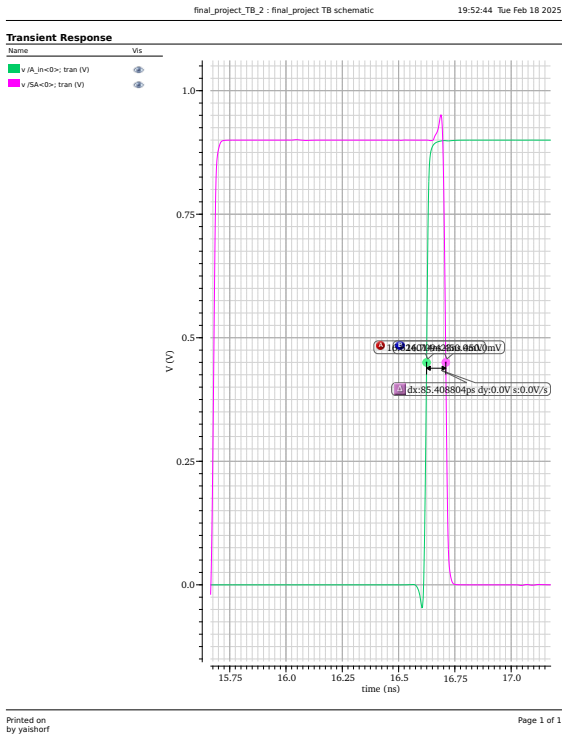


Figure 23: Minimum delay path - Adder @ 0.9V

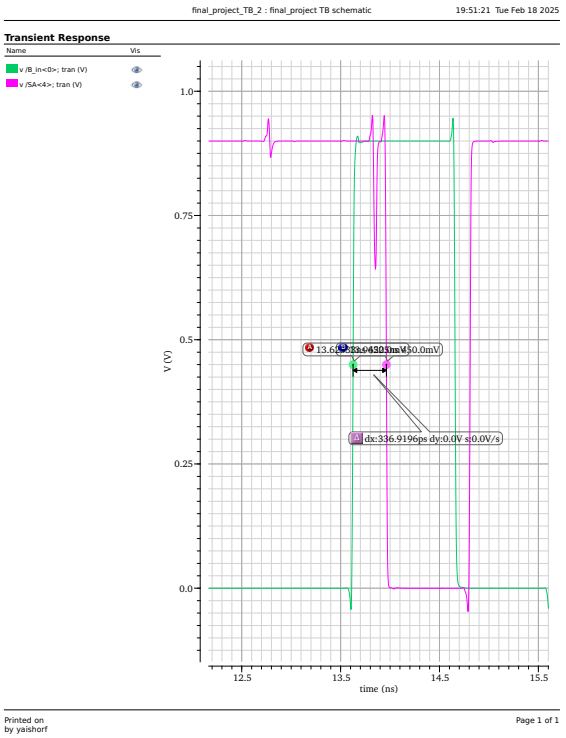


Figure 24: Maximum delay path - Adder @ 0.9V

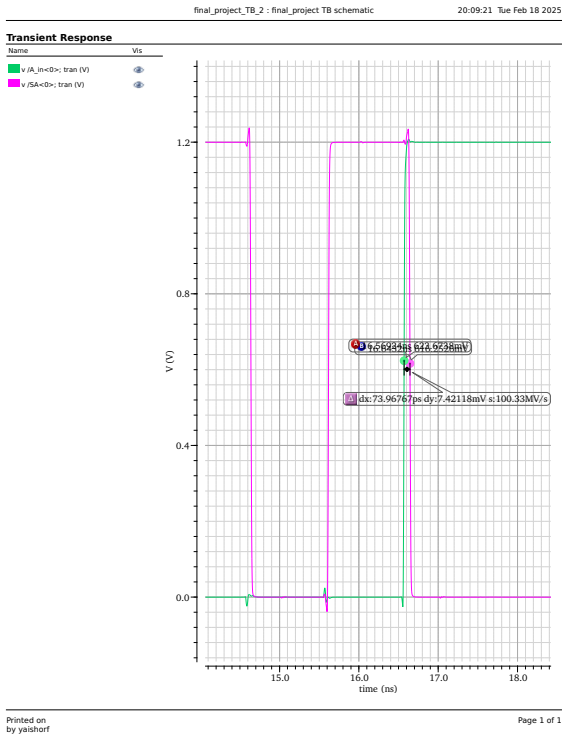


Figure 25: Minimum delay path - Adder @ 1.2V (After Extraction)

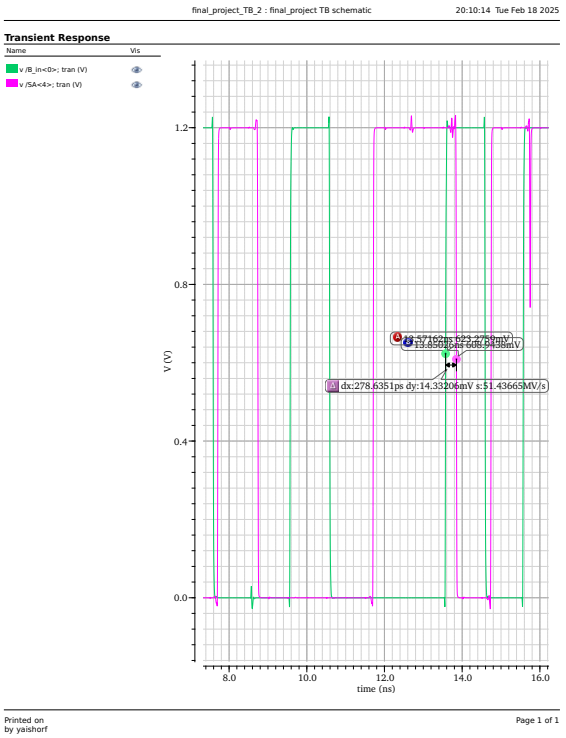


Figure 26: Maximum delay path - Adder @ 1.2V (After Extraction)

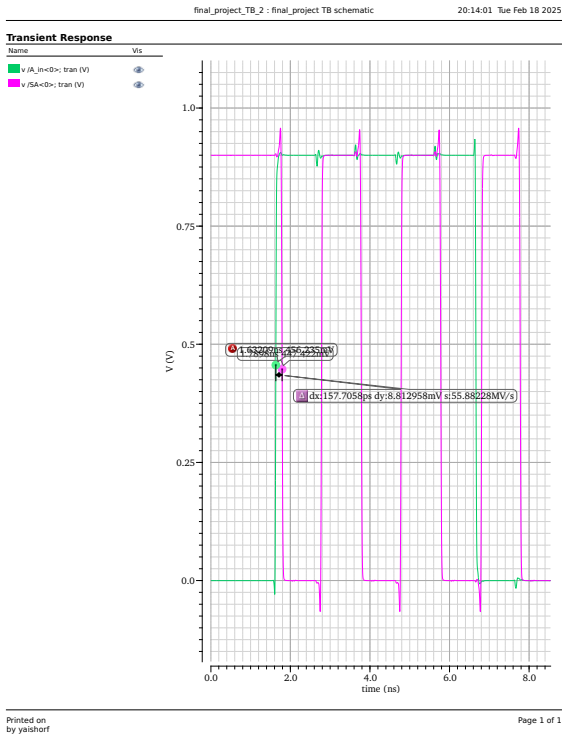


Figure 27: Minimum delay path - Adder @ 0.9V (After Extraction)

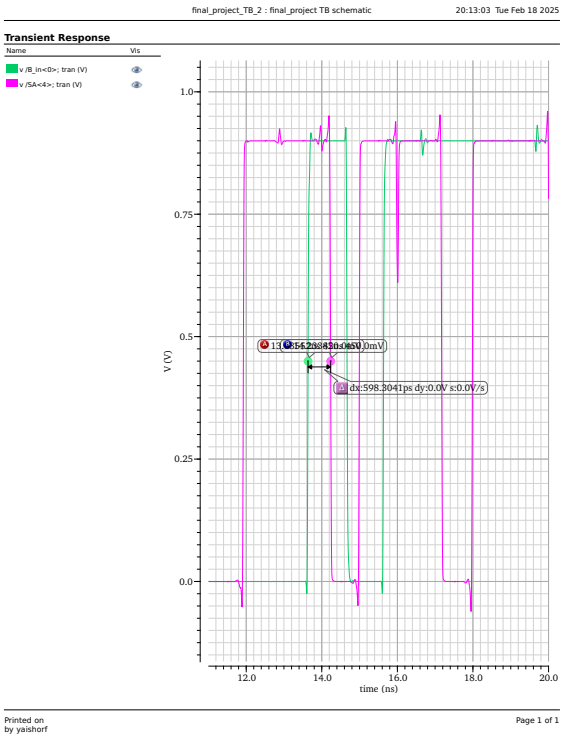


Figure 28: Maximum delay path - Adder @ 0.9V (After Extraction)

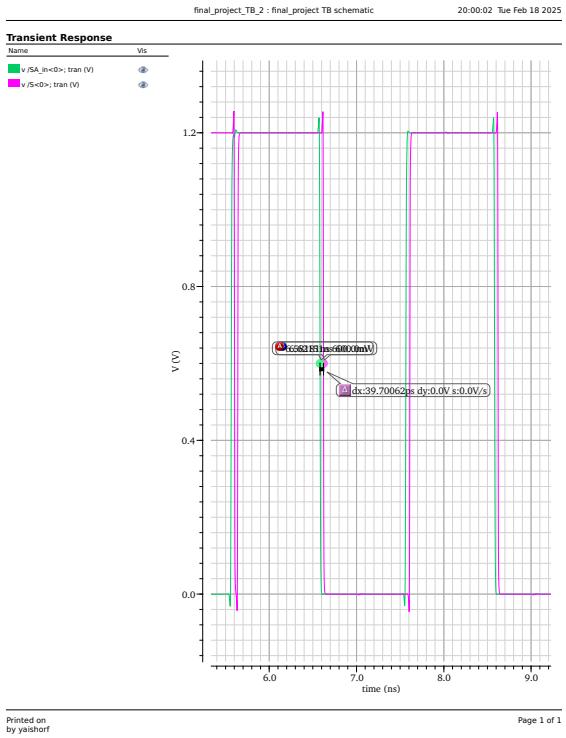


Figure 29: Minimum delay path - Subtractor @ 1.2V

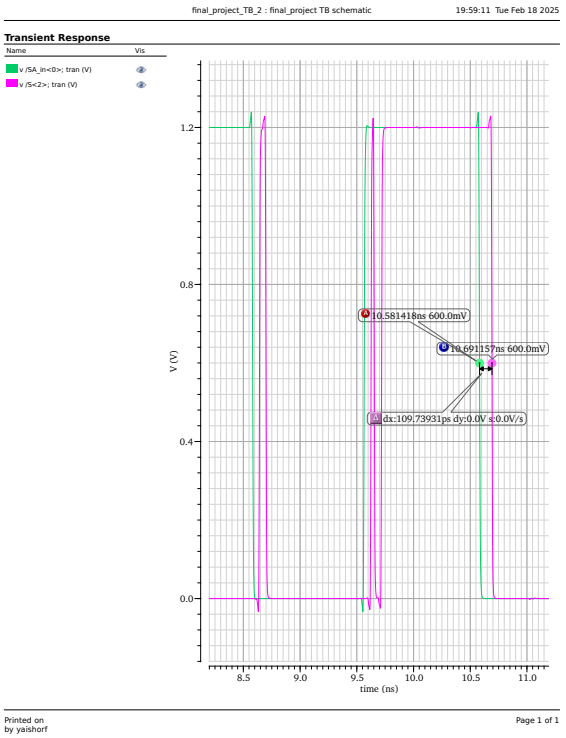


Figure 30: Maximum delay path - Subtractor @ 1.2V

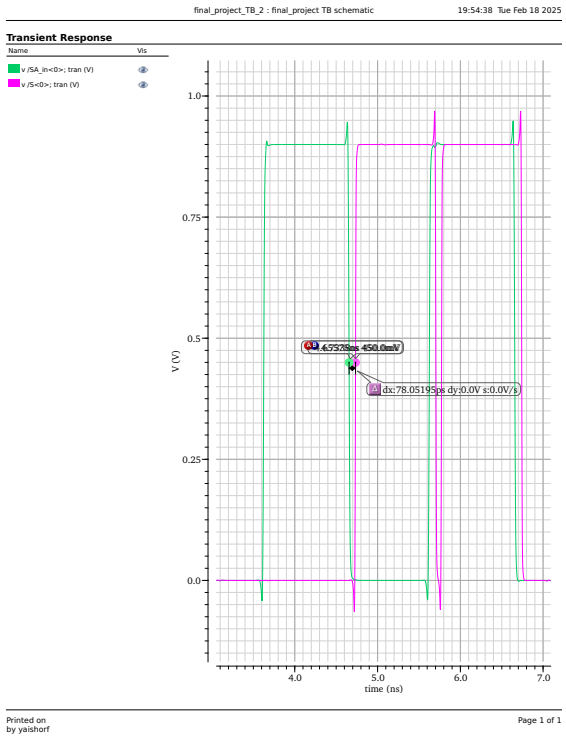


Figure 31: Minimum delay path - Subtractor @ 0.9V

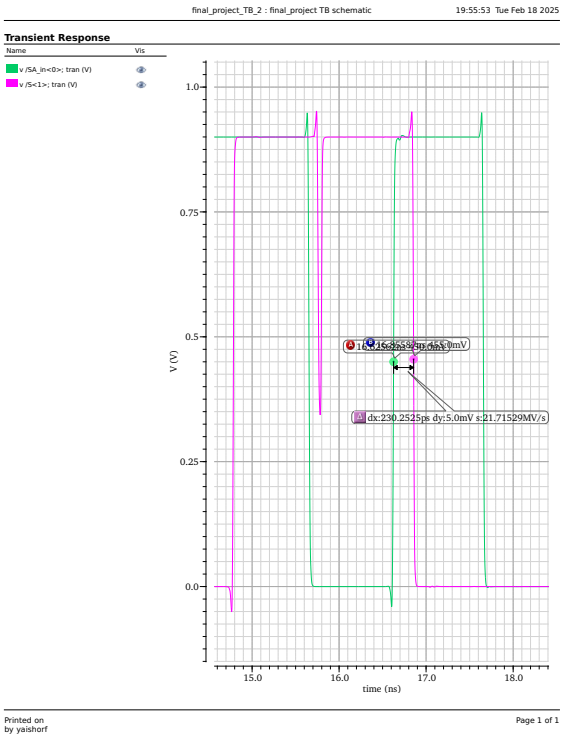


Figure 32: Maximum delay path - Subtractor @ 0.9V

The results indicate that the extracted circuits exhibit higher delays compared to pre-extraction results due to parasitic effects. The subtractor generally maintains slightly lower delays compared to the adder, which aligns with expectations based on the logical structure.

To further illustrate the critical path analysis, the minimum and maximum delay paths are highlighted in the circuit diagrams. The shortest path is marked in **green**, while the longest (critical) path is marked in **red**.

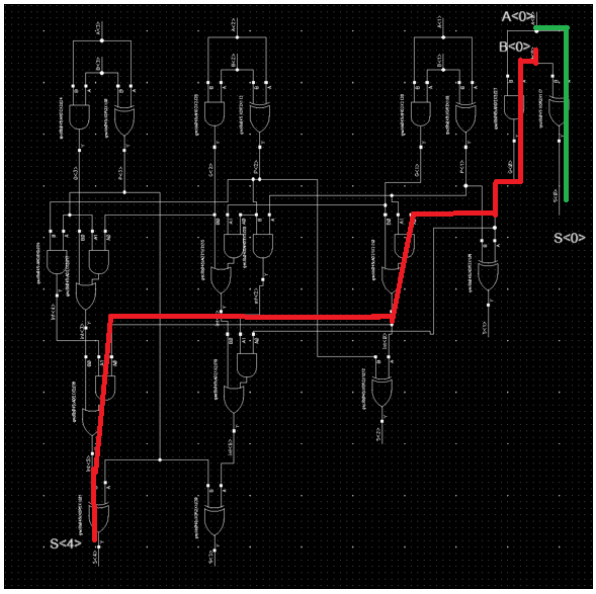


Figure 33: Critical path in the adder.

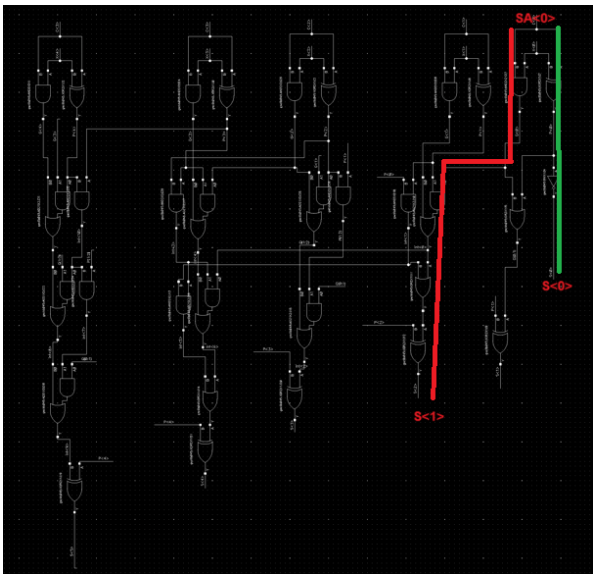


Figure 34: Critical path in the subtractor.

## 8.4 Estimation of Maximum Operating Frequency Based on Hold & Setup Constraints

To determine the maximum allowable clock frequency, we analyzed the setup and hold constraints across the different register-to-register paths. The relevant flip-flop delays were obtained for each scenario before and after extraction (EX) and at two operating voltages (0.9V and 1.2V).

The **FF4** represents the input register to the adder, while **FF4 & FF1** correspond to the output of the adder and input to the subtractor, and **FF4 & FF2** correspond to the subtractor's output.

The following constraints were considered:

- **Setup constraint**: The clock period $T_{clock}$ must be greater than the longest REG-to-REG delay:
$$T_{clock} \geq T_{setup} + T_{CQ} + T_{logic\_max}$$
- **Hold constraint**: The hold condition must be satisfied:
$$T_{hold} \geq T_{CQ} + T_{logic\_min}$$
Since $T_{hold}$ is significantly smaller than the required values, no hold-time violations were observed.

The estimated maximum frequency is given by:

$$f_{max} = \frac{1}{T_{clock}}$$

where $T_{clock}$ is derived from the most restrictive delay values across both the adder and subtractor.

**Calculation:**

For each scenario, we compute the worst-case clock period:
**Adder Analysis:**
**Before Extraction (1.2V)**:

$$T_{clock} = T_{setup} + T_{CQ} + T_{logic\_max}$$

$$T_{clock} = 13ps + 62.2ps + 150.8ps = 226ps$$

$$f_{max} = \frac{1}{226ps} = 4.42GHz$$

**After Extraction (1.2V)**:

$$T_{clock} = 13ps + 62.2ps + 279.4ps = 354.6ps$$

$$f_{max} = \frac{1}{354.6ps} = 2.82GHz$$

**Before Extraction (0.9V)**:

$$T_{clock} = 32ps + 123ps + 336.9ps = 491.9ps$$

$$f_{max} = \frac{1}{491.9ps} = 2.03GHz$$

**After Extraction (0.9V)**:

$$T_{clock} = 32ps + 123ps + 598.8ps = 753.8ps$$

$$f_{max} = \frac{1}{753.8ps} = 1.33GHz$$

**Subtractor Analysis:**
**Before Extraction (1.2V)**:

$$T_{clock} = 15ps + 52ps + 114.2ps = 181.2ps$$

$$f_{max} = \frac{1}{181.2ps} = 5.52GHz$$

**After Extraction (1.2V)**:

$$T_{clock} = 15ps + 52ps + 279.4ps = 346.4ps$$

$$f_{max} = \frac{1}{346.4ps} = 2.89GHz$$

**Before Extraction (0.9V)**:

$$T_{clock} = 36ps + 104ps + 162.2ps = 302.2ps$$

$$f_{max} = \frac{1}{302.2ps} = 3.31GHz$$

**After Extraction (0.9V)**:

$$T_{clock} = 36ps + 104ps + 598.8ps = 738.8ps$$

$$f_{max} = \frac{1}{738.8ps} = 1.35GHz$$

**Final Operating Frequency Selection:**

The final maximum frequency must be the lowest common frequency that satisfies both the adder and subtractor constraints.

| Condition | Voltage | Final $f_{max}$ (GHz) |
|---|---|---|
| Before EX | 1.2V | 4.42 |
| After EX | 1.2V | 2.82 |
| Before EX | 0.9V | 2.97 |
| After EX | 0.9V | 1.35 |

Table 5: Final maximum operating frequency selection

## 8.5 Verification of Maximum Operating Frequency

To ensure the circuit's correctness at the estimated maximum operating frequency, two key aspects were examined:

- **Logical correctness**: Verifying that after two clock cycles from the input application, the expected output is correctly produced.
- **Transition time validation**: Ensuring that the transition times (rise and fall) remain within acceptable limits.

To efficiently verify transition times across all signals in both the adder and subtractor, a custom script was used to measure rise and fall times. The following is a characteristic output from the script:

```
Transition Time Analysis Report
==============================
Clock Period (t_CLK): 0.45 nS
Supply Voltage (VDD): 1.2 V

Signal                          Rise Time (ps)    Fall Time (ps)    Status
-------------------------------------------------------------------------
/A_in<0>                        19.4              19.4              OK
/A_in<1>                        21.6              21.6              OK
/A_in<2>                        19.9              19.9              OK
/A_in<3>                        19.4              19.4              OK
/B_in<0>                        27.9              27.9              OK
/B_in<1>                        27.6              27.6              OK
/B_in<2>                        28.0              28.0              OK
/B_in<3>                        29.9              29.9              OK
/C_in<0>                        9.6               9.6               OK
/C_in<1>                        9.7               9.7               OK
/C_in<2>                        9.3               9.3               OK
/C_in<3>                        12.8              12.8              OK
/SA<0>                          19.4              19.4              OK
/SA<1>                          21.7              21.7              OK
/SA<2>                          21.8              21.8              OK
/SA<3>                          20.9              20.9              OK
/SA<4>                          20.1              20.1              OK
/S<0>                           8.6               8.6               OK
/S<1>                           10.8              10.8              OK
/S<2>                           11.2              11.2              OK
/S<3>                           10.8              10.8              OK
/S<4>                           11.3              11.3              OK
/S<5>                           11.2              11.2              OK
/SA_in<0>                       14.2              14.2              OK
/SA_in<1>                       14.5              14.5              OK
/SA_in<2>                       14.4              14.4              OK
/SA_in<3>                       13.9              13.9              OK
/SA_in<4>                       12.9              12.9              OK
/S_in<0>                        9.9               9.9               OK
/S_in<1>                        9.9               9.9               OK
/S_in<2>                        9.9               9.9               OK
/S_in<3>                        9.9               9.9               OK
/S_in<4>                        10.0              10.0              OK
/S_in<5>                        10.0              10.0              OK
/I17/P<0>                       18.1              18.1              OK
/I17/P<1>                       18.7              18.7              OK
/I17/P<2>                       18.8              18.8              OK
/I17/P<3>                       19.4              19.4              OK
/I17/P<4>                       20.0              20.0              OK
/I17/G<0>                       12.7              12.7              OK
/I17/G<1>                       12.4              12.4              OK
/I17/G<2>                       12.9              12.9              OK
/I17/G<3>                       12.5              12.5              OK
```

Figure 35: Measured transition times at 1.2V after extraction.

As expected, the actual operating frequency was slightly lower than the initially estimated values.

| Voltage | Estimated Period (ps) | Verified Period (ps) | Max Transition Time (ps) |
|---|---|---|---|
| 1.2V (Before EX) | 226 | 300 | 14.2 |
| 0.9V (Before EX) | 491.9 | 600 | 32.0 |
| 1.2V (After EX) | 354.6 | 450 | 30.0 |
| 0.9V (After EX) | 753.8 | 800 | 46.9 |

Table 6: Comparison of Estimated vs. Verified Maximum Operating Frequency

The results confirm that the transition times increase with lower supply voltages and after extraction due to additional parasitics. Despite the small deviation from the expected values, the circuit remains within acceptable operating limits.

# 9 Conclusions

This project successfully demonstrated the design and implementation of a **4-bit ALU** using **gpdk045/gsclib045** technology. The final implementation met all the original design requirements: the circuit area remained within the allowed limits (**56.29** $\mu m^2$ compared to the **82.32** $\mu m^2$ constraint), rise and fall times were kept below **50ps**, and the circuit operated correctly under both required supply voltages (**0.9V and 1.2V**).

The use of the **Knowles adder** enabled an efficient balance between speed and power consumption, achieving a maximum operating frequency of **2.82GHz** at **1.2V** and **1.35GHz** at **0.9V** after the extraction process. The most significant challenge was the **layout design**, which required careful optimization of component placement and wiring paths to meet area constraints while maintaining optimal performance.

For future improvements, further optimizations in cell placement and wiring design could be explored to reduce delays and improve circuit density.

# 10 References


- Weste, Neil, and David Harris. "CMOS VLSI Design: A Circuits and Systems Perspective." 4th ed. Addison-Wesley, 2010.