LDO for a Digital High Frequency Clock Source Chip

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Pursuing the Unknown

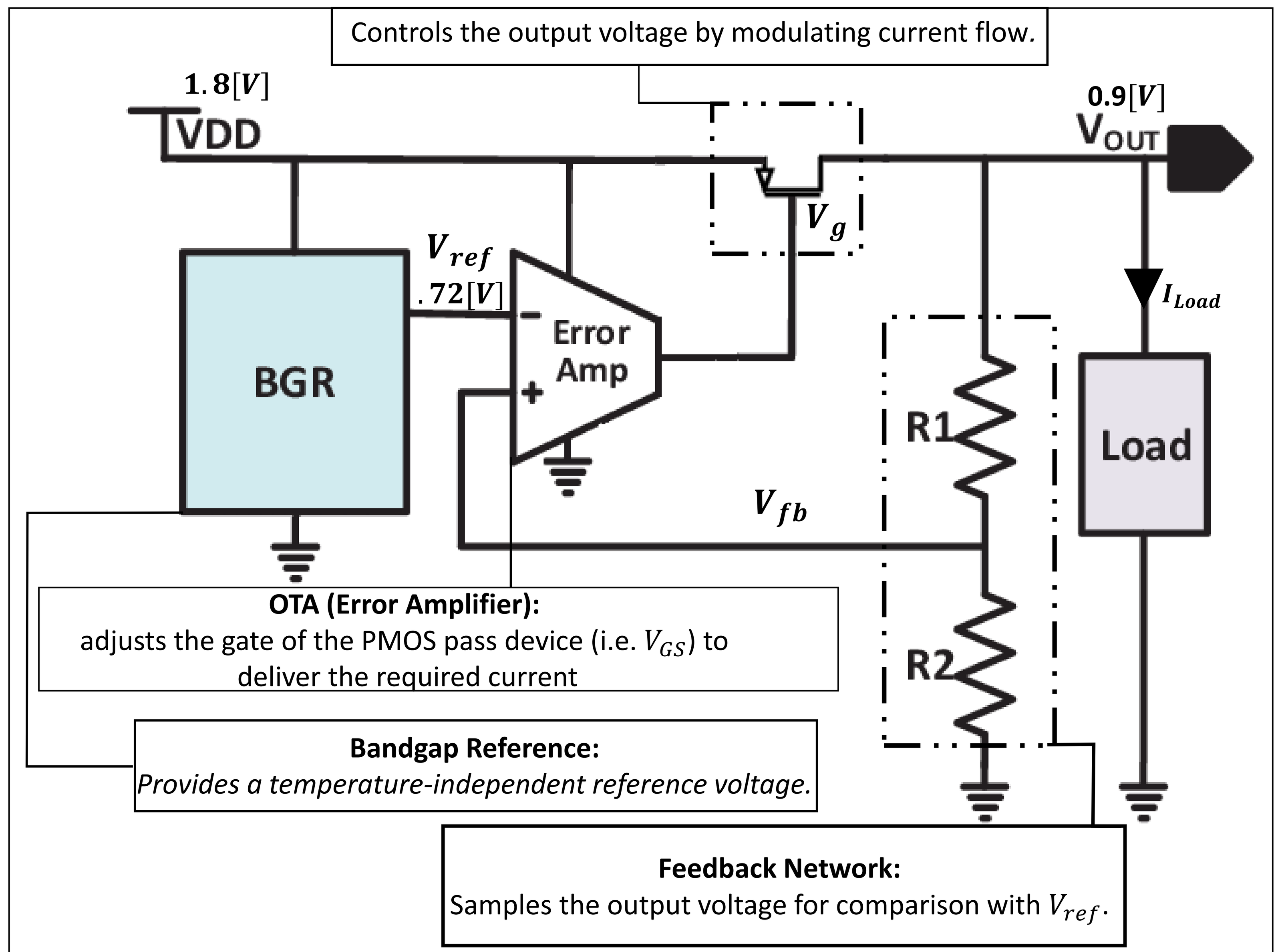
DPLL 2025/26

Motivation & Objective

To ensure low phase noise and precise timing, the DPLL needs a stable, low-noise supply. Our LDO is designed to provide a consistent output across supply and temperature variations, tailored specifically for DPLL requirements.

Operating Principle

Internal architecture of the LDO:



$V_{fb} > V_{ref}$: $V_g \uparrow \implies V_{sg} \downarrow \implies I_{SD} \downarrow \implies V_{fb} \downarrow$

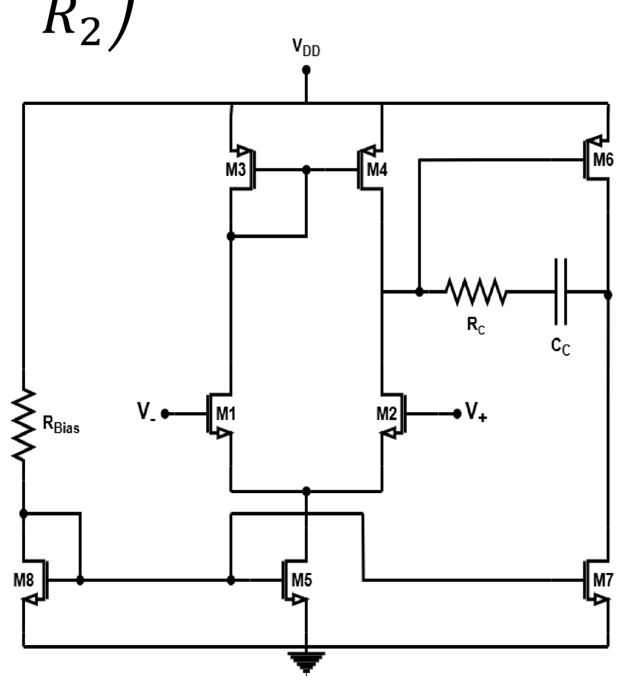
$V_{fb} < V_{ref}$: $V_g \downarrow \implies V_{sg} \uparrow \implies I_{SD} \uparrow \implies V_{fb} \uparrow$

The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

Miller OTA as an Error Amplifier:

In BGR, forces $V_A = V_B$ to generate a temperature-independent current.
In LDO, used as a current regulator that stabilizes V_{out}.
High gain ($\sim 80dB$) improves accuracy and regulation.



The Bandgap Reference

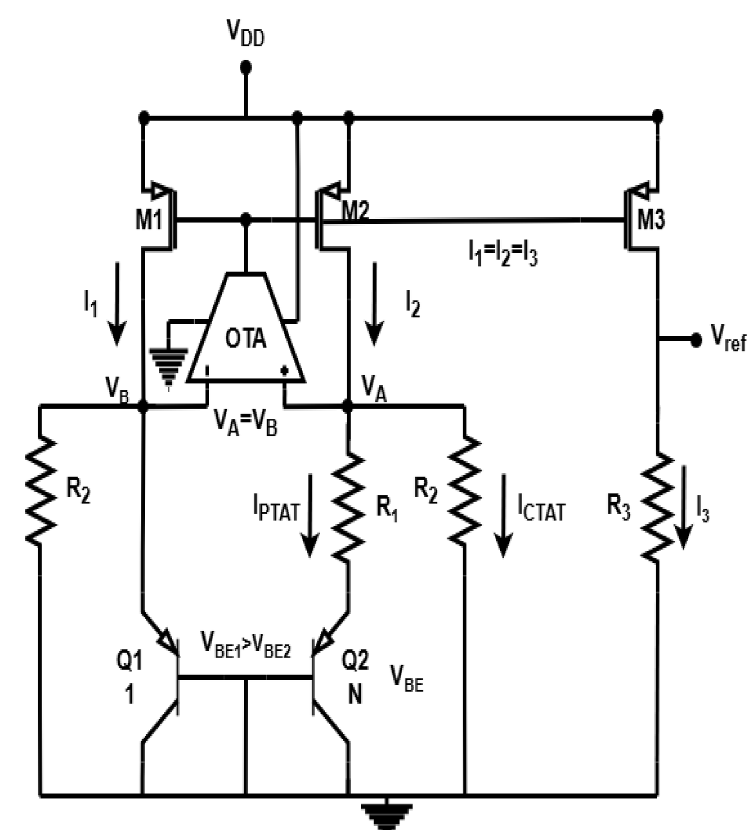
The bandgap reference generates a precise, temperature-independent voltage.

$$V_{BE1} = V_{PTAT}$$

$$V_A = \frac{kT}{q} ln\left(\frac{I}{N \times I_s}\right) + IR_1 = \frac{k\boldsymbol{T}}{q} ln\left(\frac{I}{I_s}\right) = Vzv_B$$

$$I = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{k\boldsymbol{T}}{qR_1}\ln(N) \rightarrow PTAT\ current$$

$$V_{ref} = R_3(I_{PTAT} + I_{CTAT}) = R_3\left(\frac{\ln(N)V_T}{R_1} + \frac{V_A}{R_2}\right) \rightarrow \frac{\partial V_{ref}}{\partial T} = 0$$



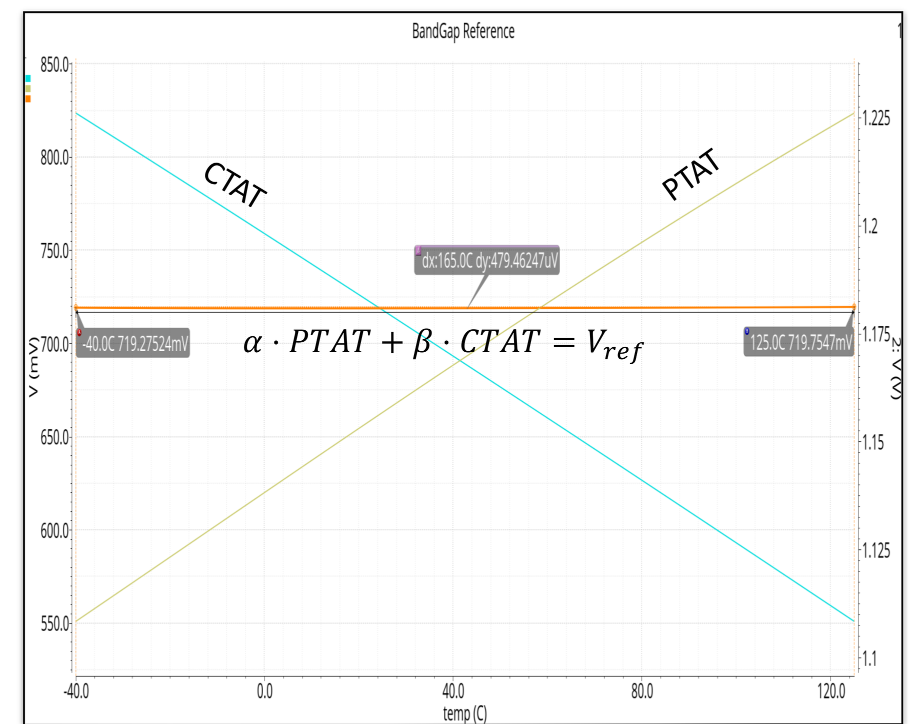


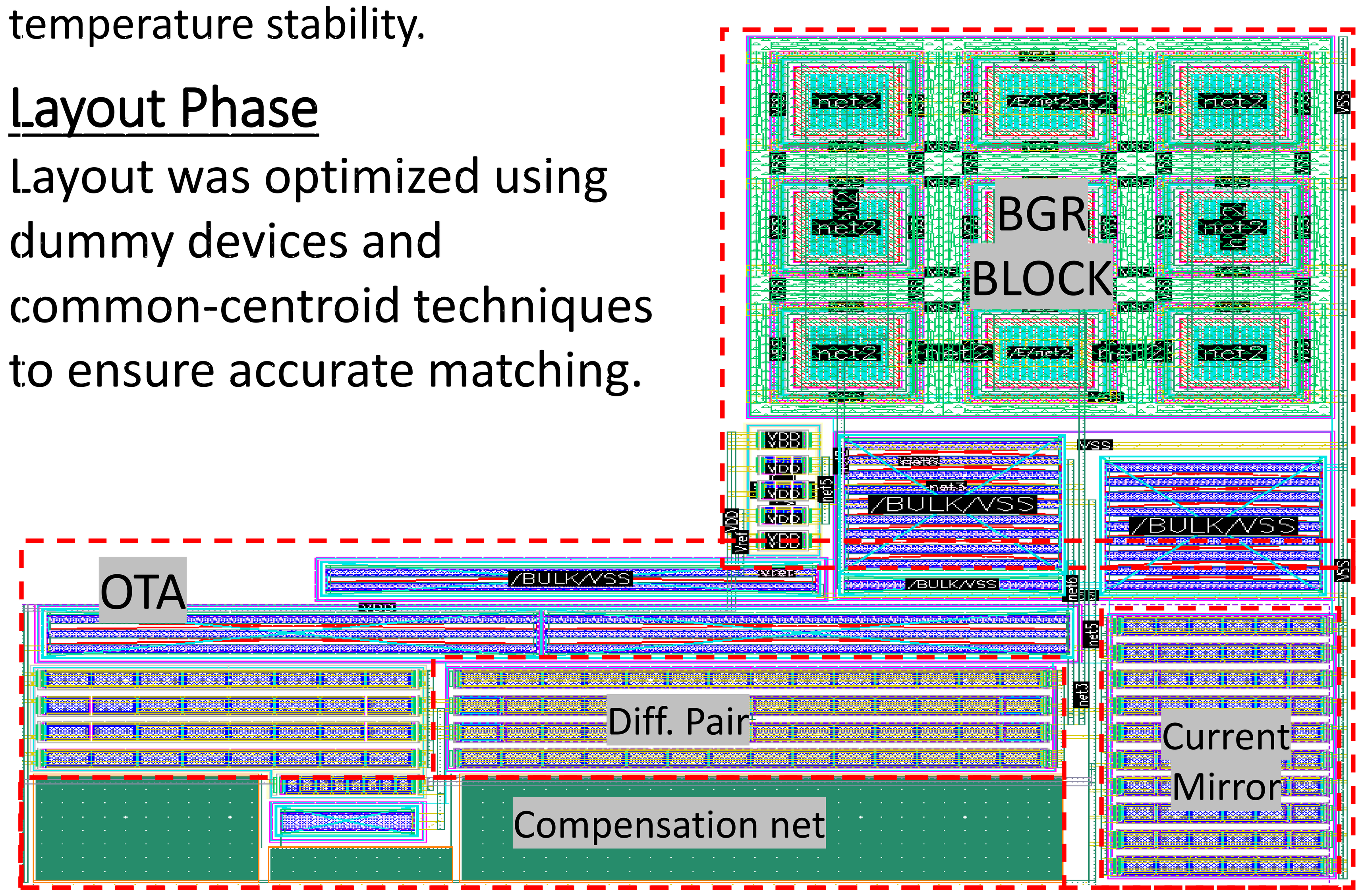
figure 1: Operating principle of the BandGap reference

Implementation

The LDO, designed in TSMC 28nm with a two-stage OTA and modified bandgap (0.72V), reliably regulates 0.9V across varying loads and supply levels with improved temperature stability.

Layout Phase

Layout was optimized using dummy devices and common-centroid techniques to ensure accurate matching.



Results

The following table summarizes three critical performance metrics of the LDO:

Metric	Definition	Requirement	Achieved
Temperature Coefficient	$\frac{dV_{out}}{dT}$(ppm/°C)	< 60	5.8 (↑90.3%)
Line Regulation	$\frac{\Delta V_{out}}{\Delta V_{DD}}$(%)	< 1%	0.12% (↑88%)
Load Regulation	$\frac{\Delta V_{out}}{\Delta I_{load}}$(%)	< 10%	0.41% (↑95.9%)

Table 1: Summary of the three critical performance metrics of the LDO.

Our LDO maintains excellent output stability across a wide operating range:

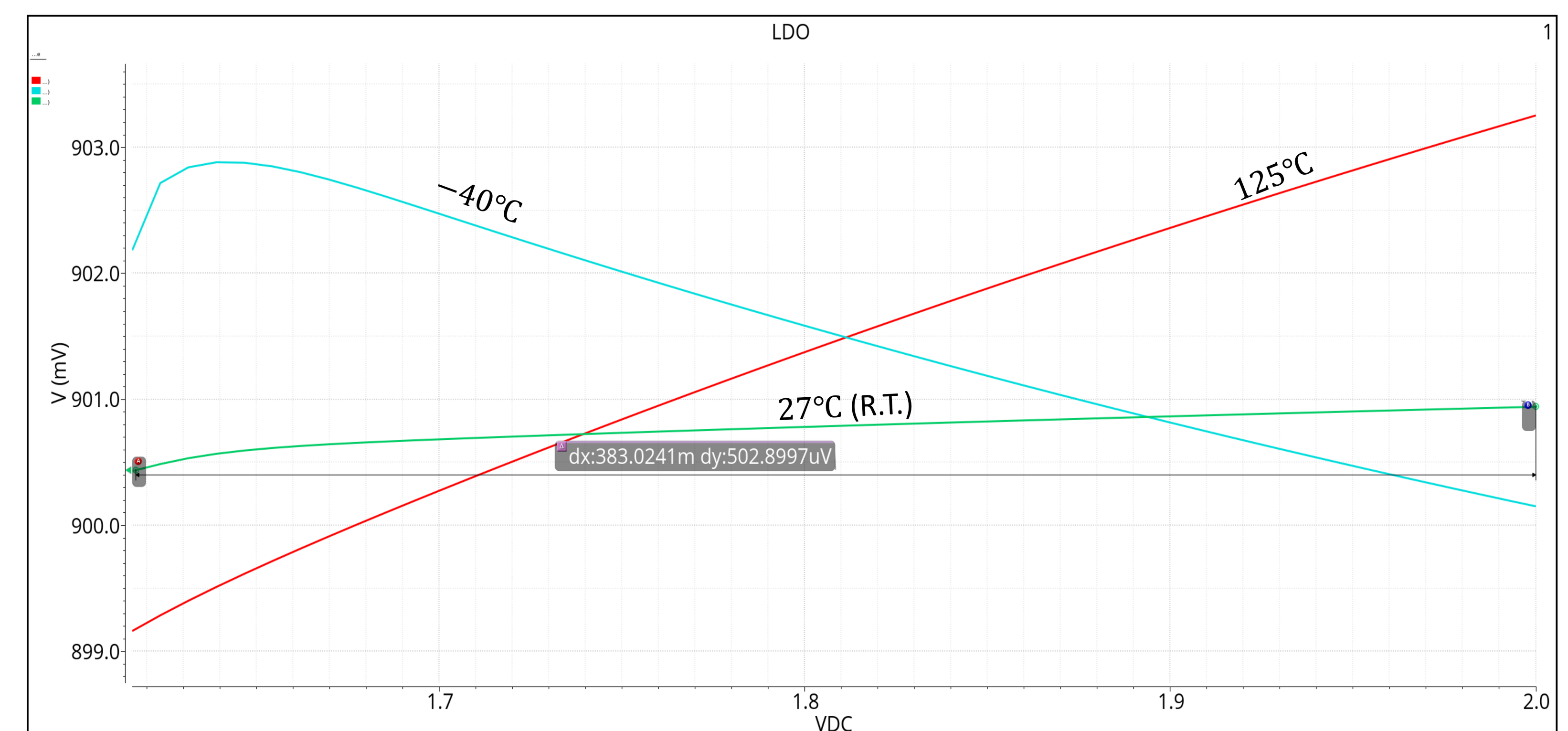


figure 2: V_{out} against Supply Voltage for a different temperature

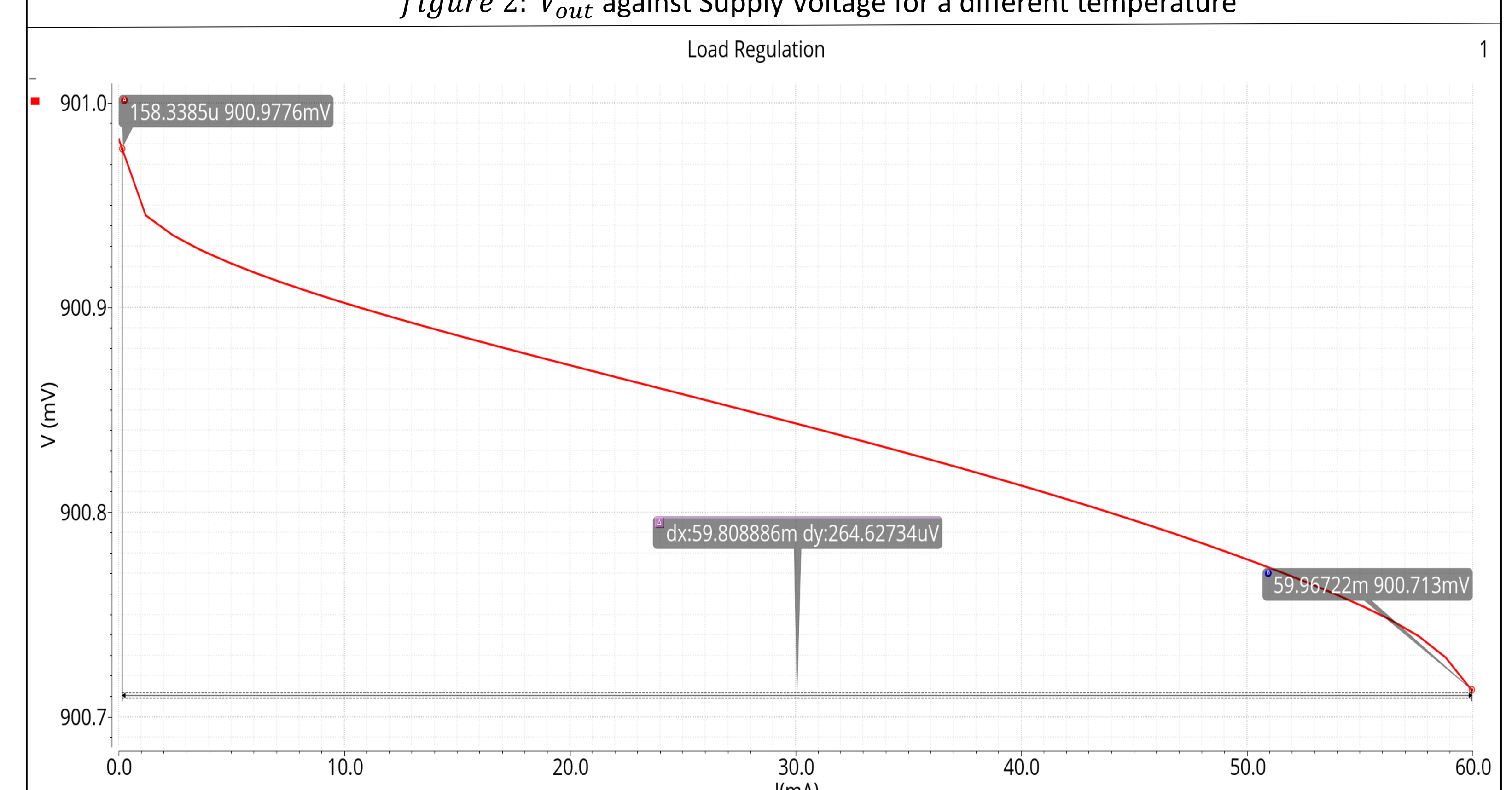


figure 3: V_{out} against I_{load} $[0 - 60mA]$