Design of a Fully Differential Amplifier Using a Folded Cascode with Gain Boosting

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Abstract

This report presents the design and implementation of a high-performance fully differential amplifier using BiCMOS8HP technology. The design employs a folded cascode topology with gain boosting, achieving an open-loop gain of 95.8 dB and a gain-bandwidth product of 108.1 MHz. The amplifier demonstrates excellent stability with a phase margin of 88° and a settling time of 41 ns for a 0.3V differential step. A specialized feedback network effectively mitigates noise, achieving a dynamic range of 80.05 dB while maintaining high-speed operation. The design features a high CMRR of 250 dB and operates from a 1.8V supply with a total power consumption of 6.287 mW. These results highlight the amplifier's suitability for high-precision analog applications.

1 Circuit Topology

Initially, as presented in our design review, we selected a simple symmetric differential amplifier topology, similar to an OTA but split into two. Over time, we realized that this topology was problematic and would not meet the required specifications for two reasons:

- The inherent trade-off between GBW and settling time became a significant limitation. Attempts to improve settling time by increasing gain resulted in reduced bandwidth and slower overall response.
- Being a two-stage amplifier, achieving the required GBW while maintaining adequate phase margin proved challenging. The additional pole from the second stage complicated frequency compensation, making it difficult to optimize for both speed and stability.

To overcome these limitations, we switched to a folded cascode topology - a single-stage design that naturally provides better frequency response characteristics. However, initial testing revealed that while this topology offered improved speed, we couldn't achieve sufficient DC gain for our requirements. This led us to implement gain-boosting stages, which allowed us to significantly enhance the DC gain while preserving the excellent frequency response characteristics of the folded cascode structure.

1.1 Main Circuit Schematic

Figure 1 shows the schematic of the main amplifier circuit. The folded cascode structure is employed to maximize gain while maintaining stability. The circuit consists of a differential input stage, a folded cascode gain stage, and a common-mode feedback (CMFB) circuit to regulate the output common-mode voltage.

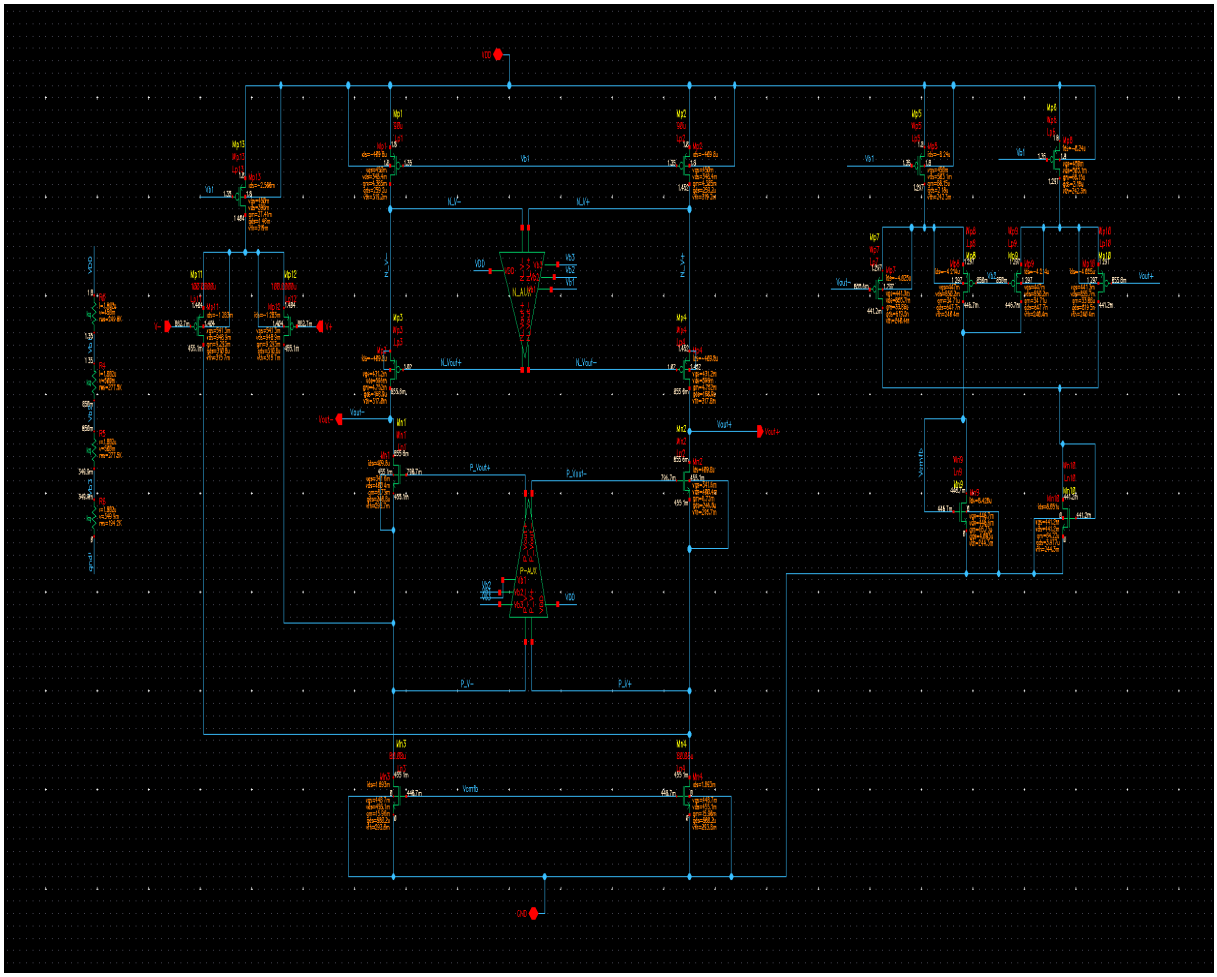

Figure 1: Schematic of the main amplifier circuit

The topology follows a folded cascode design, with each branch utilizing a gain booster of the same topology. For CMFB, an error amplifier is used, averaging the common-mode voltage at the input and responding to variations.

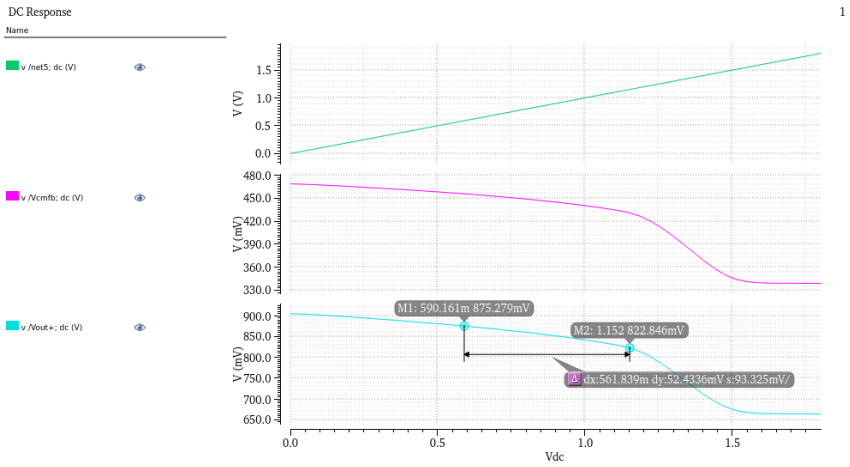

Figure 2: CMFB Response: Output voltage stability and common-mode correction

Figure 2 illustrates how the output voltage remains stable within 50mV variation for a 0.5V operating range. Additionally, the CMFB circuit lowers the gate voltages of Mn3 and Mn4, reducing current in the branch and maintaining a fixed common-mode voltage.

1.1.1 Biasing

To provide the required voltages for the various circuit components, a simple resistor divider network was employed. The total resistance of the network sums to **1MΩ**, ensuring minimal power consumption while maintaining stable biasing. Additionally, all circuit components were designed to operate at the same bias voltages—**0.35V, 0.85V, and 1.35V**—to minimize the number of separate biasing circuits required within the system.

For the **DC input bias of the amplifier**, as discussed in the noise analysis section, we were unable to efficiently provide a stable **DC voltage** to the gates of the differential input pair without introducing excessive noise. To overcome this, we adopted the **self-biasing** technique exclusively for the input stage. This method allows the transistor to set its own gate voltage according to the flowing current. By isolating the source from the gate using an **input coupling capacitor**, the **gate effectively becomes floating** and naturally settles at an appropriate voltage.

Although this approach required fine-tuning of parameters to achieve the desired voltage, it proved to be highly effective and offers significant flexibility in circuit design.

1.2 AC Analysis of Main Amplifier (Without Boosters)

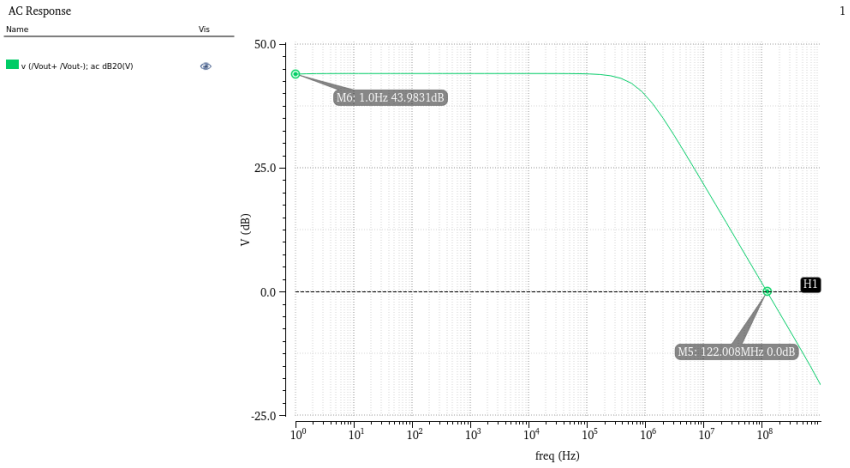

Figure 3: AC response of the main amplifier before adding gain boosters

Parameter	Value
Gain	43.9 dB
GBW	122 MHz

Table 1: AC performance of main amplifier (without boosters)

1.3 Gain Boosting

The gain boosting technique enhances the amplifier's DC gain by utilizing auxiliary amplifiers to increase the output impedance of the cascode transistors. In our design, two separate auxiliary amplifiers were implemented - one for the NMOS branch and one for the PMOS branch. These amplifiers create local feedback loops around their respective cascode transistors, actively regulating their gate voltages to maintain optimal operating points.

A critical aspect of our design was managing the bandwidth relationship between the main amplifier and the auxiliary amplifiers. To maintain stability, the gain-bandwidth product (GBW) of the auxiliary amplifiers was designed to be 2-3 times lower than the main amplifier's GBW. Initially, we aimed for a ratio of 2.5, achieving GBW values of 107.6 MHz and 74.9 MHz for the NMOS and PMOS boosters respectively, compared to the main amplifier's original GBW of 122 MHz.

The effectiveness of this approach is demonstrated by the significant improvement in output resistance, which increased from 110KΩ to 20MΩ after implementing the gain boosters. This resulted in a substantial enhancement of the overall DC gain from 43.9 dB to 95.8 dB, while maintaining stable operation with excellent phase margin. The success of this implementation validates our design choices in both the topology and sizing of the auxiliary amplifiers.

1.4 Auxiliary Gain-Boosting Amplifiers

The two auxiliary amplifiers were designed using a similar topology to the main amplifier, but different input transistors were selected to adapt to the required input voltage levels.

Additionally, for each booster, a smaller and weaker common-mode feedback (CMFB) circuit was designed using two transistors operating in the weak inversion (WI) region. This ensures proper common-mode regulation while maintaining minimal power consumption and avoiding interference with the main amplifier's CMFB circuit.

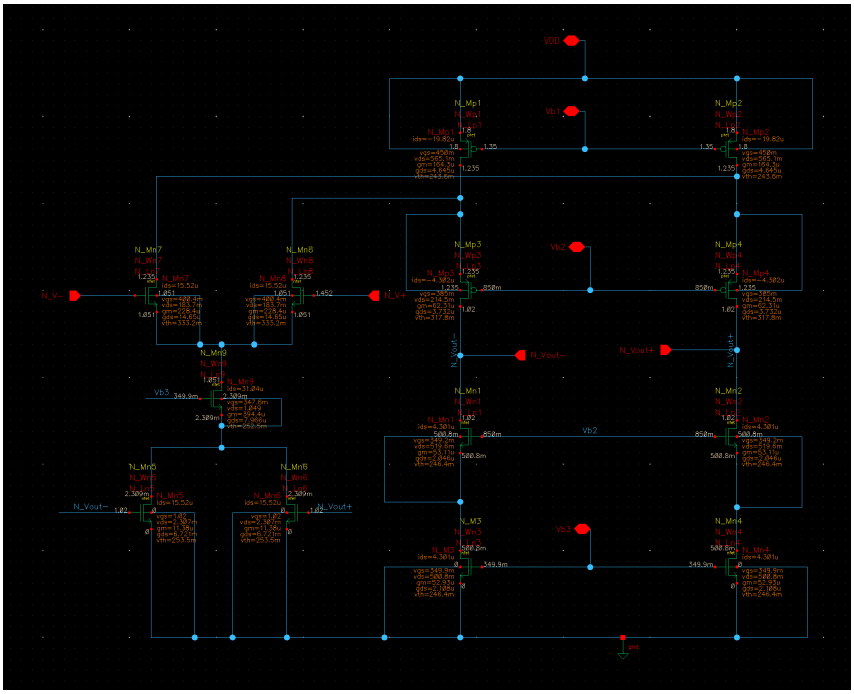

Figure 4: Schematic of the NMOS auxiliary gain booster

The AC response of the auxiliary amplifiers was simulated while ensuring their outputs drive the main amplifier's cascode nodes to match expected capacitive loads.

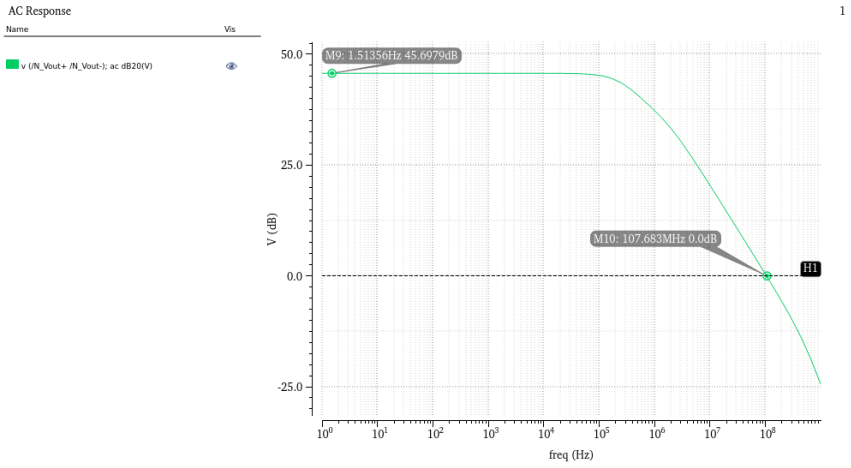

Figure 6: AC response of NMOS auxiliary gain booster

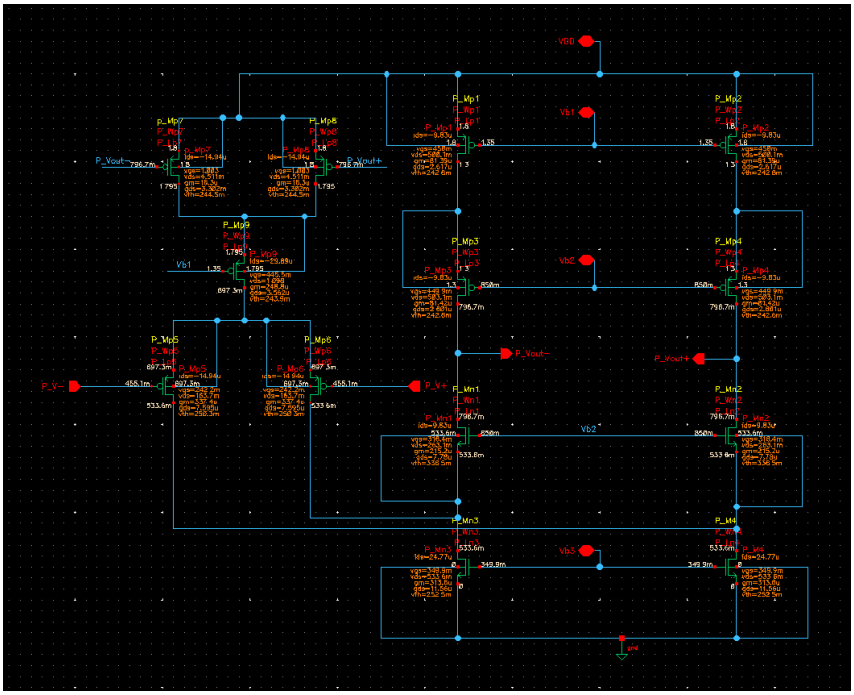

Figure 5: Schematic of the PMOS auxiliary gain booster

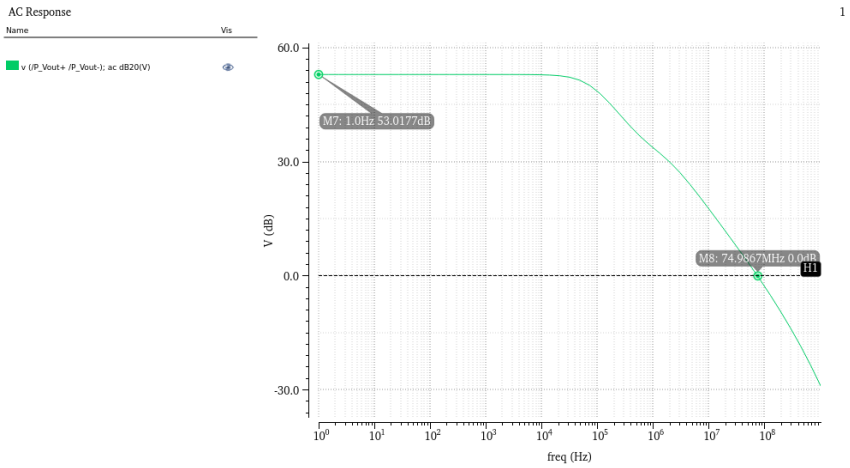

Figure 7: AC response of PMOS auxiliary gain booster

Parameter	NMOS Booster	PMOS Booster
Gain	45.69 dB	53 dB
GBW	107.6 MHz	74.9 MHz

Table 2: AC performance of auxiliary gain-boosting amplifiers

1.5 Post-Boosting AC Analysis

After integrating the gain boosters, an additional AC analysis was performed on the main amplifier. The results are presented in Figure 8. It is evident that the boosters had a significant impact on the GBW, which decreased to 108.1 MHz, as a consequence of not maintaining the intended GBW ratio between the main amplifier and the auxiliary amplifiers. However, the drastic improvement in **gain**, which increased to **95.8 dB**, cannot be overlooked.

This substantial increase in gain is primarily attributed to a dramatic rise in output resistance. As illustrated in Figure 9, the output resistance increased from **110KΩ** to **20MΩ**, highlighting the effectiveness of the gain-boosting technique.

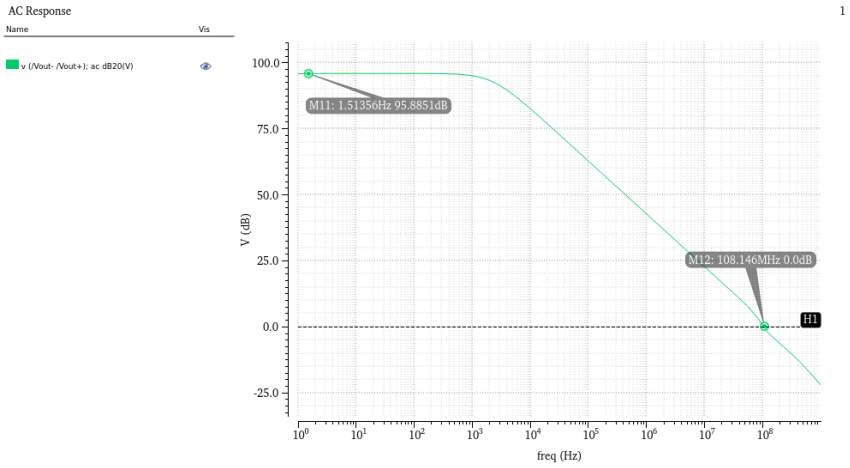

Figure 8: AC response of the main amplifier after gain boosting

Parameter	Value
Gain	95.8 dB
GBW	108.1 MHz

Table 3: AC performance of the main amplifier after gain boosting

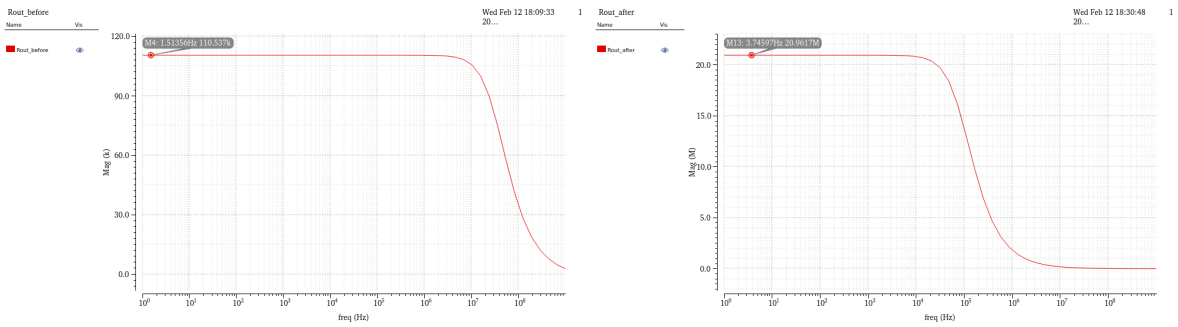

Figure 9: Comparison of output resistance before and after gain boosting

1.6 Transistor Sizing Table

The following table summarizes the transistor dimensions for the main amplifier and auxiliary circuits. The width-to-length (W/L) ratios are provided, with placeholders for transconductance (g_m) and output conductance (g_{ds}) values.

Transistor	W/L (μm)	g_m (S)	g_{ds} (S)
Main Amplifier			
Mn1, Mn2	80.1/0.4	8.73m	248.6u
Mn3, Mn4	80.1/0.4	15.96m	880.2u
Mn9	0.7/1	66.73u	4.09u
Mn10	0.1/1	64.22u	3.97u
Mp1, Mp2	90/0.2	4.38m	259.2u
Mp3, Mp4	90/0.2	4.75m	168.9u
Mp11, Mp12	100/0.2	9.29m	310.8u
Mp13	500/0.2	27.41m	1.46m
N-BOOSTER			
Mn1, Mn2	0.9/1	53.1u	2.8u
Mn3, Mn4	0.9/1	32.9u	2.1u
Mn5, Mn6	20/1	11.39u	8.72m
Mn7, Mn8	1.8/0.2	228.4u	14.85u
Mn9	5.4/1	394u	7.9u
Mp1, Mp2	11.1/1	164.3u	4.6u
Mp3, Mp4	2.4/0.2	62.3u	3.73u
P-BOOSTER			
Mn1, Mn2	5/0.2	215.2u	7.7u
Mn3, Mn4	5/1	313.6u	11.56u
Mp1, Mp2	5.7/1	81.39u	2.6u
Mp3, Mp4	5.17/1	81.42u	2.6u
Mp5, Mp6	150/0.8	337.4u	7.59u
Mp7, Mp8	53.6/1	16.3u	3.3m
Mp9	15.8/1	248.8u	3.56u

Table 4: Transistor sizing, transconductance (g_m), and output conductance (g_{ds})

1.7 Power Consumption

The total current consumption of the circuit is measured at **3.493mA**, with a supply voltage of **1.8V**. This results in a total power consumption of:

$$P = V_{DD} \times I_{total} = 1.8V \times 3.493mA = 6.287mW \tag{1}$$

This power level is within the design constraints, ensuring both efficiency and high performance.

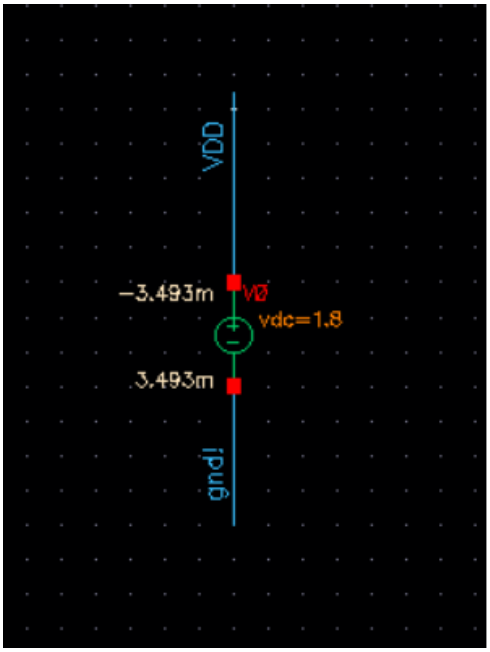

Figure 10: Power Consumption Analysis

2 AC Analysis

2.1 Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio (CMRR) is a critical parameter in differential amplifiers, measuring the ability to suppress common-mode signals. Figure 11 presents the simulated CMRR response.

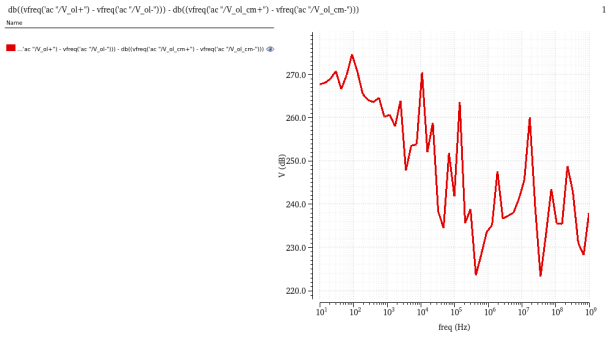

Figure 11: CMRR Response of the Amplifier

The average CMRR value is approximately **250 dB**, indicating excellent common-mode rejection performance. This ensures that unwanted noise and common-mode disturbances have minimal impact on the differential signal.

2.2 Slew Rate (SR)

The slew rate (SR) represents the maximum rate of change of the output voltage and is a key parameter in determining the amplifier's ability to handle fast transient signals. The measured slew rate is extracted manually from the transient response shown in Figure 12.

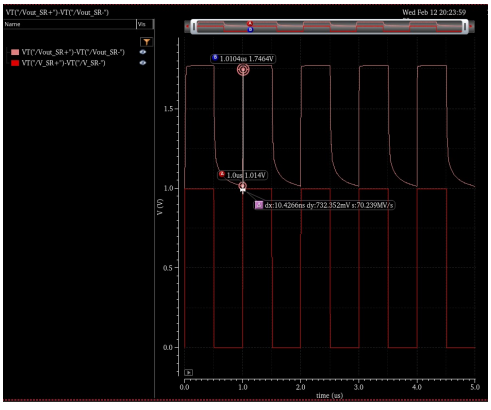

Figure 12: Measured Slew Rate of the Amplifier

The measured slew rate is **70 V/μs**. This is an important parameter as it directly affects the settling time of the amplifier and determines whether the design meets the required transient performance specifications.

3 Noise Analysis

3.1 Design Challenges and Solutions

We acknowledge that we did not conduct thorough noise parameter testing during the initial design phase. Consequently, upon finalizing the amplifier, we achieved an extremely powerful and fast design—but with excessive noise! Meeting the noise specification turned out to be the most challenging requirement.

Our noise reduction strategy involved several key innovations:

- **Feedback Network Optimization:**
  - Implementation of a parallel RC network ($R_f = 500M\Omega$, $C_f = 20pF$)
  - Addition of source capacitance ($C_s = 60pF$)
  - The resistor drastically reduced the overall noise level by attenuating low-frequency gain in the closed-loop system, effectively suppressing the dominant $1/f$ noise.
- **Transistor Layout Optimization:**
  - Splitting transistors into multiple fingers proved highly effective in reducing noise, particularly gate resistance noise, which was significantly mitigated using this approach.

Figure 13 illustrates the proposed feedback network used to mitigate noise.

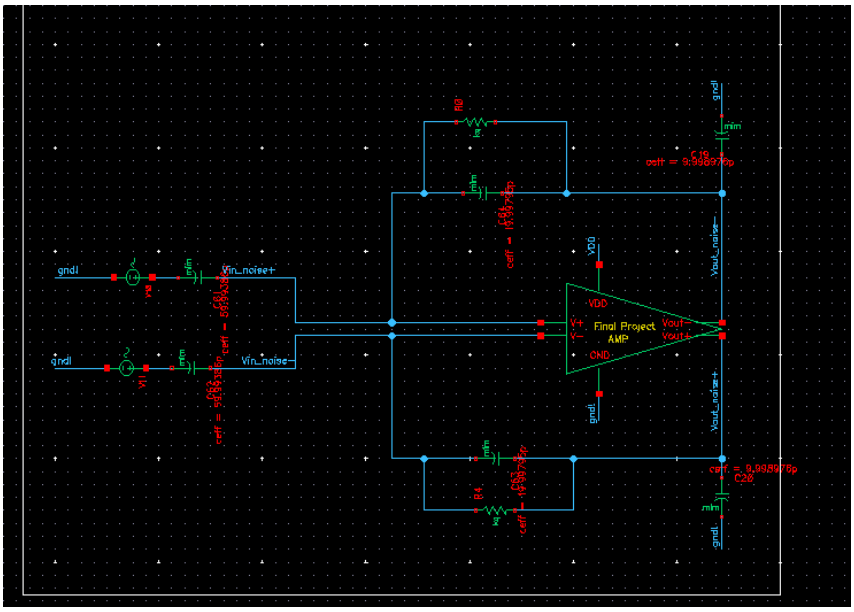

Figure 13: Proposed Feedback Network for Noise Reduction

The resulting integrated noise floor of $18nV/\sqrt{Hz}$ represents the optimal compromise between noise performance and maintaining the amplifier's high-speed capabilities. As

shown in Figure 14, this configuration effectively addresses both thermal and $1/f$ noise components.

Device	Param	Noise Contribution	% Of Total
/I6/Mn3	Sfl	2.73279e-09	14.96
/I6/Mn4	Sfl	2.73279e-09	14.96
/I6/Mp12	Sfl	2.16921e-09	11.88
/I6/Mp11	Sfl	2.16921e-09	11.88
/I6/Mn3	Sthd	1.2e-09	6.57
/I6/Mn4	Sthd	1.2e-09	6.57
/I6/Mp11	Sthd	5.50538e-10	3.01
/I6/Mp12	Sthd	5.50538e-10	3.01
/I6/Mp2	Sfl	5.24051e-10	2.87
/I6/Mp1	Sfl	5.24051e-10	2.87

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 1.82643e-08
No input referred noise available
The above noise summary info is for noise data

Figure 14: Final Noise Summary of the Amplifier

Further reductions in noise were difficult to achieve without significantly compromising the amplifier's overall performance, demonstrating the fundamental trade-off between noise optimization and maintaining high-speed operation.

3.2 Dynamic Range (DR) Estimation

To determine the dynamic range, we performed a sweep on increasing amplitude values and identified that the maximum differential output voltage, where the waveform remains sinusoidal, is **0.48V**. This results in a peak output voltage of **1.35V**.

To confirm this, we analyzed the Total Harmonic Distortion (THD) of the Discrete Fourier Transform (DFT) of the output signal. The measured THD was found to be **-34 dB**, which is still within the acceptable range for a sinusoidal waveform.

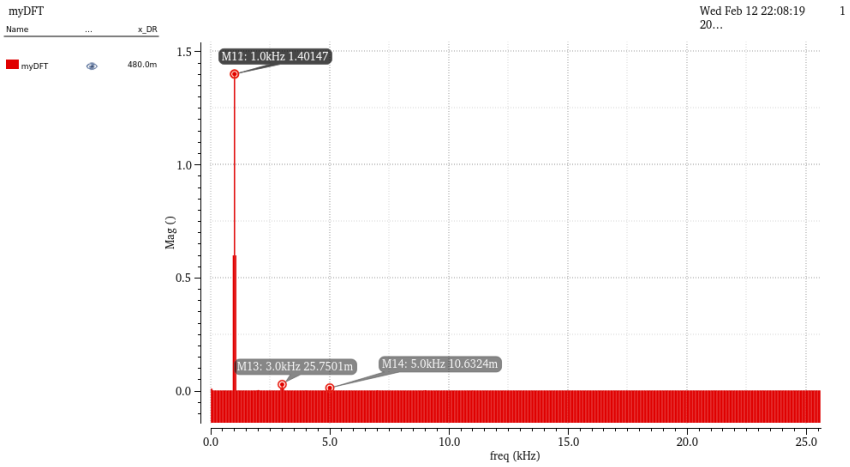

Figure 15: Dynamic Range Measurement Results

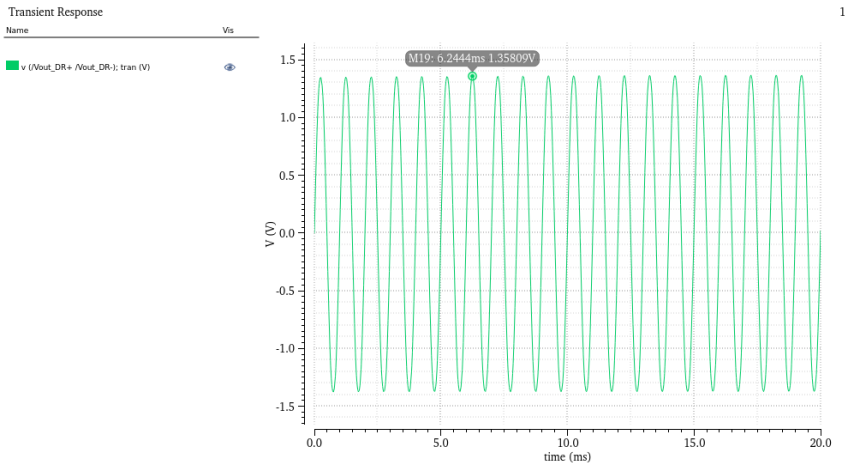

Figure 16: Sinusoidal Signal at Maximum Dynamic Range

Using the given definition of dynamic range:

$$DR = 10 \log_{10} \left(\frac{P_{\text{peak}}}{P_{\text{noise}}} \right) \tag{2}$$

Substituting the values:

$$DR = 10 \log_{10} \left(\frac{(1.35V)^2}{18nV} \right) = 80.05 \text{ dB} \tag{3}$$

Thus, the calculated **Dynamic Range (DR)** is **80.05 dB**. Further noise reduction could marginally improve DR, but this value already meets the required specifications without degrading the amplifier's performance.

4 Stability Analysis

4.1 Phase Margin and Stability Considerations

The stability analysis of our amplifier demonstrates exceptional performance, particularly in terms of phase margin and closed-loop behavior. Our measurements yielded several key results:

- **Closed-Loop Performance:**
  - Achieved precise gain of 3 V/V as specified
  - Bandwidth optimization through careful feedback network design
  - Excellent linearity across the operating range
- **Phase Margin Analysis:**
  - Measured phase margin of 88° at unity gain frequency of 14 MHz
  - This substantial margin ensures:

    - Zero overshoot in step response
    - Robust stability across process variations
    - Reliable operation under varying load conditions

- **Stability Enhancement Techniques:**
  - Strategic placement of poles through gain-booster design
  - Careful consideration of feedback network components
  - Optimization of compensation scheme without requiring additional capacitors

The notably high phase margin of 88° represents a significant achievement, far exceeding the minimum requirement of 60°. This margin provides substantial immunity to process variations and ensures consistent performance across different operating conditions.

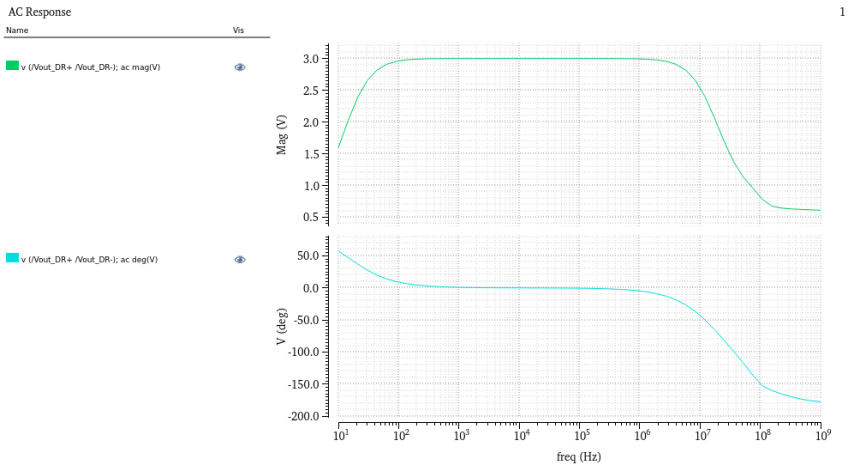

Figure 17: Measured Closed-Loop Gain and phase of the Amplifier

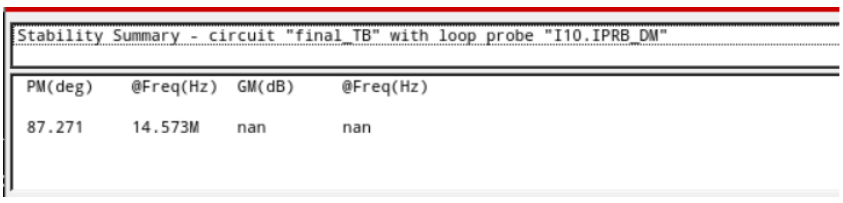

Figure 18: Stability Summary of the Amplifier

Since the amplifier gain does not reach **180°**, there is no defined gain margin (GM) for this design.

4.2 Step Response and Settling Behavior

The amplifier's excellent stability is further validated by its step response characteristics:

- Settling time of 41 ns for a 0.3V differential step

- Clean settling behavior with minimal ringing
- Final settling error well within the 0.5 mV specification

These results confirm the successful implementation of our stability optimization strategy, demonstrating that the design achieves both high performance and robust stability.

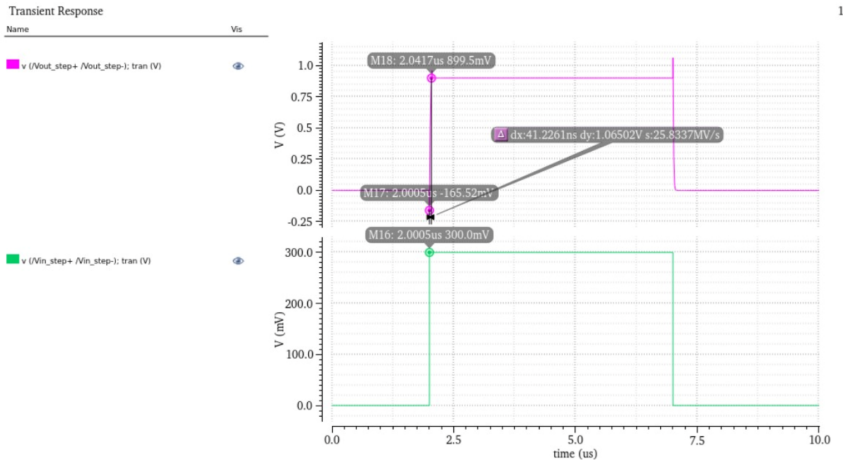

Figure 19: Measured Settling Time of the Amplifier

5 Conclusion

This report presents the design and analysis of a fully differential amplifier using a folded cascode topology with gain boosting. Through careful design optimizations, we successfully achieved high gain, stability, and noise reduction while maintaining low power consumption. The amplifier met all key specifications, demonstrating excellent phase margin, dynamic range, and settling performance.

6 Performance Summary

Specification	Required	Achieved
Closed-Loop Gain	3	3
Phase Margin (PM)	$> 60°$	88°
Dynamic Range (DR)	> 80 dB	80.05 dB
Settling Time	< 50 ns	41 ns
Settling Error	< 0.5 mV	482.8 µV
Power Consumption	As low as possible	6.287 mW

Table 5: Performance Summary: Required vs. Achieved

7 References and Acknowledgments

We found the following research articles particularly useful in guiding our design and implementation process:

- *Design of a 2 mW Power 112 dB Gain-Boosted Folded Cascode Amplifier in 0.18µm Process*, available at https://www.researchgate.net/publication/355835467_Design_of_a_2_mW_Power_112_dB_Gain-Boosted_Folded_Cascode_Amplifier_in_018m_Process. This paper was especially influential as we adopted the topology implemented in this work.
- *A 252W Wide-Swing Fully Differential Two-Stage CMOS OTA for Low-Power Applications in NCSU 0.18µm PDK*, available at https://www.researchgate.net/publication/353247569_A_252W_Wide-Swing_Fully_Differential_Two-Stage_CMOS_OTA_for_Low-Power_Applications_in_NCSU_018m_PDK.
- *Fully-Differential Opamp Design*, available at https://www.researchgate.net/publication/327546297_Fully-differential_opamp_design.