Iby and Aladar Fleischman Faculty of Engineering Tel Aviv University
הפקולטה להנדסה ע"ש איבי ואלדר פליישמן אוניברסיטת תל-אביב

The School of Electrical Engineering **בי"ס להנדסת חשמל**

Project Work Plan

Project Number : 3097

Project Name: Digital High Frequency Chip – Linear Low Dropout Regulator

Students:

Name: Arsen Arutyunov I.D. [redacted]

Name: Or Fahima I.D. [redacted]

Project carried out at: University

For the project instructor:

I approve the submission of the following report

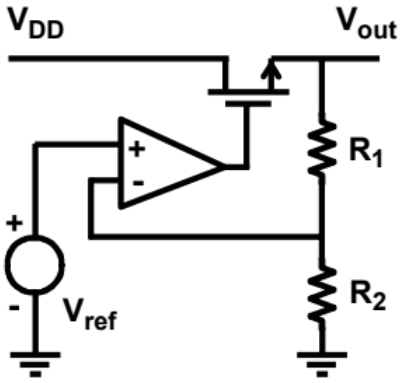
_ Signature: __*Tal Elazar*_____

Name: _Tal Elazar_

1 – Abstract

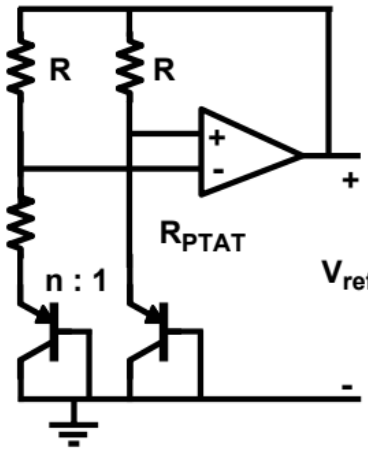
This project focuses on designing a linear low dropout (LDO) voltage regulator which provides a stable voltage supply, in a wide temperature range and immune to a range of line and load fluctuations, for a digital phase-locked-loop (PLL), which digital parts will be designed by several other project groups.

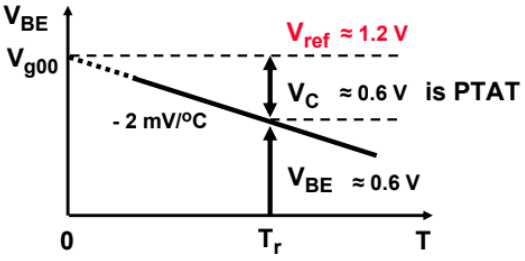
[1]The first building block of the LDO consists of an operational amplifier in an error amplifier configuration, a pass transistor (PMOS or NMOS), and two resistors forming a feedback loop .The error amplifier's purpose is to compare the feedback voltage set by the two resistors voltage divider with a stable reference voltage (set by the second building block – the bandgap reference circuit), and adjust accordingly the MOSFET gate voltage, so the transistor can drive the required current to match the feedback voltage with the reference voltage precisely.



As previously mentioned, the stable reference voltage is provided by a bandgap reference circuit, which works by summing the base-emitter voltage of the BJT transistor in FA mode, which is negatively proportional to absolute temperature in the desired temperature range (CTAT), with a component that is positively proportional to absolute temperature in the same temperature range (PTAT). Combined, the output voltage remains constant across this temperature range and is insensitive to a range of line and load fluctuations. There are multiple possible topologies to implement a bandgap reference, we will focus on a topology based on an op-amp.

$$V_{out} = V_{ref} \frac{R_1 + R_2}{R_2}$$





$$V_{ref} = V_{BE} + V_{R_{PTAT}} = 1.2V$$

[1] Pictures are taken from W. Sansen, Analog Design Essentials, 2006.

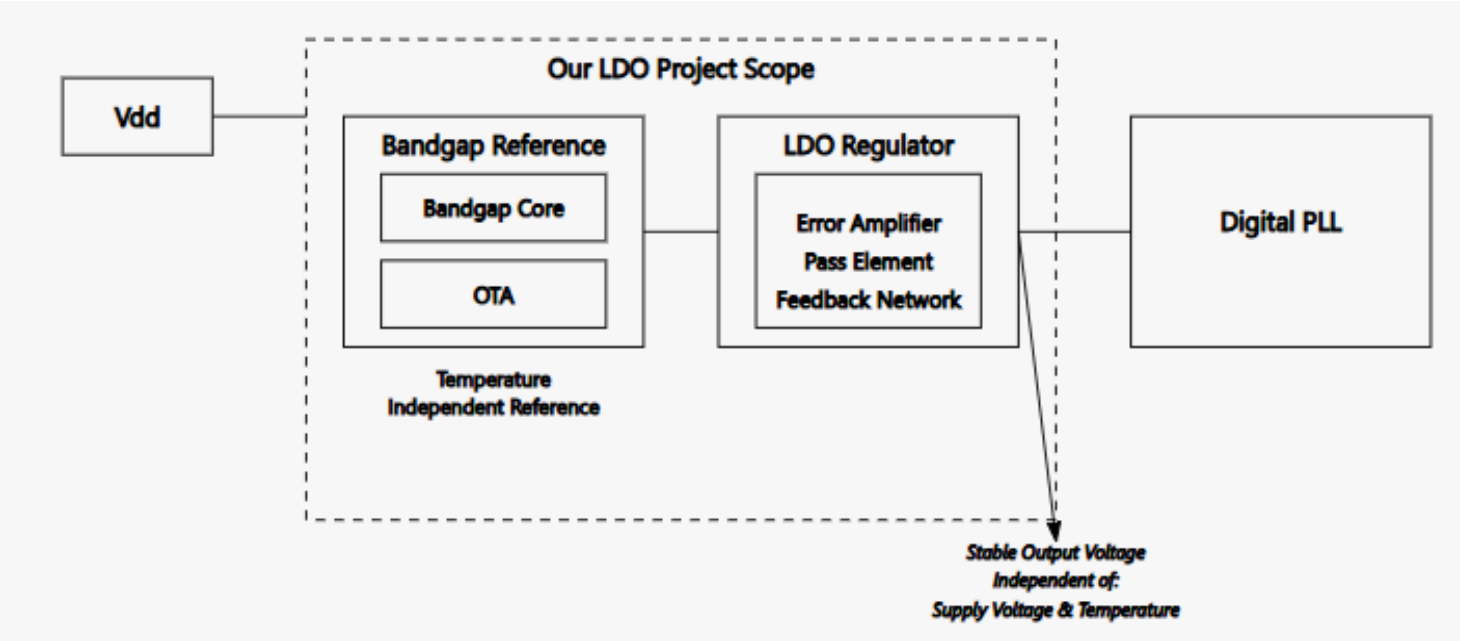
The op-amp is a vital component in both circuits and will be fully designed as well to match the requirements of both blocks.

LDO regulators are widely used in electronic systems and integrated circuits (ICs) to supply consistent, noise-immune voltage to sensitive analog, digital and mixed-signal circuits, such as PLLs, data converters and radio frequency circuits. The highly precise, low power and stable behavior of the LDO regulators are crucial in such circuits to prevent possible glitches caused by voltage fluctuations or noise. In the case of the PLL, it requires stable input voltage to ensure accurate frequency synthesis and high signal integrity in timing-critical applications like digital communication systems and microprocessors.

The project involves the schematic and layout design of a bandgap reference circuit, an op-amp in error amplifier configuration, and the LDO regulator circuit. After receiving the output voltage, load current, PSSR specifications and the line and load requirements, we will begin the design of the bandgap reference circuit, which will utilize at first an ideal built in Virtuoso op-amp block. Following successful simulations testing its performance and ensuring it meets the desired specifications, we will implement its layout and then run layout-vs-schematic and design rule checks and extract layout parasitics and perform post-layout simulations to verify that the performance still meets the requirements.
Then we will design the schematic and implement the layout of the op-amp configuration needed in both the bandgap reference circuit and the LDO regulator and run post-layout simulations to test its performance.
Finally, the LDO regulator block schematic, including the working bandgap reference circuit and the op-amp blocks, will be designed, and then its layout will be built. Final simulation tests, including the LVS, DRC checks and the extraction of parasitics, will be utilized to verify the entire circuit’s performance meets the requirements and specifications.
Upon completion, the circuit will be sent to tape out and a project book, including design details and its challenges, analysis and simulation results, will be compiled.

The entire project will be implemented in Cadence Virtuoso under the TSMC 28nm technology node.

The block diagram**:**



2 – Motivation

The fundamental motivation for this project stems from the critical requirements of modern Digital Phase-Locked Loop (PLL) circuits. In high-frequency digital PLLs, maintaining precise timing and phase alignment is crucial, which demands an extremely stable power supply. Any fluctuation in the supply voltage can directly impact the PLL's performance, causing jitter and phase noise that degrade the overall system performance.

The Linear Low Dropout (LDO) regulator serves as a vital component in this context, providing a constant output voltage that remains stable regardless of power supply variations and temperature changes. This stability is essential for the PLL's voltage-controlled oscillator (VCO) and other sensitive components, where even minor voltage variations can significantly affect the output frequency accuracy.

While alternatives like switching regulators exist, they introduce switching noise that can severely impact the PLL's performance. Traditional linear regulators suffer from poor temperature compensation and limited power supply rejection. Our LDO implementation addresses these challenges by providing precise regulation with high PSRR (Power Supply Rejection Ratio), enabling optimal PLL performance in high-frequency applications.

The successful implementation of this project will enhance the reliability and accuracy of digital PLL systems by ensuring stable, noise-free power delivery to critical components.

3 – Statement of Work

This project consists of the planning, schematic design, simulation, and layout implementation of a linear low dropout voltage regulator, which includes a bandgap reference circuit. The purpose of this circuit is to supply a stable temperature-independent voltage to a digital phase-locked-loop (PLL). Hence, this project requires a solid foundational theoretical knowledge in analog circuit design, as well as practical knowledge in Cadence Virtuoso with the TSMC 28nm technology node for the design, simulation and layout implementation of the circuit.

The theoretical background knowledge required for this project is the following:

1) Fundamentals of analog circuit design, including MOSFET operation, BJT operation, basic amplifier topologies, differential amplifiers, current mirrors, operational amplifiers, feedback and stability.

2) Basic principles and different topologies of LDO voltage regulators – understanding its function and necessity, its different possible topologies, understanding the purpose of each component – pass transistors, error amplifiers, feedback resistors network. Understanding the concepts of temperature independent voltage reference, line regulation, load regulation.

3) Bandgap reference circuits – understanding their function and necessity, exploring different possible topologies and the pros and cons of each (current mirror vs. op amps configurations etc.), learning the concepts of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltages and how components with such voltages are used to produce a stable reference circuit.

4) Operational amplifier design and stability analysis – learning how to design an op-amp with the required gain that meets the power limitations in this project and ensuring it’s stable by implementing a resistors network feedback loop.

Key resources include:

1) For basic review of analog circuits analysis – the analog electronics circuit course materials, including the course book SEDRA/SMITH Microelectronic Circuits 7th Edition.

2) For more advanced material, focusing on synthesis of circuits – the integrated analog circuits course materials, including the course books Analog Design Essentials by W. Sansen, and Design of Analog CMOS Integrated Circuits by B. Razavi.

3) Additional online resources for the TSMC 28nm technology node and Virtuoso.

The project consists of several key phases – theoretical study, schematic planning and design, circuit simulation, layout implementation, and finally validation. In detail:

1) After reviewing fundamentals of analog circuit design, and learning the principles of LDOs, bandgap reference circuits, op-amps, digital PLL, we will begin to gather the specifications and requirements for the LDO. These include required output voltage, supplied voltage to the LDO and its fluctuations (PSSR and line regulation requirements), load (PLL) current and its fluctuations (load regulation requirement), allowed max current to feedback resistors in LDO, temperature range and voltage temperature coefficients in $\frac{ppm}{^\circ C}$.

2) Design, simulation, and layout implementation of the bandgap reference circuit:

- Topology selection and design – exploring different possible topologies and picking one to design. Implementing the PTAT and CTAT to obtain a stable reference voltage. At this stage using a built-in op-amp in Virtuoso to complete the design.
- Simulation – simulating the circuit in Virtuoso to verify it provides a stable output across the required temperature range.
- After successful simulations, implementing the layout of the circuit in Virtuoso, while ensuring parasitic effects and layout size are minimized. Then, conducting layout-vs-schematic (LVS) and design rule (DRC) checks to

confirm the layout matches the schematic and complies with the technology design rules. Finally, performing post layout simulations that include parasitics to verify circuit still meets performance requirements.

3) Design, simulation, and layout implementation of the op-amp:

- Picking a suitable op-amp topology to meet required gain and stability requirements for both bandgap reference circuit and the LDO circuit. Testing its performance with simulations in Virtuoso. Then implementing its layout, verifying through post layout simulations.

4) Design and simulation of the LDO circuit – selecting the MOSFET transistor and size based on the dropout voltage requirements and output current. Designing the feedback network so it meets the desired output voltage and current requirements. Integration of all components together and implementation of the layout, with LVS and DRC checks, performing parasitics extraction and performing final post-layout simulations under various load and temperature conditions to verify design. After successful completion, compiling a project book to document the design, challenges, analysis and results.

The project will solely use Cadence Virtuoso for the schematic design of the circuits, their simulations and their layout implementation and verification.

4 – Project Deliverables

1. System Requirements*

1. Reference voltage value – 1.1-1.2V.
2. Output voltage value – 0.8-0.9V.
3. Load current drawn – 4-5mA.
4. Feedback network resistance current drawn – < 40-50uA.
5. Power Supply Rejection Ratio (PSRR) ≥ 40dB at frequencies up to 1kHz.
6. Output voltage temperature coefficient – variation ≤ 1% across temperature range of -40°C to 125°C $(60\,\frac{ppm}{^\circ C})$.
7. Load regulation ≤ 0.1% for load current changes from 0 to 10mA.
8. Dropout voltage ≤ 20mV at maximum load current.

*Note: Specifications may be adjusted based on final PLL system requirements, additional requirements (e.g. power dissipation) will be known later.

2. Design and Simulation Deliverables

First Semester:

- Bandgap Reference Circuit: schematic design, temperature stability simulations in virtuoso, OP simulations, initial layout*, LVS and DRC checks*, post-layout performance simulations with parasitics extracted*.
- Operational Amplifier: schematic design, operating point simulation, performance (gain) measurements, initial layout*.

*Note – the full completion of layout design for both parts before the end of the first semester isn't guaranteed.

Second Semester:

- Complete LDO Circuit: final schematic, final layout with all components integrated, post-layout simulations that verify requirements are met.

3. Testing Methods (All in Cadence Virtuoso)

- DC OP Analysis: load/line regulation, dropout voltage
- AC Analysis: PSRR, loop stability, phase margin
- Load/Line Analysis: performance across varying load and supply voltages
- Temperature Analysis: performance across temperature range

5 – Project Schedule

	Milestone	Description (2-3 lines)	Planned Date
1.	Literature review and background study	Review analog circuit design fundamentals, review material about digital PLL, review material about LDO circuits, bandgap reference circuits.	Early November 2024
2.	Submitting project workplan	Including defining project quantitative requirements, e.g. voltages, currents, PSSR	24/11/24
3.	Summary of a digital PLL and the LDO, BGR circuits	Compiling short reports on LDO circuit, bandgap reference circuit and basic digital PLL to build a solid theoretical foundation.	Late November 2024
4.	Schematic design of the bandgap reference circuit	Designing the schematic block of the bandgap reference circuit with an ideal built-in op-amp block in Virtuoso and testing it with simulations.	Early December 2024
5.	Layout design of the bandgap reference circuit	Designing the initial layout of the bandgap reference circuit, running LVS and DRC checks to ensure layout matches schematic and meets the design rules	Early January 2025
6.	Schematic design of the op-amp	Designing and simulating op-amp to meet desired gain and specifications for bandgap reference circuit. The same or very similar design will also be used in the LDO circuit.	Late January 2025
7.	Layout design of the op-amp	Designing the layout of the op-amp and integrating in the bandgap reference circuit, running LVS and DRC checks to ensure layout matches schematic and meets the design rules	Late February 2025
8.	Progress Presentation Submission		Early March 2025
9.	Schematic design of the LDO circuit	Designing the schematic block of the linear dropout circuit including the V_{ref} from the bandgap reference circuit and the op-amp designed, testing through simulations and fine tuning in Virtuoso.	March 2025
10.	Layout design of the LDO circuit	Implementing the layout of the LDO, running LVS and DRC checks to ensure layout matches schematic and meets the design rules	Early April 2025
11.	Final testing (post layout) and validation	Extracting layout parasitic parameters, performing post layout simulations, and ensuring quantitative objectives regarding PSSR, load regulation, line regulation, temperature stability are met.	Late April 2025

12.	Poster Submission and finishing the work		Late May 2025
13.	Writing project book and final presentation preparation	Summarizing the project steps, discussing challenges, presenting simulation results.	June 2025
14.	Final deliverables submission		July 2025