Schematics	Revision	Date	Release Information
SRT-96B-MAIN-IOT-NBIOT-STM-MP157	1.0	OCT 2018	first version release
	1.1	SEP 2019	second version release
	1.2	OCT 2019	Changing Stackup

01

01 Revision History
02 Block Diagram
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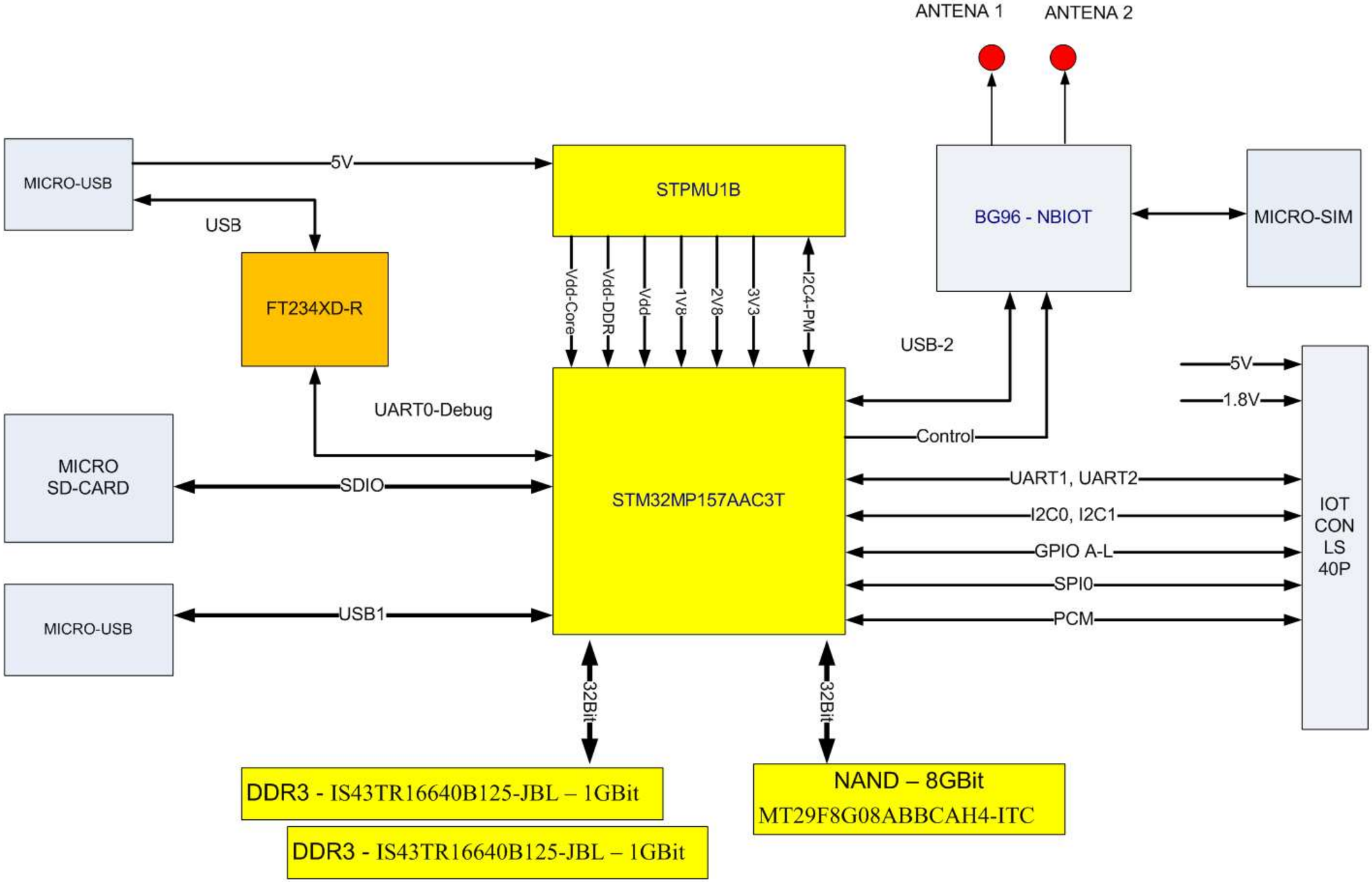
11 SD-CARD
12 USB-PORTS
13 Peripherals (LEDS, JTAG)
14 MODEM - 1
15 MODEM - 2
16 MISC

Silk:

Stinger96
SRT-PCB-01001
REV 1.2

Shiratech Solutions	Revision History			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
Tuesday, November 05, 2019	Scale		Sheet 1 of 16	

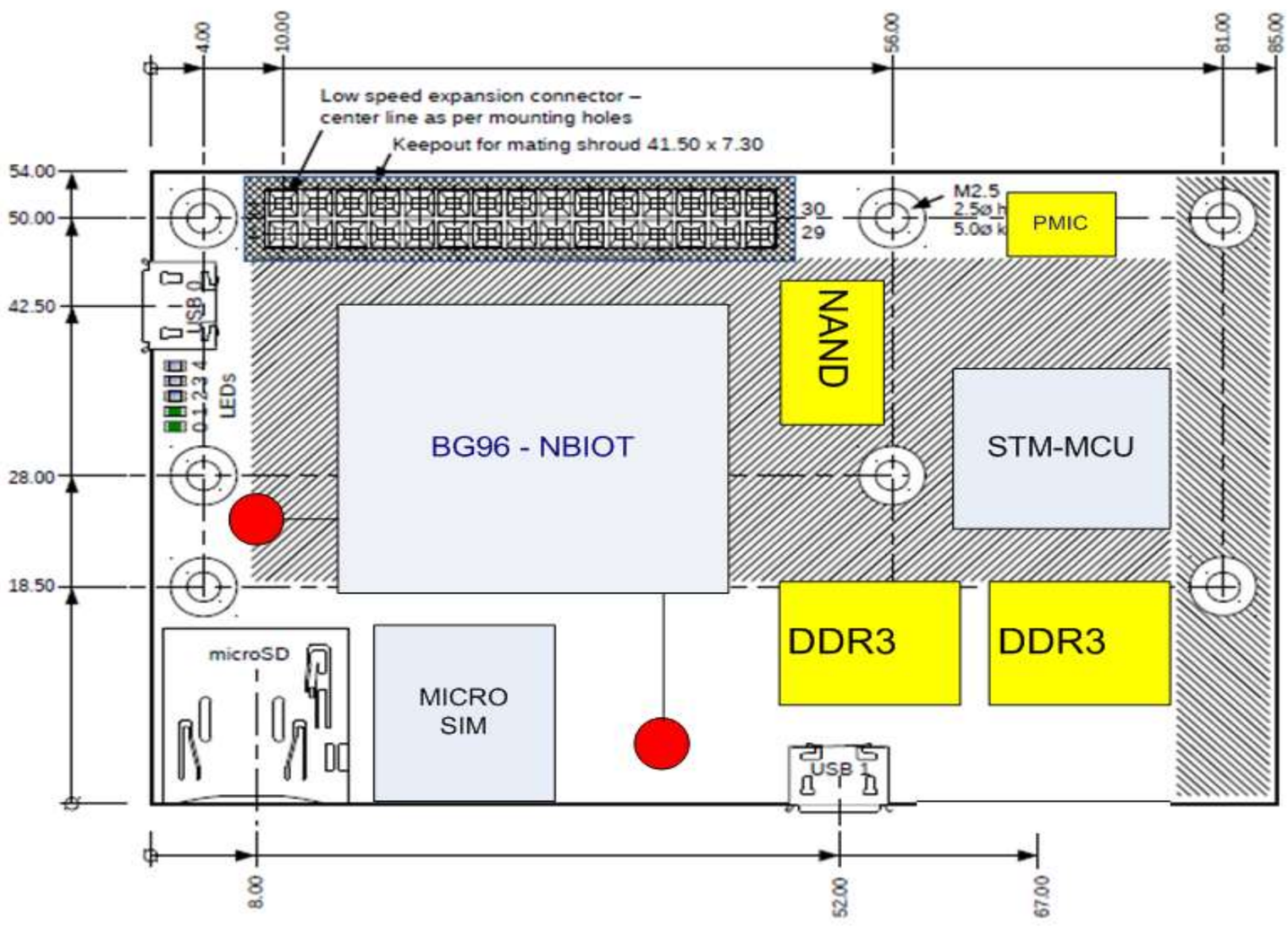
02

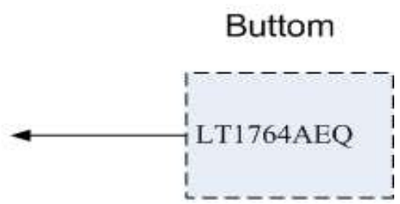


Shiratech Solutions	Block Diagram			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 2 of 16	

SRT-96B-MAIN-IOT-NBIOT-STM-MP157

03





ANTENNA

Shiratech Solutions	DXF			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 3 of 16	

layer	name	cu thickness (mil)	dielectric thickness (mil)	line width base (mil)	differential space (mil)	er	Zo (ohms)	Zdiff (ohms)
foils- Date:06/01/13 Customer: valens Boardname:10 layers				6	8	3.8	50.68710153	89.37827105
1 (coated microstrip)	pln	2.1		5	10	3.8	54.75657557	99.64842697
pp glass epoxy (tg 180)			4					
2 (ref. plane)	pln	1.4						
core glass epoxy (tg 180)			5	4.5	5	3.8	50.15743385	90.47649966
3 (offset stripline)	sig	0.7		4	7	3.8	52.99137943	100.0845077
pp glass epoxy (tg 180)			5	3.5	4.5			98.4
4 (ref. plane)	pln	1.4						
core glass epoxy (tg 180)			4	5.5		3.8	50.90751816	
5 (offset stripline)	sig	0.7		4	5.5	3.8	58.67816363	100.0605955
pp glass epoxy (tg 180)			14	3.5	4.5			100.88
6 (offset stripline)	sig	0.7		5.5		3.8	50.90751816	
core glass epoxy (tg 180)			4	4	5.5	3.8	58.67816363	100.0605955
7 (ref. plane)	pln	1.4		3.5	4.5			100.88
pp glass epoxy (tg 180)			5					
8 (offset stripline)	sig	0.7		4.5	5	3.8	50.15743385	90.47649966
core glass epoxy (tg 180)			5	4	7	3.8	52.99137943	100.0845077
9 (ref. plane)	pln	1.4		3.5	4.5			98.4
pp glass epoxy (tg 180)			4					
10 (coated microstrip)	sig	2.1		6	8	3.8	50.68710153	89.37827105
				5	10	3.8	54.75657557	99.64842697
		0.34004	1.27					
total thickness (including plating and solder mask) +/- 10%			1.61004					

impedance on the manufactured boards will be within +/- 10% of the values calculated above

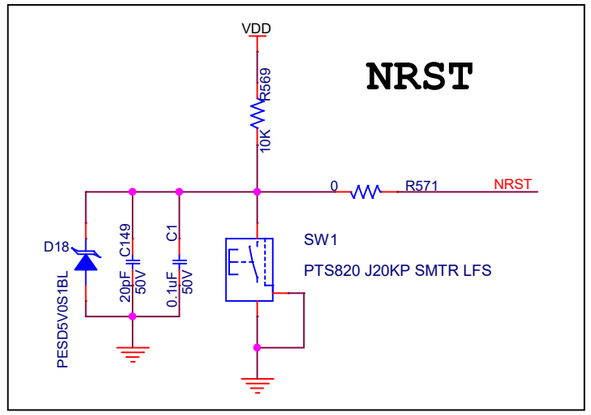
VIA SIZE

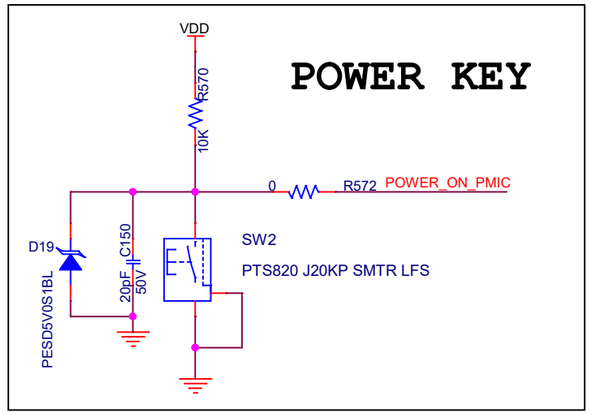
LAYER	PAD	HOLE
1--12	16	8
1--2, 11-12	10	4
2--3, 10-11	10	4
3--10	16	8

04

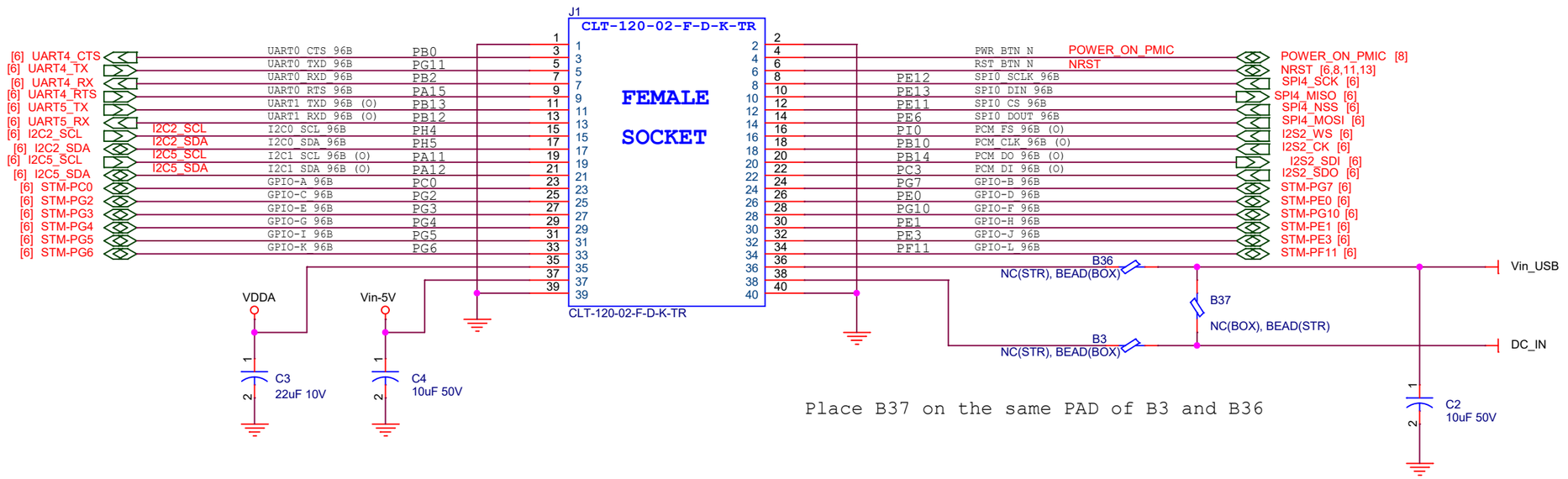
Shiratech Solutions	Stuck Up		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 4 of 16

05

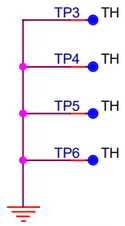




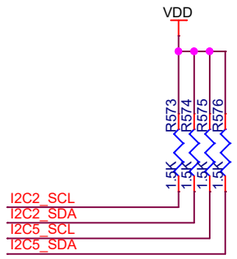
MATING - tmmh-120-05-f-dv-m-tr



Place B37 on the same PAD of B3 and B36



Place 4 TP's at the PCB corners

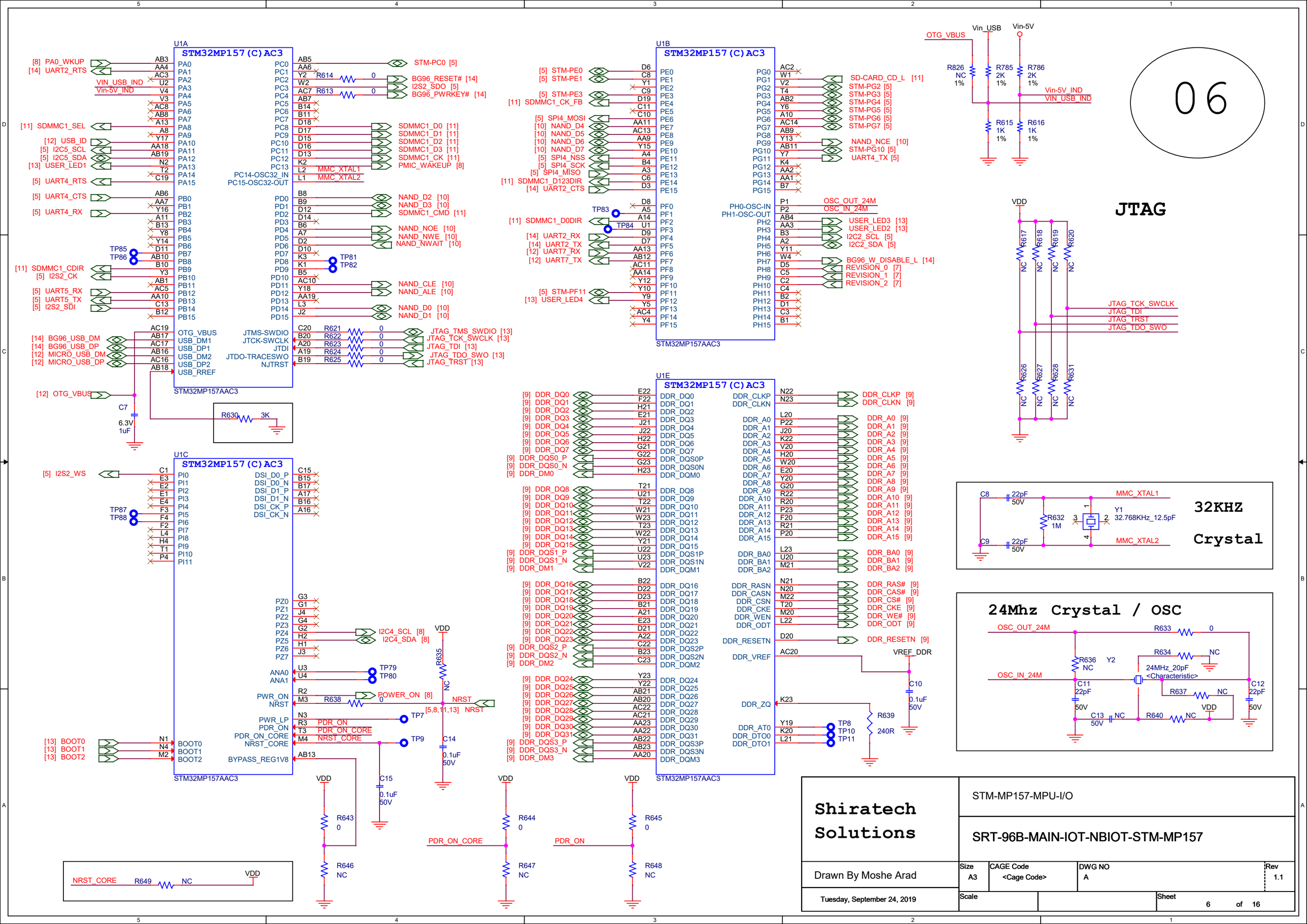


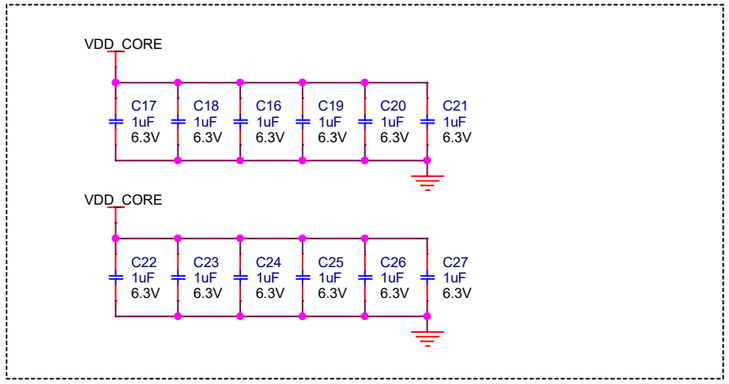
PCB

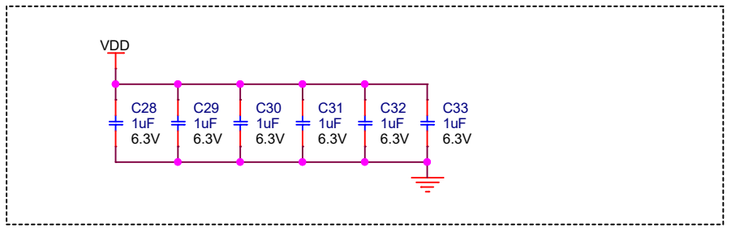
PCB REV 1.2

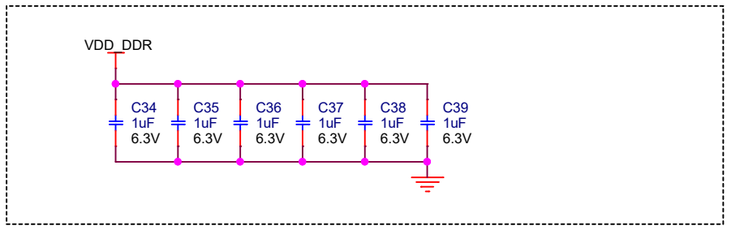
SRT-PCB-01001

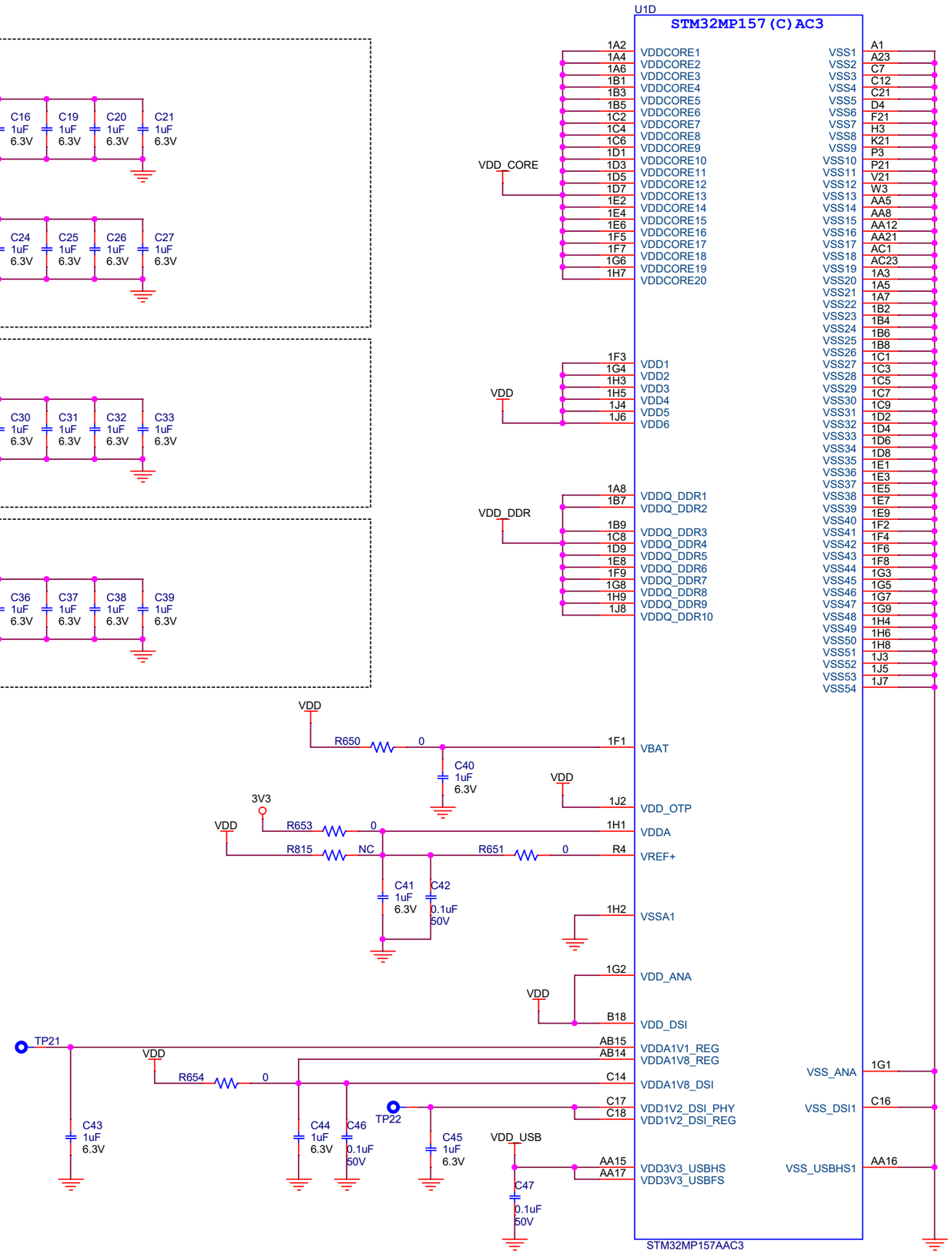
Shiratech Solutions	96Board Expantion Connecto		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Mosha Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 5 of 16

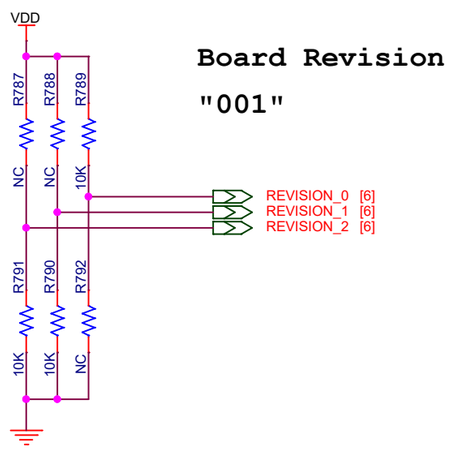

U1A
STM32MP157(C)AC3
STM32MP157AAC3
U1B
STM32MP157(C)AC3
STM32MP157AAC3
U1C
STM32MP157(C)AC3
STM32MP157AAC3
U1E
STM32MP157(C)AC3
STM32MP157AAC3
06
JTAG
32KHZ Crystal
24Mhz Crystal / OSC
Shiratech Solutions
STM-MP157-MPU-I/O
SRT-96B-MAIN-IOT-NBIOT-STM-MP157
Drawn By Moshe Arad
Tuesday, September 24, 2019
Size A3
CAGE Code <Cage Code>
DWG NO A
Rev 1.1
Scale
Sheet 6 of 16





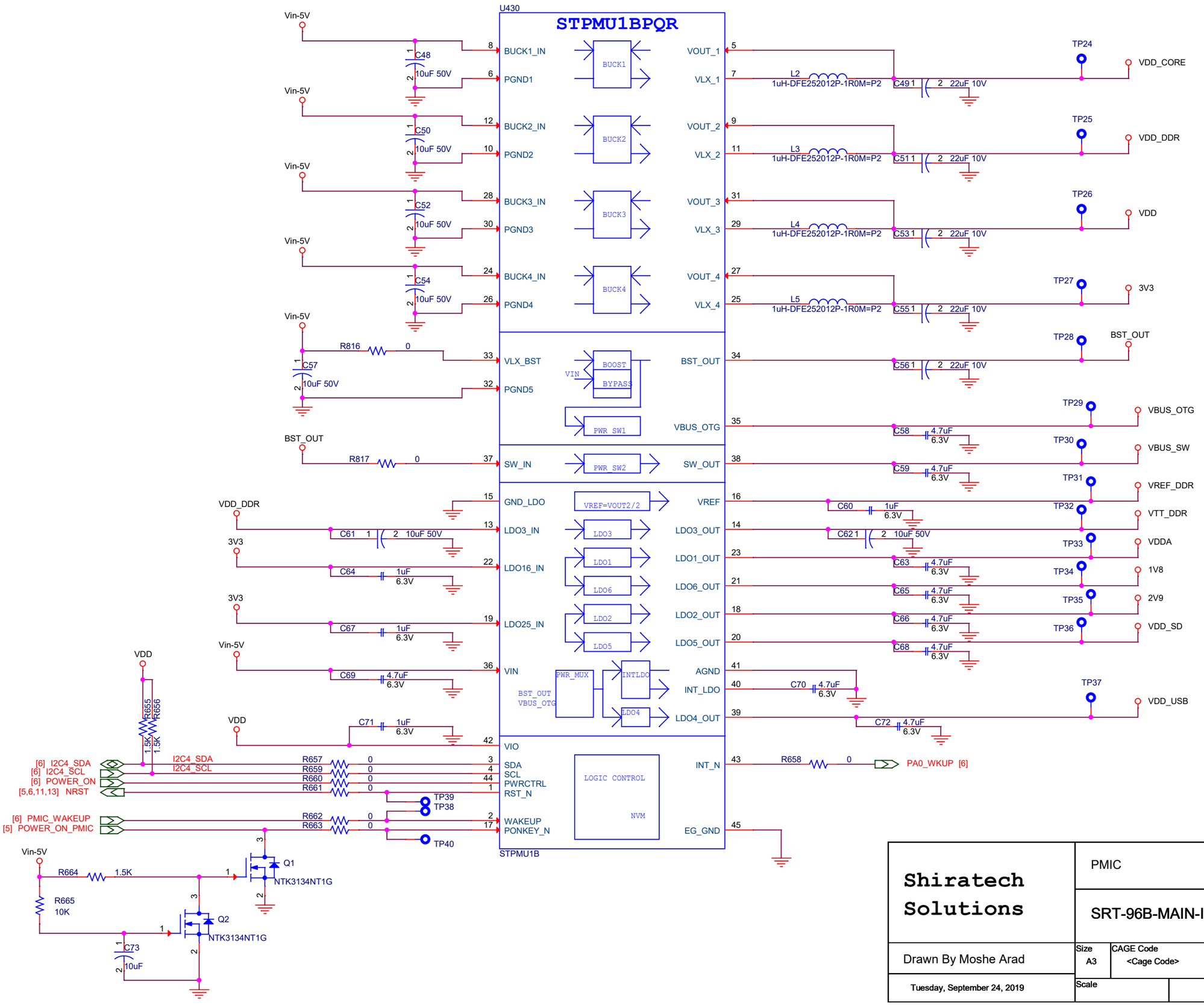






07

Shiratech Solutions	STM-MP157-MPU-POWER		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 7 of 16



A, V, NC

1.5A, 1.2V

1A, 1.1V

0.5A, 1.8V

2A, 3.3V

1.1A, 5.2V

0.5A

1A, NC

0.55V

100mA, 1.8V

350mA, 1.8V

150mA, 1V, NC

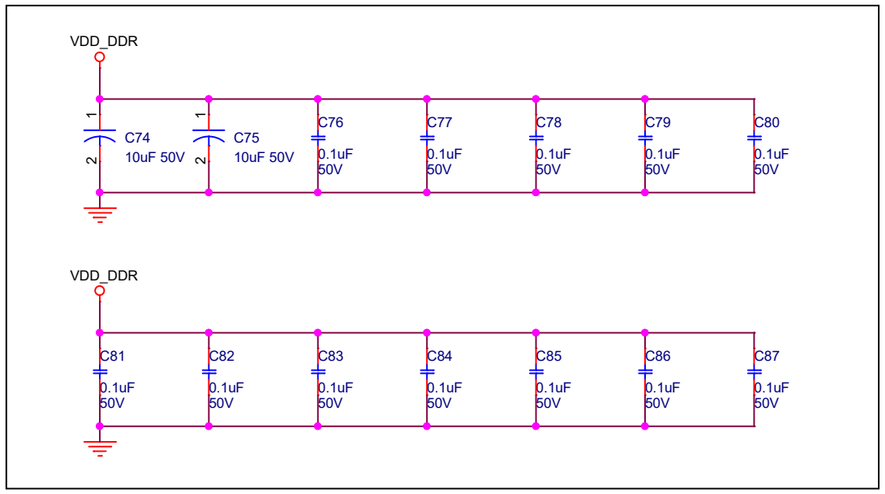
350mA, 2.9V, NC

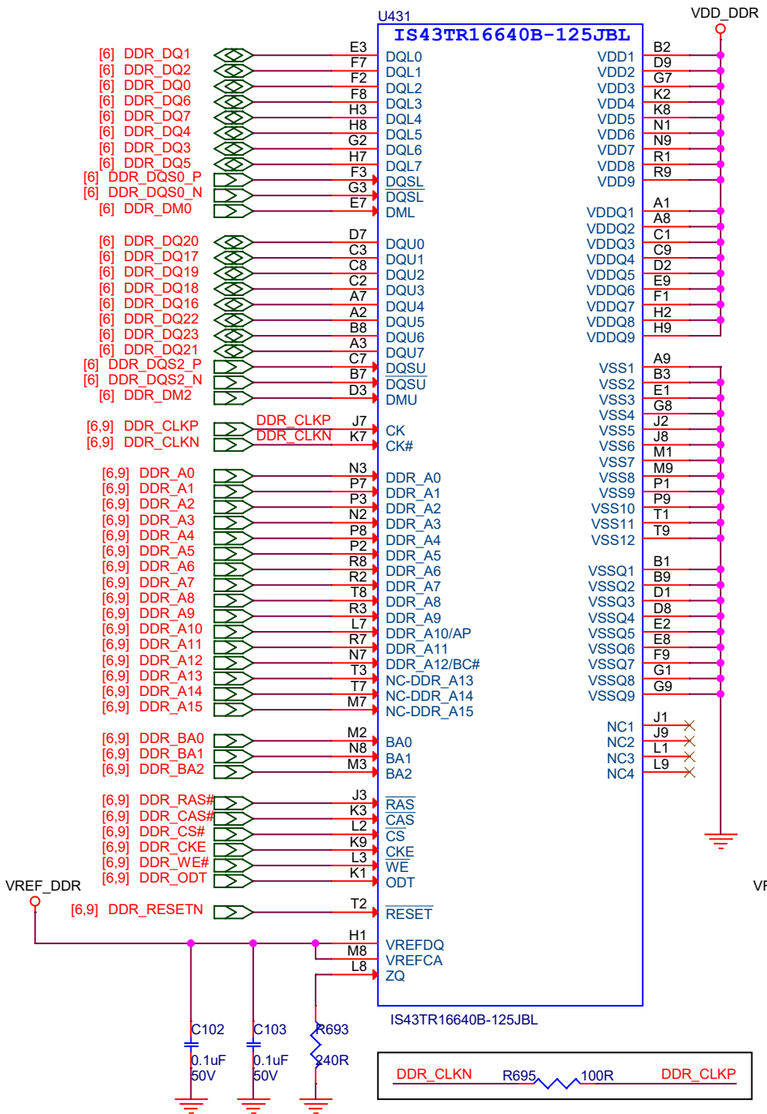
350mA, 2.9V

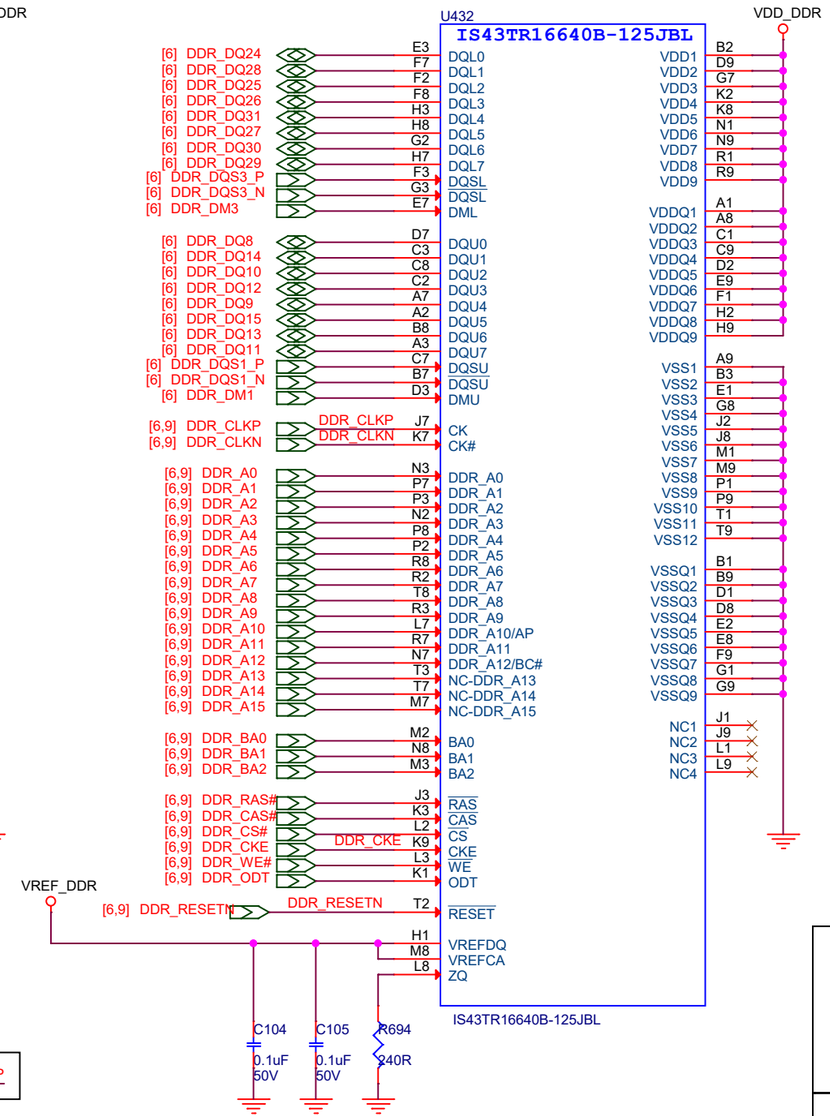
50mA, 3.3V

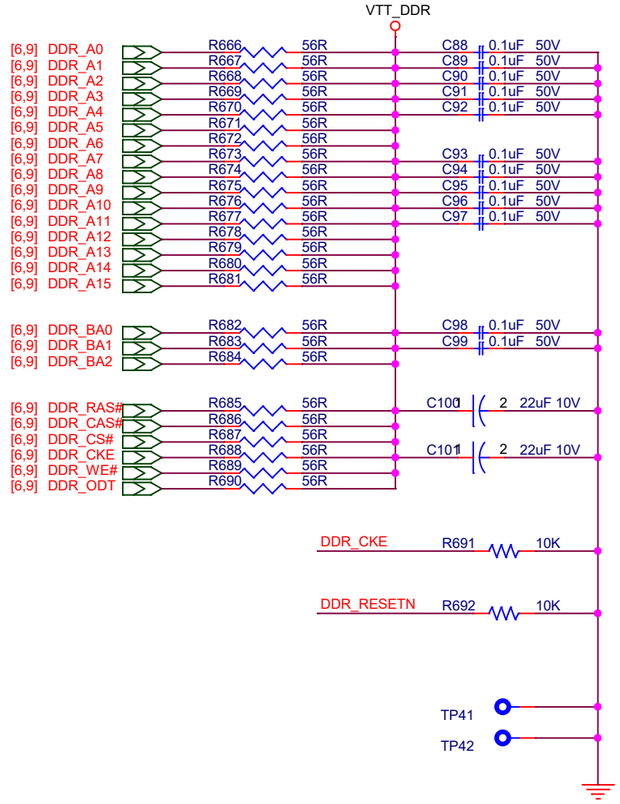
Shiratech Solutions	PMIC		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 8 of 16

09





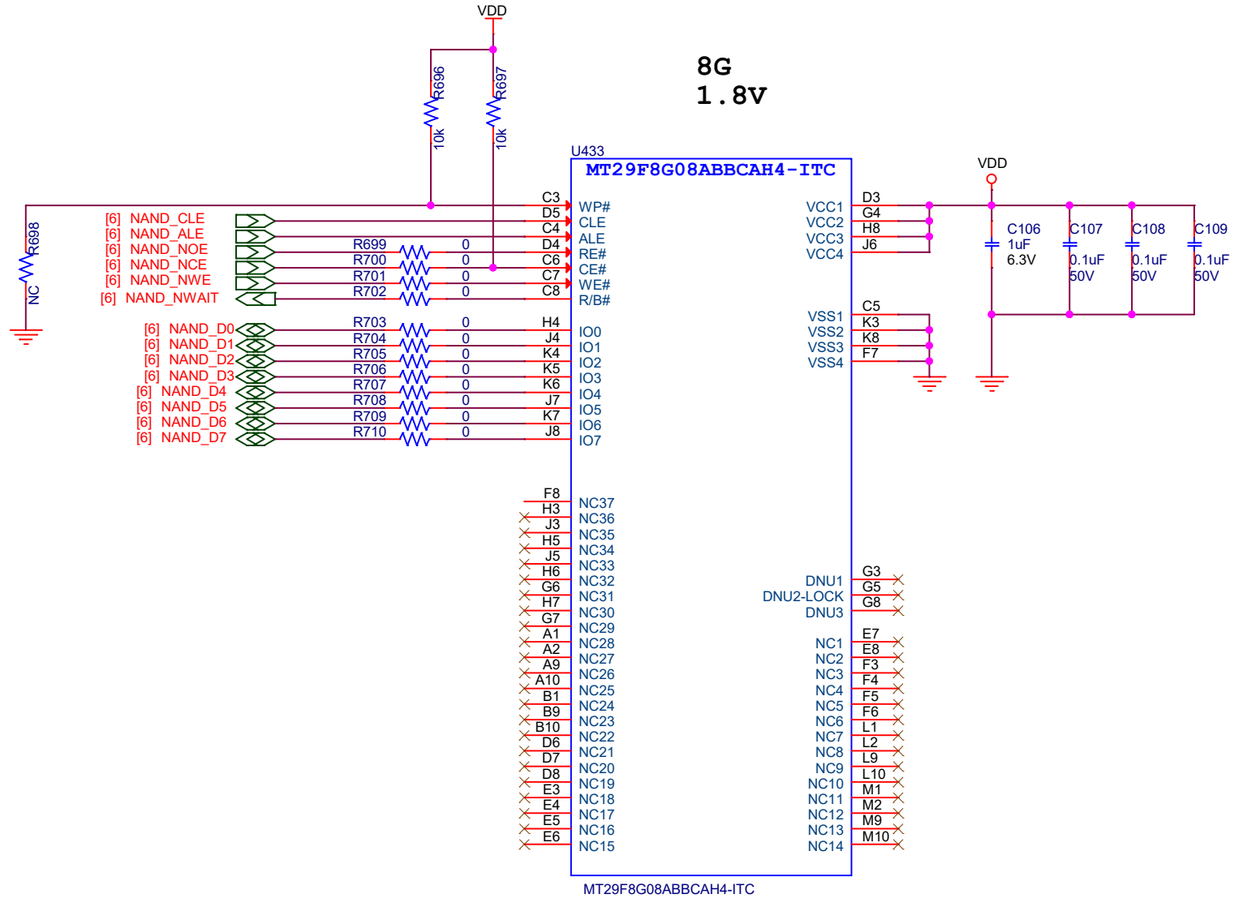




Shiratech Solutions	DDR3		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Wednesday, October 02, 2019	Scale		Sheet 9 of 16

10

8G
1.8V



Shiratech Solutions	NAND FLASH			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 10 of 16	

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VDD
R794 10k
U436
[6] SDMMC1_D0 R805 22R D1 DATA0 DATA0_SD D5 SDMMC_D0_SD
[6] SDMMC1_D1 R806 22R E1 DATA1 DATA1_SD E5 SDMMC_D1_SD
[6] SDMMC1_D2 R807 22R A1 DATA2 DATA2_SD A5 SDMMC_D2_SD
[6] SDMMC1_D3 R808 22R B1 DATA3 DATA3_SD B5 SDMMC_D3_SD
[6] SDMMC1_D0DIR R810 0 A3 DIR_0 CLK_SD C5 SDMMC_CLK_SD
[6] SDMMC1_D123DIR R811 0 E3 DIR_1_3 CMD_SD D4 SDMMC_CMD_SD
[6] SDMMC1_CMD R812 0 D2 CMD WP E4 TP89
[6] SDMMC1_CDIR R813 0 A2 DIR_CMD CD D3 SD-CARD_CD_L
VLDO B4 SDMMC_VLDO
[6] SDMMC1_CK R804 22R C1 CLK_IN VSD_REF C4
[6] SDMMC1_CK_FB R809 22R E2 CLK_FB VCCA B3
VSUPPLY A4
[6] SDMMC1_SEL R814 0 B2 SEL GND C3
C2 ENABLE
IP4856CX25/C
C148 1uF 6.3V
VDD_SD 0 R798
3V3
VDD
R818 NC
C146 0.1uF 50V
C144 0.1uF 50V
C145 0.1uF 50V
R825 NC
R799 10k
R800 NC
C147 NC 50V
R801 10k
R802 10k
R803 10k
VDD
[5,6,8,13] NRST
D17 NC
R795 NC
SDMMC_VLDO
VDD_SD
VDD
R797 NC
R711 NC
R712 NC
R713 NC
R714 NC
R715 NC
R716 NC
[6] SD-CARD_CD_L
Micro SD
J2
SW2-CD
SW1-Common
CASE
SCHA4B0419
ALPS
SDMMC_D1_SD
SDMMC_D0_SD
SDMMC_CLK_SD
SDMMC_CMD_SD
SDMMC_D3_SD
SDMMC_D2_SD
C110 1uF 6.3V
C111 0.1uF 50V

SSD
SDSQUNS-016G-GN3MN
Only for BOM

ESD PROTECTION
CLOSE TO CONNECTOR
D1
SDMMC_D0_SD 1 IO1 NC 8
SDMMC_D1_SD 2 IO2
SDMMC_D2_SD 3 IO3
SDMMC_D3_SD 4 IO4
SDMMC_CMD_SD 6 IO5
SDMMC_CLK_SD 7 IO6
SD-CARD_CD_L 9 IO7
10 IO8 GND 5
VDD_SD
SP3003-08ATG

Shiratech Solutions	SD-CARD		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
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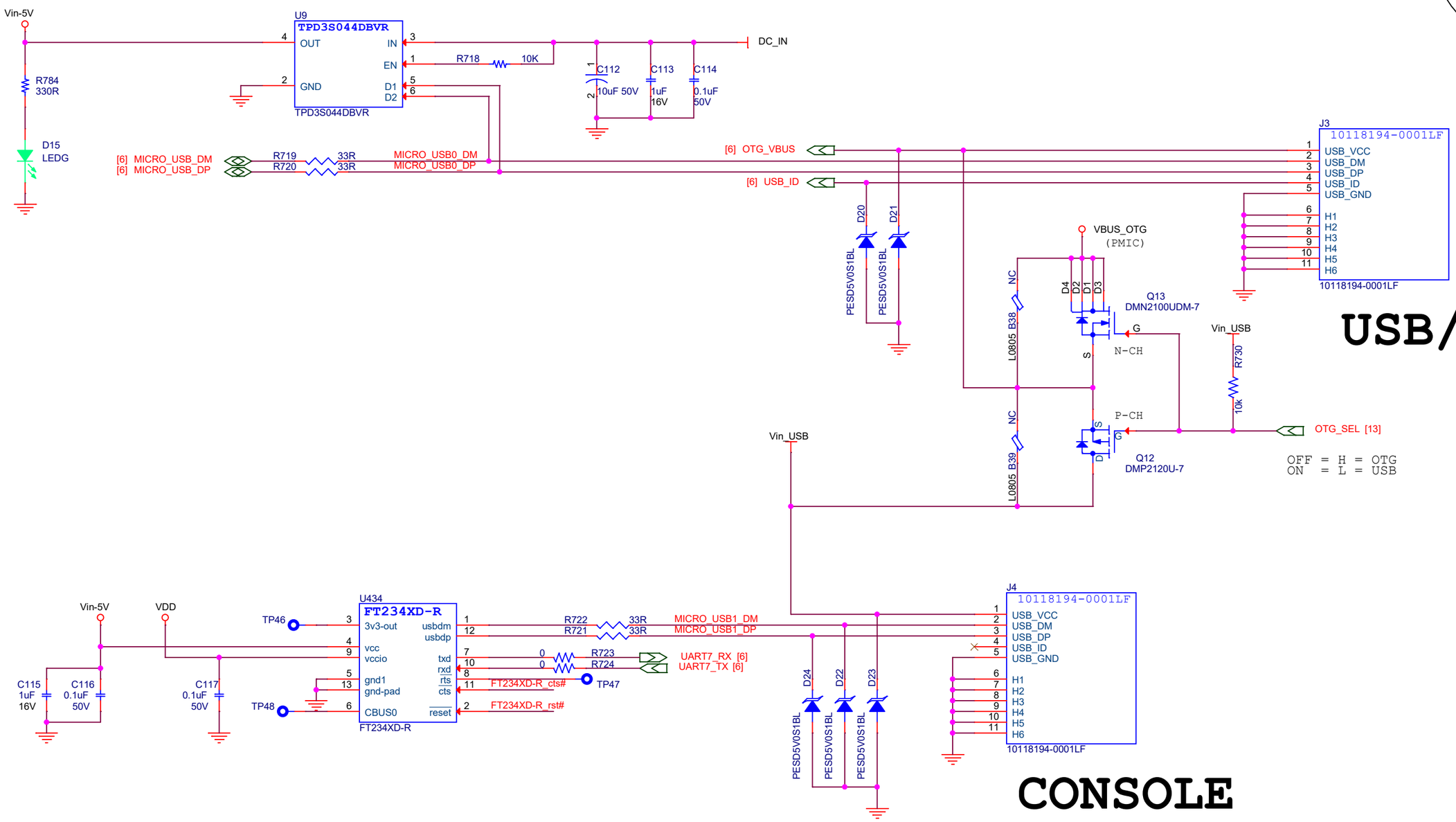
1.5A - MAX



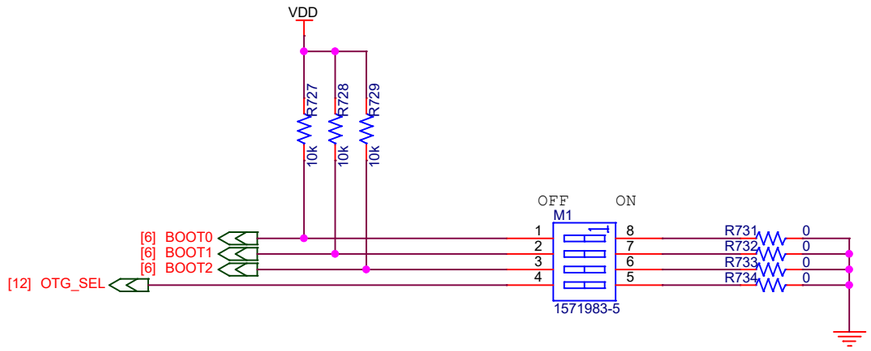
Shiratech Solutions	USB-PORTS			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
Thursday, September 26, 2019	Scale		Sheet 12 of 16	

Table 2. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB high-speed device(2)
0	0	1	Serial NOR Flash(3)	Serial NOR Flash on QUADSPI(4)
0	1	0	e•MMC(3)	e•MMC on SDMMC2 (default)(4)(5)
0	1	1	NAND Flash(3)	SLC NAND Flash on FMC
1	0	0	Reserved (NoBoot)	Used to get debug access without boot from Flash memory
1	0	1	SD card(3)	SD card on SDMMC1 (default)(4)(5)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND Flash(3)	Serial NAND Flash on QUADSPI(4)

1. can be disabled by OTP settings.
2. USB requires 24 MHz HSE clock/crystal if OTP is not programmed for different frequency.
3. Boot source can be changed by OTP settings (e.g. initial boot on SD card, then e•MMC with OTP settings).
4. Default pins can be altered by OTP.
5. Alternatively, another SDMMC1 or SDMMC2 interface than this default can be selected by OTP.

BOOT MODE SEL



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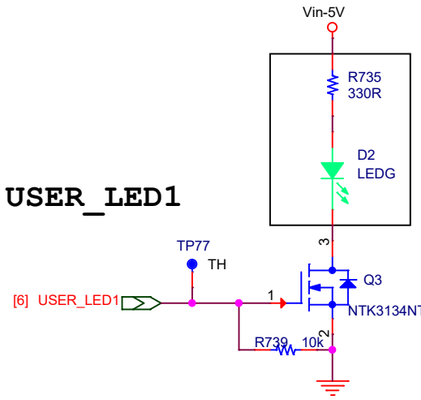
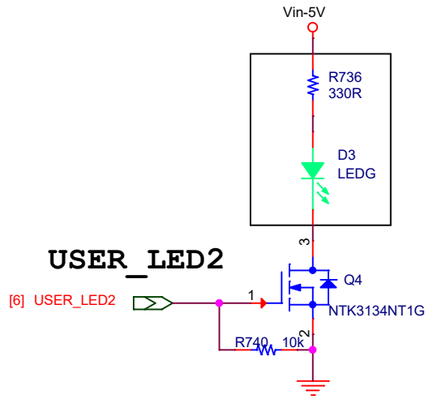
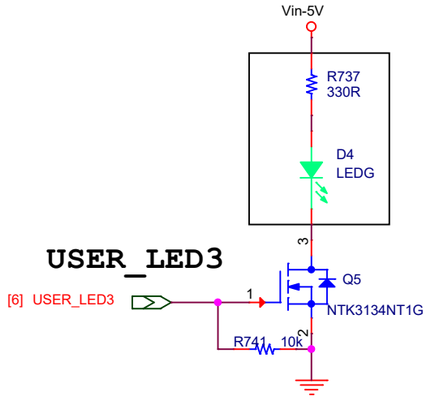
USER_LED1



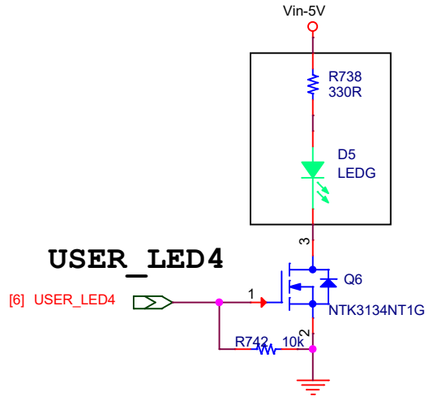
USER_LED2



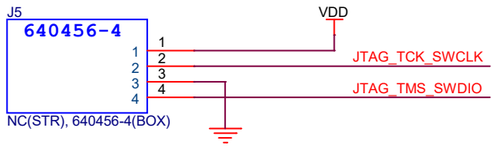
USER_LED3



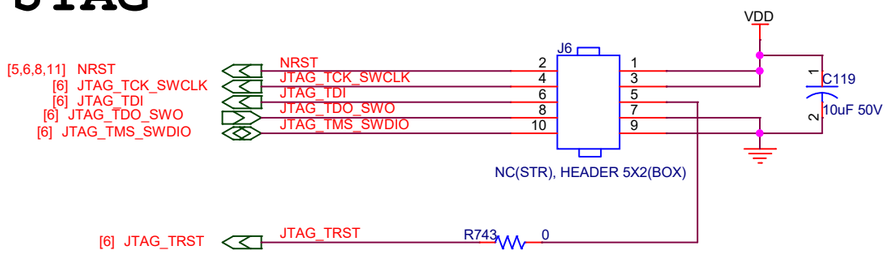
USER_LED4



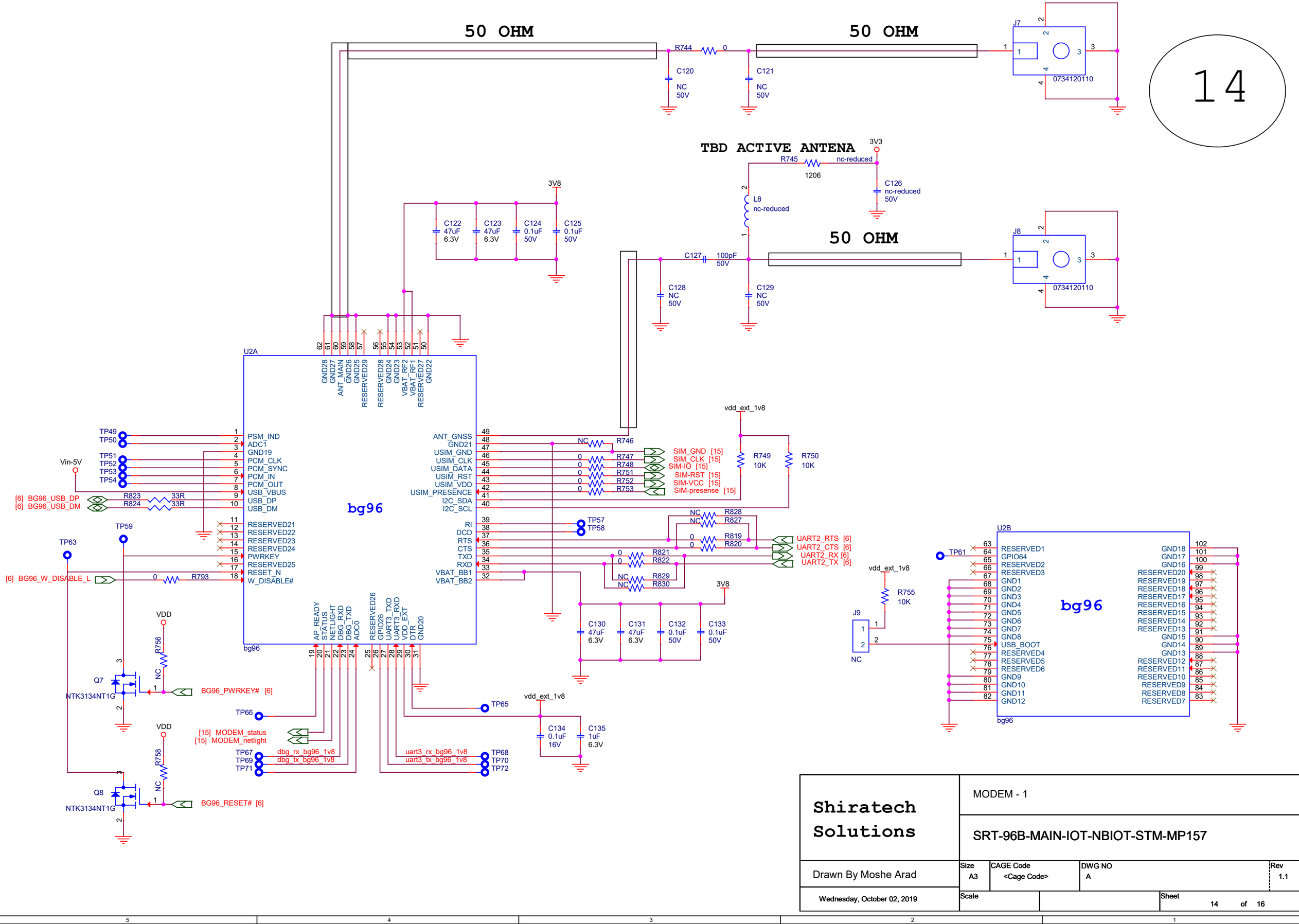
ST-LINK



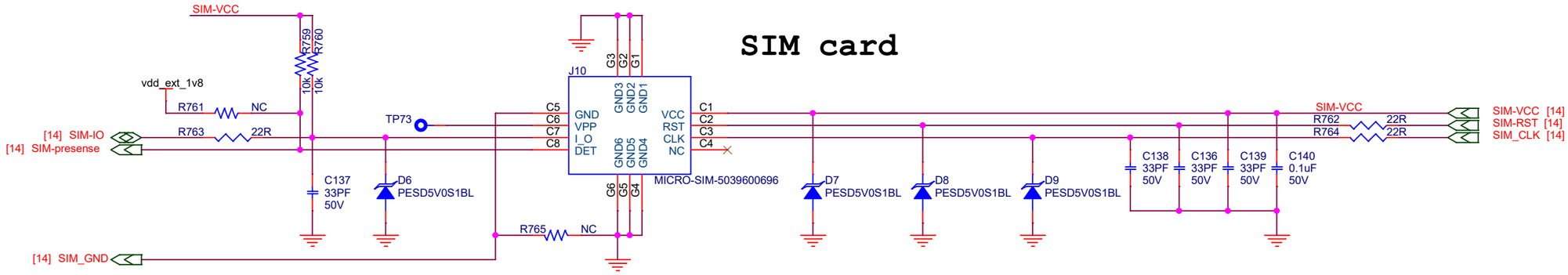
JTAG

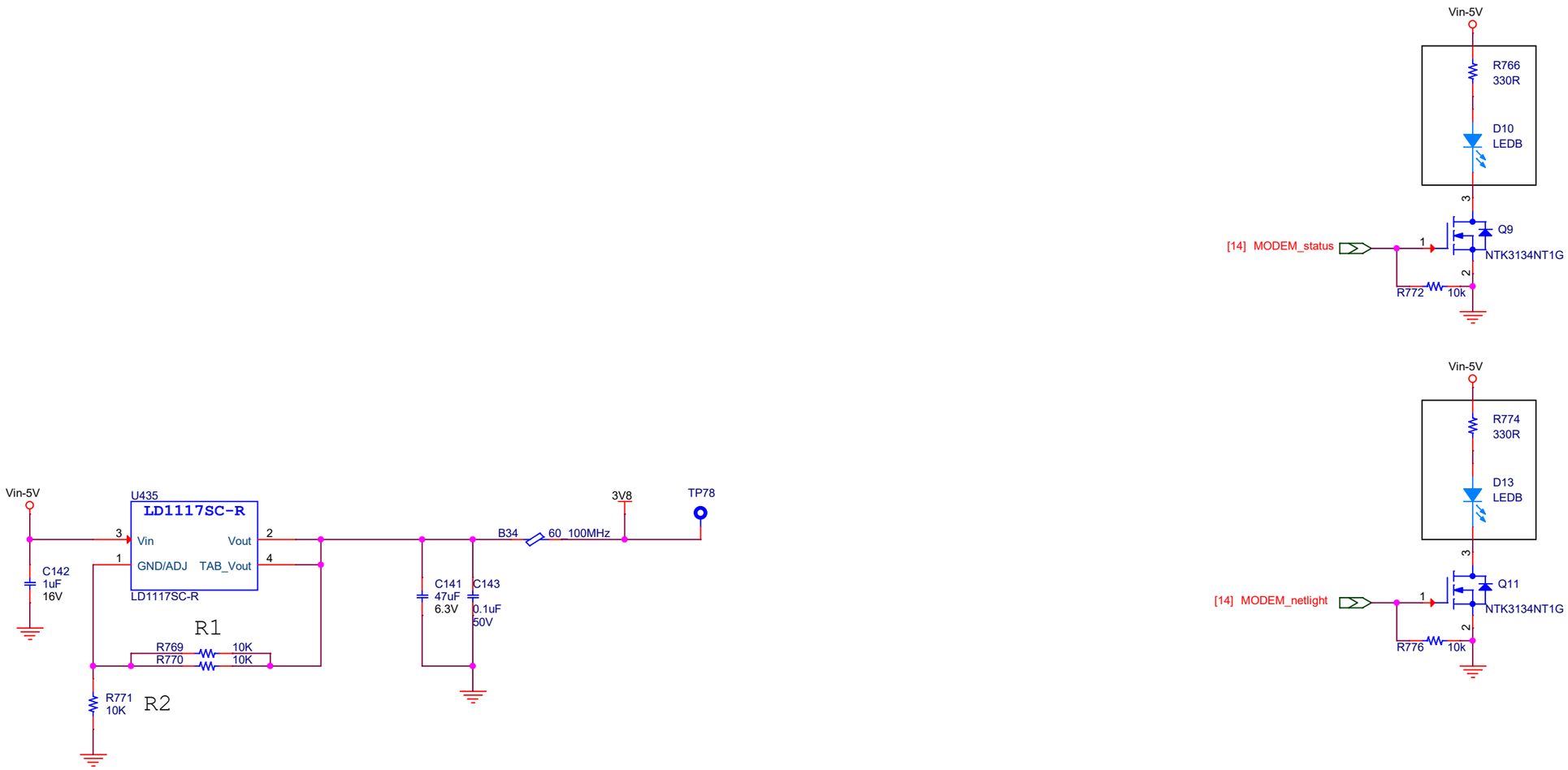


Shiratech Solutions	Peripherals (LEDS, JTAG)		
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
Tuesday, September 24, 2019	Scale		Sheet 13 of 16


50 OHM
50 OHM
R744
0
C120
NC
50V
C121
NC
50V
J7
2
2
1
1
3
3
4
4
0734120110
14
TBD ACTIVE ANTENA
3V3
R745
nc-reduced
1206
C126
nc-reduced
50V
L8
nc-reduced
2
1
50 OHM
J8
C127
100pF
50V
C128
NC
50V
C129
NC
50V
0734120110
3V8
C122
47uF
6.3V
C123
47uF
6.3V
C124
0.1uF
50V
C125
0.1uF
50V
U2A
62 GND28
61 GND27
60 ANT_MAIN
59 GND26
58 GND25
57 RESERVED29
56 RESERVED28
55 GND24
54 GND23
53 VBAT_RF2
52 VBAT_RF1
51 RESERVED27
50 GND22
TP49
TP50
TP51
TP52
TP53
TP54
Vin-5V
1 PSM_IND
2 ADC1
3 GND19
4 PCM_CLK
5 PCM_SYNC
6 PCM_IN
7 PCM_OUT
8 USB_VBUS
9 USB_DP
10 USB_DM
[6] BG96_USB_DP
[6] BG96_USB_DM
R823
33R
R824
33R
11 RESERVED21
12 RESERVED22
13 RESERVED23
14 RESERVED24
15 PWRKEY
16 RESERVED25
17 RESET_N
18 W_DISABLE#
TP59
TP63
[6] BG96_W_DISABLE_L
0
R793
bg96
49 ANT_GNSS
48 GND21
47 USIM_GND
46 USIM_CLK
45 USIM_DATA
44 USIM_RST
43 USIM_VDD
42 USIM_PRESENCE
41 I2C_SDA
40 I2C_SCL
39 RI
38 DCD
37 RTS
36 CTS
35 TXD
34 RXD
33 VBAT_BB1
32 VBAT_BB2
NC
R746
0
R747
0
R748
0
R751
0
R752
0
R753
SIM_GND [15]
SIM_CLK [15]
SIM-IO [15]
SIM-RST [15]
SIM-VCC [15]
SIM-presense [15]
R749
10K
R750
10K
vdd_ext_1v8
TP57
TP58
NC
R828
NC
R827
0
R819
0
R820
UART2_RTS [6]
UART2_CTS [6]
UART2_RX [6]
UART2_TX [6]
0
R821
0
R822
NC
R829
NC
R830
3V8
C130
47uF
6.3V
C131
47uF
6.3V
C132
0.1uF
50V
C133
0.1uF
50V
AP_READY 19
STATUS 20
NETLIGHT 21
DBG_RXD 22
DBG_TXD 23
ADC0 24
RESERVED26 25
GPIO26 26
UART3_TXD 27
UART3_RXD 28
VDD_EXT 29
DTR 30
GND20 31
TP66
[15] MODEM_status
[15] MODEM_netlight
TP67
TP69
TP71
dbg_rx_bg96_1v8
dbg_tx_bg96_1v8
uart3_rx_bg96_1v8
uart3_tx_bg96_1v8
TP68
TP70
TP72
TP65
vdd_ext_1v8
C134
0.1uF
16V
C135
1uF
6.3V
VDD
R756
NC
Q7
NTK3134NT1G
BG96_PWRKEY# [6]
VDD
R758
NC
Q8
NTK3134NT1G
BG96_RESET# [6]
U2B
TP61
vdd_ext_1v8
R755
10K
J9
1
2
NC
63 RESERVED1
64 GPIO64
65 RESERVED2
66 RESERVED3
67 GND1
68 GND2
69 GND3
70 GND4
71 GND5
72 GND6
73 GND7
74 GND8
75 USB_BOOT
76 RESERVED4
77 RESERVED5
78 RESERVED6
79 GND9
80 GND10
81 GND11
82 GND12
bg96
GND18 102
GND17 101
GND16 100
RESERVED20 99
RESERVED19 98
RESERVED18 97
RESERVED17 96
RESERVED16 95
RESERVED15 94
RESERVED14 93
RESERVED13 92
GND15 91
GND14 90
GND13 89
RESERVED12 88
RESERVED11 87
RESERVED10 86
RESERVED9 85
RESERVED8 84
RESERVED7 83
Shiratech Solutions
MODEM - 1
SRT-96B-MAIN-IOT-NBIOT-STM-MP157
Drawn By Moshe Arad
Wednesday, October 02, 2019
Size A3
CAGE Code <Cage Code>
DWG NO A
Rev 1.1
Scale
Sheet 14 of 16

SIM card





Vout = 1.25(1+R2/R1)

Shiratech Solutions	MODEM - 2			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
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LEFT FOR MISC AND FUTURE REMARKS

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Shiratech Solutions	MISC			
	SRT-96B-MAIN-IOT-NBIOT-STM-MP157			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
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