MM Assignment -2

02 April 2020

1.

Microprocessor	Microcontroller
* It is on IC which has only CPU inside them it doesn't have RAM, ROM and other peripheral on the chip	* It has CPU, in addition to it RAM, ROM and other peripherals
* A system designer has to add them externally	* No need to add externally
* It finds application where tasks are unspecific	* These are designed to perform specific tasks
* Relationship b/w input and output is not defined	* Here it is defined
* Expensive than microcontroller	* Cheaper than MP

2. ARM uses a modified RISC design philosophy that also that also targets good code destiny and low power consumption. An embedded system consists of a processor core surrounded by caches, memory and peripherals. The system is controlled by OS that manages application tasks. This improves performance by reducing the complexity of instructions, to speed up instruction processing by using a pipeline, to provide a large register set to store data near the core, and to use a load store architecture.

Embedded system includes ARM processors that are found embedded in chips. Programmers access peripherals through memory mapped registers.

It has a controller which is used to configure higher level functions such as memory and interrupts. It also includes software components. Initialization code configures the hardware to a known state. Once configured, OS can be loaded and executed. Device drivers provide a standard interface to peripherals.

3. RISC philosophy concentrates on reducing the complexity of instructions performed by the hardware because it is easier to provide greater flexibility and intelligence in software rather than hardware.

It is implemented with four major design rules:

i) Instructions: RISC-processors have a reduced number of instruction classes. These classes provide simple operations that can each execute in a single cycle. The instruction has a fixed length to allow the pipeline to fetch future instructions before decoding current instruction

ii) Pipelines: The processing of instructions is broken down into smaller units that can be executed in parallel by pipelines

iii) Registers: Act as the fast local memory store for all data processing operations

iv) Load store architecture: Load and store instructions transfer data between the register bank and external memory. This when loaded and stored separately has an advantage as it can provide multiple tasks.

4. 4th answer is nearly equivalent to 2nd answer.
as ARM embedded system use ARM design philosophy

5. The features the ARM processor includes are:
i) Load/store architecture: The ARM processor loads and stores the data input separately between the register bank and the memory as it can provide multiple tasks while loading and storing
ii) An orthogonal instruction set: All instruction types can use all addressing modes. The instruction type and the addressing mode vary independently It does not impose a limitation that requires a certain instruction to use a specific register so there is little overlapping of instruction functionality
iii) Single cycle execution: CPU executes each instruction in one cycle.
iv) Enhanced power saving: The ARM having 64 and 32 bit execution states can change the modes in order to power saving while executing the codes.

6. It has 1 register with 32 bit capacity hold either data or an address and are identified with letter r prefixed to register number. Registers r0 to r15 are data registers visible to programmer and 2 processor status registers CPSR, SPSR. The three registers r13, r14, r15 are assigned a particular task. They are special purpose registers
- r13 - used as stack pointer to store start of stack
r14 - used as link register to store return address whenever it calls a subroutine
r15 - used as program counter to store address of next instruction.
r0 to r13 are orthogonal

These are the ARM register sets

7. CPSR is a dedicated 32 bit register resides in register file, used to monitor and control internal operation. It has 4 fields each 8 bit wide flag, status, extension and control.

The control field (8 bits) contains processor mode (5 bits, 0 to 4) state (T, 5th bit and T=1 Thumb state T=0 ARM state) and interrupt masks bits (I, F, 7, 6 bits for masking IRQ, FIQ)

The flag field contains 5 condition flags and one J field, status and extension field are not used

C (Carry) : To indicate generation of carry

V (Overflow): To indicate overflow

Q (Saturation) : To indicate saturation in result.

Flags (8)						Status (8)	Extension (8)	Control (8)			
N	Z	C	V	Q	J			I	F	T	Processor mode
31	30	29	28	27	24	16	15	7	6	5	4 0

8. The processor cannot execute ARM instructions. The Thumb instruction set is a subset of the ARM instruction set, reencoded to 16 bits. The programming model has 7 modes that is ARM processor will be in these modes.

i) Supervisor mode: When the user switches on it will be in supervisor mode

ii) User mode: While programming the user must code in user mode

iii) System call mode:

iv) FIQ: Fast Interrupt mode

v) IRQ mode: It has normal interrupt IRQ and software interrupt IRQ modes

vi) Undefined mode: The mode will be undefined it can either be supervisor mode or user mode

vii) Abort mode: Halting of the debugging.

(9,10) Same question It enhances the processor speed

1st	Instruction	execution phase
2nd	Instruction	decoding phase
3rd	Instruction	fetch phase.

... The execution phase fetches the data and decodes the data and executes the code or the program

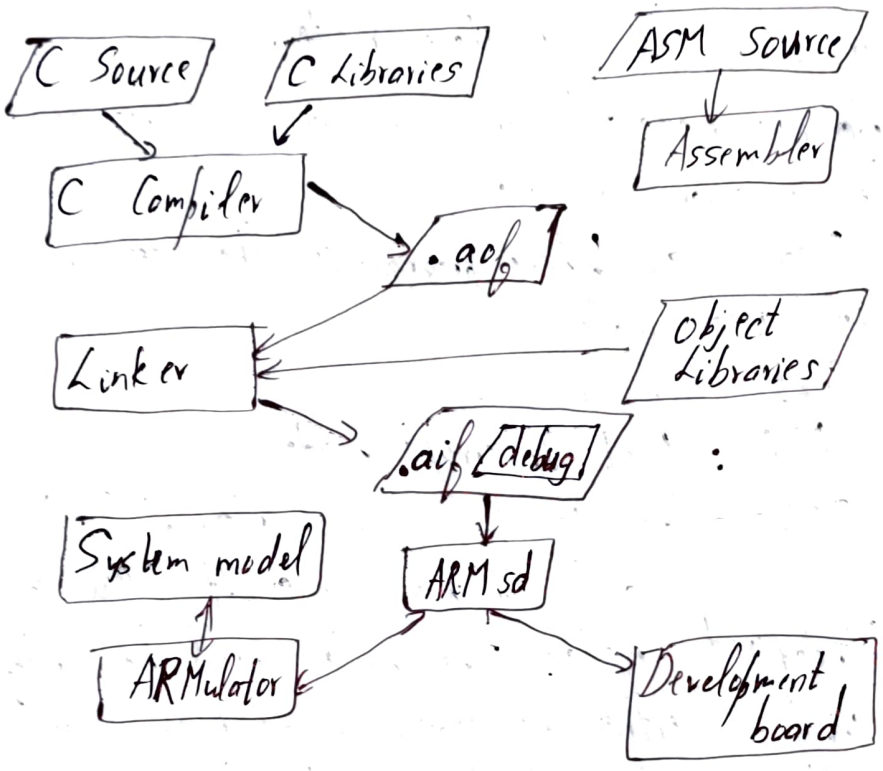
The decoding phase is used to decode the fetched data.

The fetch phase fetches the data from the user

When the first instruction is fetched and decoded during the decoding period of 1st instruction the 2nd instruction is fetched. When 2nd instruction enters decode phase 3rd instruction is fetched at the same time

11. 11th question same as 6th questions.
Registers under various modes are the register sets under ARM

12.

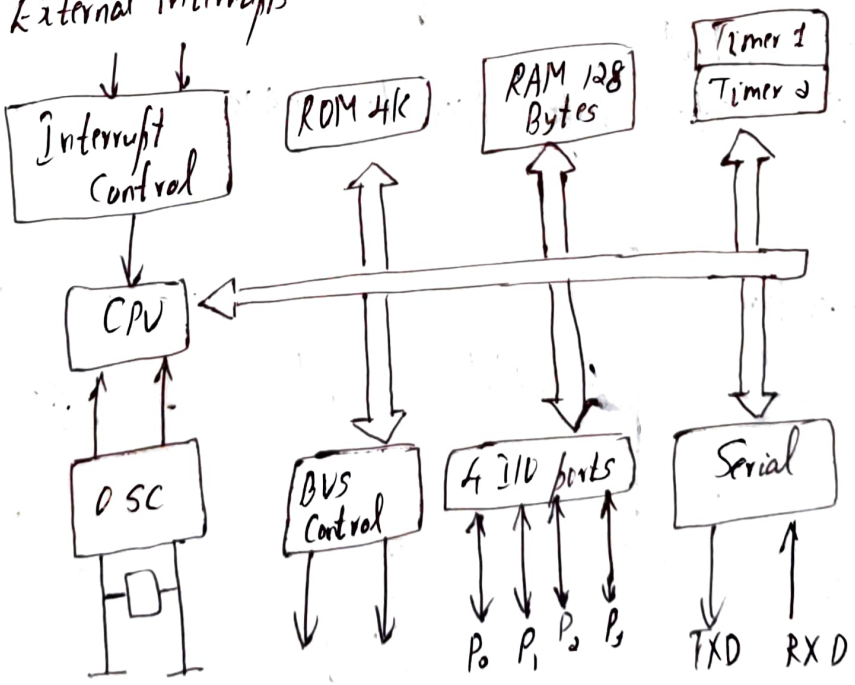


→ C Compiler produces arm object format, assembly source output, thumb code
→ Assembler can be linked with compiler output
→ Linker resolves symbolic references between object files.
→ ARMsd - ARM symbolic debugger, used in debugging embedded cores
→ ARMulator - It models the behaviour of ARM processor core in software on a host system
→ Development board has an ARM core, Memory components, Programmable devices.

13. Among all the 37 registers in register file. 20 are hidden from a program at different times and these 20 registers are called banked registers.
These registers are available only when the processor is in particular mode.
The processor modes except user mode can be changed by writing mode bits of the CPSR register, have a set of banked registers that are subset of main 16 register.
This register maps one-to-one onto a user mode register when you change processor mode. The user mode registers are not affected by the instruction referencing these registers

SPSR_fiq Banked registers are identified by an underline character post fixed to mode mnemonic

14, 15 Same

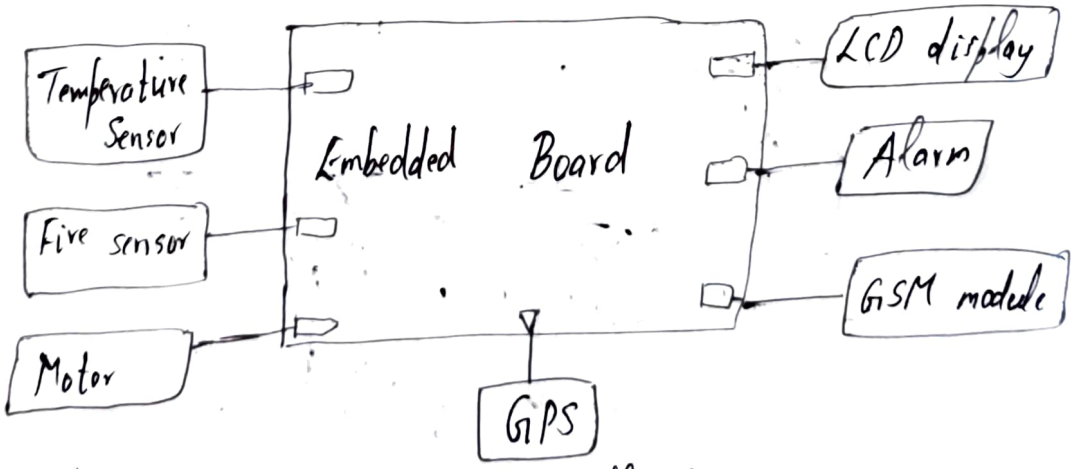


16. The Instruction set is a part of computer that pertains to programming, which is basically machine language. It provides commands to the processor, to tell it what it needs to do. It consists of addressing modes, instructions, native data types, registers, memory architecture, interrupt and exception handling, and external I/O. It can be built into the hardware of the processor, or it can be emulated in software, using an interpreter.

examples:

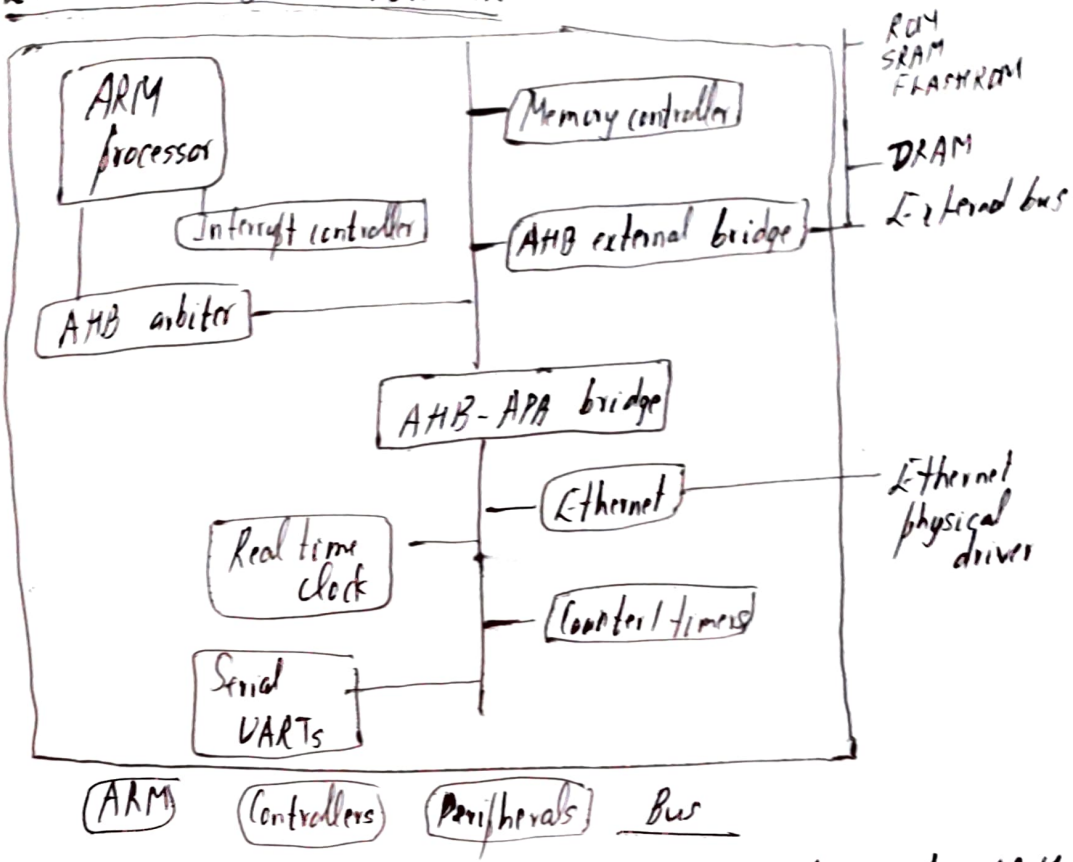
ADD - to add two numbers together
COMPARE - compare numbers
IN - Input information
LOAD - Load information from RAM to CPU
OUT - Output
STORE - Store information to RAM

18.



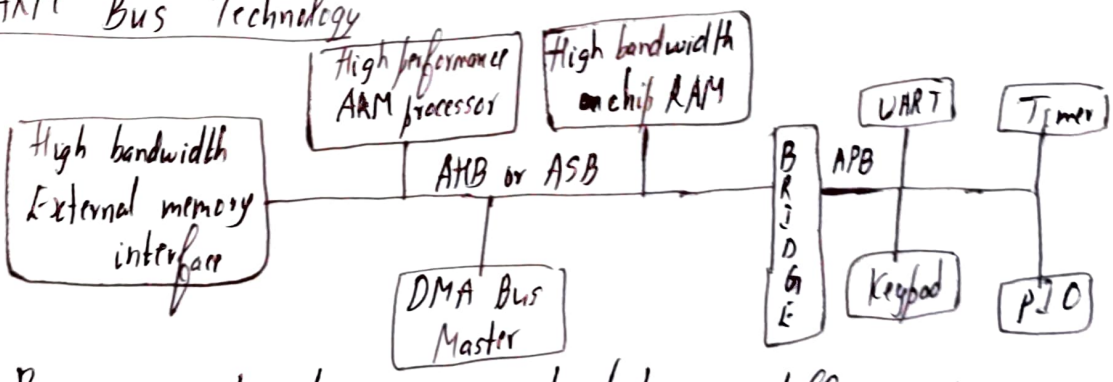
It has temperature sensor to tell the exact temperature
Fire sensor to sense the heat if it exceeds the required temperature
GPS to track location. etc,

17. Embedded system hardware



ARM processor controls the embedded device. An ARM processor comprises a core plus the extensions interface it with a bus.

ARM Bus Technology



Bus is used to communicate between different parts of the Device

AMBA stands for Advanced Microcontroller BUS Architecture.

AMBA AHB and ASB

High performance
Pipelined operation
Multiple Bus masters

AMBA APB

Low power
Simple interface
Suitable for many peripherals