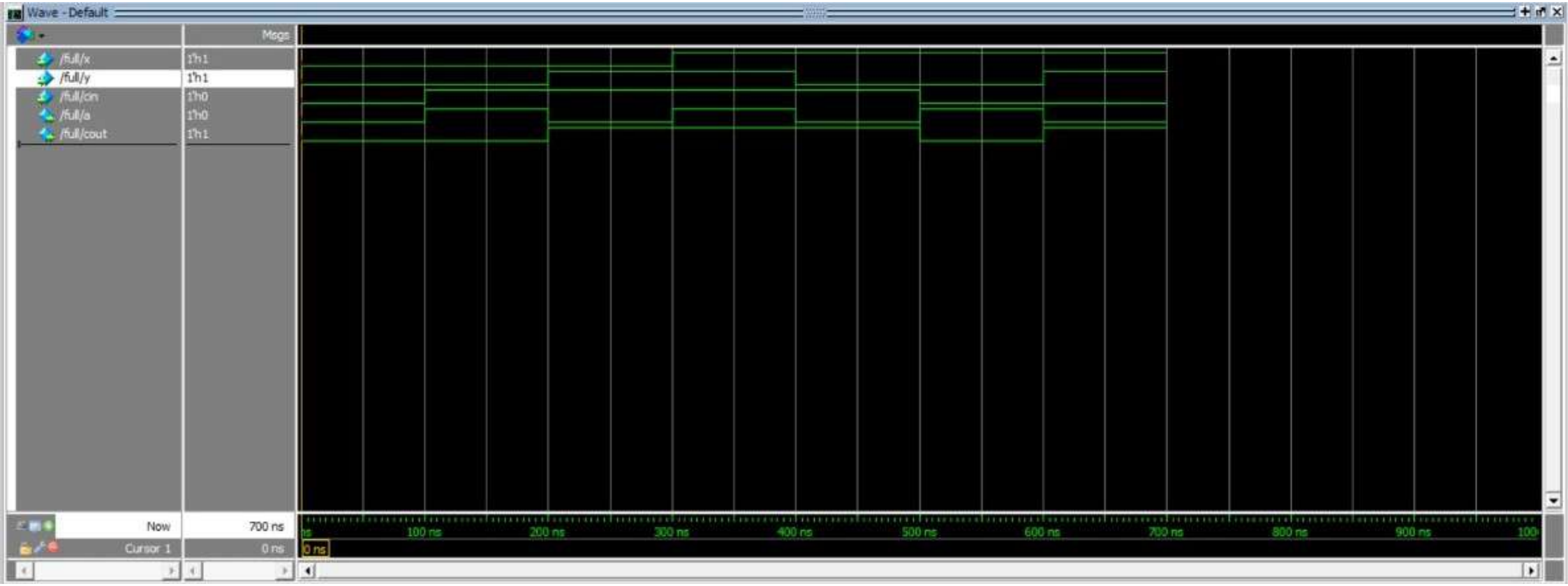
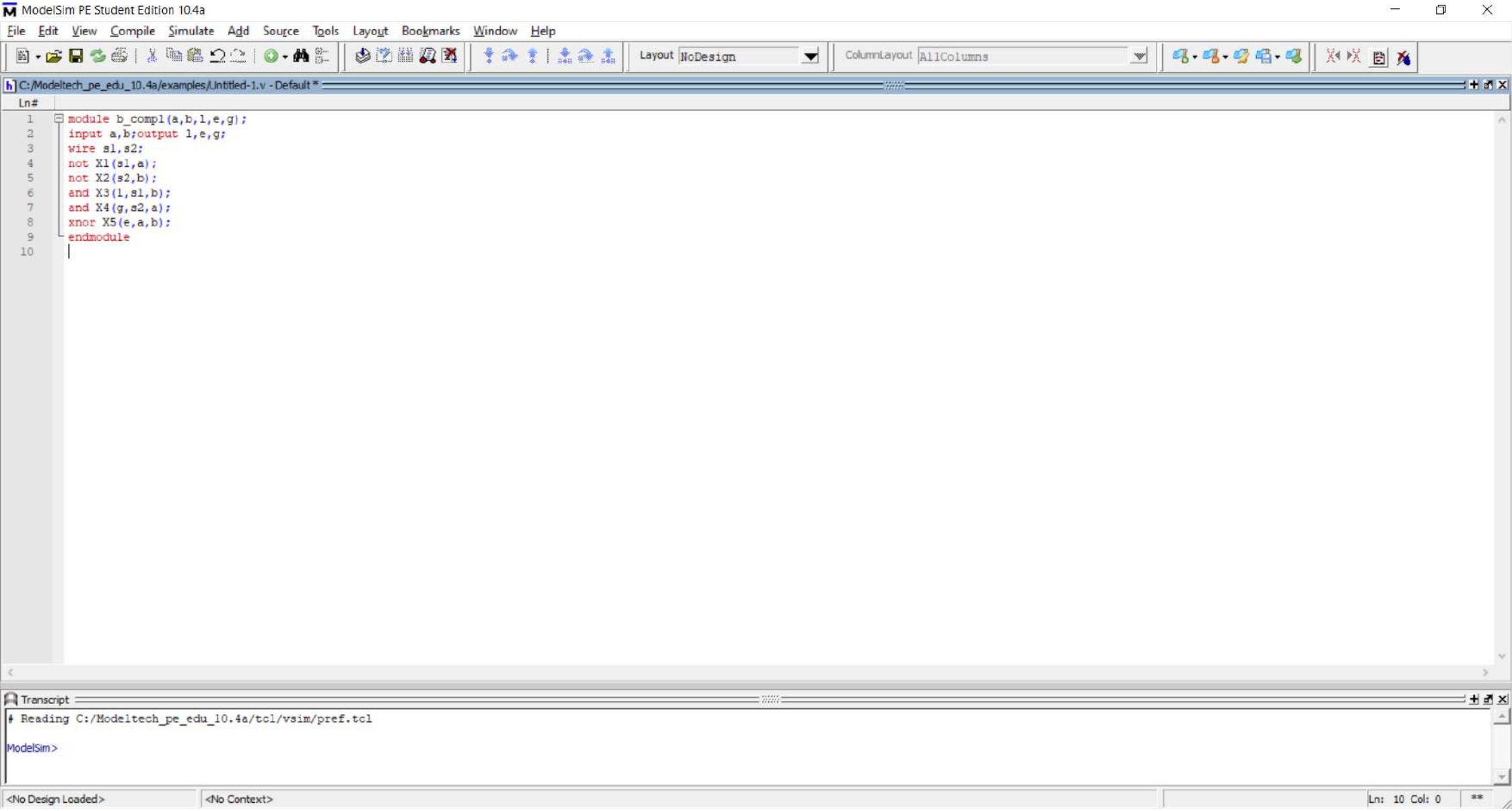
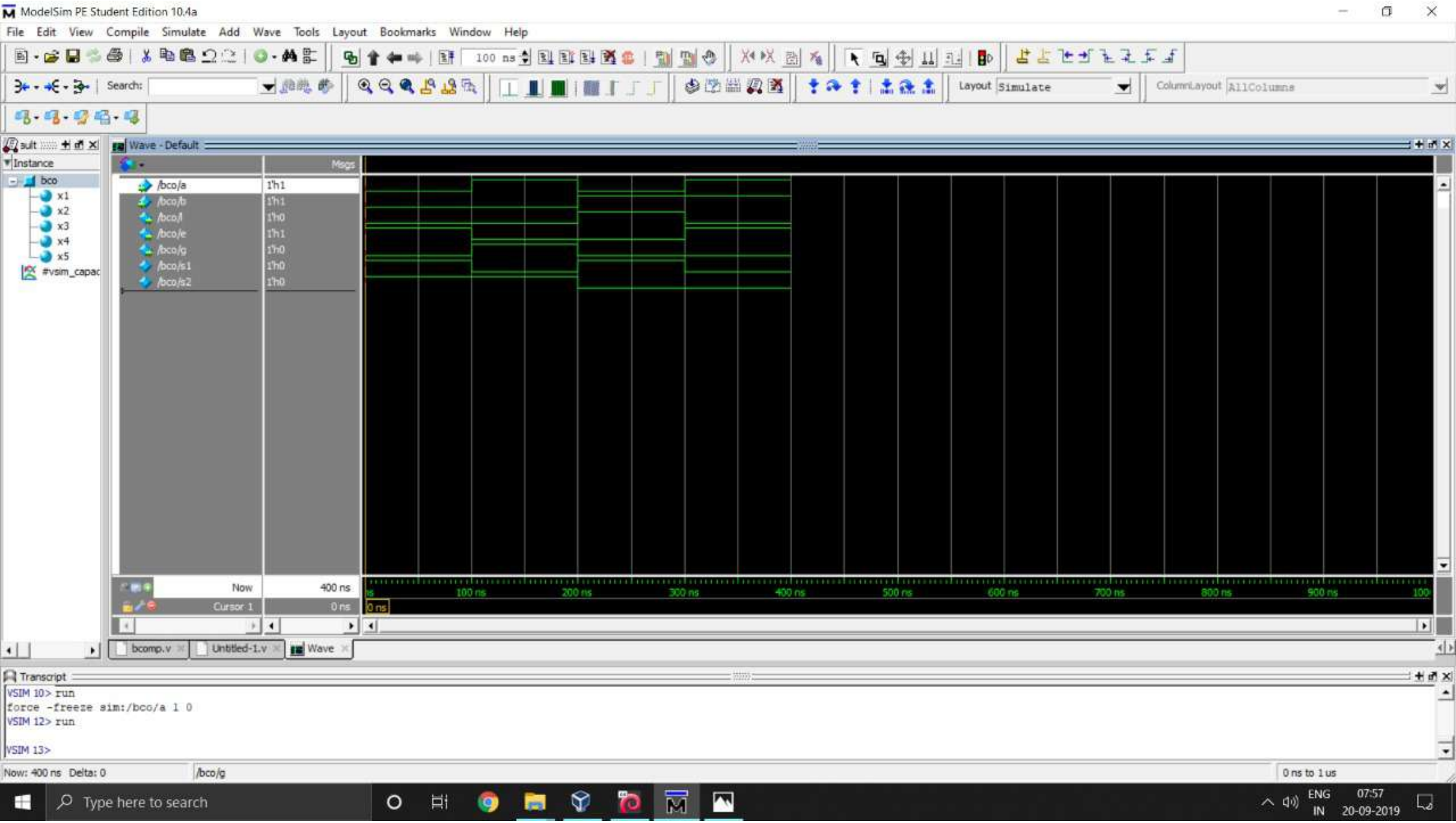
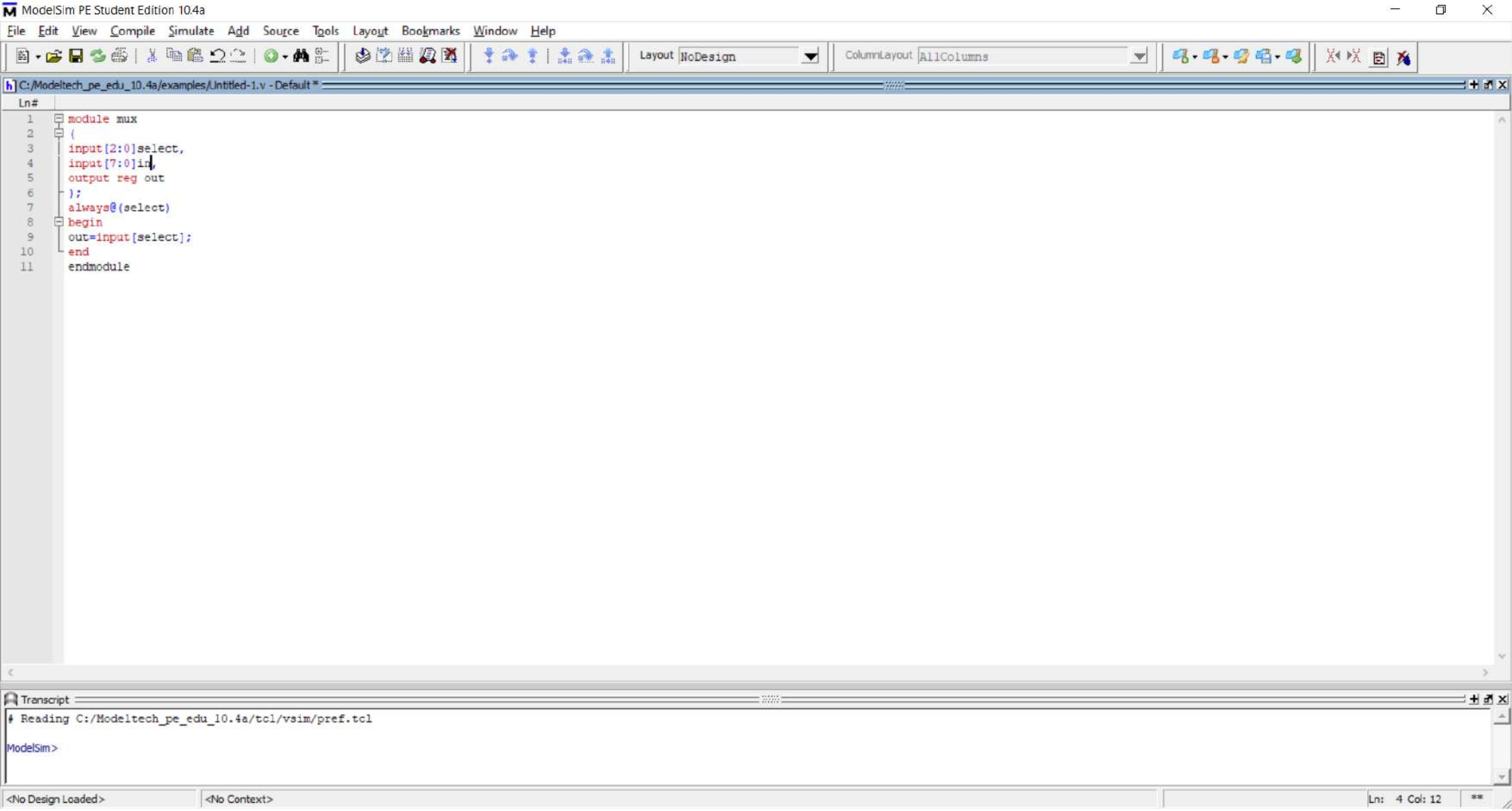
C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *

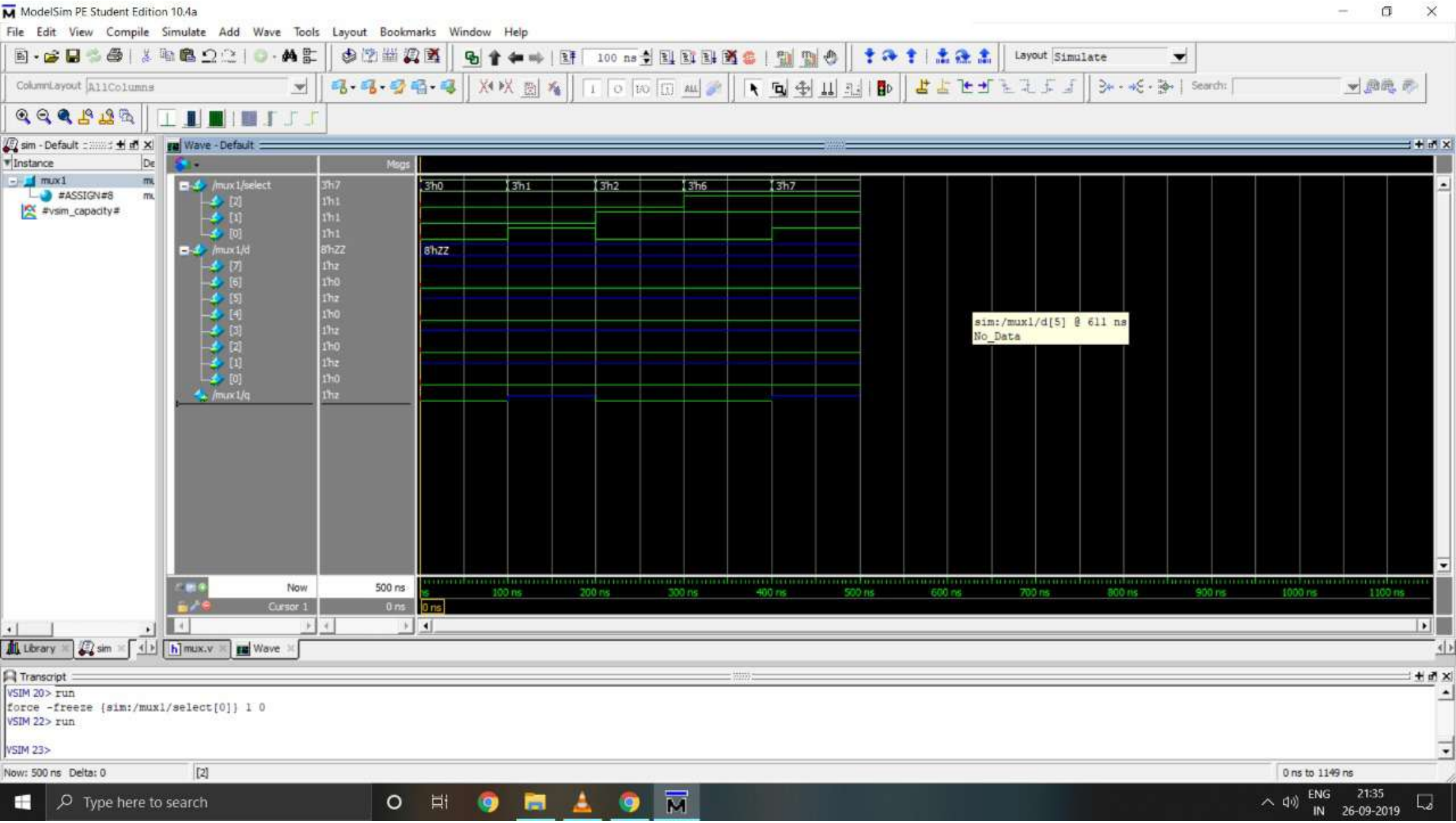
```
Ln#
 1  module fulladder
 2  (
 3  input x,
 4  input y,
 5  input cin,
 6  output A,
 7  output cout
 8  );
 9  assign{cout,A}=cin+y+x;
10  endmodule
```


Wave - Default
Msgs
/full/x
/full/y
/full/cin
/full/a
/full/cout
1'h1
1'h1
1'h0
1'h0
1'h1
Now
700 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
0 ns


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *
Ln#
1 module b_compl(a,b,l,e,g);
2 input a,b;output l,e,g;
3 wire s1,s2;
4 not X1(s1,a);
5 not X2(s2,b);
6 and X3(l,s1,b);
7 and X4(g,s2,a);
8 xnor X5(e,a,b);
9 endmodule
10
Transcript
Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl
ModelSim>
<No Design Loaded>
<No Context>
Ln: 10 Col: 0


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Instance
bco
x1
x2
x3
x4
x5
Msgs
/bco/a 1'h1
/bco/b 1'h1
/bco/f 1'h0
/bco/e 1'h1
/bco/g 1'h0
/bco/s1 1'h0
/bco/s2 1'h0
Now 400 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
bcomp.v
Untitled-1.v
Wave
Transcript
VSIM 10> run
force -freeze sim:/bco/a 1 0
VSIM 12> run
VSIM 13>
Now: 400 ns Delta: 0
/bco/g
0 ns to 1 us
Type here to search
ENG
IN
07:57
20-09-2019


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *
Ln#
1 module mux
2 (
3 input[2:0]select,
4 input[7:0]in,
5 output reg out
6);
7 always@(select)
8 begin
9 out=input[select];
10 end
11 endmodule
Transcript
Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl
ModelSim>
<No Design Loaded>
<No Context>
Ln: 4 Col: 12


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
mux1
#ASSIGN#8
#vsim_capacity#
Wave - Default
Msgs
/mux1/select
[2]
[1]
[0]
/mux1/d
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
/mux1/q
3'h0
3'h1
3'h2
3'h6
3'h7
8'hZZ
sim:/mux1/d[5] @ 611 ns
No_Data
Now
500 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns
1100 ns
Library
sim
mux.v
Wave
Transcript
VSIM 20> run
force -freeze {sim:/mux1/select[0]} 1 0
VSIM 22> run
VSIM 23>
Now: 500 ns Delta: 0
[2]
0 ns to 1149 ns
Type here to search
ENG
IN
21:35
26-09-2019

C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *

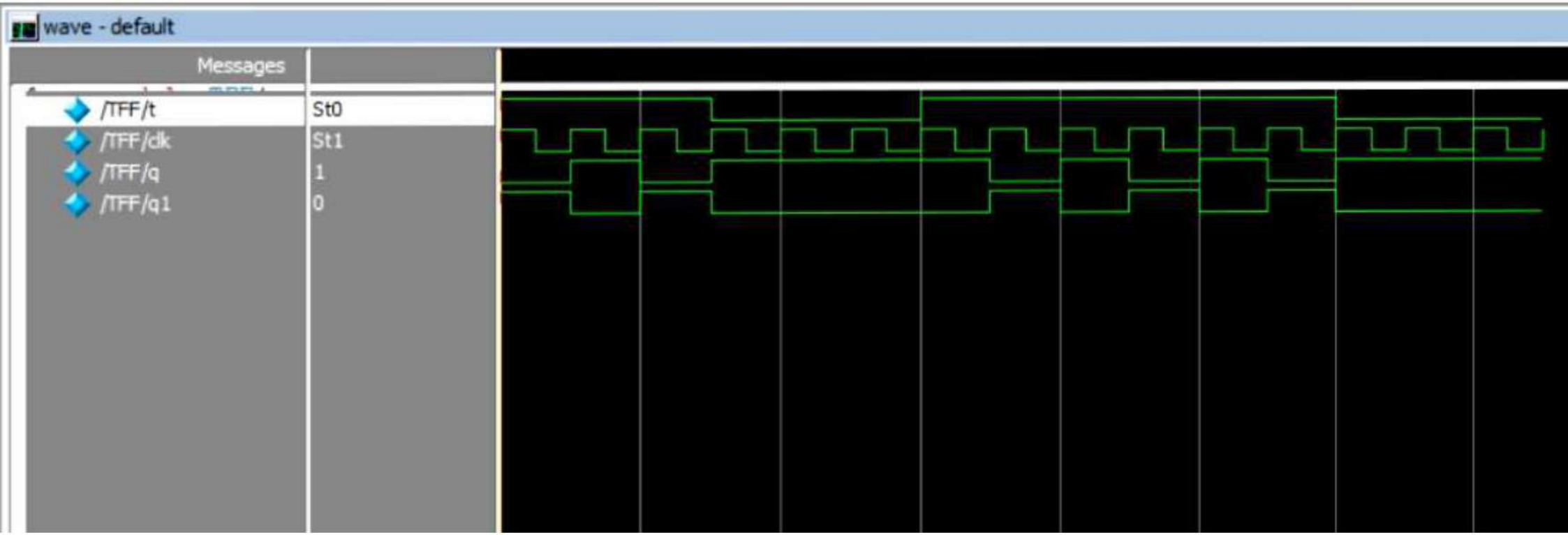
```
Ln#
 1  module srff(q,ql,r,s,clk);
 2  output q,ql;
 3  input r,s,clk;
 4  reg q,ql;
 5  inital
 6  begin
 7  q=1'b0;
 8  ql=1'b1;
 9  end
10  always@(posedge clk)
11  begin
12  case({s,r})
13  {1'b0,1'b0}:begin q=q;ql=ql;end
14  {1'b0,1'b1}:begin q=1'b0;ql=1'b1;end
15  {1'b1,1'b0}:begin q=1'b1;ql=1'b0;end
16  {1'b1,1'b1}:begin q=1'bx;ql=1'bx;end
17  endcase
18  end
19
```


sim - Default
Instance
srff
#vsim_capacity#
Wave - Default
Msgs
/srff/q
/srff/q1
/srff/r
/srff/s
/srff/clk
1'h1
1'h0
1'h0
1'h0
1'h1
Now
800 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns

C:/modeltech_6.4/examples/TFF.v

Ln#

```
 1    module TFF(
 2      input t,clk,
 3      output reg q,q1
 4      );
 5      initial
 6      begin
 7        q=1'b1;
 8        q1=1'b0;
 9      end
10     always@(posedge clk)
11     begin
12       if(clk)
13         begin
14          if(t==1'b0)begin q=q;q1=q1; end
15          else begin q=~q;q1=~q1; end
16         end
17     end
18   endmodule
```


wave - default
Messages
/TFF/t
St0
/TFF/clk
St1
/TFF/q
1
/TFF/q1
0

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout NoDesign ColumnLayout

C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *

Ln#

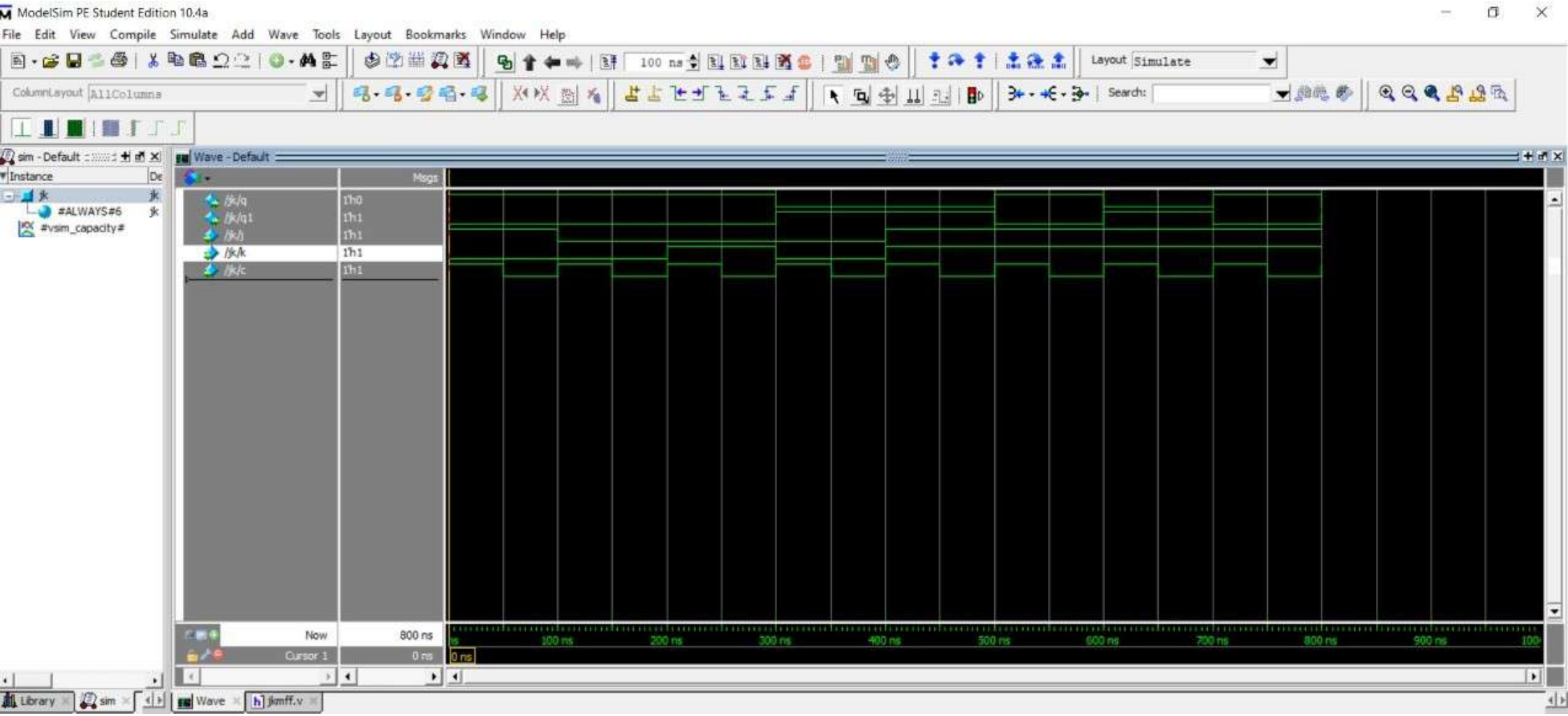
```
1  module jk(q,ql,j,k,c);
2  output q,ql;
3  input j,k,c;
4  reg q,ql;
5  initial begin q=1'b0;ql=1'b1;end
6  always@(posedge c)
7  begin
8  case({j,k})
9  {1'b0,1'b0}:begin q=q;ql=ql;end
10 {1'b0,1'b1}:begin q=1'b0;ql=1'b1;end
11 {1'b0,1'b0}:begin q=1'b1;ql=1'b0;end
12 {1'b0,1'b0}:begin q=~q;ql=~ql;end
13 endcase
14 end
15 endmodule
```

Transcript

```
# Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl

ModelSim>
```

<No Design Loaded>

Ln: 15 Col: 9

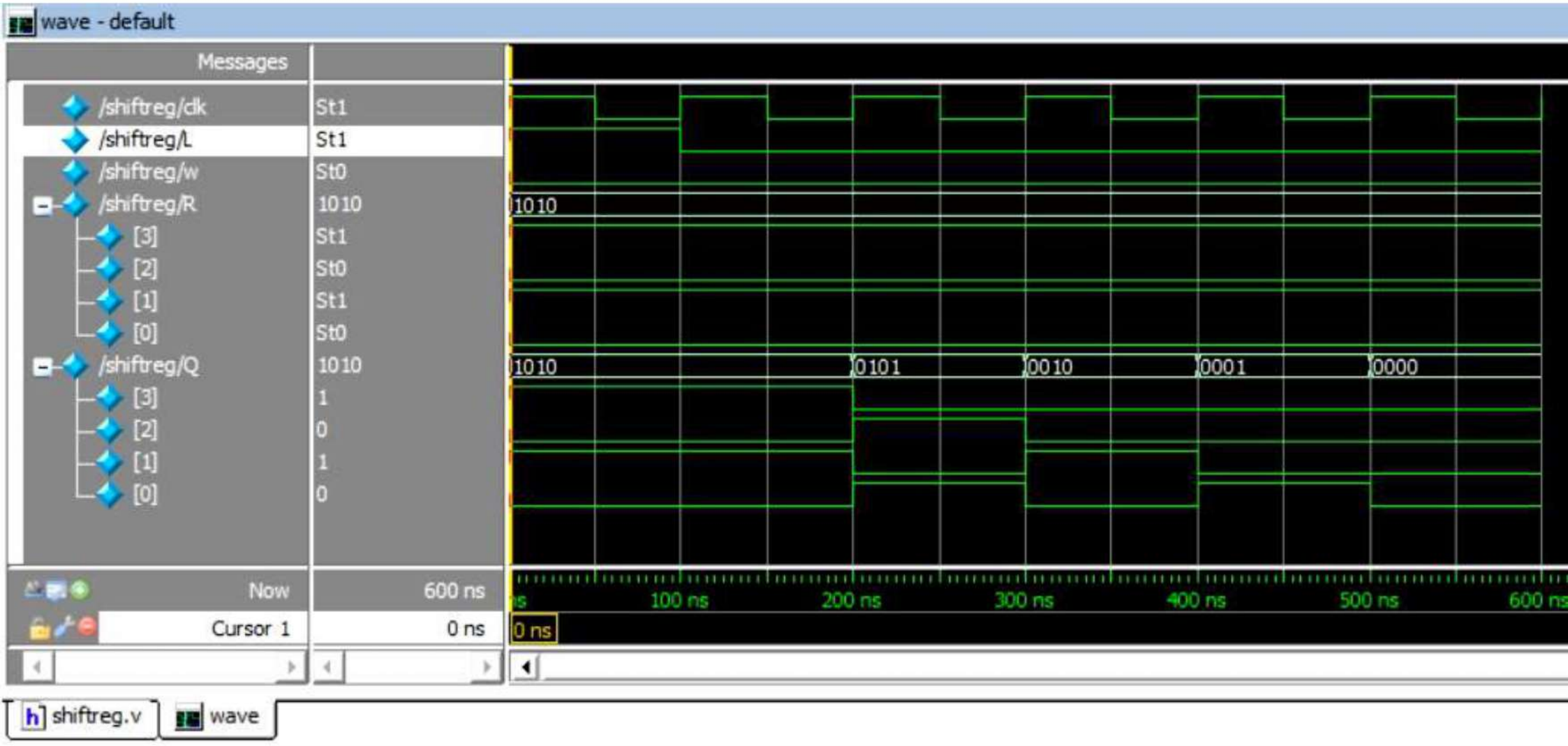

ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
jk
#ALWAYS#6
#vsim_capacity#
Wave - Default
Msgs
/jk/q
/jk/q1
/jk/j
/jk/k
/jk/c
1'h0
1'h1
1'h1
1'h1
1'h1
Now
800 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Library
sim
Wave
jkmff.v

C:/modeltech_6.4/examples/shiftreg.v

Ln#

```
 1    module shiftreg(
 2      input [3:0]R,
 3      input L,w,clk,
 4      output reg [3:0]Q
 5      );
 6      always@(posedge clk)
 7      if(L)
 8        Q<=R;
 9      else
10        begin
11          Q[0]<=Q[1];
12          Q[1]<=Q[2];
13          Q[2]<=Q[3];
14          Q[3]<=w;
15        end
16     endmodule
17
```

shiftreg.v | wave

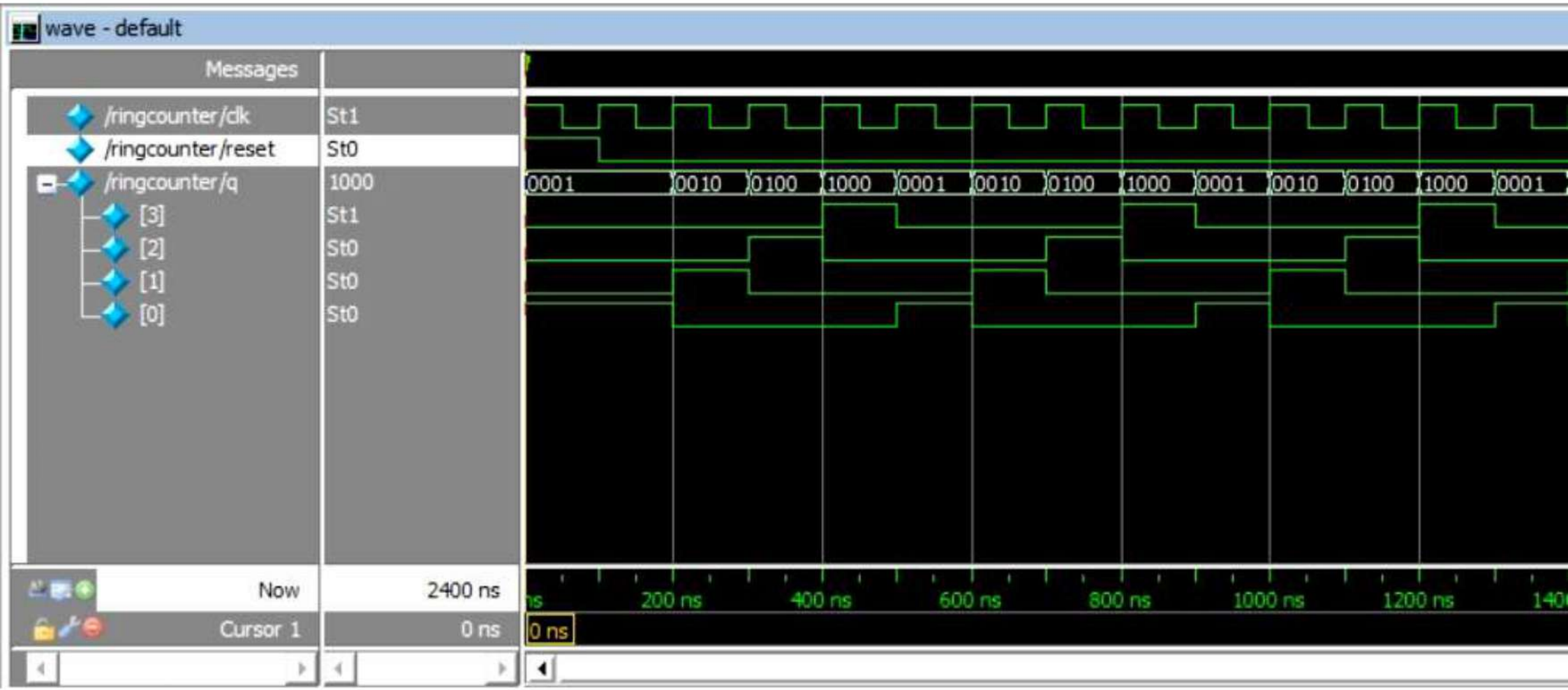

wave - default
Messages
/shiftreg/clk
/shiftreg/L
/shiftreg/w
/shiftreg/R
[3]
[2]
[1]
[0]
/shiftreg/Q
[3]
[2]
[1]
[0]
St1
St1
St0
1010
St1
St0
St1
St0
1010
1
0
1
0
1010
0101
0010
0001
0000
Now
600 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
0 ns
shiftreg.v
wave

C:/modeltech_6.4/examples/ringcounter.v

Ln#

```
 1    module ringcounter(
 2      input clk,reset,
 3      output [3:0]q
 4      );
 5      reg [3:0]a;
 6      always@(posedge clk)
 7      if(reset)
 8        a=4'b0001;
 9      else
10      begin
11        a<=a<<1; //blocked assignment
12        a[0]<=a[3];
13      end
14      assign q=a;
15    endmodule
16
17
```

wave | ringcounter.v


wave - default
Messages
/ringcounter/clk
/ringcounter/reset
/ringcounter/q
[3]
[2]
[1]
[0]
St1
St0
1000
St1
St0
St0
St0
0001
0010
0100
1000
0001
0010
0100
1000
0001
0010
0100
1000
0001
Now
2400 ns
Cursor 1
0 ns
200 ns
400 ns
600 ns
800 ns
1000 ns
1200 ns
0 ns

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout NoDesign ColumnLayout

C:/Modeltech_pe_edu_10.4a/examples/Untitled-1.v - Default *

Ln#

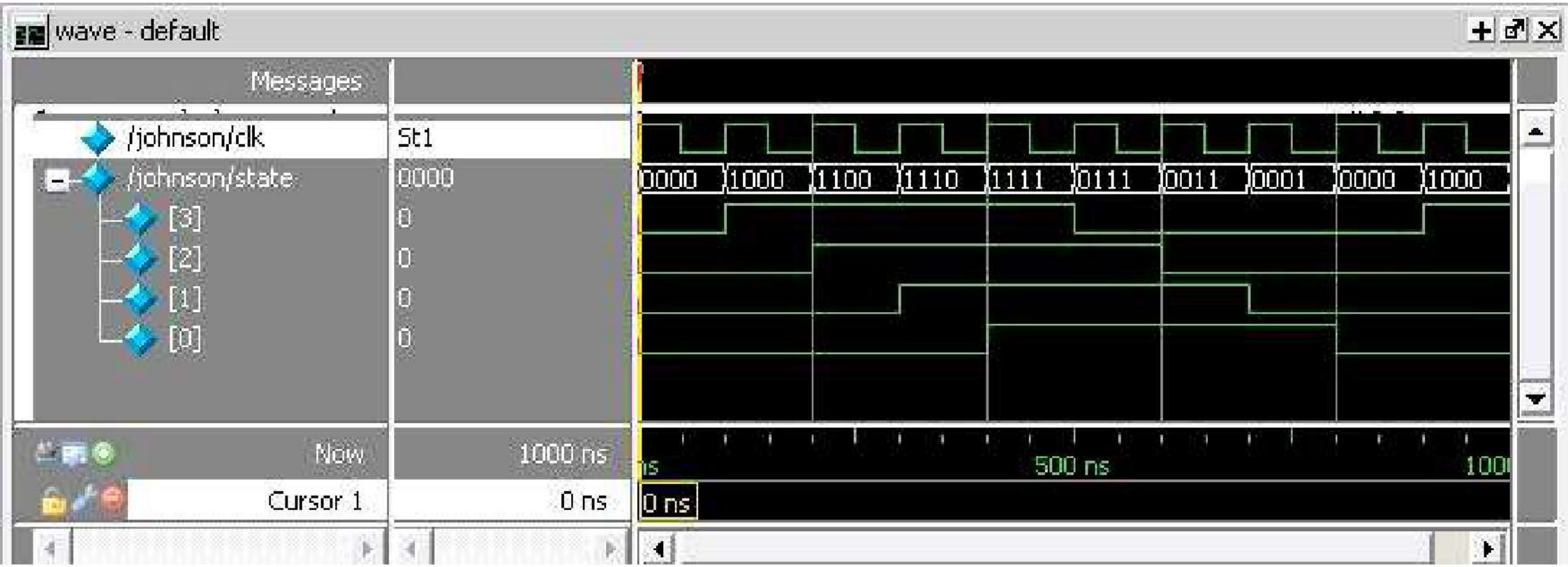
```
1  module johnson_counter(out,reset,clk);
2  input clk,reset;
3  output[3:0]out;
4  reg[3:0]q;
5  always@(posedge clk)
6  begin
7  if(reset)
8  q=4'd0;
9  else
10 begin
11 q[3]<=q[2];
12 q[2]<=q[1];
13 q[1]<=q[0];
14 q[0]<=(~q[3]);
15 end
16 end
17 assign out=q;
18 endmodule
19
```

Transcript

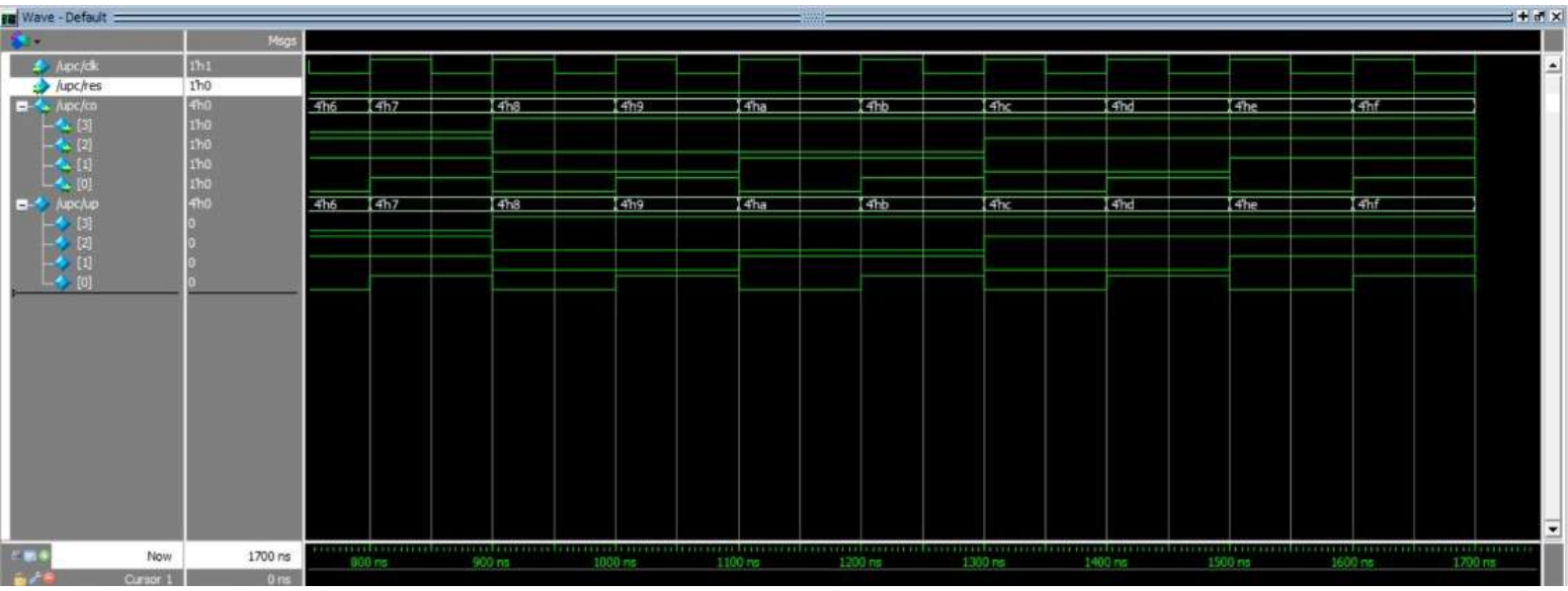
```
# Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl

ModelSim>
```

<No Design Loaded>

Ln: 18 Col: 9


wave - default
Messages
/johnson/clk
St1
/johnson/state
0000
[3]
0
[2]
0
[1]
0
[0]
0
0000
1000
1100
1110
1111
0111
0011
0001
0000
1000
Now
1000 ns
500 ns
Cursor 1
0 ns
0 ns

```
Ln#
 1  module up_counter[input clk, reset, output[3:0] count);
 2  reg[3:0] up;
 3  always@(posedge clk or posedge reset)
 4  begin
 5  if(resrt)
 6  up<=4'd0;
 7  else
 8  up<=up+4'd1;
 9  end
10  assign count=up;
11  endmodule
12
```


Wave - Default
Msgs
/upc/clk
/upc/res
/upc/co
[3]
[2]
[1]
[0]
/upc/up
[3]
[2]
[1]
[0]
1'h1
1'h0
4'h0
1'h0
1'h0
1'h0
1'h0
4'h0
0
0
0
0
4'h6
4'h7
4'h8
4'h9
4'ha
4'hb
4'hc
4'hd
4'he
4'hf
Now
1700 ns
Cursor 1
0 ns
800 ns
900 ns
1000 ns
1100 ns
1200 ns
1300 ns
1400 ns
1500 ns
1600 ns
1700 ns