DSLD Question Bank

Module 1:

1. Design a tri-state buffer and represent its working using switches.
2. Design a logic circuit for a 2-bit fast adder and explain in detail.
3. Explain with logical circuit, truth table and associated boolean equations the basic and universal gates
4. Universality of NAND and NOR gates
5. An asymmetrical signal waveform is high for 2 ms and low for 3 ms.. Find a) Frequency b) Period c) Duty Cycle Low d) Duty Cycle High
6. Explain the role of forbidden region and switching time in digital circuits.
7. Represent the basic gates in terms of switching circuits.
8. Explain the working of the following arithmetic circuits: adder-subtracter circuit, fast adder, arithmetic logic unit
9. Mention the basic arithmetic building blocks and explain in detail.
10. Plot Boolean expressions on the K-map

i. Y=ABĆ+ABC+ÁB′C

ii. Y=(A+B+C+D)(A+B′+Ć+D)(A+B+Ć+D′)(Á+B′+C+D′)(Á+B′+Ć+D)

Module 2:

1. Suppose a three variable truth table has a high output for the following input conditions: 000, 010,100 and 110. What is the sum-of-products circuit?
2. Determine the prime implicants and essential prime implicants using Quine_McClusky method for the following expression: F(A,B,C)= ∑m(1,2,3,4,6,7, 10,11)
3. For the given Boolean expression: f = xy'z + x'y'z + w'xy + wx'y + wxy
   A) Obtain the truth table
   B) Simplify the function using K Map
   C) Boolean Expression in Σ_m and Π_M form.
   D) Implement the simplified SOP expression in NAND NAND gates
4. Express the following expression in its Canonical Form
   A) (xy + z) (y + xz)
   B) x'y' + xy + x'y
5. Simplify the following using K-map:
   A)F(P, Q, R, S) = Σ(0,1,2,3,4,6,12) + d(15)
   B)F(w,x,y,z)= Σ(2,4,5,7,9,10,14) + d(0,1,12)
   C)F(a,b,c) = Σ(1,3,7) + d(2)
6. Minimize the given POS expression: F (A, B, C, D) = πM (4,5,6,7,8,12,13) + Σd (1,2,3,9,11,14,15).
7. Using QM Method simplify the following expression and implement the simplified expression using NAND NAND gates
   F (W , X , Y , Z)= Σ_m (0 , 3 , 5 , 6 , 7 , 10 , 12 , 13) + d(2 , 9 , 15)
8. For the given expression:

A)F = A`B`C`+A`BC` + ABC` d=A`B`C +A`BC + AB`C
B)F(A,B,C)= Σ_m(1,2,3,6)
simplify using K Map and derive the POS Expression

Module 3:

9. Implement the boolean function expressed by SOP: f(a,b,c,d) = Σ_m (1,2,5,6,9,12) using 8:1 MUX
10. Design a 2 Bit Magnitude Comparator
11. Mention the different types of decoders (all decoders)and their working with suitable truth table and logic circuits.
12. Implementation of 8:1 and 4:1 using 2:1, 16:1 and 8:1 using 4:1 multiplexer
13. Architecture of parity generator, checker, and its applications.
14. Types of encoders.

Module 4:

1. Differentiate between a latch and a gated flip flop. Explain the NOR-gate latch and NAND -gate latch
2. Give the state transition diagram and characteristic equation of SR, D, T and JK Flip Flop
3. Explain the working of a S R flip flop with suitable logic diagram, excitation table, characteristic equation, and timing diagram
4. Using positive edge triggered D flip flop, explain the operation of Parallel in Serial out Shift registers explain its working to load 1010 into it and shift the same
5. What are registers? Explain the working of a SISO, PISO, PIPO, SIPO Shift Register by storing and reading 1010 from MSB to LSB
6. List the applications of registers. Explain any two in detail.
7. Differentiate between a latch and a gated flip flop. Explain the NOR-gate latch and NAND -gate latch
8. Differentiate between Negative edge triggering and positive edge triggering with suitable flip flops and timing diagram
9. Convert the following FFs
   SR to D FF

   JK SR to T FF

   SR to FFFF
10. Conversion of SR flip flop to JK flip flop with suitable state synthesis table
11. Differentiate between Race around condition and Toggle condition with suitable diagrams. Explain the operation of master -slave J K flip flop. How is race around condition eliminated in JK -FF

Module 5:

12. Design a self-correcting Mod- 6 synchronous up counter using JK flip flops. Assume 100 as the next state for all the unused states
13. Explain the working of a 3 bit Negative Edge Triggered Serial Down counter
14. Write Verilog code for: Ring Counter
15. Design a mod 6 counter using JK flip flop and K map simplification method

16. Design a mod 10 counter using mod-5 counter. Explain using appropriate truth table and waveforms
17. Write a verilog code in the structural way for the expression y= a'b'+bcd'+acd
18. Write a verilog code for Ring counter and explain its working by specifying the input settings.
19. Design a mod-8 binary counter with parallel clock input.
20. Explain about 3 bit binary up-down counter.
21. A Sequential circuit has one input and one output. The state diagram is shown in figure 2. Design the sequential circuit with D flip-flops.