MODULE 5 AND VIVA QUESTIONS :ARM7

1. What is the size of the ARM processor?
2. State the design policy of the ARM processor
3. What is the minimum data handling capability of ARM
4. Name the inbuilt debugger used in ARM7
5. What are t, d, m, I stands for in ARM7TDMI?
6. ARM 7 operates in which mode
7. How many instructions pipelining is used in ARM, list the stages
8. What is the size of cache memory size available in ARM7
9. What is the need of barrel shifter in ARM
10. Explain the processor modes with mode bit
11. list and explain the various condition flags in ARM
12. Explain pipeline concept for the following code having three instructions

    1 st instruction: ADD Ld, Ln,Lm

    2nd Sub Ld, Ln,Lm

    3 rd Cmp Rn, Rm (8M)

13. Explain the interrupt vector table in ARM (6M)
14. Illustrate the barrel shfter in ARM (4M)
15. List the salient features of ARM instruction set (2M)
16. Explain the various ADD instructions in ARM with suitable examples
17. Explain the following instructions with suitable examples

a. CMP b. CMN c.TST d. TEQ f. AND g. ORR h. EOR i. BIC

18. Illustrate with suitable example the working of MUL instruction in
19. ARM, also explain the following instructions

a. MUL b,MLA c.SMLAL d. UMLAL e. SMULL f. UMULL

20. Illustrate the need of a Branch instruction and explain the following with suitable examples i. B ii. BL iii. BX iv. BLX
21. List and explain the various LOAD and STORE instructions in ARM
22. Explain the following with suitable examples

a. LDR b. STR c. LDRB d. STRB c. LDHH d. STRH e. LDRSB f. LDR SH , ADR

14. Explain the various Single register transfer Instructions set with suitable examples

15. Explain Multiple register transfer Instructions set with suitable examples

16. Write short notes on Software Interrupt Instruction SWI explain each instruction with suitable examples

17. Explain the Program Status registers, CPSR and SPSR and the corresponding instructions related to the two registers

18. List the atomic instructions in ARM

19.Explain the SWAP instruction in ARM , illustrate its working .