Computer Organization

[18IS3DCCOG]

Question Bank

MODULE 1:

Basic Structure of Computers
Machine Instructions and Programs

1. Briefly explain all functional units of computer. (10)

2. Explain the following.
   i.Processor clock
   ii. Basic performance equation
   iii. Clock rate (06)

3. Draw and explain the connection between memory and processor with the respective registers. (08)

4. Explain the basic operational concepts of a computer. (08)

5. Briefly explain the following with example.
   (i) Sign and Magnitude
   (ii)1's Complement
   (iii) 2's Complement
   (08)

6. Perform the following operation on 5 bit signed numbers using 2's compliment representation system. Also indicate whether overflow occurred or not.
   (i) (-10) + (-13)
   (ii)(-10) – (+4)
   (iii)(-3) + (-8)
   (iv) (-10) – (+7)
   (10)

7. Derive the basic performance equation. Discuss the measure to improve the performance. (10)

8. Write a note on byte addressability. (04)

9. Explain with neat diagram Big-Endian and Little-Endian assignment? (06)

10. Explain word alignment with neat diagram. (05)

MODULE 2:

Input/Output Organization

1. Define memory mapped I/O and I/O mapped I/O with examples. (5)
2. Explain program controlled I/O with example. (8)
3. What is an interrupt? With example illustrate the concept of interrupt. (6)
4. Explain how interrupt request from several devices are communicated to a processor through a single INTR line. (6)
5. Explain the concept of Enabling and Disabling of Interrupts. (5)
6. Explain the following
   (i) Polling
   (i) Vectored Interrupt
   (ii) Interrupt Nesting (10)
7. With a neat diagram explain daisy chain technique. (6)
8. Explain how the device requests on controlled. (6)
9. What is exception? Explain the kinds of exceptions in detail. (10)
10. Explain in detail, the situation where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems? (08)

MODULE 3:
Input/output Organization cntd :

1. Define Bus Arbitration. Explain in detail two approaches of bus arbitration. (10)
2. What is DMA? Explain the registers used in DMA controller and describe with a neat diagram, the use of DMA controller in a computer system. (10)
3. List the SCSI bus signals with their functionalities. (04)
4. Describe how a read operation is performed on a PCI bus (10)
5. Briefly explain PCI bus with neat diagram. (10)
6. Explain data transfer signals on the PCI bus. (06)
7. Explain read operation sequence of events in SCSI bus. (08)
8. Explain the following w.r.t SCSI bus
   a. Arbitration
   b. Selection
   c. Information transfer
   d. Reselection. (10)
9. Explain the synchronous and asynchronous bus with neat diagram. (10)
10. Expalin the architecture and addressing scheme of USB. (08)
11. Explain briefly protocols of USB.

Module 4: Memory system

1. Discuss the internal organization of a 2Mx8 asynchronous DRAM chip. (10)

OR

With neat diagram explain asynchronous DRAM.

2. With neat diagram explain synchronous DRAM. (08)

3. Explain basic memory concept with block diagram.

2. Explain with a neat diagram the working of 16 mega bit DRAM chip configured as 2M X 8. Also explain how it can be made to work with fast page mode. (10)

3. With neat diagram explain the internal organization of memory chip. (6)

3. Explain 1Kx1 Memory chip with neat diagram. (6)

4. Explain with diagram the memory hierarchy with respect to speed, size and cost. (6)

5. With figure explain about direct mapping, associative and set-associative cache memory mapping functions. (10)

6. What is virtual memory? Explain with its organization. (10)

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What is Virtual Memory? With a neat diagram explain how virtual memory address is translated.

7. Discuss in detail the features of memory design which leads to improved performance of computer. (10)

Module 5: Arithmetic:

1. Explain with figure the design of a 4-bit carry look ahead adder. (10 Marks)
2. Explain Booths algorithm with some example. (08/10 Marks)
3. What is fast multiplication? Explain Bit-pair recording of multiplier with an example. (10 Marks)
4. Explain the following w.r.t Integer division with neat diagram.
   i. Restoring division
   ii. Non restoring division.
   (10 Marks)
5. Explain IEEE standard for floating-point number representation. (10 Marks)
6. With figure explain circuit arrangement for binary division. Explain the non-restoring division algorithm with suitable example. (10 Marks)
7. Multiply 14 X -8 using Booth's algorithm. (6 Marks)
8. Explain Normalization, excess-exponent and special values with respect to IEEE floating point representation. (6 Marks)
9. Using a block diagram, which shows the register configuration, perform sequential circuit binary multiplication of multiplicand =1010 and multiplier =1101. (8 Marks)
10. Write and explain the algorithm for binary division using restoring division method, with an example. (6 Marks)
11. What is fast multiplication? Explain Bit-pair recording of multiplier with an example. (10 Marks)
12. Perform signed multiplication of numbers (-13) and (-20) using booth multiplication algorithm. (10 Marks)
13. Perform division of numbers 8 by 3 (8÷3), using non-restoring division algorithm. (08 Marks)
14. Illustrate the steps for non-restoring division algorithm for the following data: Dividend =1011,Divisor=0101. (05 Marks)
15. Explain Booth's algorithm and solve problem with multiplicand (-13) and multiplier (+11). (08 Marks)

16. Explain the design of 16 bit carry look ahead adder with a neat diagram.

OR

Explain with figure the design and working of a 16-bit carry-look ahead adder built from 4-bit adders. (06 Marks)

17. Differentiate between restoring and non-restoring division. (04 Marks)

18. Explain bit pair recoding technique by multiplying the numbers +13 and -6. (06 Marks)

19. Explain restoring division using 4-bit example. (06 Marks)