

MODULE A - FLIP FLOPS & REGISTERS

Flip Flops: Clocked & Flip Flops, Edge-triggered & flip flop, Edge triggered JK flip flop, Flip Flop Timing, JK Master Slave Flip Flop, Various representation of Flip Flops, Analysis of sequential circuits.

Registers: Types of registers, SISO, SIPO, PISO, PIPO, Universal Shift Register, Applications of Shift Registers.

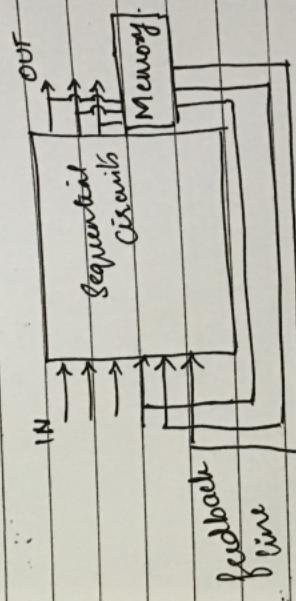
C03, C04, C05

8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.8, 8.10, 8.11

9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7

Introduction to Sequential Circuits:

A sequential circuit is a logical circuit where the output depends on the present value of the input signal as well as the sequence of past inputs. A sequential circuit is a combination of combinational circuit & a storage element.



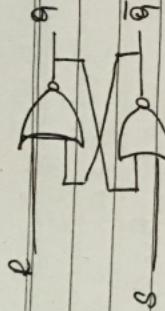
A bistable device is a device that can be either in one of the two possible states such as on or off, 0 or 1.
Ex: flip-flops, counters, registers.

NOR-gate latch:

Basic storage element is called as a latch. - 0

Two inputs: R & S

Two outputs: Q & \bar{Q}



Noe

Case 4:

$$a) \quad S=0, \quad R=1$$

In case if any i/p is 1, off is 0. $\therefore R = 1, Q = 0$ [RESET]

b) On removing the i/p $\Sigma=0 \& \ell=1$, where both gen

$$Q = 0 \quad f = 0$$

when, $R = 0$, $\bar{q}_1 = 1$, $\bar{q} = 0$

1

- here the effort is same as the previous case

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In case if any α_p is 1, α_p is 0. i.e. $\overline{\alpha} = 0$

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- On removing the tip, $S=1$ & $R=0$, when both are 0.

$$Q = 0 \quad \theta = 0$$

when $Q = 1$, $\underline{g} = 0$,

11

- here the off is same as the previous one.

case 3:

$$S=1, R=1$$

if $S=1, R=1$, $Q=0, \bar{Q}=1$ is not possible

$$S=0, R=0, Q=0, \bar{Q}=1$$

b) $S=0, R=0, Q=0, \bar{Q}=1$ (not storing the previous state)

$$\left\{ \begin{array}{l} S=0, R=0, \bar{Q}=0, Q=1 \\ \therefore \bar{Q}=1, R=0, Q=0. \end{array} \right.$$

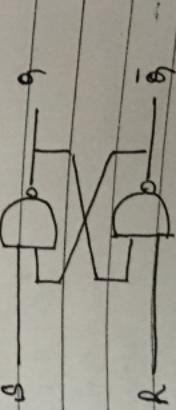
~~both~~

-	S	Q	\bar{Q}
-	R	\bar{Q}	0

Truth table:

S	R	Q	\bar{Q}
0	0	last state	-
0	1	0	1
1	0	1	0
1	1	forbidden	-

NAND Gate switch:



two inputs: S & R

two outputs: Q & \bar{Q}

Case 1:

a) $S = 0, R = 1,$

$$Q = 1,$$

$\bar{Q} = 0, \because Q = 1, R = 1$

NAND

	A	B	Y
0	0	0	1
0	0	1	1
1	0	1	1
1	1	0	1
			0

Truth Table:

S	R	Q	\bar{Q}
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory	

a) $S = 1, R = 0, \bar{Q} = 1$

$\therefore Q = 0 \quad \because \bar{Q} = 1, S = 1$

Case 2:

S	R	Q	\bar{Q}
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory	

Case 3:

a) $S = 0, R = 0, Q = 1,$

$\bar{Q} = 1, \quad \therefore Q = 0, R = 0$

$Q = 1, \bar{Q} = 1 \quad \rightarrow \text{Not possible.}$

Difference b/w latches & flip flops

latches:

- bistable device used to store either a 0 or 1.
- change in state can be observed based on
- change in the input - no clock signal required
- gated latches - enable signal

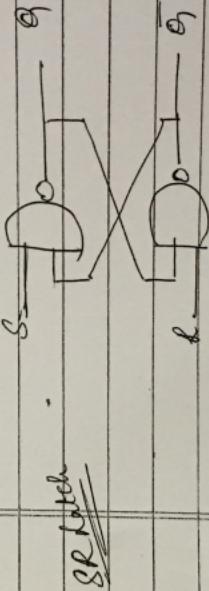
Ex: D-L, T-L, SR-L, JK-L

flip flops:

- bistable device used to store either a 0 or 1
- changes state based on a clocked signal
- clock controls the entire operation of the flip flop
- edge triggered flip flops. A pulse triggered flip flop

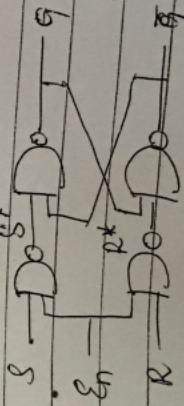
Ex:

D-FF, T-FF, SR-FF, JK-FF

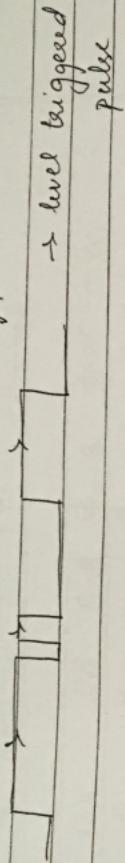


~~SR latch~~

The inputs S & R can be changed accidentally or intentionally without any control input. Introduction of the control input is done by



If the control q_p is the enable signal, the circuit behaves like a latch - level triggered.

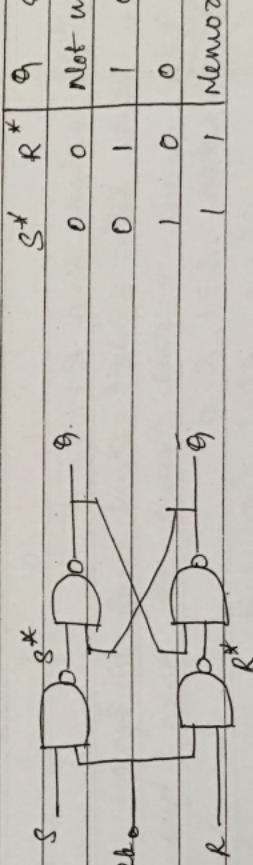


$$En = 1, \quad En = 0 \\ Q^* = \overline{S} \quad S^* = 1, \quad R^* = 1 \quad \text{memory state.}$$

Instead of enable - if we have the clock, the circuit behaves like a flip flop. - only in case of triggering i.e. level sensitive.

latch is level sensitive
flip flop is edge sensitive

Introduction to SR flip flop:



$$S^* = (S, \overline{Q_R}) = \overline{S} + \overline{Q_R}$$

$$R^* = (\overline{R}, \overline{Q_L}) = \overline{R} + \overline{Q_L}$$

\rightarrow ~~edge triggered~~

Case 1:

When $\text{CH} = 0$

$S^* = 1, P^* = 1$ memory

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$$R^* = R = 1$$

Wegen $\zeta = 0, k = 0, \zeta = 1, k = 1$

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$$0^* = 0$$

$$S = 0 \quad \cancel{K = 1}$$

$$k^* = 1$$

1

100

$$S^* = \{ \rho^* \}$$

$$I = 48, \quad Q = 12, \quad \dots$$

$$\text{in } g=1, R=0$$

$$S^* = 0, \quad R^* = 1, \quad \theta^* = 1 =$$

1

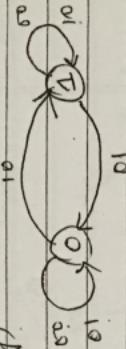
when $\delta = 1$, $R = 1$

$$S^* = 0, R^* = 0, \theta \propto \bar{\theta} = \text{Not used}$$

Characteristic table 4 excitation table for SR flip flop

Truth Table:-

S_n	R_n	S	R	Q_{n+1} - Next state
0	X	X	X	Q_n - Present state
1	0	0	0	Q_n (Memory)
1	0	1	0	0
1	1	0	1	1
1	1	1	1	Invalid



Characteristic table: [cell = 1]

clock

now

next

state

group

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Refines the
state of each
flip flop as a
function of its
inputs &
previous state.

Using the characteristic table - next state is derived using the present state & inputs S & R.

Excitation table

S & R values are found out using the values of Q_n & Q_{n+1}

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$Q_{n+1} = \begin{cases} S \\ Q_n \end{cases}$

0	0	0	1	1	0	0	1	1
1	1	0	0	1	1	0	1	1

~~App. 2~~

$Q_{n+1} = \overline{S} + \overline{Q_n R}$

Excitation table shows the minimum steps that are necessary to generate a particular next state when the current state is known.

Introduction to SR flip-flop: (data)

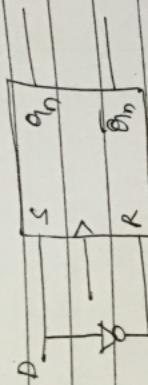
Truth Table for SR flip flop:

Clk	S	R	Q_{n+1}	Memory	SR flip-flop
0	X	X	Q_n	Q_n	Set
1	0	0	Q_n	Q_n	Set
1	0	1	0	0	Reset
1	1	0	1	1	Invalid
1	1	1	1	1	Invalid

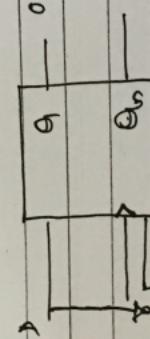
θ_{n+1}	θ_n	τ
0	0	0
0	-1	-1
-1	0	0
-1	1	1

Inputs are given / remove the clk to show the

→ to store the
use D flip
to give the ip
the data A sum
clock.



$$\therefore \text{when } D=0, S=0, R=1 \\ D=1, S=1, R=0$$



T.R for D flip-flops-

Qn	D	Qn+1
0	X	Qn
1	0	0
1	1	1

Characteristic table & excitation table for D flip-flop

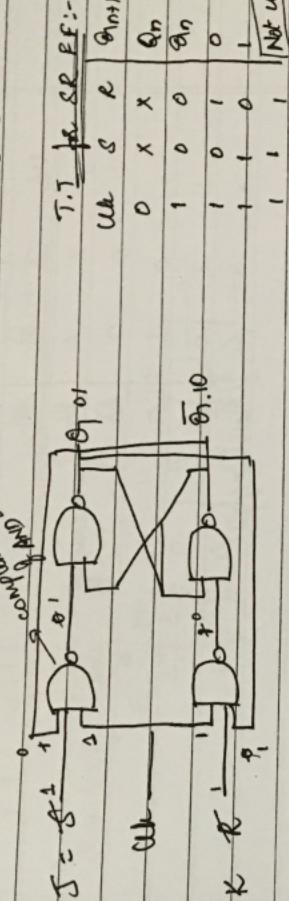
Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

$$Q_{n+1} = D$$

Introduction to JK flip flop:

Thus

In order to make the invalid state of SR flip flop usual, JK flip flops were introduced.



$Q = Q_1 \oplus Q_2$, Memory state \Rightarrow if p to NAND SR with in (1,1)

$$Q_n = 1,$$

$$J = 1, K = 0, Q_1 = 1, \bar{Q}_1 = 0$$

$$Q_n = 1$$

$$J = 0, K = 1, Q_1 = 0, \bar{Q}_1 = 1$$

$$Q_n = 0$$

Code = 1,

$$J = 1, K = 1, Q_1 = ? , \bar{Q}_1 = ?$$

assume $Q_1 = 0, \bar{Q}_1 = 1$

$K = 1, Q_1 = 1, Q_2 = 0, \text{ output} = 1 \quad \left\{ \begin{array}{l} \text{NAND SR latch} \\ \text{component} \end{array} \right.$

$J = 1, Q_1 = 1, \bar{Q}_1 = 0, \text{ output} = 0 \quad \left\{ \begin{array}{l} \text{OR gate} \\ \text{component} \end{array} \right.$

\therefore if p for NAND SR latch is 0 & 1

$$\text{by } Q = 1, \bar{Q} = 0$$

$J = 1, Q_1 = 1, \bar{Q}_1 = 0, \text{ output} = 1 \quad \left\{ \begin{array}{l} \text{OR is } Q_1 = 0, \bar{Q}_1 = 1 \\ \text{Q}_1 = 1, \bar{Q}_1 = 0, \text{ output} = 0 \end{array} \right\}$

$$\therefore Q = 0101 \\ \bar{Q} = 1010$$

if $Q_{n+1} = 0$, $Q_n = 1$

Truth Table:

<u>Q_n</u>	<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>
0	X	X	Q _n of memory.
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	Q _n (toggle)

Characteristic table:-

<u>Q_n</u>	<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table:-

<u>Q_n</u>	<u>Q_{n+1}</u>	<u>J</u>	<u>K</u>
0	0	0	X
0	1	0	X
1	0	1	X
1	1	X	0

for J:-

Q_{n+1}	J	K
0	0	0
0	1	X
1	X	0

$$J = Q_{n+1}$$

$$K = \bar{Q}_{n+1}$$

for K:-

Q_{n+1}	J	K
0	0	0
0	1	X
1	X	0

Similarly for Q_{n+1}

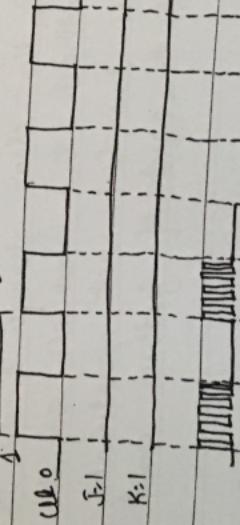
Q_{n+1}	J	K
0	00	01
0	0	0
1	1	0

$$\begin{aligned} \therefore Q_{n+1} &= \bar{I} + \bar{E} \\ &= \bar{Q}_n \bar{J} + Q_n \bar{K} \end{aligned}$$

Race around condition in JK flip flop:-

clock	J	K	Q_{n+1}	\bar{Q}_{n+1}
0	x	x	Q_n	\bar{Q}_n
1	0	0	Q_n	\bar{Q}_n
1	0	1	0	1
1	1	0	1	0
1	1	1	-	-

Elimination of the race around condition:-



If the delay t is greater than half time period, then there will be low of P will not be generated.

Delay \rightarrow caused by changing values of $T_{1/2}$

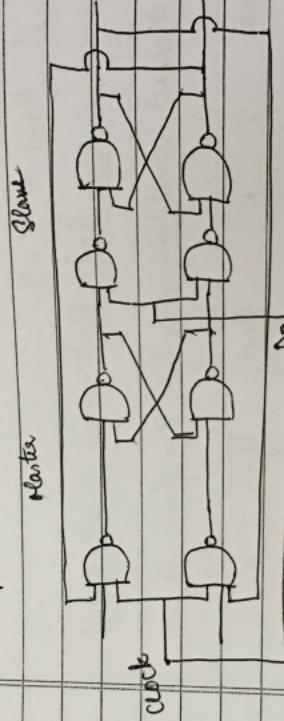
i.e. $T_{1/2} >$

Conditions to overcome racing:

- i) $T_{1/2} <$ propagation delay of the flip flop.
- ii) edge triggering
- iii) master - slave condition.

Master Slave JK flip flop:-

Teething is a controlled phenomena while racing is uncontrollable.



of
two
ways

when $J=1, K=1, Q_1 = 1$,
while slave is high, master is operational
master changes while off if the slave remains
in the memory/previous state.

- through off of the slave changes & has its
effect on the feedback line - the slave signal
thereby eliminating the effect of feedback and
racing.

when V_{DD} is high - master is operational while slave just keeps the memory.
when the clk is low - slave will be functional such that effect of the feedback is eliminated.

the opf changes once in a clock cycle

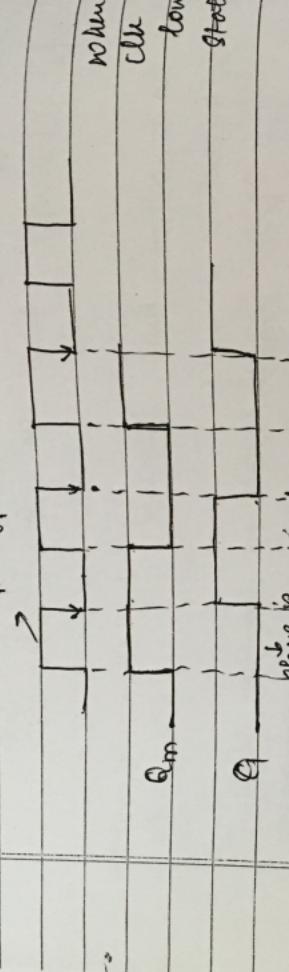
master is positive level triggered & slave is negative level triggered.

when $J=1, K=0$, master sets on positive clock transition while the slave sets on negative clock transition, thereby following the master.

when $J=0, K=1$, master resets on PT of the clock, slave results on NT of the clock when both $J \& K$ are high, master toggles on the PT of the clock, & slave toggles on the NT of the clock.

when both $J=0 \& K=0$, Q remains unchanged.

- This makes the flip flop change state in a
manner known as
negative edge triggered



Clk	J	K	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n → Toggle.

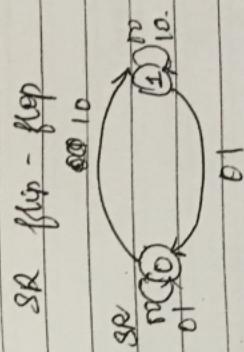
Various Representations of flip flops-

$$SR \text{ flip flop: } Q_{n+1} = S + R' Q_n$$

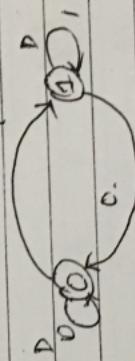
$$JK \text{ flip flop: } Q_{n+1} = J\bar{Q}_n + K Q_n$$

$$D \text{ flip flop: } Q_{n+1} = D$$

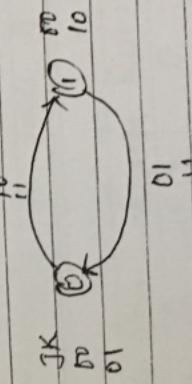
Flip flops as finite State Machine.



D flip flop

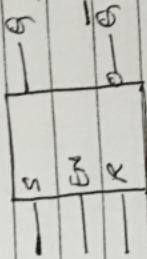


JK flip flop

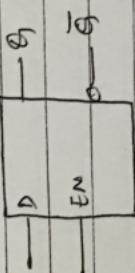


Symmetric Representation of flip flops:-

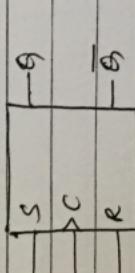
1) Clocked RS flip flop:-



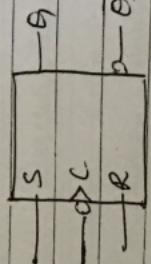
2) Clocked D flip flop:



3) Edge triggered RS flip flop:

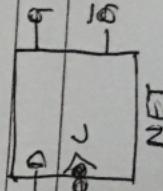
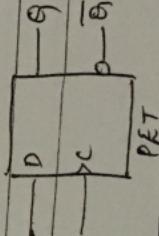


→ Positive edge triggered RS flip flop.

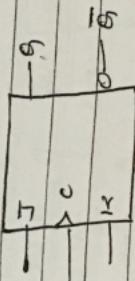


→ Negative edge triggered RS flip flop.

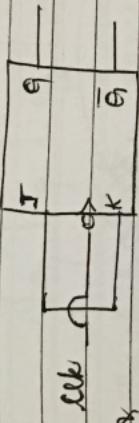
4) Edge triggered D flip flops:-



Positive edge triggered JK flip flop:



T flip flop: Toggle flip flop - can care by only toggling action



Truth Table for T flip flop:-

Qn	T	Qn+1
0	X	Qn (memory)
1	0	Qn (memory)
1	1	Qn (toggling)

Characteristic table of T flip flop:-

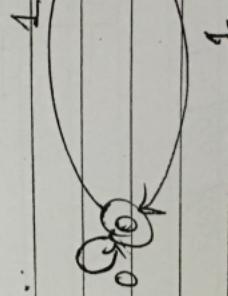
Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

Qn = 0 and T = 0 is called 1's detector.

Excitation Table

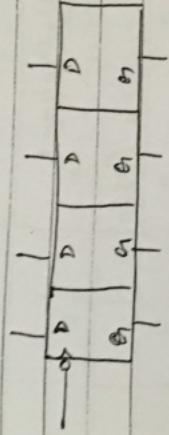
$\oplus n$	$\oplus n+1$	\ominus
0	0	0
0	1	1
1	0	1
1	1	0

$$\oplus_{n+1} = \oplus_n \oplus \ominus$$



Introduction to Registers:

A group of flip-flops used to increase the storage capacity is known as register. An n-bit register consists of 'n' no. of flip-flops & is capable of storing n-bit word.

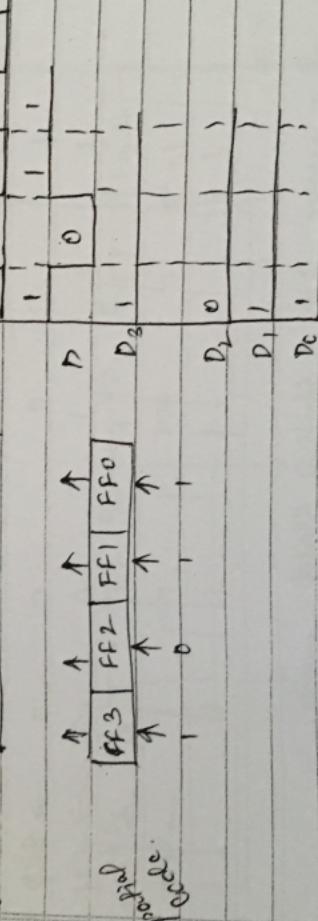


The clock is the same for all the four flip flops used here.

Data formats & classification of register:

→ Data can be stored in serial or parallel form
↓
One bit at a time.

Temporary Data \Rightarrow FF3 | FF2 | FF1 | FFO \Rightarrow

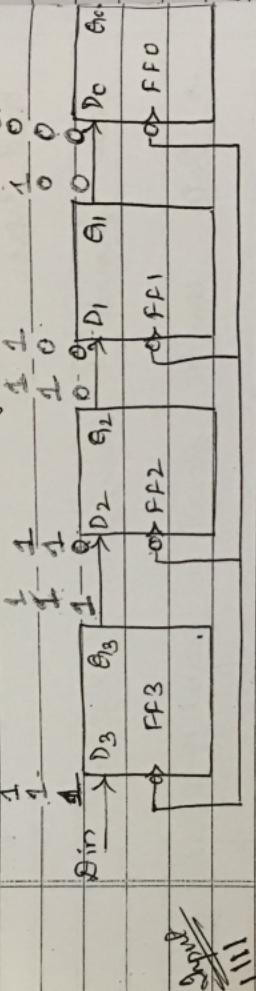


Classification of registers:-

- i) Depending on I/O - esp -
Serial I/O - serial o/p
Serial I/O - parallel o/p
parallel I/O - serial o/p
parallel o/p - parallel o/p

ii) Depending on application :-
at shift register
by storage registers (P2P)

Serial In - Serial Out Register:-

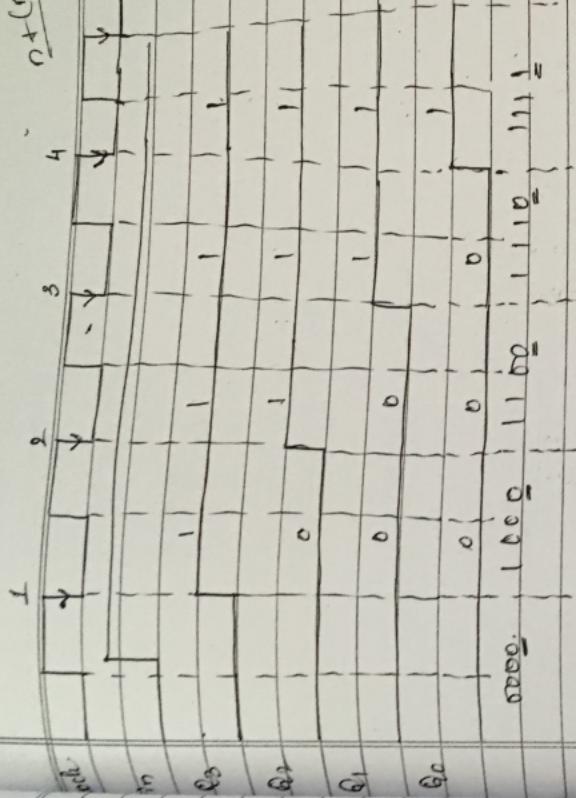


QI	Q ₃	Q ₂	Q ₁	Q ₀
↓	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1
↓	1	1	1	1

- works in shift right mode.

- used for data storage, data transfer & A/D
- & logic ~~use~~ operation.

$\overline{Q_4} \rightarrow$



FFO

Q0

Q1

Q2

Q3

Shift Register:

b) Serial input Parallel output:
 (N1) clock pulse
 to store Q_3 &
~~Q2~~

SISO - more clock pulses are required for
 data arrival - resulting in SISO.

0

1

2

3

4

5

6

7

1.1

0.0

1.0

0.1

1.1

0.0

1.0

2.1

0.0

2.0

1.1

2.1

0.0

2.0

3.1

0.0

3.0

2.1

3.1

0.0

3.0

4.1

0.0

4.0

3.1

4.1

0.0

4.0

5.1

0.0

5.0

4.1

5.1

0.0

5.0

6.1

0.0

6.0

5.1

6.1

0.0

6.0

7.1

0.0

7.0

6.1

7.1

0.0

7.0

8.1

0.0

8.0

7.1

8.1

0.0

8.0

9.1

0.0

9.0

8.1

9.1

0.0

9.0

10.1

0.0

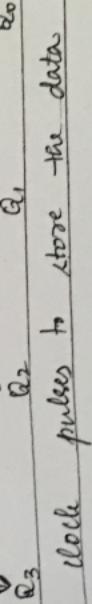
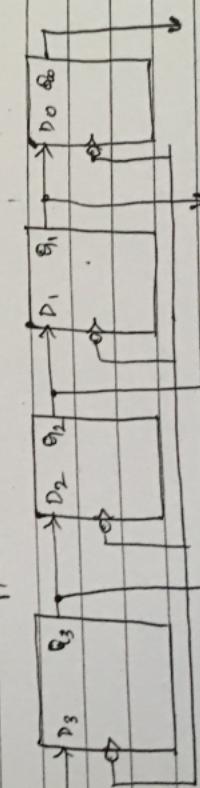
10.0

9.1

10.1

0.0

10.0

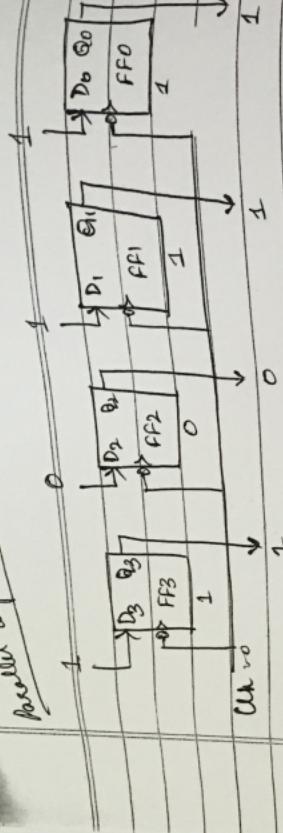


Ariti

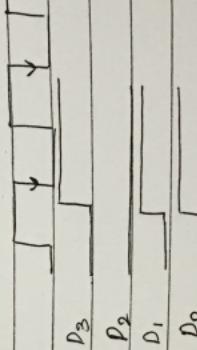
- require 4 clock pulses to store the data

clock pulse.

parallel input parallel output



- called as storage & buffer register



In D flip flop, if $D = 0$, $Q_{n+1} = 0$

if $D = 1$, $Q_{n+1} = 1$

make the $Q_n = 0$, irrespective of the value of D
 $Q_{n+1} = Q_n$ (stored value)

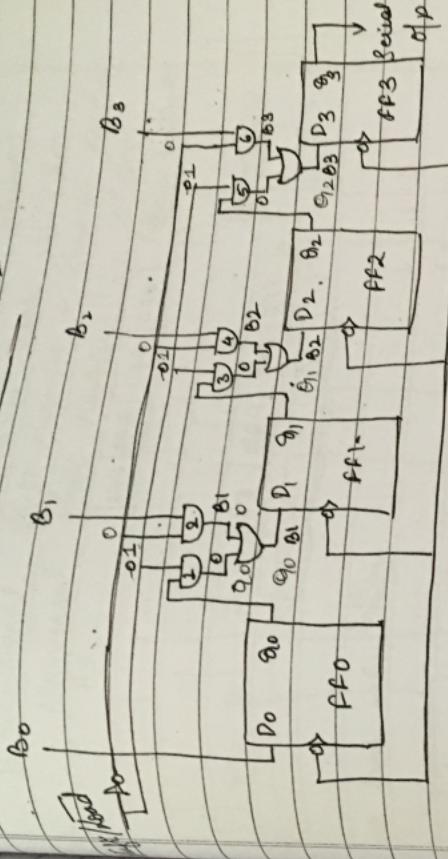
Remove it in parallel manner.

last of

when $Q_n = 1$, consider: 1000 as the new data
remove the clock to store the data &
remove it.

- Requires 1 clock pulse to store the new data & 1
clock pulse to retrieve the
data
 \Rightarrow store $(1 + (n-1))$ successive

Parallel Input Serial Output, Mode:-



Two modes:

Read mode: enter or read data bits into flip flops simultaneously. Reading happens when the SOP is low. i.e. when load is 0, data is parallel fed into the flip flops.

When load = 0, $\text{SOP} = 0$ AND gates 1, 3 & 5 are 0, if p to the AND gates 2, 4 & 6 are 1. For AND gate 4, $Q_0 = 0 \therefore 0 \text{ AND } 0 = 0$. AND gate 2, $1 \text{ AND } 0, \therefore 1 \text{ AND } 0 = 0$, AND gate 6, $1 \text{ AND } 1, \therefore 1 \text{ AND } 1 = 1$.

Shift mode: used to shift the data from one flip flop to another in order to get serial output. When shift is 0, means the changes made are null.

Consider i/p data as 1011

In the read mode:

1 0 1

read mode	FF0	FF1	FF2	FF3
	1	0	1	1

Shift mode

shift mode	FF0	FF1	FF2	FF3
	1	0	1	1

~~would open both S0:S1~~

↓ ↓ ↓ ↓

1 0 1 1

→ 1 0 1 1

→ 1 0 1 1

→ 1 0 1 1

shift right mode: S1=0, S0=1

Consider to store 1011 - In the first cycle, 1 is stored in the first flip flop, output is connected to S1 second mux - thereby shifting the data.

shift left mode:

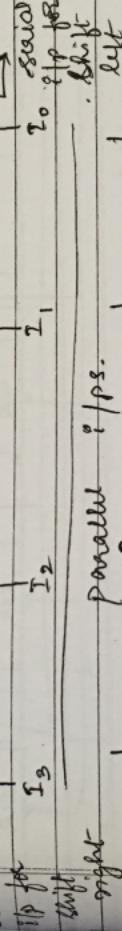
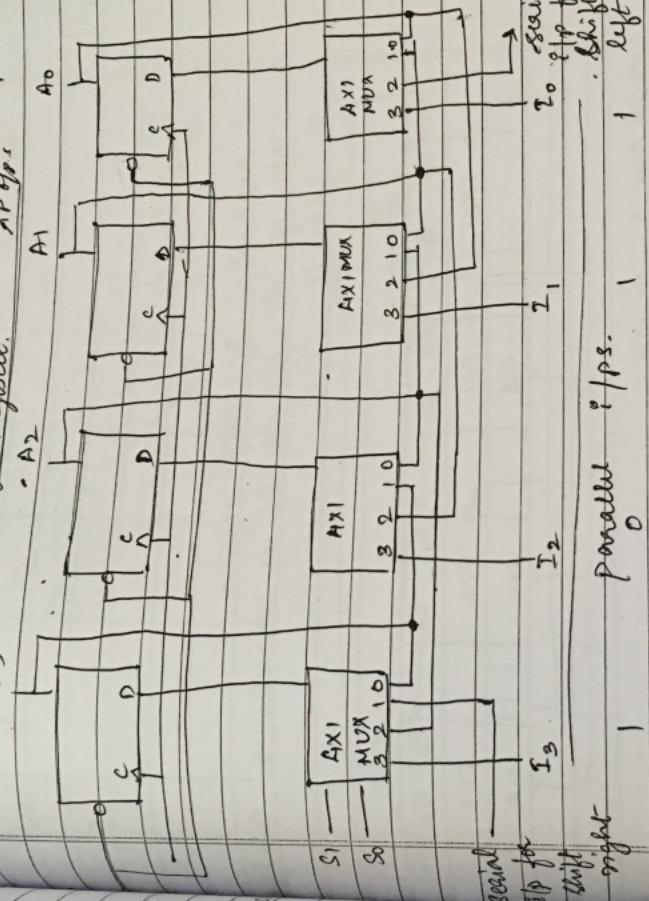
S1=1, S0=0

Consider to store 1110 - In the first cycle 1 is stored in first ff - S0 is connected to T2 of the second mux thereby shifting the data.

S1=1, S0=0

Universal Shift Registers:-

Bidirectional Shift Register + Parallel loading
= Universal Shift Register.



Mode Control

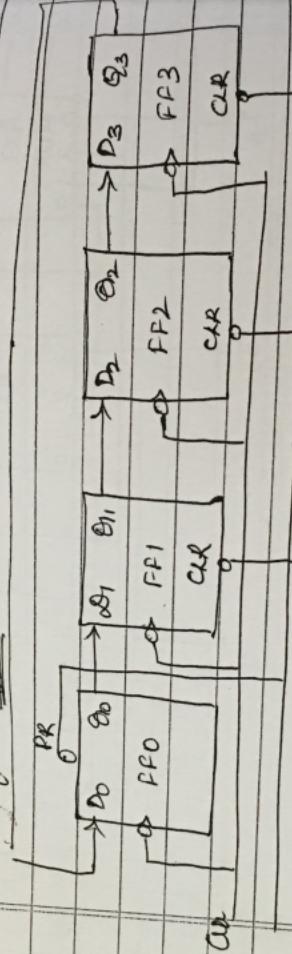
S ₁	S ₂	Reg operation :-
0	0	No change
0	1	Shift right mode.
1	0	Shift left mode
1	1	Parallel loading

4 clock pulses are required to store 1011-1
Shift right mode. Pin 2 of the M741

Ex: 1100 \rightarrow Pin 2 of the M741

Ring Counter:

- Application of shift register.
- Q₀ of the last flip flop is connected to the input of the first flip flop.



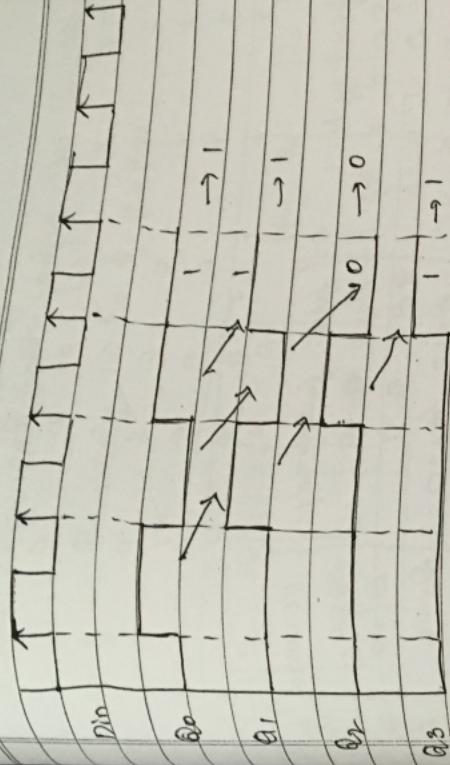
Special type of counter:

- No of states = No of flip flops used.
- Asynchronous counter - same clock is given to all ff at the same time (simultaneously)
 - ORI - given to indicate overriding i/p of PRESET if PR=0, Q=1; CLR=0, Q=0. Clearing of the counter when ORI = low, CLR=0, PR=0, where Q₀=1 (preset)

1011

pop

2



101

۷۲

PIPO

Q₃ 3 52

$$\frac{Q_A}{Q_B} = \frac{1}{2}$$

10 all

1.

100

100

next

OR I	clk	D_0	Q_1	Q_2	Q_3
T/T	x	1	0	0	0
1	↓	0	1	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1
1	↓	1	0	0	0

first cycle:

$$D_0 = 0, Q_0 = 1,$$

$$D_1 = 1, Q_1 = 0$$

$$D_2 = 0, Q_2 = 0$$

$$D_3 = 0, Q_3 = 0$$

first falling edge

$$D_0 = 0, Q_0 = 0$$

$$D_1 = 1, Q_1 = 1$$

$$D_2 = 0, Q_2 = 0$$

$$D_3 = 0, Q_3 = 0$$

second falling edge

$$D_0 = 0, Q_0 = 0$$

$$D_1 = 0, Q_1 = 0$$

$$D_2 = 1, Q_2 = 1$$

$$D_3 = 0, Q_3 = 0$$

Third falling edge:

$$D_0 = 0, Q_0 = 0$$

$$D_1 = 0, Q_1 = 0$$

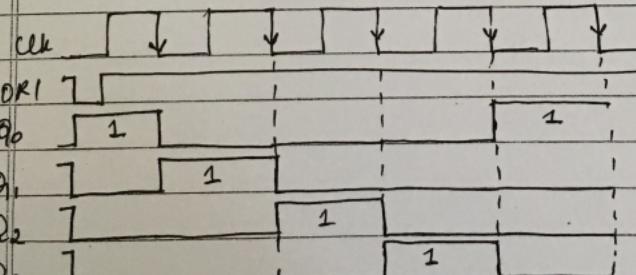
$$D_2 = 0, Q_2 = 0$$

$$D_3 = 1, Q_3 = 1$$

Fourth falling edge:

$$D_0 = 1, Q_0 = 1$$

$$D_1 =$$

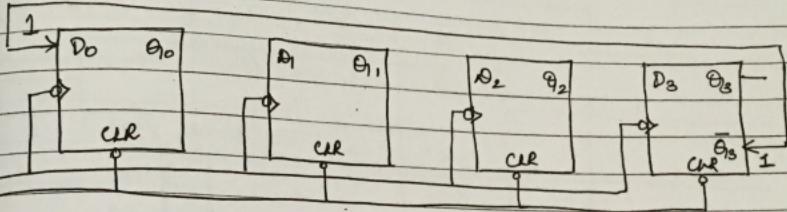


Qn
↓P

- in case of controlling several sequential operations
Ex: g

Johnson's Counter (Twisted / Switch Tail Ring Counter)

- No of states = twice the no of flip flops



CLR	CLK	Q ₀	Q ₁	Q ₂	Q ₃
1	X	0	0	0	0
1	↓	1	0	0	0
1	↓	1	1	0	0
1	↓	1	1	1	0
1	↓	1	1	1	1
1	↓	0	1	1	1
1	↓	0	0	1	1
1	↓	0	0	0	1

Using edge 1
 $Q_3 = 1, Q_0 = 1, Q_1 = 0, Q_2 = 0, Q_3 = 0, Q_0 = 0, Q_1 = 0, Q_2 = 0, Q_3 = 1$

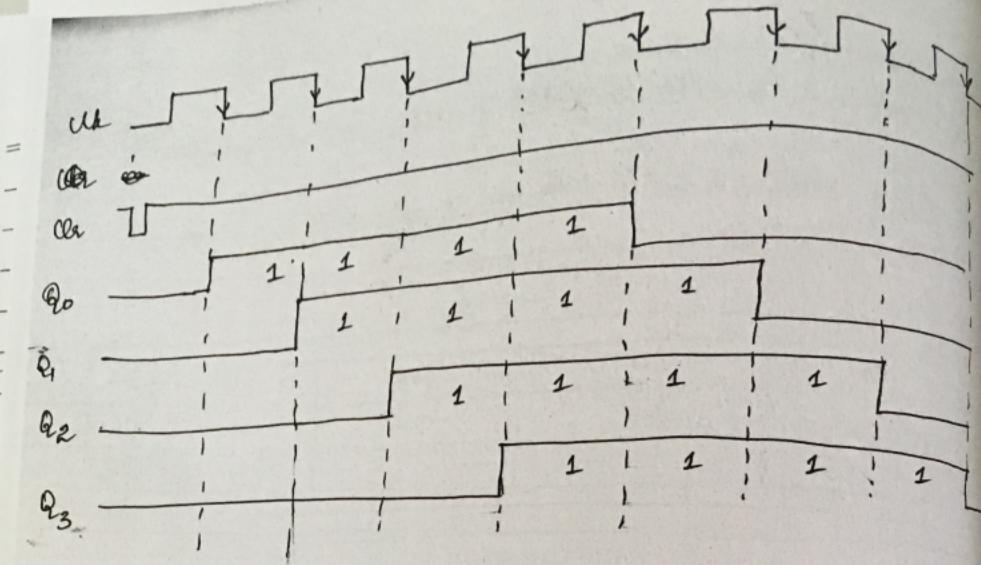
$Q_3 = 0, Q_0 = 1, Q_1 = 1, Q_2 = 0, Q_3 = 1$

$Q_3 = 0, Q_0 = 1, Q_1 = 1, Q_2 = 0, Q_3 = 1$

$Q_3 = 1, Q_0 = 0, Q_1 = 0, Q_2 = 1, Q_3 = 0$

$Q_3 = 0, Q_0 = 0, Q_1 = 1, Q_2 = 1, Q_3 = 0$

$Q_3 = 1, Q_0 = 1, Q_1 = 0, Q_2 = 1, Q_3 = 1$



Sequence Generators

To find the no. of flip flops required for the design of the sequence generator.

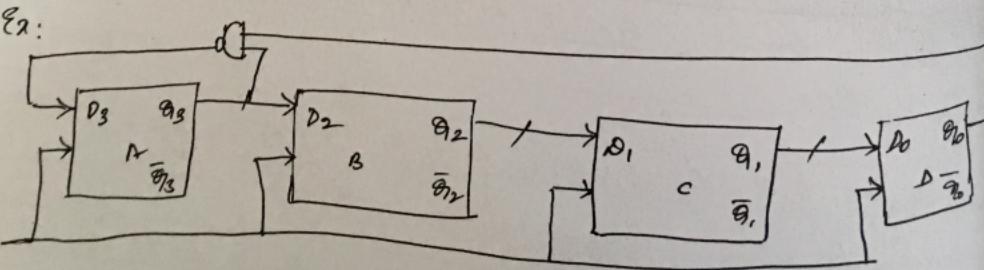
$$L \leq 2^n - 1$$

$L \rightarrow$ length of the sequence

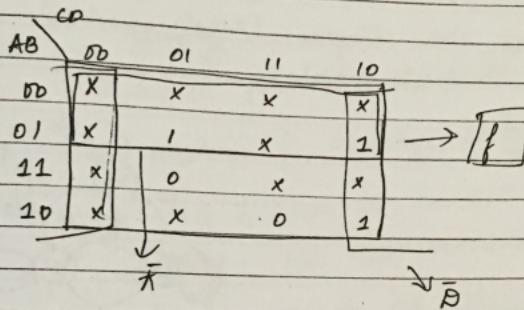
$n \rightarrow$ no of flip flops (min)

$$\text{Ex: } L=5, \quad 5 < 2^3-1$$

Ex:



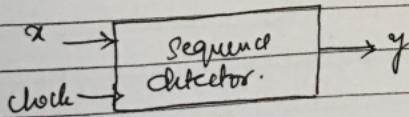
A	B	C	D	F
1	0	1	1	0
0	1	0	0	1
1	0	1	0	1
1	1	0	01	0
0	1	1	0	1



$$F = \overline{A} + \overline{B}$$

Sequence Detector.

- The stream of bit is fed as i/p , when the clock is high & a particular pattern / sequence is detected.
- Once the sequence is detected, the i/p becomes high & then becomes low.



Ex: Consider the sequence 010

- i) Overlapping (returning back to previous digit)
- ii) No overlapping

$$x = 0110\overset{b}{\underset{\downarrow}{0}}10100$$

of $y = \overset{\uparrow}{0}00001010$

Step 1:

Obtain the state diagram (Mealy machine)

S_0 = Reset (powerup)

S_1 = 0

S_2 = 01

Step 2:

State assignment

$S_0 = 00$

$S_1 = 01$

$\underline{S_2 = 10.}$

