Q. No.			Marks
1	a	A microprocessor is a _____ chip integrating all the functions of a CPU of a Computer. i) Single ii) Multiple iii) Double iv) Triple	1
	b	The purpose of the microprocessor is to control_____ i) memory ii) switches iii) processing iv) tasks	1
	c	In 8086 microprocessor , the address bus is_____ bit wide i) 12 bit ii) 10 bit iii) 16 bit iv) 20 bit	1
	d	The BP is indicated by i) base pointer ii) binary pointer iii) bit pointer iv) digital pointer	1
	e	The IF flag is i) Interrupt Flag ii) Initial Flag iii) Indicate Flag iv) Indirect Flag	1
	f	Which addressing mode is being used in the given instruction? MOV AX, [1234H] i) Base Addressing Mode ii) Immediate Addressing Mode iii) Register Addressing Mode iv) Direct Addressing Mode	1
	g	If we have single memory address then the numbers of operands allowed maximum, would be i) 1 ii) 2 iii) 3 iv) 4	1
	h	Which segment register is being used in the given instruction? MOV CX , SS: BX] i) Extra Segment Register (ES) ii) Code Segment Register (CS) iii) Stack Segment Register (SS) iv) None of the Above	1
	i	The Push instruction copies data from the source to the i) Stack ii) Memory iii) Register iv) Destination	1
	j	Which of the following is not a data copy/transfer instruction? i) MOV ii) PUSH iii) DAS iv) POP	1
	k	LEA copies the i) Physical Address ii) Effective address iii) Logical address iv) None	1
	l	The JS is called as i) jump the signed bit ii) jump single bit iii) jump simple bit iv) jump signal it	1
	m	ARM stands for _____ i) Advanced Rate Machines ii) Advanced RISC Machines iii) Artificial Running Machines iv) Aviary Running Machines	1
	n	RISC stands for _____ i) Restricted Instruction Sequencing Computer ii) Restricted Instruction Sequential Compiler iii) Reduced Instruction Set Computer iv) Reduced Induction Set Computer	1
	o	The main importance of ARM micro-processors is providing operation with _____ i) Low cost and low power consumption ii) Higher degree of multi-tasking iii) Lower error or glitches iv) Efficient memory management	1
	p	i) LEA copies the i) Physical Address ii) Effective address iii) Logical address iv) None	1
	q	Which among the following data processing instructions does not use the barrel shifter? i) ADD R2, R5, R4 ii) MOV R5, R4, LSL #2 iii) MOV r5, R4, LSR #2 iv) MOV r5, R4, ROR #2	1
	r	The Instruction , ADD #45 ,R1 does_____ i) Adds the value of 45 to the address of R1 and stores 45 in that address ii) Adds 45 to the value of R1 and stores it in R1	1

		iii) Finds the memory location 45 and adds that content tothat of R1 iv) None of the mentioned	
	s	ARM logical instructions perform _____logical operations on the two source registers i) bytewise ii) bitwise iii) wordwise iv) None of these	1
	t	In the case of Zero-address instruction method the operands are stored in _____ i) Registers ii) Accumulators iii) pushdown stack iv) Cache	1
2	a	With a neat diagram explain the memory map of a personal computer	8
	b	Explain 8086 multipurpose registers	8
3	a	Explain the following addressing modes of 8086 i) Register addressing mode ii) Register-Indirect addressing mode iii) Immediate Addressing mode iv) Direct addressing mode	8
	b	Explain Stack Addressing modes with suitable examples.	4
	c	Differentiate between Linear address and offset address .Calculate the physical address for the following. i)DS=2000H:DI=0200H ii) CS=1000h:IP=0A00	4
4	a	Explain the following Instructions with examples i) LEA ii) MOVS iii) INS iv) XLAT	8
	b	Write an ALP to perform the string operation for sorting a string in an ascending order.	8
5	a	Explain the important design rules of RISC philosophy.	8
	b	Which are the different features of ARM instruction set that make it suitable for embedded applications.	8
		OR	
6	a	With a neat diagram explain the different hardware components of an embedded device based on ARM core.	8
	b	Summarize the ARM instruction set.	8
7	a	Explain any four barrel Shifter operations.	8
	b	Explain the following instruction in ARM processor i) ADC ii) SUB iii) CMP iv) TEQ	8
		OR	
8	a	Explain the following Programming status register instructions i) CPSR ii) SPSR	8
	b	Explain the following Load-Store instructions i) LDR ii) STR iii) LDRB iv) STRB	8