

Number system :-

There are four number systems in arithmetic.
they are :-

- 1) Decimal number system.
- 2) Binary number system.
- 3) Hexadecimal number system.
- 4) Octal number system.

General rule for representing numbers in any number system is.

$$a_n a_{n-1} \dots a_2 a_1 a_0 = a_n r^n + a_{n-1} r^{n-1} + \dots + a_2 r^2 + a_1 r^1 + a_0 r^0$$

Where,

$a_n, a_{n-1}, \dots, a_0 \rightarrow$ Digits

$a_0 \rightarrow$ LSD - Least significant Digit

$a_n \rightarrow$ MSD - Most Significant Digit

$r \rightarrow$ Base of number system.

Conversions :-

Binary to Decimal conversions:-

i) $(110111)_2$.

$$\begin{aligned}(110111)_2 &= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \\ &= 32 + 16 + 0 + 4 + 2 + 1 \\ &= \underline{\underline{(55)_{10}}}\end{aligned}$$

ii) $(11101.1011)_2$,

$$\begin{aligned}&= 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} \\ &= 16 + 8 + 4 + 0 + 1 + \frac{1}{2} + 0 + \frac{1}{8} + \frac{1}{16} \\ &= \underline{\underline{(29.625)_{10}}}\end{aligned}$$

$$\text{iii) } (10110)_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 \\ = 16 + 0 + 4 + 2 + 0 \\ = \underline{\underline{(52)}_{10}}$$

$$\text{iv) } (10001101)_2 = 1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 \\ + 0 \times 2^0 \\ = 128 + 0 + 0 + 0 + 8 + 4 + 1 \\ = \underline{\underline{(141)}_{10}}$$

$$\text{v) } (10111, 1011)_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} \\ + 1 \times 2^{-3} + 1 \times 2^{-4} \\ = 16 + 0 + 4 + 2 + 1 + \frac{1}{2} + 0 + \frac{1}{8} + \frac{1}{16} \\ = 23 + 0.5 + 0.125 + 0.0625 \\ = \underline{\underline{(23.6875)}_{10}}$$

$$\text{vi) } (0.01\underline{\underline{1011}})_2 = 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} \\ = 0 + \frac{1}{4} + \frac{1}{8} + 0 + \frac{1}{32} + \frac{1}{64} \\ = 0.25 + 0.125 + 0.03125 + 0.015625 \\ = \underline{\underline{(0.421875)}_{10}}$$

$$\text{vii) } (\underline{\underline{10111}}, 101)_2 = 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + \\ 0 \times 2^{-2} + 1 \times 2^{-3} \\ = 32 + 16 + 0 + 4 + 2 + 1 + 0.5 + 0 + 0.125 \\ = \underline{\underline{(55.625)}_{10}}$$

Decimal, Binary, Octal and Hexadecimal numbers.

Decimal.	Binary	Octal.	Hexadecimal.
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Convert $(475.25)_8$ to its decimal equivalent.

$$\begin{aligned}
 (475.25)_8 &= 4 \times 8^2 + 7 \times 8^1 + 5 \times 8^0 + 2 \times 8^{-1} + 5 \times 8^{-2} \\
 &= 256 + 56 + 5 + 2 \times \frac{1}{8} + 5 \times \frac{1}{64} \\
 &= (317.32813)_{10}.
 \end{aligned}$$

$$(9B2.1A)_4 = (?)_{10}$$

$$\begin{aligned}
 &= 9 \times 16^2 + B(11) \times 16^1 + 2 \times 16^0 + 1 \times 16^{-1} + A(10) \times 16^{-2} \\
 &= 2304 + 176 + 2 + 1 \cdot \frac{1}{16} + 10 \cdot \frac{1}{256} \\
 &= 2304 + 176 + 2 + 0.0625 + 0.039 \\
 &= (2482.1)_{10}.
 \end{aligned}$$

$$* (3102.12)_4 = (?)_{10}$$

$$= 3 \times 4^3 + 1 \times 4^2 + 0 \times 4^1 + 2 \times 4^0 + 1 \times 4^{-1} + 2 \times 4^{-2}$$

$$= 192 + 16 + 0 + 2 + \frac{1}{4} + (2) \cdot \frac{1}{16}$$

$$= (210.375)_{10}$$

$$* (614.15)_7 = (?)_{10}$$

$$= 6 \times 7^2 + 1 \times 7^1 + 4 \times 7^0 + 1 \times 7^{-1} + 5 \times 7^{-2}$$

$$= 294 + 7 + 4 + \frac{1}{7} + 5 \cdot \frac{1}{49}$$

$$= 294 + 7 + 4 + 0.142857 + 0.102$$

$$= (305.24486)_{10}$$

Decimal to Binary conversion.

$$* (29)_{10} = (?)_2$$

$$= (11101)_2$$

$$\begin{array}{r} 2 | 29 \\ 2 | 14 - 1 \\ 2 | 7 - 0 \\ 2 | 3 - 1 \\ 1 - 1 \end{array} \quad \text{LSD.}$$

↑

MSD

$$* (25.375)_{10} = (?)_2$$

$$\begin{array}{r} 2 | 25 \\ 2 | 12 - 1 \\ 2 | 6 - 0 \\ 2 | 3 - 0 \\ 1 - 1 \end{array} \quad \text{LSD.}$$

↑

MSD.

$$\frac{0.375 \times 2}{0.750} = 0.$$

$$\frac{0.750 \times 2}{1.5} = 1.$$

Decimal to Octal conversion.

$$* (416.12)_{10} = (?)_8.$$

$$\begin{array}{r}
 8 | 416 \\
 8 | \underline{52} - 6 \\
 6 - 4
 \end{array}
 \quad
 \begin{array}{r}
 \frac{0.12 \times 8}{0.96} = 0. \\
 \frac{0.96 \times 8}{0.68} = 7 \\
 \frac{0.68 \times 8}{5.44} = 5 \\
 \frac{0.44 \times 8}{3.55} = 3. \\
 \frac{0.52 \times 8}{4.16} = 4. \downarrow
 \end{array}$$

$$(416.12)_{10} = (640.07534)_8$$

$$* (3964.63)_{10} = (3574.50243)_8$$

$$* (469)_{10} = (725)_8$$

Decimal to Hexadecimal conversion.

$$* (3509)_{10} = (?)_{16}.$$

$$\begin{array}{r}
 16 | 3509 \\
 16 | \underline{219} - 5. \uparrow \\
 16 | \underline{13} - 11. \left. \begin{array}{l} \\ B \end{array} \right\} \\
 0 - 13 \left. \begin{array}{l} \\ D \end{array} \right\}
 \end{array}$$

$$(3509)_{10} = (DB5)_{16}.$$

$$*(2604 \cdot 10546875)_{10} = (?)_{16}.$$

The whole number part is converted by repeated division by 16.

$$\begin{array}{r} 16 \mid 2604 \\ 16 \boxed{162} - 12(C) \\ 10(A) - 2 \end{array}$$

$$(2604)_{10} = (A2C)_{16}.$$

* The fraction part is converted by repeated multiplication by 16 and by keeping track of the integer.

$$\begin{array}{r} 0.10546875 \times 16 \\ \hline 1.6875 \quad -1. \\ \hline 0.6875 \times 16 \\ \hline 11.00 \quad -11(B). \end{array}$$

$$(0.10546875)_{10} = (.1B)_{16}.$$

$$(2604 \cdot 10546875)_{10} = (A2C \cdot 1B)_{16}.$$

Binary to Octal.

Octal number.	Binary equivalent
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1

- * For binary to octal conversion of whole numbers group the given binary number in groups of three starting from the right most [LSB] and replace each group by the octal number shown in above table.
- * For conversion of fraction part, make group of three starting with the left most bit.

$$\Rightarrow (101111)_2 = (?)_8$$

←
 101, 111
 5 7

$$\therefore (101111)_2 = (57)_8$$

$$\Rightarrow (1110.01101)_2 = (?)_8$$

<u>Whole number</u> $\underline{001}, 110$ add 1, 6.	<u>Fraction part</u> $\overbrace{011}^3 \overbrace{010}^2$ add. 3 2.
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$$(1110.01101)_2 = (16.32)_8$$

Octal numbers to binary.

* To convert octal to binary, simply replace each octal number by its equivalent.

$$\Rightarrow (724)_8 = (?)_2.$$

$$\begin{array}{r} 7 \quad 2 \quad 4 \\ 111 \quad 010 \quad 100 \end{array}$$

$$\therefore (724)_8 = (111\ 010\ 100)_2.$$

$$\Leftrightarrow (365.217)_8 = (?)_2 = (011110101 \cdot 010001111)_2$$

$$3) (0.506)_8 = (?)_2 = (0.101000110)_2.$$

1) Convert

$$\Rightarrow (284.65)_{10} = (?)_8 = (?)_{16}.$$

Integer part.

$$\begin{array}{r} 16 | 284 & 12 \\ 16 | 17 & 1 \\ \hline & 1 \end{array}$$

↑ LSD
↓ MSD

Fraction part :

$$\begin{array}{l} \frac{0.65 \times 16}{10.4} \rightarrow 10 = A \quad \downarrow \text{MSD} \\ \frac{0.4 \times 16}{6.4} \rightarrow 6 \quad \downarrow \\ \frac{0.4 \times 16}{6.4} \rightarrow 6 \quad \downarrow \text{LSD} \end{array}$$

$$(284.65)_{10} = (110.A66)_{16}.$$

$$\ast (110.A66)_{16} = 000,100,011,100 \cdot 101,001,100,110.$$

$$(110.A66)_{16} = (0434.5146)_8$$

$$\therefore (284.65)_{10} = (434.5146)_8 = (110.A66)_{16}.$$

11) Convert $(ABFE)_{16} = (?)_2 = (?)_{10}$.

$$(ABFE)_{16} = (1010\ 1011\ 1111\ 1110)_2.$$

$$(ABFE)_{16} = (10 \times 16^3) + (11 \times 16^2) + (15 \times 16^1) + (14 \times 16^0)$$

$$(ABFE)_{16} = (44030)_{10}.$$

$$(ABFE)_{16} = (1010101111110)_2 = (44030)_{10}.$$

$$2) \rightarrow (532.65)_{10} = (?)_{16} = (?)_2$$

[June -03, 4M]

Integer part

$$\begin{array}{r} 16 \overline{) 532 - 4} \\ 16 \overline{) 33 - 1} \\ 16 \overline{) 21 - 1 } \\ \hline \text{MSD.} \end{array}$$

$$(2114)_{16}$$

Fraction part

$$\begin{array}{r} 0.65 \times 16. \rightarrow 10 \\ 10.4 \\ 0.4 \times 16. \rightarrow 6 \\ 6.4 \\ 0.4 \times 16. \rightarrow 6 \\ 6.4 \\ \hline \text{LSD.} \end{array}$$

$$(0.A66)_{16}$$

$$\therefore (532.65)_{10} = (2114.A66)_{16}$$

$$(2114.A66)_{16} = (0010\ 0001\ 0100\cdot 1010.0110\ 0110)_2$$

$$\therefore (532.65)_{10} = (2114.A66)_{16} = (0010\ 0001\ 0100\cdot 1010.01100110)_2$$

$$ii) (ABCD)_{16} = (?)_2 = (?)_8$$

$$(ABCD)_{16} = (1010\ 1011\ 1100\ 1101)_2$$

$$(1,010,101,1\ 11,00\ 1,101)_2 = (125715)_8$$

$$(ABcD)_{16} = (1010\ 1011\ 1100\ 1101)_2 = (125715)_8$$

3) a) perform the following.

$$i) (57.6)_8 = (?)_2 = (?)_{16}$$

[Jan -04, 6M]

$$(57.6)_8 = (101111.110)_2 = (2F.C)_{16}$$

$$\text{i)} (193)_{16} = (?)_8 = (?)_{10}.$$

$$(193)_{16} = 0001 \ 1001 \ 0011.$$

$$(193)_{16} = (623)_8$$

$$(193)_{16} = (1 \times 16^2) + (9 \times 16^1) + (3 \times 16^0) = (403)_{10}$$

$$(57.6)_8 = (2F.C)_{16} = (403)_{10}.$$

$$4) \text{ convert } \text{i)} (526.44)_8 = (?)_2 = (?)_{10} \quad \boxed{\text{June -04, 6M}}$$

$$(526.44)_8 = (101010110).100100)_2.$$

$$(526.44)_8 = (5 \times 8^2) + (2 \times 8^1) + (6 \times 8^0) + (4 \times 8^{-1}) + (4 \times 8^{-2})$$

$$(526.44)_8 = (342 + 5625)_{10}.$$

$$(526.44)_8 = (101010110.100100)_2 = (342 + 5625)_{10}.$$

$$\text{i)} (48350)_{10} = (?)_{16} = (?)_8$$

$$\begin{array}{r} 16 \mid 48350 & 14 \\ \hline 16 \mid 3021 & 13 \\ \hline 16 \mid 188 & 12 \\ \hline 11 \quad (\text{B}) \\ \hline \end{array} \quad \begin{matrix} \text{MSD} \\ \uparrow \\ \text{LSD} \end{matrix}$$

$$(48350)_{10} = (BCDEF)_{16}.$$

$$\begin{array}{r} 8 \mid 48350 & 6 \\ \hline 8 \mid 6043 & 3 \\ \hline 8 \mid 755 & 3 \\ \hline 8 \mid 94 & 3 \\ \hline 8 \mid 11 & 6 \\ \hline 1 & 3 \\ \hline \end{array} \quad \begin{matrix} \text{MSD} \\ \uparrow \\ \text{LSD} \end{matrix}$$

$$(BCDEF)_{16} = (1011110011011110)_2 \\ = (136336)_8.$$

$$\text{OR. } (48350)_{10} = \underline{(136336)}_8$$

$$(48350)_{10} = (BCDEF)_{16} = (136336)_8.$$

4) Carryout the following conversion. Jan -05, 6M

i) $(F9AC.508B)_{16} = (?)_{10}$.

$$F=15, A=10, C=12, D=13.$$

$$\begin{aligned}(F9AC.508B)_{16} &= (15 \times 16^3) + (9 \times 16^2) + (10 \times 16^1) + (12 \times 16^0) + \\&\quad (5 \times 16^{-1}) + (3 \times 16^{-2}) + (8 \times 16^{-3}) + (11 \times 16^{-4}) \\&= (63916.36532)_{10}\end{aligned}$$

ii) $(457.248)_{16} = (?)_{10}$.

$$\begin{aligned}&= (4 \times 8^2) + (5 \times 8^1) + (7 \times 8^0) + (2 \times 8^{-1}) + \\&\quad (4 \times 8^{-2}) + (8 \times 8^{-3})\end{aligned}$$

$$(457.248)_{16} = (303.32226)_{10}$$

5) convert i) $(2AB.8)_{10} = (?)_{10} = (?)_8$

June -05, 4M

$$(2AB.8)_{16} = (?)_1 + 10 \times 16^1 + (11 \times 16^0) + (8 \times 16^{-1})$$

$$(2AB.8)_{16} = (683.5)_{10}.$$

$$\begin{array}{r} 001,010,1011.1000 \\ \text{= 1 2 5 3 . 4 0.} \end{array}$$

$$(2AB.8)_{16} = (1253.40)_8$$

$$(2AB.8)_{16} = (683.5)_{10} = (1253.40)_8.$$

$$\text{ii)} \quad (764.352)_8 = (?)_{16} = (?)_2$$

$$(764.352)_8 = 111\ 100\ 100.011\ 101\ 040.$$

$$= 1F4.F5.$$

$$(764.352)_8 = (1F4.F5)_{16}$$

$$(764.352)_8 = (1F4.F5)_{16} = (11110100.011101010)_2.$$

6) Convert the following

Jan-06, 4M

$$\text{i)} \quad (101010.101)_2 = (?)_{10}$$

$$= (1 \times 2^5) + (0 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1)$$

$$+ (0 \times 2^0) + (1 \times 2^{-1}) + (0 \times 2^{-2}) + (1 \times 2^{-3})$$

$$(101010.101)_2 = (42.625)_{10}$$

$$\text{ii)} \quad (7034)_8 = (?)_{10}$$

$$= (7 \times 8^3) + (0 \times 8^2) + (3 \times 8^1) + (4 \times 8^0)$$

$$(7034)_8 = (3612)_{10}.$$

$$\text{iii)} \quad (2616)_{10} = (?)_{16}.$$

$$(2616)_{10} = (A38)_{16}.$$

$$\begin{array}{r} 16 | 2616 \\ 16 | 163 \rightarrow 8 \\ \hline 10 \rightarrow 3 \\ \hline (A) \end{array} \quad \text{MSD} \quad \text{LSD}$$

$$\text{iv)} \quad (934)_{10} = (?)_8$$

$$(934)_{10} = (1646)_8$$

$$\begin{array}{r} 8 | 934 \\ 8 | 116 - 6 \\ \hline 14 - 4 \\ \hline 1 - 6 \\ \hline \end{array} \quad \text{MSD} \quad \text{LSB.}$$

$$\text{ii) } (ADGCB)_{16} = (?)_8 \\ = (1010 \ 1,101,011,011,001,011)_2$$

$$(ADGCB)_{10} = (255\ 3313)_2$$

$$\text{iii) } (11011,1011)_2 = (?)_8 \\ = \begin{array}{r} 11,011,101,1 \\ -3 \quad 3 \quad 5 \end{array}$$

$$(11011,1011)_2 = (33,54)_8$$

$$\text{iv) } (1011,11001)_2 = (?)_{10} \\ = (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^0) + (1 \times 2^5) + (1 \times 2^1) \\ + (1 \times 2^2) + (0 \times 2^3) + (0 \times 2^4) + (1 \times 2^5) \\ = (13,78125)_{10}.$$

$$(1011,11001)_2 = (13,78125)_{10}.$$

ii) Convert $(10110011010)_2$ into octal decimal & hexadecimal.

$$(10110011010)_2 = (?)_8 = (?)_{10} = (?)_{16} \quad \boxed{\text{June - 09, 8M}}$$

$$\rightarrow \begin{array}{r} 10,110,011,010 \\ -2 \quad 6 \quad 3 \quad 2 \end{array} = (2632)_8.$$

$$\rightarrow \begin{array}{r} 101,1001,1010 \\ -5 \quad 9 \quad A \end{array} = (59A)_{16}.$$

$$\rightarrow (1 \times 2^{10}) + (0 \times 2^9) + (1 \times 2^8) + (1 \times 2^7) + (0 \times 2^6) + (0 \times 2^5) \\ + (1 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (0 \times 2^0) \\ = (1434)_{10}.$$

$$\therefore (10110011010)_2 = (2632)_8 = (59A)_{16} = (1434)_{10}.$$

12) convert the following binary numbers to decimal numbers. Jan - 10, 5M

$$\text{i) } (1101)_2 = (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0). \\ = (13)_{10}.$$

$$\text{ii) } (10001)_2 = (1 \times 2^4) + (0 \times 2^3) + (0 \times 2^2) + (0 \times 2^1) + (1 \times 2^0). \\ = (17)_{10}.$$

$$\text{iii) } (10101)_2 = (1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (1 \times 2^1) + (0 \times 2^0) + (1 \times 2^0) \\ = (21)_{10}.$$

Binary Addition.

There are four basic cases of binary addition:

- 1) $0 + 0 = 0$
 - 2) $0 + 1 = 1$
 - 3) $1 + 0 = 1$
 - 4) $1 + 1 = 10$. [carry = 1, sum = 0]
-

* Add 13 & 10

$$\begin{array}{r}
 * (13)_{10} \\
 + (10)_{10} \\
 \hline
 (23)_{10}
 \end{array}
 \quad *
 \begin{array}{l}
 1^{\text{st}} \text{ convert decimal numbers into} \\
 \text{binary and then perform binary} \\
 \text{addition.} \\
 \text{i.e. } (13)_{10} \rightarrow 1101 \\
 (10)_{10} \rightarrow 1010 \\
 \hline
 (23)_{10} - (10111)_2
 \end{array}$$

* Add $(3.25)_{10}$ and $(5.75)_{10}$

Soln: 1st convert decimal numbers into its equivalent binary.

$$\begin{array}{r}
 \text{i.e. } (3.25)_{10} = (11.01)_2 \quad 11.01 \\
 + (5.75)_{10} = (101.11)_2 \quad 101.11 \\
 \hline
 (9.00)_{10} \quad \quad \quad (1001.00)_2
 \end{array}$$

* Add. 111.111 & 111.

$$\begin{array}{r}
 111.111 \\
 111.000 \\
 \hline
 1110.111
 \end{array}
 \quad \text{i.e. } \underline{1110.111}$$

Binary Subtraction.

There are 4 basic cases of binary subtraction

1) $0 - 0 = 0$.

2) $1 - 0 = 1$.

3) $\begin{matrix} 0 \\ (10) \end{matrix} - 1 = 1$.

4) $1 - 1 = 0$.

1) $1101 - 1010$. Step 1 :- 1101 .

$$\begin{array}{r} \\ - 1010 \\ \hline \end{array}$$

Step 2 :- 1001 .

$$\begin{array}{r} \\ - 1010 \\ \hline 0011 \end{array}$$

1's Complement :-

The 1's complement of any binary number is obtained by changing each 0's in the number by 1 and each 1's in the number by a 0.

Ex : i) $1001 \rightarrow$ 1's compliment is 0110 .

ii) $11010111 \rightarrow$ 1's compliment is 00101000 .

Subtraction using 1's complement :-

There are two cases.

Case 1 : When the subtrahend (number to be subtracted) is smaller than the minuend.

PROCEDURE :-

- i) Get the 1's complement of subtrahend.
 - ii) Add it with minuend.
 - iii) If carry is present add it to the result, Answer is positive.
 - iv) If carry is not present, take 1st complement of the result and place "a negative sign with result"
-
-

1) $(1101)_2 - (1000)_2 = (?)_2$

i) Taking 1's complement of subtrahend $\rightarrow 0111$.

ii) Add it with minuend i.e. 1101
 $+ 0111$
Carry $\rightarrow \underline{\underline{1}}0100$

iii) If carry is present, add it to the result and answer is +ve.

$$\begin{array}{r} 0100 \\ + 1 \\ \hline 0101 \end{array}$$

2) $110010 - 101101$.

i) $101101 \rightarrow$ j's complement \rightarrow ~~0~~ 010010 .

ii) 110010
 010010
Carry $\underline{\underline{1}}000100$

iii) 000100
 $j.$
 $+ \underline{\underline{000101}}$ Result is +ve.

$$3) \quad 1101011 - 1110101.$$

i) Complement 0001010.

ii) $\begin{array}{r} 1101011 \\ + 0001010 \\ \hline 1110101 \end{array}$.

$$\begin{array}{r} 1110101 \\ - 0001010 \\ \hline \end{array}$$

iii) 1110101.
iv) No carry : Answer is negative.

Taking 1's complement of the result and place a -ve sign with the result.

$$\boxed{-0001010}$$

$$4) \quad (11101)_2 - (11000)_2 = (?)_2.$$

* $\begin{array}{r} 11101 \\ - 11000 \\ \hline \end{array}$ ← Minuend

$\begin{array}{r} 00111 \\ - 11000 \\ \hline \end{array}$ ← 1's complement of Subtrahend.

Carry $\begin{array}{r} 1 \\ 00100 \\ \hline \end{array}$

* $\begin{array}{r} 00100 \\ - 1 \\ \hline 00101 \end{array}$.

$$5) \quad (11000)_2 - (11101)_2 = (?)_2.$$

$\begin{array}{r} 11000 \\ - 11101 \\ \hline \end{array}$ ← Minuend

$\begin{array}{r} 00010 \\ - 11101 \\ \hline \end{array}$ ← 1's complement of Subtrahend.

$\begin{array}{r} 11010 \\ - 11101 \\ \hline \end{array}$ ← Result.

* 1's complement the result and put -ve sign.

$$-(00101)_2.$$

Ex: $(1101)_2 \rightarrow$

- Taking 1's complement.
- Add 1 to 1's complement result
i.e. $1101 \rightarrow 0010$.

$$\begin{array}{r} & 1 \\ & \underline{0010} \end{array}$$

Subtraction using 2's complement :-

Procedure :-

- 1) Determine the 2's complement of Subtrahend.
 - 2) Add it with minuend.
 - 3) If there is a carry, discard it. Answer is positive.
 - 4) If there is No carry. Answer is negative. Taking 2's complement of the result and place a negative sign with result.
-

2's complement : Get 1's complement of a number and add 1 to it, to get 2's complement.

Ex: i) $1111 \rightarrow 0000 \leftarrow$ 1's complement
 $\begin{array}{r} 1 \\ + 0000 \\ \hline 0001 \end{array} \leftarrow$ add 1.
 $\underline{0001} \leftarrow$ 2's complement.

ii) $1101 - 1010$.

$$\text{Soln: } \begin{array}{r} 1101 \\ + 0110 \\ \hline \text{carry} \rightarrow (1) \underline{0011} \end{array} \quad \begin{array}{r} 1010 \\ 0101 \\ \hline 1 \\ 0110 \end{array}$$

* Discard (neglect) carry and result is +ve.
 $+ (0011)_2$

2) $110001 - 110101$.

$$\begin{array}{r} 110001 \\ + 001011 \\ \hline 111100 \end{array} \quad \begin{array}{r} 110101 \\ 001010 \\ \hline 1 \\ 001011 \end{array}$$

- * No carry \therefore Answer is negative.
- * Taking 2's complement of the result and place -ve sign.

$$111100 \rightarrow \begin{array}{r} 11 \\ 000011 \\ 1 \\ -(000100) \end{array}_2$$

3) $1101 - 110$

Soln: Note: Number of bits in subtrahend should be equal to number of bits in minuend.

\therefore In above problem, 0 is added to 110 to make it 0110.

$$\begin{array}{r} 1101 \\ 1010 \\ \hline \text{neglect } (1) \underline{0111} \end{array} \quad \begin{array}{r} 0110 \\ 1001 \\ \hline 1 \\ 1010 \end{array} \leftarrow 2\text{'s complement.}$$

Add the following using 2's complement:

1) 125 & -68.

Soln: 1st convert the decimal number to its equivalent binary number.

$$(125)_{10} = (1111101)_2 \quad \begin{array}{r} 2 | 125 \\ 62 - 1 \\ 34 - 0 \end{array} \quad (68)_{10} = (1000100)_2$$

$$\begin{array}{r} 1111101 \\ 1000100 \\ \hline \end{array} \leftarrow \text{Taking 2's complement.}$$

$$\begin{array}{r} 1111101 \\ 0111100 \\ \hline (1) \underline{0111100} \\ \text{neglect carry.} \end{array} \quad \begin{array}{r} 1000100 \\ 0111011 \\ \hline 1 \\ 0111100 \end{array} \leftarrow 2\text{'s complement.}$$

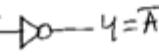
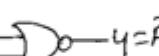
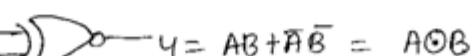
$$(0111001)_2 = (57)_{10}.$$

Logic Gates :-

A logic gate is a logic circuit with one o/p & two or more I/p's. The o/p signal is produced when there is a specified combination of I/p signals.

NOTE :-

- * Only NOT gate has one I/p.
- * The various types of gates are:-

<u>NOT</u> : 	<u>AND</u> : 
<u>OR</u> : 	<u>NAND</u> : 
<u>NOR</u> : 	<u>EX-OR</u> : 
<u>EX-NOR</u> : 	

Basic Boolean logic operation :-

Basic logic operations are :-

- 1> AND operation (Logical Multiplication).
- 2> OR operation (Logical Addition)
- 3> NOT operation (Logical complementing).

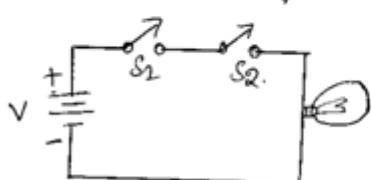
* In boolean algebra the constants & variables are allowed to have only two possible values 0 & 1, other terms used for representing 0 & 1 are as follows:

0	1
Logic 0	Logic 1
false	True
OFF	ON
Low	High
open switch	closed switch
NO	YES.

AND Gate :-

- * An AND Gate has two or more I/p's and a single o/p.
- * AND gate is an electronic circuit in which all the I/p's must be HIGH in order to have HIGH o/p.

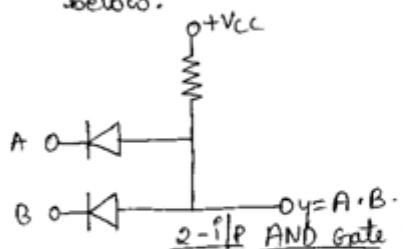
The AND function can be explained by following series - switching circuit.



Input		Output
S_1	S_2	
Open (low)	Open (low)	Lamp OFF (low)
open (low)	close (high)	Lamp OFF (low)
Close (high)	open (low)	Lamp OFF (low)
close (high)	close (high)	Lamp ON (high)

- * the lamp will glow only if the switches A & B are simultaneously ON.

A diode logic for an AND gate is shown in figure below.



Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table for 2 Input AND Gate.

- case 1 : When A=0V & B=0V

When both voltages A & B are low, the cathodes of both diodes are grounded. The diodes get forward biased & hence they conduct & the o/p voltage becomes zero.

case 2 : When A=0 & B=1 (high) :-

- * Since A is low (grounded), the +ve supply voltage V_{cc} forward biases the diode D₁ & the diode D₁ conducts. Hence the o/p voltage becomes zero.
- * Diode D₂ is reverse biased hence it does not conduct.
∴ o/p is low.

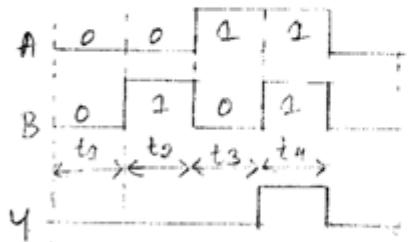
case 3 : When A=1 & B=0 :-

- * Since voltage B is low (grounded), the +ve supply voltage V_{cc} forward biases the diode D₂ & the diode D₂ conducts. Hence the o/p voltage is zero.
- * Diode D₁ is reversed biased, hence it does not conduct.
∴ o/p is low.

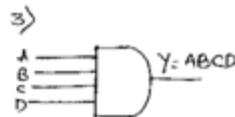
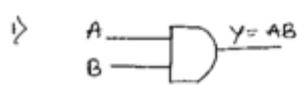
case 4 : When A = 1 & B = 1 :-

When both voltages A & B are high (+5V), both diodes get reversed biased, hence they do not conduct. Thus V_{cc} appears across o/p. i.e. o/p becomes HIGH.

Timing diagram for 2-I/P AND Gate :-



Logic symbol :-



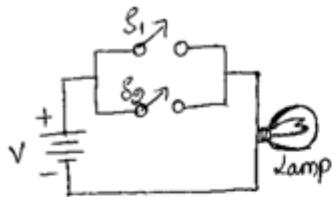
AND Laws :-

1. $AB = BA$
2. $AA = A$
3. $A \cdot 1 = A$
4. $A \cdot 0 = 0$
5. $A \cdot \bar{A} = 0$
6. $ABC = AB(C) = A(BC)$
7. $A(B+C) = AB + AC$

OR Gate :-

* The o/p of an OR gate is high if any one I/p is high or more I/p's have one.

The OR function can be explained by following parallel switching circuit.



Input		Output
S_1	S_2	
open (low)	open (low)	Lamp OFF (low)
open (low)	open (high)	Lamp ON (high)
close (high)	open (low)	Lamp ON (high)
close (high)	close (high)	Lamp ON (high)

* The circuit consists of a battery, a lamp & 2 parallel switches S_1 & S_2 . If any one of the switch is closed then lamp glows.

* S_1, S_2 are I/p's.

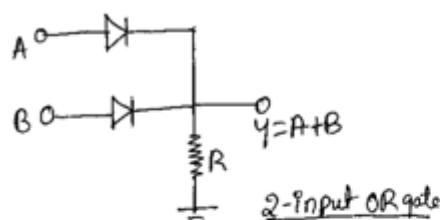
Switch closed = 1

Switch open = 0

Lamp glows = 1

Lamp OFF = 0

* The diode circuit for a 2-I/p OR gate is given below:



Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Truth table for 2-input OR gate

* A & B are I/p's. A & B will have I/p voltages of either 0V & 5V. Y is the O/p.

case 1 : When A=0 & B=0 :-

Both diodes are NOT conducting \therefore O/p Y is low.

case 2 : When A=0 & B=1 :-

Diode D_1 does not conduct. Diode D_2 conduct

\therefore O/p Y is High.

Case 3 : When A=1 & B=0 :-

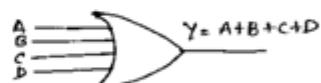
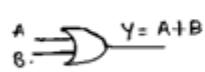
Diode D_1 conducts & diode D_2 does not conduct.

\therefore o/p Y is High.

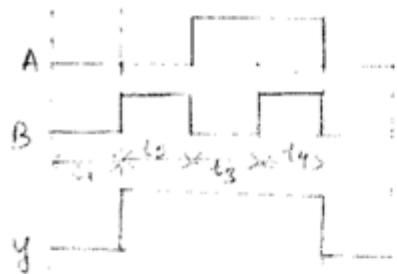
Case 4 : When A=1 & B=1 :-

Both diodes are forward biased. \therefore o/p Y is High.

* OR gate symbol for 2-IIP, 3-IIP & 4-IIP are shown below.



Timing Diagram :-



Timing diagram for 2-input OR Gate

OR Laws :-

1) $A + 0 = A$

2) $A + 1 = 1$

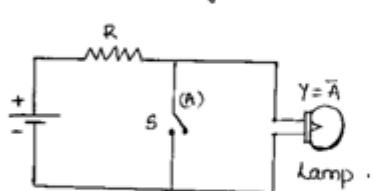
3) $A + A = A$

4) $A + B = B + A$

5) $A + B + C = (A + B) + C = A + (B + C)$.

NOT Gate :-

- * A gate that performs the mathematical operation of taking the complement is called a NOT gate.
- * A NOT circuit has a single I/p & single O/p. NOT gate can be analysed by the circuit below.



I/p	O/p
Switch open (LOW)	Lamp ON (High)
Switch close (High)	Lamp OFF (Low).

$$Y = \bar{A}$$

- * When switch A is open, bulb glows \therefore current will flow through the lamp.
- * When switch A is closed, all current flows through short circuit & bulb will be OFF.

Realization of NOT gate using transistor :-

- * When $A = \text{High}$, transistor is turned ON & acts as a short circuit. Thus entire V_{cc} flows to ground. \therefore O/p is LOW.
- * When $A = \text{Low}$, transistor is turned OFF & acts as an open circuit. Thus entire V_{cc} appears across o/p. \therefore o/p is HIGH.

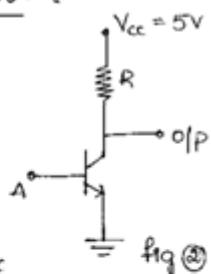


fig ②

Timing diagram:-



output of an inverter for pulse input.

NOT Laws:-

- $\bar{\bar{A}} = A$
- $A \cdot \bar{A} = 0$
- $A + \bar{A} = 1$
- $A + \bar{A}B = A + B$.

Boolean Algebra

Rules in Boolean Algebra :-

Rule 1 : $0 + \begin{matrix} 0 \\ 1 \end{matrix} = \begin{matrix} 0 \\ 1 \end{matrix} \Rightarrow 0+A=A \text{ or } A+0=A$

Rule 2 : $1 + \begin{matrix} 0 \\ 1 \end{matrix} = \begin{matrix} 1 \\ 1 \end{matrix} \Rightarrow 1+A=1 \text{ or } A+1=1$

Rule 3 : $0 + \begin{matrix} 0 \\ 1 \end{matrix} = \begin{matrix} 0 \\ 1 \end{matrix} \Rightarrow A+A=A$

Rule 4 : $0 + \begin{matrix} 1 \\ 0 \end{matrix} = \begin{matrix} 1 \\ 1 \end{matrix} \Rightarrow A+\bar{A}=1 \text{ or } \bar{A}+A=1$

Rule 5 : $0 \cdot \begin{matrix} 0 \\ 1 \end{matrix} = 0 \Rightarrow 0 \cdot A = 0 \text{ or } A \cdot 0 = 0$

Rule 6 : $1 \cdot \begin{matrix} 0 \\ 1 \end{matrix} = \begin{matrix} 0 \\ 1 \end{matrix} \Rightarrow 1 \cdot A = A \text{ or } A \cdot 1 = A$

Rule 7 : $0 \cdot \begin{matrix} 0 \\ 1 \end{matrix} = \begin{matrix} 0 \\ 1 \end{matrix} \Rightarrow A \cdot A = A$

Rule 8 : $0 \cdot \begin{matrix} 1 \\ 0 \end{matrix} = 0 \Rightarrow A \cdot \bar{A} = 0 \text{ or } \bar{A} \cdot A = 0$

Rule 9 : $\begin{matrix} \bar{0} \\ \bar{1} \end{matrix} = \begin{matrix} 0 \\ 1 \end{matrix} \Rightarrow \bar{\bar{A}} = A \text{ (Involution)}$

DeMorgan's Theorems:-

i) $\bar{AB} = \bar{A} + \bar{B}$

The complement of a product is equal to the sum of the complements.

A	B	\bar{AB}	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

v) $\overline{A+B} = \overline{A} \cdot \overline{B}$

the complement of a sum is equal to the product
of the complements.

A	B	$A+B$	$\overline{A} \cdot \overline{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Additional Rules in Boolean Algebra :-

* These rules are derived from the basic rules & laws
of boolean algebra.

1) $A + AB = A$

Proof :- $A + AB = A[1+B] \quad \because [1+B] = 1$
 $= A(1) \quad \because A \cdot 1 = A$

$$\boxed{A+AB = A}$$

2) $A + \overline{A}B = A + B$

Proof :- $A + \overline{A}B = A + AB + \overline{A}B \quad \because A + AB = A$
 $= A + B[A + \overline{A}] \quad \because A + \overline{A} = 1$
 $= A + B(1) \quad \because B \cdot 1 = B.$

$$\boxed{A+\overline{A}B = A+B}$$

3) $A(A+B) = A$

Proof :- $A(A+B) = AA + AB \quad \because A \cdot A = A$
 $= A + AB \quad \because (1+B) = 1$
 $= A[1+B]$
 $= A(1)$

$$\boxed{A(A+B) = A}$$

4) $(A+B)(A+C) = A + BC$

Proof :- $(A+B)(A+C) = AA + AC + AB + BC \quad \because [1+A] = 1$
 $= A + AC + AB + BC \quad \because [1+A+B] = 1$
 $= A[1 + C + B] + BC \quad \because [1 + A + B + X] = 1$
 $= A(1) + BC$

$$(A+B)(A+C) = A + BC$$

Simplification of Boolean Algebra :-

1. prove $A + BC = (A+B)(A+C)$

$$\begin{aligned}
 A + BC &= A \cdot 1 + BC && \because (1+B) = 1 \\
 &= A(1+B) + BC && (1+A) = 1 \\
 &= A + AB + BC && (1+C) = 1 \\
 &= A(1+C) + AB + BC && (A+A) = A \\
 &= A + AC + AB + BC && \\
 &= A \cdot A + AC + AB + BC && \\
 &= A[A+C] + B[A+C] && \\
 &= [A+C](A+B)
 \end{aligned}$$

$$A + BC = (A+B)(A+C).$$

2. prove $AB + BC + \bar{B}C = AB + C$

$$\begin{aligned}
 AB + BC + \bar{B}C &= AB + C [B + \bar{B}] && \because B + \bar{B} = 1 \\
 AB + BC + \bar{B}C &= AB + C
 \end{aligned}$$

3. Simplify $A(AB+C)$.

$$\begin{aligned}
 A(AB+C) &= AAB + AC && AAB = AB \\
 &= AB + AC. \\
 A(AB+C) &= A(B+C).
 \end{aligned}$$

4. $\bar{A}B + AB + \bar{A}\bar{B} = B[\bar{A}+A] + \bar{A}\bar{B}$

$$\begin{aligned}
 &= B + \bar{A}\bar{B} && 1 + \bar{A} = 1 \\
 &= (B+\bar{A})(B+\bar{B}) && \because (B+\bar{A})(B+\bar{B}) = B + \bar{A}\bar{B} \\
 &= \bar{A} + B && BB + B\bar{B} + \bar{A}B + \bar{A}\bar{B} \\
 & && B + \bar{A}B + \bar{A}\bar{B} \\
 & && B[1+\bar{A}] + \bar{A}\bar{B} \\
 & && B + \bar{A}\bar{B} \\
 &\Rightarrow [\bar{B} + \bar{B}] = 1.
 \end{aligned}$$

$$\begin{aligned}
 5) \quad A + A\bar{B} + \bar{A}B &= A[1 + \bar{B}] + \bar{A}B \\
 &= A + \bar{A}B \\
 &= (A + \bar{A})(A + B) \\
 &= \underline{\underline{A + B}}
 \end{aligned}$$

$$\begin{aligned}
 6) \quad Y &= (\bar{A} + B)(A + B) \\
 Y &= \bar{A}A + \bar{A}B + AB + BB \\
 &= \bar{A}B + AB + B \\
 &= B[\bar{A} + A + 1] \\
 \boxed{Y = B}
 \end{aligned}$$

$$\begin{aligned}
 7) \quad \text{Show that } ABC + A\bar{B}C + A\bar{B}\bar{C} &= A(B+C) \\
 ABC + A\bar{B}C + A\bar{B}\bar{C} &= AC[B + \bar{B}] + A\bar{B}\bar{C} \\
 \therefore (c+\bar{c})(B+c) &= cB + cc + B\bar{c} + c\bar{c} \\
 &= c + Bc + B\bar{c} \\
 &= c[1+e] + B\bar{c} \\
 (c\bar{c})(B+c) &= c + B\bar{c}
 \end{aligned}$$

$$\begin{aligned}
 8) \quad \text{P.T. } \overline{AB + \bar{A} + AB} &= 0 & \overline{A + B + C} &= \bar{A}\bar{B}\bar{C} \\
 \overline{AB} + \bar{A} \cdot \overline{AB} &= 0 & AAB &= AB \\
 ABA + \overline{AB} &= 0 & \overline{AB} &= \bar{A} + \bar{B} \\
 AB(\bar{A} + \bar{B}) &= 0 & A\bar{A} &= 0 \\
 A\bar{A}B + ABB &= 0 & A\bar{A}B &= 0 \\
 0 + 0 &= 0, & B\bar{B} &= 0 \\
 0 &= 0 & ABB &= 0, \\
 \text{LHS} &= \text{RHS} & &
 \end{aligned}$$

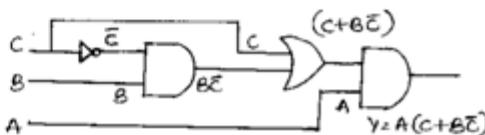
$$\begin{aligned}
 9) \quad Y &= (A+B\bar{C})(\bar{A}+B+\bar{C}) \\
 &= A\bar{A} + AB + A\bar{C} + \bar{A}B\bar{C} + BB\bar{C} + B\bar{C}\bar{C} \\
 &= AB + A\bar{C} + \bar{A}B\bar{C} + B\bar{C} + B\bar{C} \\
 &= AB + A\bar{C} + B\bar{C} [1+1+\bar{A}] \\
 Y &= AB + A\bar{C} + B\bar{C}
 \end{aligned}$$

10) Simplify the following boolean expressions & realize using logic gates.

$$\begin{aligned}
 Y &= ABC + A\bar{B}C + A\bar{B}\bar{C} \quad B + \bar{B} = 1 \\
 &= AC[B + \bar{B}] + A\bar{B}\bar{C} \quad \because A + \bar{A}B = A + B \\
 &= AC(1) + A\bar{B}\bar{C} \quad \text{Hence } C + \bar{C}B = C + B
 \end{aligned}$$

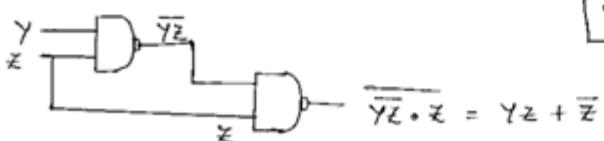
$$Y = A[C + B\bar{C}]$$

$$Y = A(C + B)$$



Realize Using NAND gate

$$\begin{aligned}
 11) \quad XY\bar{Z} + X\bar{Y}Z + Y\bar{Z} + \bar{Z} &\quad \because A + A = A \\
 &= XY\bar{Z} + X\bar{Y}Z + Y\bar{Z} + \bar{Z} \quad XY\bar{Z} + X\bar{Y}Z = XY\bar{Z} \\
 &= XY\bar{Z} + Y\bar{Z} + \bar{Z} \\
 &= Y\bar{Z}[1 + X] + \bar{Z} \quad \because \overline{YZ} \cdot Z \\
 &= Y\bar{Z} + \bar{Z} \quad \overline{YZ} + \bar{Z} \\
 &= \boxed{YZ + \bar{Z}}
 \end{aligned}$$



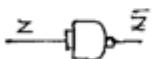
$$16) \quad Y = (A + \bar{B}C) \underbrace{(\bar{A} + B + \bar{C})}_{X^4} (A + \bar{B})$$

$$\begin{aligned}
 Y &= (A + \bar{B}C) (\bar{A}\bar{A} + \bar{A}\bar{B} + AB + B\bar{B} + A\bar{C} + \bar{B}\bar{C}) \\
 &= (A + \bar{B}C) \underbrace{(\bar{A}\bar{B} + AB + A\bar{C} + \bar{B}\bar{C})}_{X^4} \\
 &= A\cancel{\bar{A}\bar{B}} + AAB + AA\bar{C} + A\bar{B}\bar{C} + \cancel{A\bar{B}\bar{B}C} + \cancel{A\bar{B}BC} + \cancel{A\bar{C}BC} \\
 &= AAB + AA\bar{C} + A\bar{B}\bar{C} + \cancel{A\bar{B}\bar{B}C} \\
 &= AB + A\bar{C} + A\bar{B}\bar{C} + \cancel{A\bar{B}C} \\
 &= AB + A\bar{C} [1 + \bar{B}] + \cancel{A\bar{B}C}. \quad \because 1 + \bar{B} = 1.
 \end{aligned}$$

$$Y = AB + A\bar{C} + A\bar{B}C$$

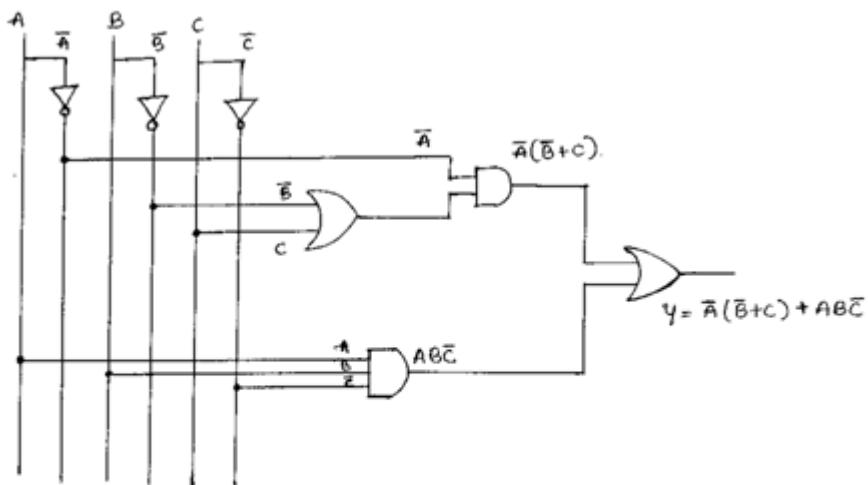
$$17) \quad \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z}$$

$$\begin{aligned}
 &= \bar{X}\bar{Y}\bar{Z} + [\bar{X} + \bar{Y}]\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z} \quad 1 + \bar{X} = 1 \\
 &= \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Z} + \bar{Y}\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z} \\
 &= \bar{Y}\bar{Z} [1 + \bar{X}] + \bar{X}\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z} \\
 &= \bar{Y}\bar{Z} + \bar{X}\bar{Z} + \bar{Y}\bar{Z} + X\bar{Z} \quad \bar{A} + \bar{A} = A \\
 &= \bar{Y}\bar{Z} + \bar{X}\bar{Z} + X\bar{Z} \quad \bar{Y}\bar{Z} + \bar{Y}\bar{Z} = \bar{Y}\bar{Z} \\
 &= \bar{Y}\bar{Z} + \bar{Z}[\bar{X} + X] \\
 &= \bar{Y}\bar{Z} + \bar{Z}[1] \\
 &= \bar{Z}[1 + \bar{Y}] \quad 1 \times \bar{Y} = 1. \\
 &= \bar{Z}
 \end{aligned}$$



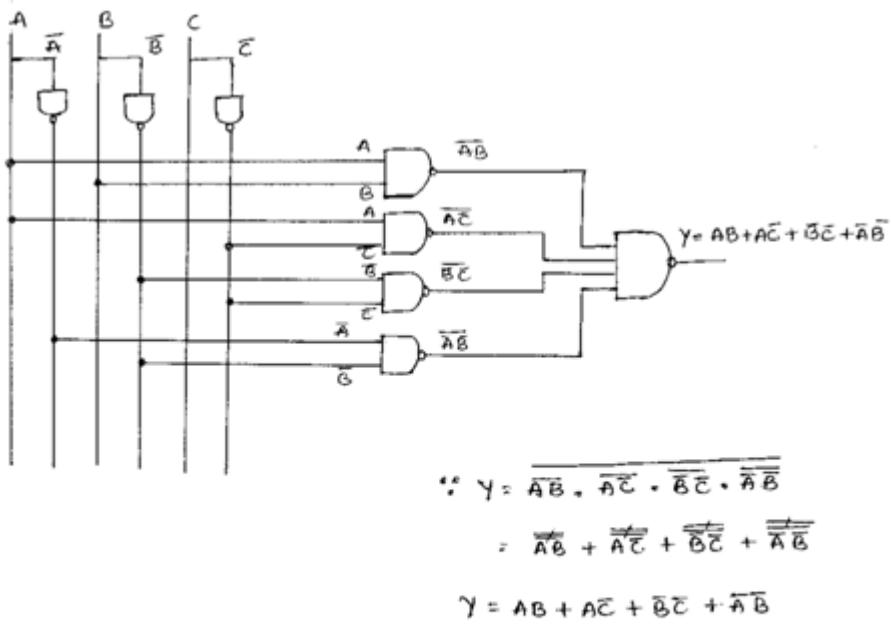
$$\begin{aligned}
 18) & (A + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})(\bar{A} + B) \\
 & = (A + \bar{B} + C)[\cancel{\bar{A}\bar{A}} + \cancel{\bar{A}B} + \cancel{\bar{A}\bar{B}} + \cancel{B\bar{B}} + \cancel{\bar{A}\bar{C}} + \cancel{B\bar{C}}] \quad \because \bar{A}\bar{A} = \bar{A} \\
 & = (A + \bar{B} + C)[\cancel{\bar{A}} + \cancel{\bar{A}B} + \cancel{\bar{A}\bar{B}} + \cancel{\bar{A}\bar{C}} + \cancel{B\bar{C}}] \\
 & = (A + \bar{B} + C)[\bar{A}(1 + \bar{B}) + \bar{A}B + \bar{A}\bar{C} + B\bar{C}] \\
 & = (A + \bar{B} + C)[\bar{A} + \bar{A}B + \cancel{\bar{A}\bar{C}} + B\bar{C}] \\
 & = (A + \bar{B} + C)[\bar{A}[1 + \bar{C}] + \bar{A}B + B\bar{C}] \\
 & = (A + \bar{B} + C)[\bar{A} + \bar{A}B + B\bar{C}] \\
 & = (A + \bar{B} + C)[\bar{A}(1 + B) + B\bar{C}] \\
 & = (A + \bar{B} + C)[\bar{A} + B\bar{C}] \\
 & = A\bar{A} + AB\bar{C} + \bar{A}\bar{B} + B\bar{B}\bar{C} + \bar{A}C + BC\bar{C} \\
 & = \bar{A}\bar{B} + \bar{A}C + ABC \\
 & = \bar{A}[\bar{B} + C] + ABC.
 \end{aligned}$$

Realize using logic gates.



19) Simplify & realize using only NAND gates.

$$\begin{aligned}
 & (A + \bar{B} + C) \underbrace{(\bar{A} + B + \bar{C})}_{\text{why?}} (A + \bar{B}) \\
 & = [\bar{A}\bar{A} + AB + A\bar{C} + \bar{A}\bar{B} + B\bar{B} + \bar{B}\bar{C} + \bar{A}C + BC + C\bar{C}] (A + \bar{B}) \\
 & = [AB + A\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}C + \bar{A}C + BC] (A + \bar{B}) \\
 & = AAB + AAC + A\bar{B}\bar{B} + A\bar{B}\bar{C} + A\bar{A}C + ABC + A\bar{B}\bar{B} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{B} + \\
 & \quad \bar{B}\bar{B}\bar{C} + \bar{A}\bar{B}C + B\bar{B}C \\
 & = AB + A\bar{C} + A\bar{B}\bar{C} + ABC + A\bar{B}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} \\
 & = AB + ABC + A\bar{B}\bar{C} + A\bar{C} + A\bar{B}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} \\
 & = AB[1+C] + AC[1+B] + BC[1+A] + \bar{A}\bar{B}[1+C] \\
 & = AB + AC + BC + \bar{A}\bar{B}
 \end{aligned}$$

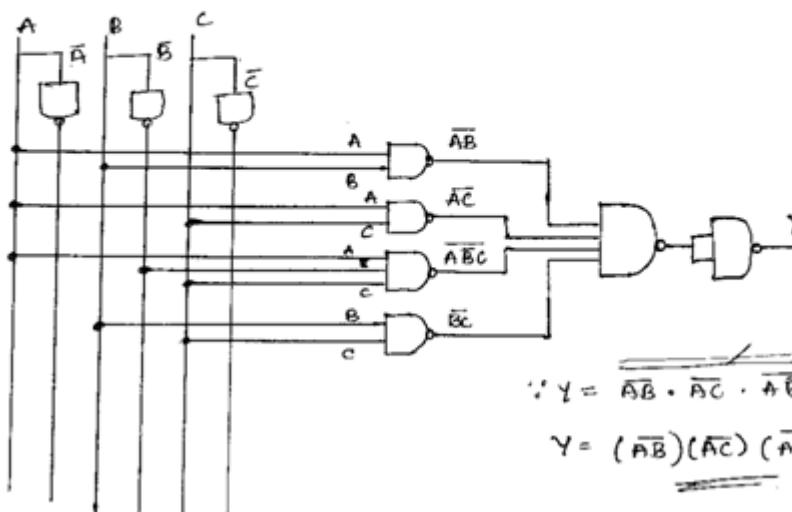


80.

$$Y = \overbrace{(A + \bar{B} + C) (\bar{B} + B + C) (A + B)}^{X^4} \dots$$

$$\begin{aligned}
 Y &= (A + \bar{B} + C) [\cancel{\bar{B}\bar{A}} + AB + AC + \bar{A}B + \cancel{B} + \cancel{BC}] \\
 &= (A + \bar{B} + C) [AB + AC + \bar{A}B + B(1+C)] && (1+C) = 1 \\
 &= (A + \bar{B} + C) [AB + AC + \bar{A}B + BC] && (1+A) = 1 \\
 &= (A + \bar{B} + C) [AB + AC + \bar{A}B + B] && (1+\bar{A}) = 1 \\
 &= (A + \bar{B} + C) [B(1+A) + AC + \bar{A}B] \\
 &= (A + \bar{B} + C) [B + AC + \bar{A}B] \\
 &= (A + \bar{B} + C) [B[1 + \bar{A}] + AC] \\
 &= (A + \bar{B} + C) [B(1 + \bar{A}) + AC] \\
 &= (A + \bar{B} + C) [B[1 + \bar{A}] + AC] \\
 &= (A + \bar{B} + C) [B + AC] \\
 &= \overbrace{AB + AAC + B\bar{B} + A\bar{B}C + BC + ACC}^{AC + AC = A} \\
 &= AB + AC + A\bar{B}\bar{C} + BC + AC \\
 &= AB + AC + A\bar{B}C + BC
 \end{aligned}$$

$$Y = \underline{\underline{(AB)(AC)(\bar{A}\bar{B}C)(BC)}}$$



$$\therefore Y = \underline{\underline{\bar{A}\bar{B} \cdot \bar{A}\bar{C} \cdot \bar{A}\bar{B}\bar{C} \cdot \bar{B}\bar{C}}}$$

$$Y = \underline{\underline{(AB)(AC)(\bar{A}\bar{B}C)(BC)}}$$

31. P.T. $x(x+y) = x$

$$\begin{aligned}x(x+y) &= xx + xy \\&= x + xy \\&= x[1+y] \\x(x+y) &= x\end{aligned}$$

32. P.T. $xy + yz + \bar{y}z = xy + z$ $y + \bar{y} = 1$.

$$\begin{aligned}xy + yz + \bar{y}z &= xy + z[y + \bar{y}] \\&= xy + z(1) \\xy + yz + \bar{y}z &= xy + z\end{aligned}$$

33. $\overline{\bar{A}\bar{B} + \bar{A} + AB} = \overline{(\bar{A} + \bar{B}) + \bar{A} + AB}$ $\bar{A} + \bar{A} = \bar{A}$

$$\begin{aligned}&= \overline{\bar{A} + \bar{B} + \bar{A} + AB} \\&= \overline{\bar{A} + \bar{B} + AB} \\&= \bar{A} \cdot \bar{B} \cdot \bar{AB} \\&= AB - (\bar{A} + \bar{B}) \\&= AB\bar{A} + AB\bar{B} \\&= 0.\end{aligned}$$

25. Simplify & implement using only NOR gates.

$$Y = (\bar{A} + \bar{B} + C)(\bar{A} + B + C)(A + B)$$

Complementing both sides.

$$\bar{Y} = (\bar{A} + \bar{B} + C)(\bar{A} + B + C)(A + B)$$

$$= \underbrace{(\bar{A} + \bar{B} + C)}_{x4} (\bar{A} + B + C)(A + B).$$

$$= [\cancel{\bar{A}\bar{B}} + AB + AC + \cancel{\bar{A}\bar{B}} + \cancel{B\bar{B}} + BC + \cancel{\bar{A}C} + \cancel{BC} + \cancel{CC}] (A + B)$$

$$= [AB + AC + \bar{A}\bar{B} + BC + \bar{A}C + C[1+B]] (A + B)$$

$$= [AB + AC + \bar{A}\bar{B} + BC + \bar{A}C + C] (A + B)$$

$$= [AB + C[1+A] + \bar{A}\bar{B} + BC + \bar{A}C] (A + B)$$

$$= [AB + C + \bar{A}\bar{B} + BC + \bar{A}C] (A + B)$$

$$= [AB + C(1+B) + \bar{A}\bar{B} + \bar{A}C] (A + B)$$

$$= [AB + C + \bar{A}\bar{B} + \bar{A}C] (A + B)$$

$$= [AB + C(1+\bar{A}) + \bar{A}\bar{B}] (A + B)$$

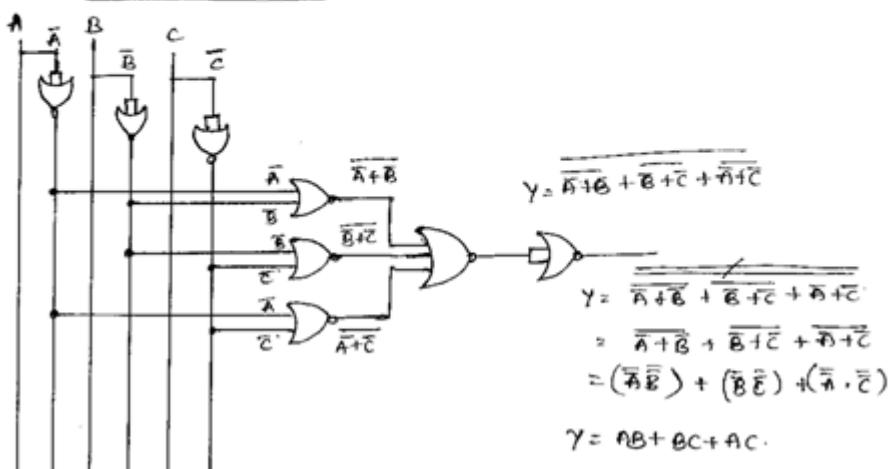
$$= [AB + C + \bar{A}\bar{B}] (A + B)$$

$$= AAB + AC + A\cancel{A}\bar{B} + ABB + BC + \cancel{A}\cancel{B}B$$

$$= AB + AC + AB + BC$$

$$\bar{Y} = AB + BC + AC$$

$$Y = \overline{AB + BC + AC}$$



26. $Y = (A+B)(A+\bar{B})(\bar{A}+B)$ Realize using NOR gate

$$Y = (AA + A\bar{B} + AB + B\bar{B})(\bar{A}+B)$$

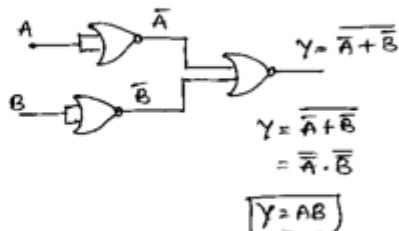
$$= (A + A\bar{B} + AB)(\bar{A}+B)$$

$$= (A[1+\bar{B}+B])(\bar{A}+B)$$

$$= (A)(\bar{A}+B)$$

$$= A\bar{A} + AB$$

$$\boxed{Y = AB}$$



$$27. Y = \bar{A}BC + A\bar{B}C + ABC$$

$$= \bar{A}BC + AC[B + \bar{B}]$$

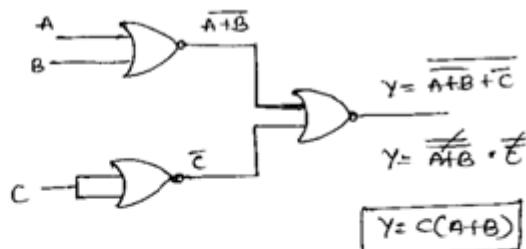
$$B + \bar{B} = 1$$

$$= \bar{A}BC + AC$$

$$A + \bar{A}B = A + B$$

$$= C[A + \bar{A}B]$$

$$\boxed{Y = C(A+B)}$$



28. Simplify & realize using NAND gates only.

$$F = XYZ + YZ + \bar{Z}$$

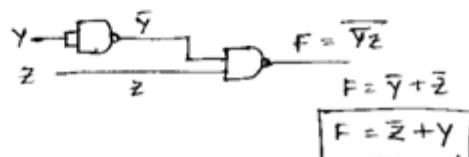
$$\bar{A} + AB = \bar{A} + B$$

$$= YZ[1+X] + \bar{Z}$$

$$\text{if } \bar{X} + YZ = \bar{Z} + Y$$

$$= YZ + \bar{Z}$$

$$\boxed{F = \bar{Z} + Y}$$



Q9. $Y = \underbrace{(A+BC)(\bar{A}+B+\bar{C})(A+\bar{B})}_{X^4}$

$$Y = [\bar{A}\bar{A} + AB + AC + \bar{A}\bar{B}C + B\bar{B}C + \bar{B}C\bar{C}] (A+\bar{B}).$$

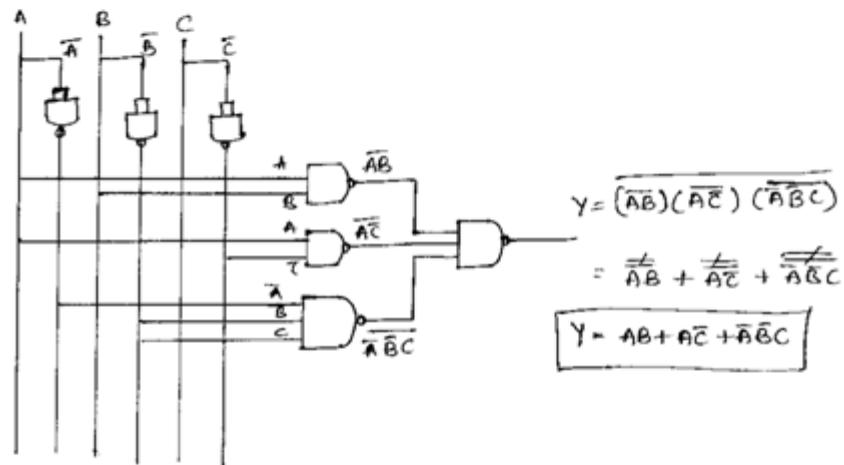
$$= [AB + A\bar{C} + \bar{A}\bar{B}C] (A+\bar{B}).$$

$$= AAB + AAC + A\bar{A}\bar{B}C + A\bar{B}\bar{B} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$

$$= AB + \underline{A\bar{C}} + \underline{A\bar{B}\bar{C}} + \bar{A}\bar{B}C \quad ; \because B \cdot \bar{B} = 0$$

$$= AB + A\bar{C} [1 + \bar{B}] + \bar{A}\bar{B}C$$

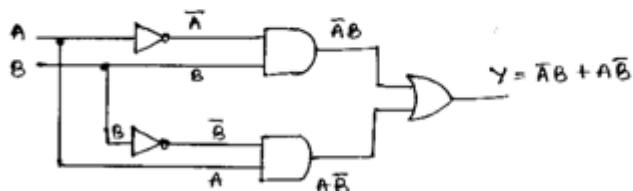
$$Y = AB + A\bar{C} + \bar{A}\bar{B}C$$



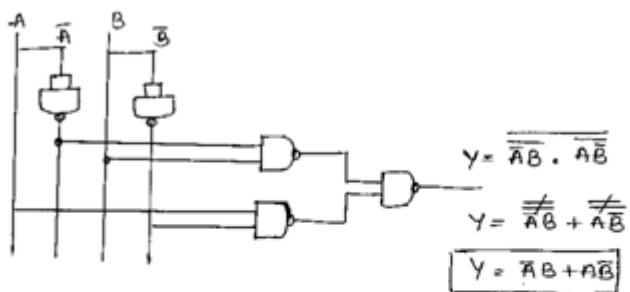
30. Realize $Y = \bar{A}B + A\bar{B}$ using ① basic gates ② only NAND gate

③ only NOR gates.

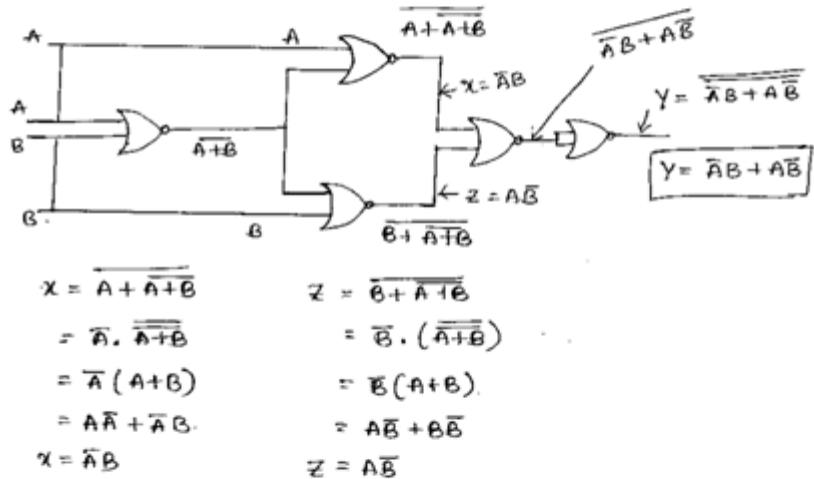
a) Basic gate :-



b) Using only NAND gates :-



c) Using only NOR gate :-



31. $ABCD + ABD = ABD[1+C]$
 $= ABD$

32. $ABCD + A\overline{B}CD = ACD[B + \overline{B}]$
 $= ACD[1]$
 $= ACD.$

$$\begin{aligned}
 33. \quad A(A+B) &= AA + AB \\
 &= A + AB \\
 &= A[1+B] \\
 &= A
 \end{aligned}$$

$$\begin{aligned}
 34. \quad AB + ABC + AB[D+E] &= AB + ABC + ABD + ABE \\
 &= AB[1+C+D+E] \\
 &= AB.
 \end{aligned}$$

$$\begin{aligned}
 35. \quad XY + XYZ + XY\bar{Z} + \bar{X}YZ &= XY[1+Z] + XY\bar{Z} + \bar{X}YZ \\
 &= XY + XY\bar{Z} + \bar{X}YZ \\
 &= XY[1+\bar{Z}] + \bar{X}YZ \\
 &= XY + \bar{X}YZ \\
 &= Y[X + \bar{X}Z] \quad A + \bar{A}B = A + B \\
 &= Y[X + Z] \quad X + \bar{X}Z = X + Z
 \end{aligned}$$

$$\begin{aligned}
 36. \quad \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC &= \bar{A}\bar{C}[\bar{B} + B] + \bar{A}BC \\
 &= \bar{A}\bar{C} + \bar{A}BC. \quad A + AB = A + B \\
 &= \bar{A}[\bar{C} + BC] \quad \bar{A} + AB = \bar{A} + B \\
 &= \bar{A}[\bar{C} + B] \quad \text{Hence } \bar{C} + CB = C + B.
 \end{aligned}$$

$$37. \quad ABC + A\bar{B}C + A\bar{B}\bar{C} = A[C + B]$$

Show that:

$$\begin{aligned}
 &AC[B + \bar{B}] + A\bar{B}\bar{C} \quad B + \bar{B} = 1 \\
 &AC + A\bar{B}\bar{C} \quad A + \bar{A}B = A + B \\
 &A[C + \bar{C}B] \quad \text{Hence } C + \bar{C}B = C + B. \\
 &A[C + B] = A[C + B]
 \end{aligned}$$

$$\begin{aligned}
 38. \quad & \bar{A}BC\bar{D} + BC\bar{D} + B\bar{C}\bar{D} + B\bar{C}D \\
 & = BC\bar{D} [1 + \bar{A}] + B\bar{C}\bar{D} + B\bar{C}D \\
 & = BC\bar{D} + B\bar{C}\bar{D} + B\bar{C}D \\
 & = B\bar{D} [C + \bar{C}] + B\bar{C}D \\
 & = B\bar{D} + B\bar{C}D \\
 & = B[\bar{D} + \bar{C}D]
 \end{aligned}$$

$$\begin{aligned}
 39. \quad AC + A C [A + \bar{A}B] &= AC + AC + \bar{A}CB \\
 &\equiv AC + \bar{A}CB \quad A + \bar{A}B = A + B. \\
 &\equiv C[A + \bar{A}B] \\
 &\equiv C[A + B]
 \end{aligned}$$

$$\begin{aligned}
 40. \quad \bar{A}B\bar{C}D + \bar{A}B\bar{C}D + ABD &= \bar{A}BD [\bar{C} + C] + ABD \\
 &= \bar{A}BD + ABD \\
 &= BD[\bar{A} + A] \\
 &= BD.
 \end{aligned}$$

$$\begin{aligned}
 41. \text{ Show that } \quad & A + \bar{A}B + AB = A + B \\
 & A[1 + \bar{B}] + \bar{A}B = A + B. \\
 & A + \bar{A}B = A + B. \quad A + \bar{A}B = A + B. \\
 & A + B = A + B
 \end{aligned}$$

$$\begin{aligned}
 42. \quad \overline{\bar{A}B + \bar{A} + AB} &= \overline{\bar{A} + \bar{B} + \underline{\bar{A} + AB}} \quad \bar{A} + AB = \bar{A} + B \\
 &= \overline{\bar{A} + \bar{B} + \bar{A} + B}. \quad B + \bar{B} = 1 \\
 &= \overline{\bar{A} + \bar{B} + B + B}. \quad \bar{A} + \bar{B} = \bar{A} \\
 &= \overline{\bar{A} + 1}. \\
 &= \bar{A} \cdot (1) \\
 &= A \cdot 0 \\
 &= 0
 \end{aligned}$$

$$\begin{aligned}
 43. \quad Y &= (A+B)(\bar{A}+C)(\bar{B}+\bar{C}) \\
 &= (A\bar{A} + AC + \bar{A}B + BC)(\bar{B}+\bar{C}) \\
 &= (AC + \bar{A}B + BC)(\bar{B}+\bar{C}) \\
 &= ABC + \bar{A}\bar{B}\bar{C} + B\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} + B\bar{C}\bar{C} \\
 Y &= A\bar{B}C + \bar{A}B\bar{C}
 \end{aligned}$$

$$\begin{aligned}
 44. \quad (\bar{A}+\bar{B})(\bar{A}+B) &= (\bar{A}+\bar{B}) + (\bar{A}+B) \\
 &= \bar{A} \cdot \bar{B} + \bar{A} \cdot B \\
 &= \bar{A}B + A \cdot \bar{B} \\
 &= A \oplus B.
 \end{aligned}$$

$$\begin{aligned}
 45. \quad \overline{\overline{ABC}D} &= \overline{\overline{ABC}} + \overline{D} \\
 &= \overline{ABC} + \overline{D} \\
 &= (\bar{A}+\bar{B})C + \overline{D}
 \end{aligned}$$

$$\begin{aligned}
 46. \quad Y &= \overline{\bar{A}+B+\bar{C}D} \\
 &= (\bar{A}+B) \cdot \overline{\bar{C}D} \\
 &= (\bar{A} \cdot \bar{B}) \cdot CD \\
 Y &= A\bar{B}CD
 \end{aligned}$$

$$\begin{aligned}
 47. \quad Y &= A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C \\
 &= \bar{B}\bar{C}[A+\bar{A}] + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} \\
 &= \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} \quad \bar{A} + A\bar{B} = \bar{A} + B \\
 &= \bar{B}[\bar{C} + \bar{A}C] + \bar{A}B\bar{C} \quad \text{Hence } \bar{C} + \bar{A}C = \bar{C} + \bar{A} \\
 &= \bar{B}[\bar{C} + \bar{A}] + \bar{A}B\bar{C} \\
 &= \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}B\bar{C} \\
 &= \bar{B}\bar{C} + \bar{A}[\bar{B} + B\bar{C}] \quad \bar{A} + A\bar{B} = \bar{A} + B \\
 &= \bar{B}\bar{C} + \bar{A}[\bar{B} + \bar{C}] \quad \text{Hence } \bar{B} + B\bar{C} = \bar{B} + \bar{C} \\
 Y &= \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}C
 \end{aligned}$$

Basic Gates:-

* All boolean expressions consist of various combinations of the basic expressions OR, AND & NOT. Any expressions can be implemented using AND, OR & NOT gates.

UNIVERSAL Gates:-

* NAND & NOR Gates are called universal gates because it is possible to implement all logic expressions using only NAND or NOR gates.

Adder:-

Computer performs various arithmetic operations. The most basic operation is the addition of two binary digits. The simple addition consists of four possible elementary operations, namely.

$$\begin{array}{ll} 0 + 0 = 0 & \begin{array}{c} 1 \\ 1 \\ \hline \end{array} \\ 0 + 1 = 1 & \begin{array}{c} 1 \\ \downarrow \\ 1 \\ \hline \end{array} \\ 1 + 0 = 1 & \begin{array}{c} 1 \\ \uparrow \\ 1 \\ \hline \end{array} \\ 1 + 1 = 10. & \text{Carry} \end{array}$$

- * The first three operations produce a sum whose length is one-digit, but when the last operation is performed, sum is two digits.
- * The higher significant bit of this result is called a carry. & lower significant bit is called sum.
- { * The logic circuit which performs this operation is called a Half adder. }
- * A logic circuit which adds two one-bit binary numbers is called a Half-adder.

Half adder:-

- * Half adder adds two binary numbers bit by bit giving the sum & possibly a carry.
- * Half adder comprises of an AND gate whose output gives the carry & an XOR gate whose output gives the sum.

Let A, B be Jip's.

$S \rightarrow$ sum } be op's.
 $C \rightarrow$ carry } be op's.

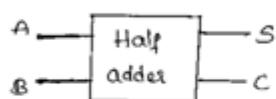


fig ① Symbol.

Truth Table:-

A	B	carry C	sum S
0	0	0	0
1	1	0	1
1	0	0	1
1	1	1	0

From above truth table sum & carry are expressed as

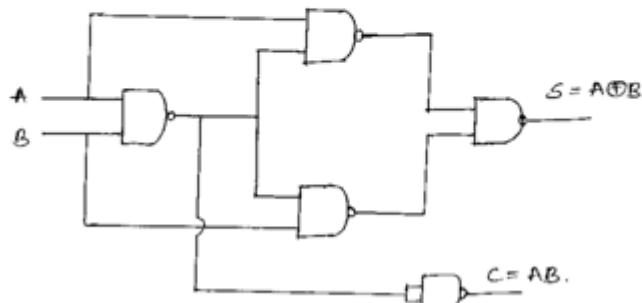
$$\therefore \text{Sum} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry} = AB$$

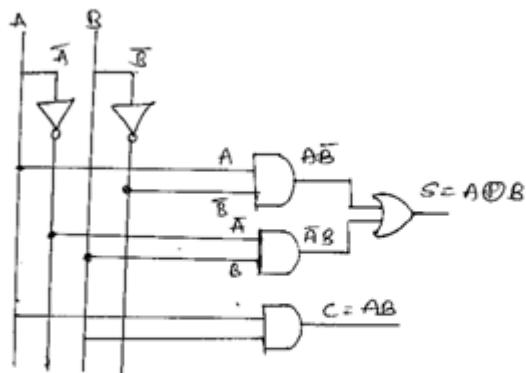


fig ② : logic circuit for half-adder.

Realization of Half adder Using only NAND Gates:-



Implementation of Half adder using basic Gates:-



Limitation of Half adder:-

- * In multidigit addition we have to add two bit along with the carry of previous digit addition. So such addition requires addition of three bits. This is not possible with half adder.

Hence half adders are not used in practice.

Full adder:-

- * In full adder, three bits can be added at a time. The 3rd bit is a carry from the previous lower significant position.
- * Thus full adder is a (combinational) logic circuit that performs the arithmetic sum of three I/p bits. The three I/p's are A, B & Cin & two o/p's sum & carry.

NOTE :-

The third input C_{in} , represents the carry from the previous lower significant bit.

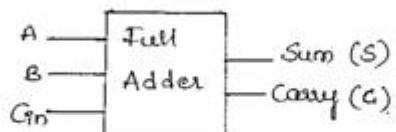


Fig ① : Symbol.

Truth table :-

A	B	C_{in}	Carry (C)	Sum (S)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

From above truth table, sum & carry are expressed as:

$$\begin{aligned}
 S &= \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C}_{in} + A\overline{B}C_{in} + ABC_{in} \\
 &= \overline{C}_{in} [\overline{A}\overline{B} + A\overline{B}] + C_{in} [\overline{A}\overline{B} + AB] \\
 &= \overline{C}_{in} [A \oplus B] + C_{in} [\overline{A} \oplus B] \quad \text{put,} \\
 &= \overline{C}_{in} [x] + C_{in} [\bar{x}] \quad x = A \oplus B \\
 &= C_{in} \oplus x \\
 &= C_{in} \oplus A \oplus B
 \end{aligned}$$

$S = A \oplus B \oplus C_{in}$

$$\begin{aligned}
 x &= A \oplus B \\
 \bar{x} &= \overline{A \oplus B}
 \end{aligned}$$

$$\begin{aligned}
 C &= \overline{ABC}_{in} + A\overline{B}C_{in} + A\overline{B}\overline{C}_{in} + ABC_{in} + A\overline{BC}_{in} \\
 &= BG_{in} [A + \overline{A}] + A\overline{B}C_{in} + A\overline{B}\overline{C}_{in} + ABC_{in} + A\overline{BC}_{in} \\
 &= BG_{in} + A C_{in} [B + \overline{B}] + AB\overline{C}_{in} + ABC_{in} \\
 &= BG_{in} + A C_{in} + AB [C_{in} + \overline{C}_{in}] \\
 C &= BG_{in} + A C_{in} + AB \\
 C &= AB + BG_{in} + AC_{in}
 \end{aligned}$$

- * The full adder can also be implemented with two half adders & one OR gate as shown in fig@.
- * The sum output from the second half adder is the EX-OR of C_{in} & the sum of the 1st half adder giving,

$$\text{Sum} = C_{in} \oplus (A \oplus B) \text{ or } \text{Sum} = (A \oplus B) \oplus C_{in}$$

$$\text{Put } X = A \oplus B \quad X = A \oplus B = \overline{AB} + AB$$

$$\begin{aligned}
 \text{Sum} &= X \oplus C_{in} \\
 &= XC_{in} + \overline{X}C_{in} \\
 &= (\overline{AB} + AB)\overline{C_{in}} + (\overline{AB} + AB)C_{in} \\
 &= \overline{C_{in}}(\overline{AB} + AB) + C_{in}[(\overline{AB}) + (AB)] \\
 &= \overline{C_{in}}(\overline{AB} + AB) + C_{in}(A + B) \cdot (A + B) \\
 &= \overline{C_{in}}(\overline{AB} + AB) + C_{in}[\cancel{AA} + AB + \cancel{AB} + B^2] \\
 &= \overline{C_{in}}(\overline{AB} + AB) + C_{in}(AB + \overline{AB})
 \end{aligned}$$

$$\boxed{\text{Sum} = \overline{AB}\overline{C_{in}} + A\overline{B}C_{in} + ABC_{in} + \overline{ABC}_{in}}$$

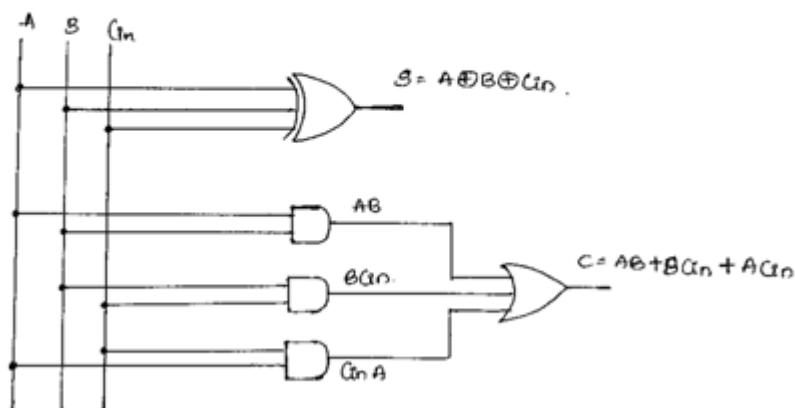
& the carry is,

$$\begin{aligned}
 C &= AB + C_{in}(A \oplus B) \quad C_{in} + 1 = 1 \\
 &= AB + C_{in}(\overline{AB} + AB) \\
 &= AB + \overline{ABC}_{in} + A\overline{B}C_{in} \\
 &= AB[C_{in} + 1] + \overline{ABC}_{in} + A\overline{B}C_{in} \\
 &= \cancel{ABC}_{in} + AB + \cancel{ABC}_{in} + \cancel{A\overline{B}C_{in}} \\
 &= AB + \overline{ABC}_{in} + A C_{in}[B + \overline{B}] \\
 &= AB[1 + C_{in}] + \overline{ABC}_{in} + A C_{in} \\
 &= AB + \underline{ABC}_{in} + \overline{ABC}_{in} + A C_{in}
 \end{aligned}$$

$$= AB + A\bar{C}_{in} + \bar{B}C_{in}[A + \bar{A}]$$

$$C = AB + A\bar{C}_{in} + \bar{B}C_{in}$$

Logic diagram :-



Full adder using two half adder :-

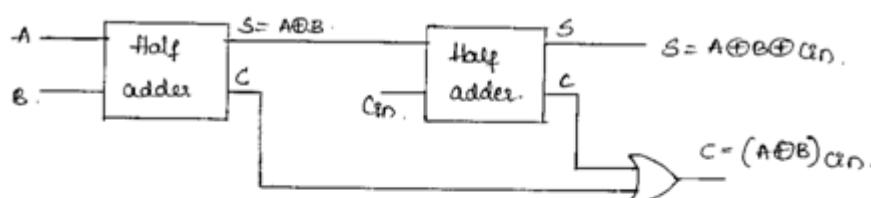


Fig ① Full adder using two half adder.

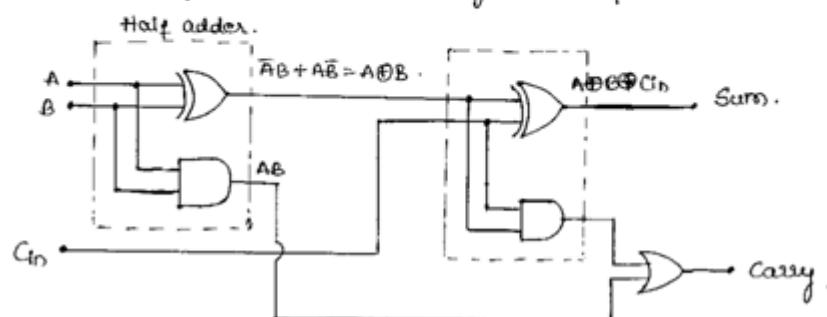


Fig ②: Logic diagram of full adder Using Two half adder.

Module-2

TRANSISTORS

INTRODUCTION :-

- ❖ Transistor was invented by William Shockley in 1947.
- ❖ Invention of transistor made the electronic circuits smaller, more efficient & less expensive.
- ❖ Transistor has a very important property that it can raise (Increase) the strength of a weak signal. This property is called **amplification**.

Transistor :-

A transistor consists of two PN junctions. The junctions are formed by sandwiching either P-type or N-type semiconductor layers between a pair of opposite types as shown below. Transistors are of two types.

1) NPN Transistor :-

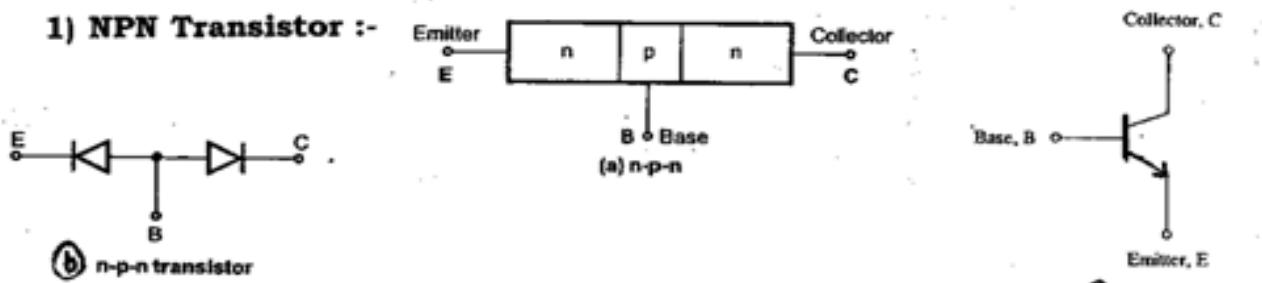
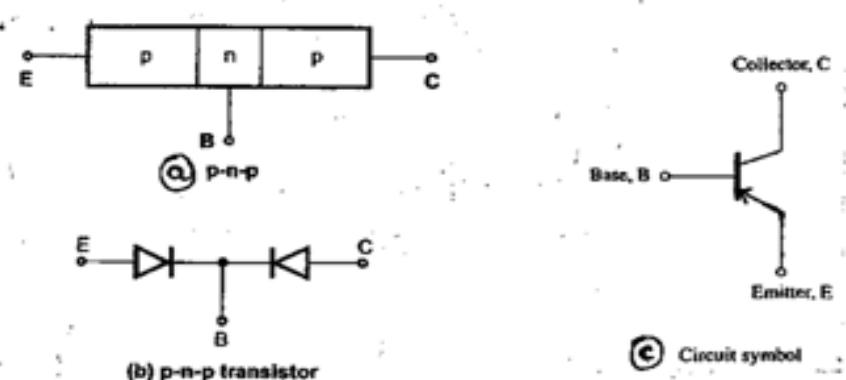


Fig. Two-diode transistor analogy

2) PNP Transistor :-



Transistors Classification :-

Transistors are classified into two types :

1) Unipolar Junction Transistor (UJT) :-

In UJT, current conduction is only due to one type of charge carriers, that to majority carriers.

2) Bipolar Junction Transistor (BJT) :-

In BJT, current conduction is due to both the type of charge carriers i.e holes & electrons are the majority & minority carriers.

Transistor Terminals :-

Transistor terminals are Emitter, Base & Collector.

❖ Emitter (E):-

- ◆ Emitter is heavily doped than other two regions. Its function is to supply majority carriers (either electrons or holes) to the other two regions.
- ◆ Emitter is always forward biased w.r.to base.

❖ Base (B):-

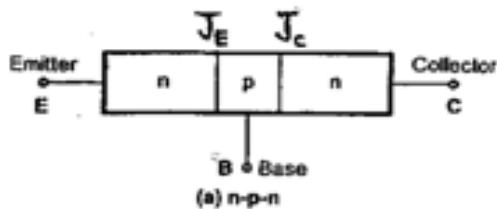
- ◆ It is the middle region that forms two P-N junctions in the transistor.
- ◆ The base is lightly doped & much thinner than the emitter & collector region.

❖ Collector (C):-

- ◆ It is a region situated in the other side of transistor(i.e. the side opposite to the emitter), which collects charge carriers(i.e. holes & electrons).
- ◆ The collector of a transistor is always larger than the emitter & base of a transistor.

- Collector is moderately doped (i.e doping level of the collector is intermediate between the heavily doped emitter & lightly doped base)

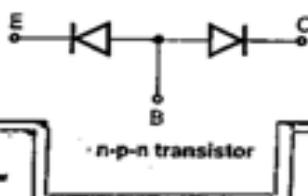
Transistor Junctions :-



The transistor has two PN junctions J_E & J_C as shown in figure. The junction J_E is a junction between emitter & base regions. Thus it is known as emitter-base junction.(Forward Biased).

Similarly, the junction J_C is a junction between collector & base regions. Thus it is known as Collector-base junction.(Reversed Biased).

Thus transistor is like two PN junction diodes connected back to back as shown in figure 2.



Origin of the name "Transistor" :-

- As we know transistor has two PN junction. One junction is forward biased & the other is reverse biased.
- The forward bias junction has a low resistance path where as reverse biased junction has a high resistance path.
- The weak signal is introduced in the low resistance circuit & output is taken from the high resistance circuit.
- Therefore, a transistor transfers a signal from a low resistance to high resistance & consequently name transistor is given by

TRANSfer + resISTOR = TRANSISTOR

i) Operation of NPN transistor :-

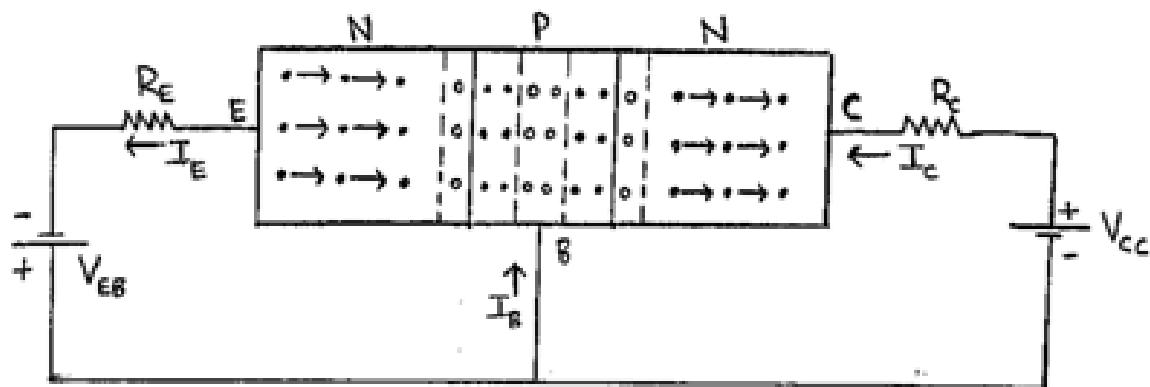


Fig ①: operation of NPN transistor

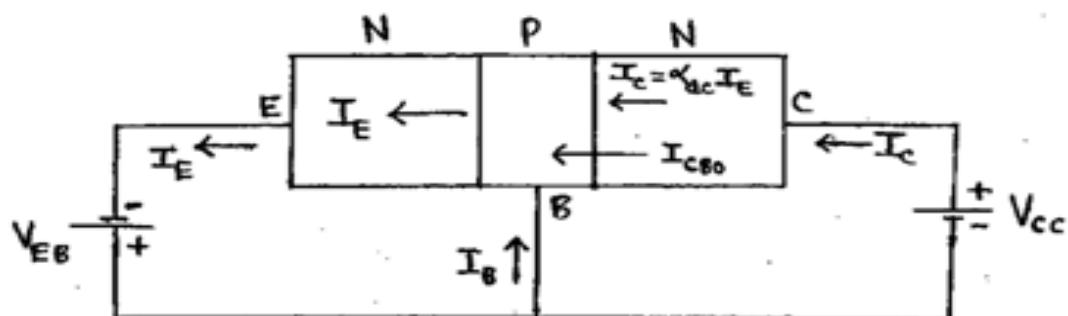


Fig ②: Currents in a NPN Transistor

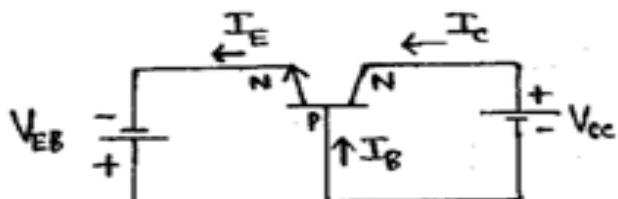


Fig ③ : Currents in a NPN Transistor.

- ❖ In NPN transistor current is due to the movement of free electrons. The emitter to base of a transistor is forward biased & collector to base junction is reversed biased.
- ❖ When V_{EB} is greater than barrier potential (V_T), emitter to base junction is forward biased causes the free electrons in the N-type emitter to flow towards the base region. This constitutes the emitter current I_E .
- ❖ As base is lightly doped, only few electrons combine with the holes & constitute base current I_B . Thus most of the electrons will diffuse to the collector region & constitutes collector current I_C .
- ❖ There is another component of collector current due to thermally generated carriers. This current component is called reverse saturation current & is quite small.

- * In NPN transistors, electrons are injected into the base. These electrons constitute the emitter current ' I_E '.
- * Assume that 100 electrons are injected into the base region. Since the base is very thin, only few electrons say 2 in number, recombine with the holes. This constitute the base current ' I_B '. The remaining 98 electrons cross the base-collector, constituting collector current ' I_C '.

$$\therefore \boxed{I_E = I_B + I_C} \rightarrow ①$$

WKT $\alpha_{dc} = \frac{I_C}{I_E}$

$$\boxed{I_C = \alpha_{dc} I_E} \rightarrow ②$$

α_{dc} is the emitter-collector current gain & is typically 0.96 to 0.995.

Thus $\boxed{I_C \approx I_E}$

- * When collector-base junction is reverse biased, a very small reverse saturation current (I_{CBO}) flows across the junction, called collector-to-base leakage current ' I_{CBO} ' & it is very small & can be neglected.

- * Substituting eq ① in eq ②, we get

$$I_C = \alpha_{dc} [I_B + I_C]$$

$$\overbrace{I_C}^{\leftarrow} = \alpha_{dc} I_B + \alpha_{dc} I_C$$

$$I_C - \alpha_{dc} I_C = \alpha_{dc} I_B$$

$$I_C [1 - \alpha_{dc}] = \alpha_{dc} I_B$$

$$I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} \cdot I_B$$

$$I_C = \beta_{dc} I_B$$

Where $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$

* β_{dc} is the base-collector current gain. Typically β_{dc} ranges from 25 to 300.

WKT $I_E = I_B + I_C \rightarrow ①$

Dividing on both sides of eq ① by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{I_E}{I_B} = \frac{I_B}{I_C} + 1 \rightarrow ②$$

WKT

$\beta = I_C/I_B$	$\alpha = I_C/I_E$
$\gamma_B = I_B/I_C$	$\gamma_\alpha = I_E/I_C$

Then eq ② becomes

$$\gamma_\alpha = \gamma_B + 1$$

$$\gamma_\alpha = \frac{1+\beta}{\beta}$$

$$\therefore \alpha = \frac{\beta}{1+\beta} \rightarrow ③$$

Eq ③ can be written as

$$\alpha(1+\beta) = \beta$$

$$\alpha + \cancel{\alpha\beta} = \cancel{\beta}$$

$$\alpha = \beta - \alpha\beta$$

ii) Operation of PNP transistor :-

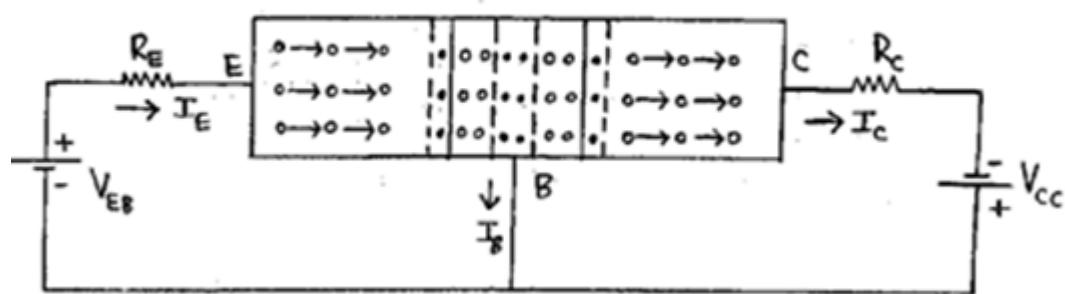
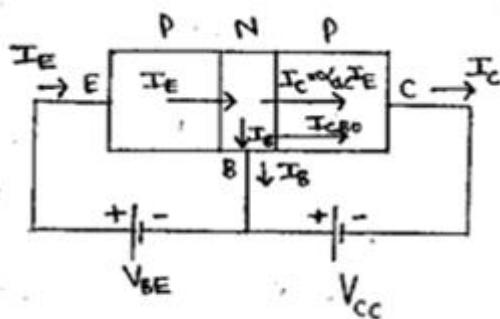


Fig ①: operation of PNP transistor



Currents in a PNP transistor

- ❖ Figure 1 shows an PNP transistor biased in active mode. In PNP transistor current is due to the movement of holes. The emitter to base junction is forward biased & collector to base junction is reversed biased.
- ❖ When V_{BE} is greater than barrier potential (V_T), emitter to base junction is forward biased causes the holes in the emitter region to flow towards the base region. This constitutes the emitter current I_E .
- ❖ As base is lightly doped only few holes combines with the holes & constitute base current ' I_B '. Thus most of the holes will diffuse to the collector region & constitutes collector current ' I_C '.
- ❖ There is another component of collector current due to thermally generated carriers. This current component is called reverse saturation current & is quite small.

- * In Fig ①, the current flowing into the emitter terminal is referred to as a emitter current ' I_E '.
- * Base current ' I_B ' & collector current ' I_C ' both flow out of the transistor, while ' I_E ' flow into the transistor.

$$\therefore \boxed{I_E = I_B + I_C} \rightarrow ①$$

- * Almost all of emitter current ' I_E ' crosses to the collector & only a small portion flow out of the base terminal.
Typically 96% to 99.5% of I_E flow across the collector to base junction to become collector current.

$$\boxed{I_C = \alpha_{dc} I_E} \rightarrow ②$$

WKT

$$\alpha_{dc} = \frac{I_C}{I_E - I_C}$$

Where α_{dc} is the emitter to collector current gain & is typically 0.96 to 0.995.
Thus, the collector current is almost equal to the emitter current i.e. $I_C \approx I_E$.

- * When C-B junction is reverse biased, a very small reverse saturation current ' I_{CBO} ' flows across the junction, called collector to base leakage current ' I_{CBO} ' & it is very small & can be neglected.

- * From eq ① & ②

$$\boxed{I_E = I_B + I_C} \rightarrow ①$$

$$\boxed{I_C = \alpha_{dc} I_E} \rightarrow ②$$

Substituting eq ① in eq ②

$$I_C = \alpha_{dc} [I_B + I_c]$$

$$I_c = \alpha_{dc} I_B + \alpha_{dc} I_c$$

$$\alpha_{dc} I_B = \underline{I_c} - \alpha_{dc} \underline{I_c}$$

$$\alpha_{dc} I_B = \underline{I_c} [1 - \alpha_{dc}]$$

$$I_c = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B$$

$$I_c = \beta_{dc} I_B$$

Where, $\beta_{dc} = \alpha_{dc} / 1 - \alpha_{dc}$

WKT $I_E = I_B + I_C \rightarrow ①$

Dividing on both sides of eq ① by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{I_E}{I_B} = \frac{I_B}{I_C} + 1 \rightarrow ②$$

WKT

$\beta = I_C/I_B$	$\alpha = I_C/I_E$
$\gamma_B = I_B/I_C$	$\gamma_\alpha = I_E/I_C$

Then eq ② becomes

$$\gamma_\alpha = \gamma_B + 1$$

$$\gamma_\alpha = \frac{1+\beta}{\beta}$$

$$\therefore \alpha = \frac{\beta}{1+\beta} \rightarrow ③$$

Eq ③ can be written as

$$\alpha(1+\beta) = \beta$$

$$\alpha + \cancel{\alpha\beta} = \cancel{\beta}$$

$$\alpha = \beta - \alpha\beta$$

* calculate α_{dc} and β_{dc} for the transistor if I_c is measured as 1mA and I_B is 25μA. also determine the new base current to give $I_c = 5\text{mA}$.

[June - 08, 6M]

Given :- (i) $I_c = 1\text{mA}$, $I_B = 25\mu\text{A}$, $\alpha_{dc} = ?$, $\beta_{dc} = ?$

(ii) $I_c = 5\text{mA}$, $I_B = ?$

Sol :-

$$\Rightarrow * \beta_{dc} = \frac{I_c}{I_B} = \frac{1\text{mA}}{25\mu\text{A}} = 40.$$

$$* \alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{40}{1 + 40} = 0.9756.$$

ii) When $I_c = 5\text{mA}$

$$* I_B = \frac{I_c}{\beta_{dc}} = \frac{5\text{mA}}{40} = 125\mu\text{A}.$$

* calculate the values of I_c , I_E and β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 120\mu\text{A}$.

[Jan - 09, 4M]

Given: $\alpha_{dc} = 0.98$, $I_B = 120\mu\text{A}$, $I_c = ?$, $I_E = ?$ & $\beta_{dc} = ?$.

Sol :-

$$* \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} = 49$$

$$* I_c = \beta_{dc} I_B = 49 \times 120\mu\text{A} = 5.88\text{mA}.$$

* Given $I_E = 2.5\text{mA}$, $\alpha = 0.98$ and $I_{CBO} = 10\mu\text{A}$, calculate I_B and I_c

[Jan - 11, 4M]

Sol :- NKT $\alpha = \frac{I_c}{I_E}$

$$I_c = \alpha I_E = 0.98 \times 2.5\text{mA}$$

$$I_c = 2.45\text{mA}$$

$$\text{NKT} \quad I_E = I_B + I_c$$

$$I_B = I_E - I_c = 2.5\text{mA} - 2.45\text{mA}$$

$$I_B = 50\mu\text{A}$$

1) calculate I_c & I_E for a transistor that has $\alpha_{dc} = 0.98$ & $I_B = 100 \mu A$. Also determine the value of P_{dc} for the transistor. (Reference book).

Sol:

$$* I_c = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B = \frac{0.98}{1 - 0.98} * 100 \mu A = 4.9 \text{ mA}$$

$$* I_E = \alpha_{dc} I_E ,$$

$$I_E = \frac{I_c}{\alpha_{dc}} = \frac{4.9 \text{ mA}}{0.98} = 5 \text{ mA}$$

$$* P_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} = 49.$$

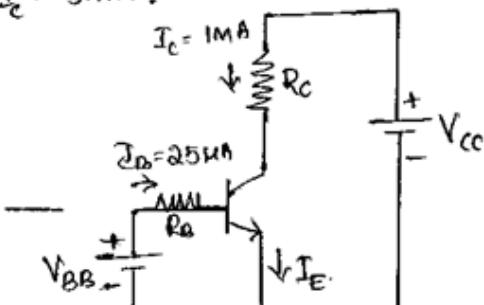
2) calculate α_{dc} & P_{dc} for the transistor in fig ① if I_c is measured as 1mA, & I_B is 25 μA . Also determine the new base current to give $I_c = 5 \text{ mA}$.

Sol: * $B_{dc} = \frac{I_c}{I_B} = \frac{1 \text{ mA}}{25 \mu A} = 40$

$$* I_E = I_B + I_c = 1 \text{ mA} + 25 \mu A = 1.025 \text{ mA}$$

$$* \alpha_{dc} = \frac{I_c}{I_E} = \frac{1 \text{ mA}}{1.025 \text{ mA}} = 0.976$$

$$* \text{New base current to give } I_c = 5 \text{ mA} \\ \therefore I_B = \frac{I_c}{B_{dc}} = \frac{5 \text{ mA}}{40} = 125 \mu A$$



(Reference book)

8) A transistor has $I_B = 100 \mu A$ & $I_C = 2mA$, find

July 06, 10M

- β of the transistor.
- α of the transistor.
- emitter current I_E
- If I_B changes by $+25 \mu A$ & I_C changes by $+0.6 mA$.
find the new value of β .

Sol:- Given : $I_B = 100 \mu A$ & $I_C = 2mA$;

$$i) \beta = \frac{I_C}{I_B} , \frac{2mA}{100\mu A} = \frac{2mA}{100\mu A} = 20$$

$$ii) \alpha = \frac{\beta}{1+\beta} = \frac{20}{1+20} = 0.952 .$$

$$iii) I_E = I_B + I_C = 100 \mu A + 2mA = 2.1mA$$

$$iv) \text{New } I_B = 100 \mu A + 25 \mu A = 125 \mu A$$

$$\text{New } I_C = 2mA + 0.6 mA = 2.6 mA$$

$$\text{New } \beta = \frac{2.6mA}{125 \mu A} = 20.8$$

2. If α for a transistor is 0.99, the base current is $100 \mu A$, estimate the collector current.

March - 99, 5M

Sol: Given $I_B = 100 \mu A$, $\alpha = 0.99$

WKT. $\beta = \frac{I_C}{I_B}$ & $\beta = \frac{\alpha}{1-\alpha}$

$$\beta = \frac{0.99}{1-0.99} = 99$$

$$I_C = \beta I_B$$
$$= 99 \times 100 \mu A$$

$$I_C = 9.9 mA$$

5) For a transistor $I_E = 1\text{mA}$, $I_B = 10\text{\mu A}$, determine α & β .

Sol: $I_E = 1\text{mA}$, $I_B = 10\text{\mu A}$.

March - 2001, 5M

WKT.

$$I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

$$I_E = I_B [1 + \beta]$$

$$[1 + \beta] = \frac{I_E}{I_B} = \frac{1\text{mA}}{10\text{\mu A}} = 100$$

$$1 + \beta = 100$$

$$\boxed{\beta = 99}$$

$$\alpha = \frac{\beta}{1 + \beta} = \frac{99}{1 + 99} = \underline{\underline{0.99}}$$

Transistor Configurations :-

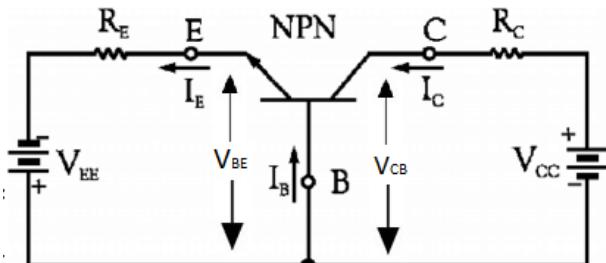
Transistor has three terminals namely **Emitter (E)**, **Base(B)** & **Collector(C)**. When a transistor is connected in a circuit, we require four terminals i.e. two terminals for input and two for output.

Thus out of three terminals, **one terminal is made common to both input and output terminals**.

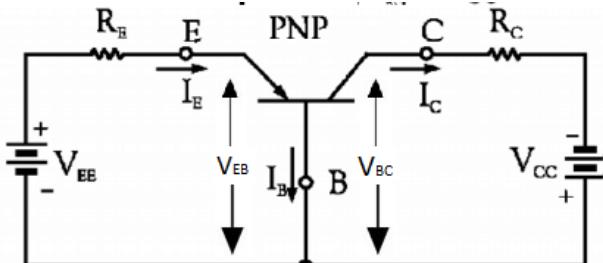
There are three different types of configurations or connection :

- 1) Common-Base Configuration (**CB**)
- 2) Common-Emitter Configuration (**CE**)
- 3) Common-Collector Configuration (**CC**)

Common-Base Configuration (**CB**)



(a) Common-base NPN transistor circuit.



(b) Common-base PNP transistor circuit.

In common base configuration, emitter is the input terminal, collector is the output terminal and base terminal is connected as a common terminal for both input and output. That means the emitter terminal and common base terminal are known as input terminals whereas the collector terminal and common base terminal are known as output terminals.

In common base configuration, the base terminal is grounded so the common base configuration is also known as grounded base configuration. Sometimes common base configuration is referred to as common base amplifier, CB amplifier, or CB configuration.

- { * In fig ①, the emitter-base Junction (JE) is forward biased
* the collector-base Junction (JC) is reverse biased.
* The emitter current I_E flows in the IIP ckt & the collector current I_C flows in the OIP ckt.
}.

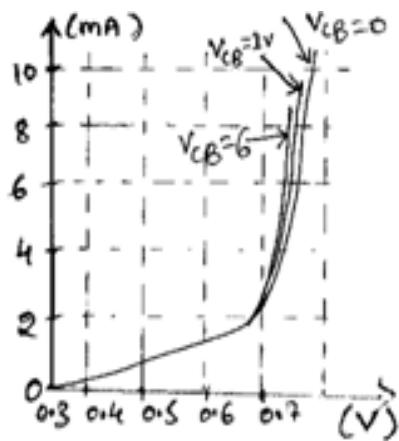
IIP characteristics:-

- * It is the curve between emitter current ' I_E ' & emitter to base voltage ' V_{EB} ' at constant collector-base voltage ' V_{CB} '.
* The emitter current is generally taken along Y-axis & emitter base voltage along X-axis as shown in fig ②.
{ } Keep O/P voltage V_{CB} to constant.

2) Increase I/p voltage V_{EB} in small suitable steps.

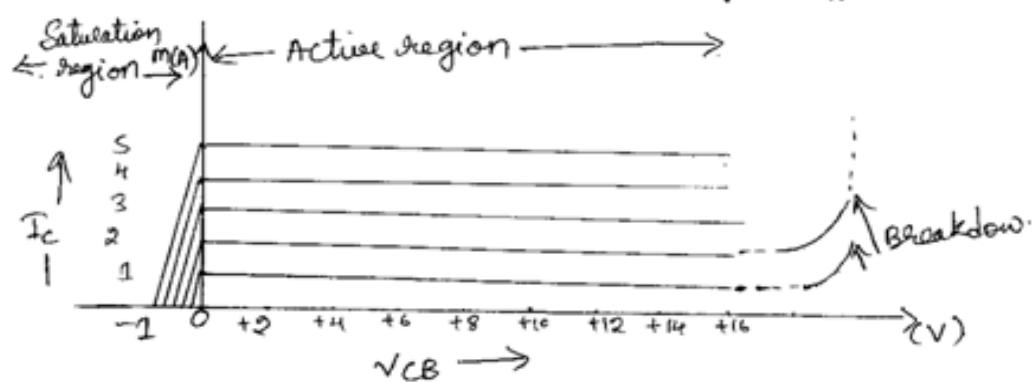
3) Note down the corresponding I/p current ' I_E '.

- * To obtain the Z/p characteristic, the o/p voltage ' V_{CE} ' is kept constant, I/p voltage ' V_{EB} ' is varied in small intervals & the corresponding change in Z/p current ' I_E ' is recorded.
- * I_E is then plotted against V_{EB} as shown in fig⑤. The experiment is repeated for other values of V_{CE} say 1V & 6V etc.
- * The emitter current ' I_E ' increases rapidly with small increase in emitter-base voltage ' V_{EB} '. It means the Z/p resistance is very small.



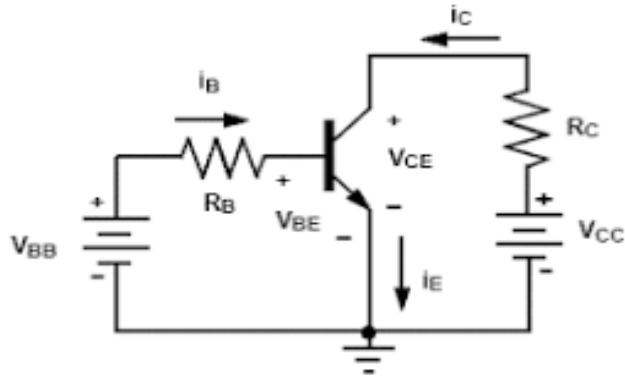
Olp characteristics :-

- * These curves give the relationship between the collector current ' I_c ' & the collector-base voltage ' V_{CB} ' for a constant emitter current ' I_E '.
- * Collector current is taken along y-axis & collector voltage along x-axis.
- * We have to adjust the emitter-base voltage ' V_{EB} ' to get a suitable value of emitter current ' I_E ' (say $I_E = 1\text{mA}, 2\text{mA}$ etc)
- * The o/p characteristics is obtained by keeping ' I_E ' constant & by noting variation in collector current ' I_c ' with variation in collector-base voltage ' V_{CB} '.
- * If we plot a graph with collector-base voltage ' V_{CB} ' along with the horizontal axis & the collector current I_c along the vertical axis, which results fig (3) o/p characteristics.



- i) In saturation region, collector to base voltage ' V_{CB} ' is -ve for a NPN transistor. It means that collector-base junction of a transistor is also forward bias in the saturation region. So a small change in V_{CB} results in a large value of ' I_c ' current.
- ii) In active region, the emitter-base junction ' J_E ' is forward biased & collector-base junction ' J_C ' is reversed biased. The collector current is constant & is equal to the emitter current. ($I_c \approx I_E$).
- iii) In cut-off region, both junctions of a transistor are reverse biased, hence only a small leakage current flows in the circuit.

Common Emitter Configuration



In common emitter configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal for both input and output. That means the base terminal and common emitter terminal are known as input terminals whereas collector terminal and common emitter terminal are known as output terminals.

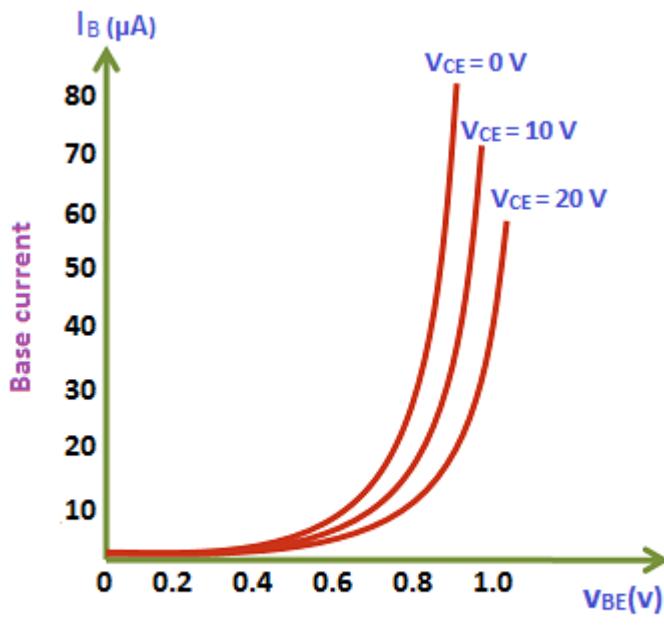
In common emitter configuration, the emitter terminal is grounded so the common emitter configuration is also known as grounded emitter configuration. Sometimes common emitter configuration is also referred to as CE configuration, common emitter amplifier, or CE amplifier. The common emitter (CE) configuration is the most widely used transistor configuration.

Input characteristics

The input characteristics describe the relationship between input current or base current (I_B) and input voltage or base-emitter voltage (V_{BE}).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or base current (I_B) is taken along y-axis (vertical line) and the input voltage (V_{BE}) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{CE} is kept constant at zero volts and the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of input voltage (V_{BE}), the corresponding input current (I_B) is recorded.



I/P characteristics CE configuration

A curve is then drawn between input current I_B and input voltage V_{BE} at constant output voltage V_{CE} (0 volts).

Next, the output voltage (V_{CE}) is increased from zero volts to certain voltage level (10 volts) and the output voltage (V_{CE}) is kept constant at 10 volts. While increasing the output voltage (V_{CE}), the input voltage (V_{BE}) is kept constant at zero volts. After we kept the output voltage (V_{CE}) constant at 10 volts, the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of input voltage (V_{BE}), the corresponding input current (I_B) is recorded.

A curve is then drawn between input current I_B and input voltage V_{BE} at constant output voltage V_{CE} (10 volts).

This process is repeated for higher fixed values of output voltage (V_{CE}).

When output voltage (V_{CE}) is at zero volts and emitter-base junction is forward biased by input voltage (V_{BE}), the emitter-base junction acts like a normal **p-n junction diode**. So the input characteristics of the CE configuration is same as the characteristics of a normal pn junction diode.

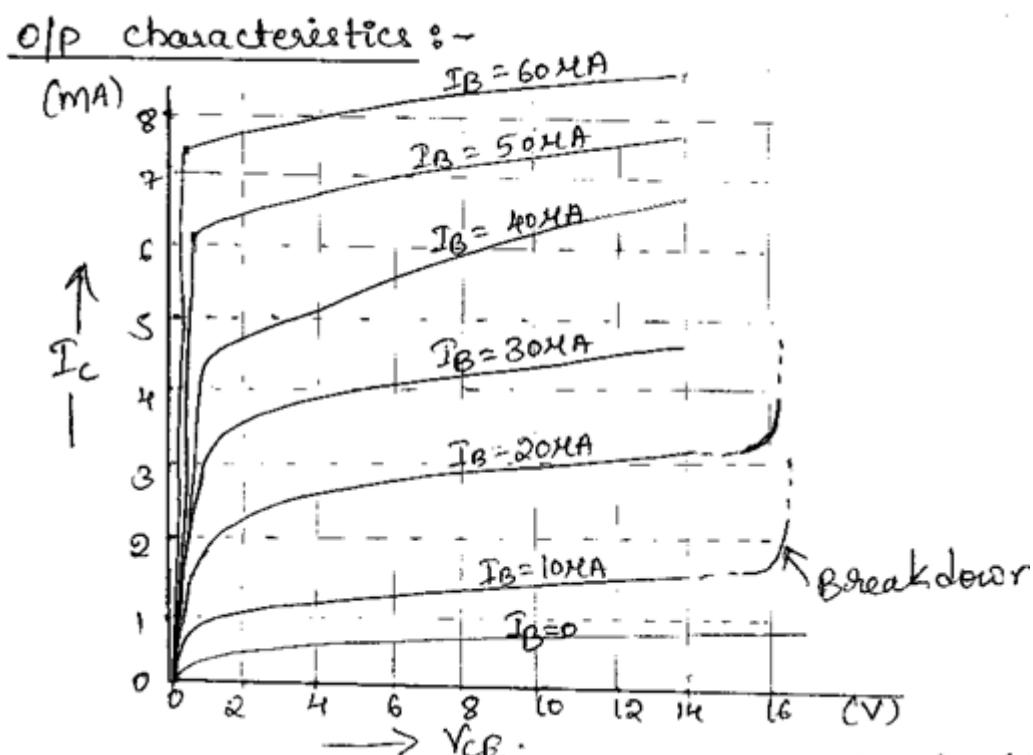
The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, we can see that after 0.7 volts, a small increase in input voltage (V_{BE}) will rapidly increases the input current (I_B).

Output characteristics

The output characteristics describe the relationship between output current (I_C) and output voltage (V_{CE}).

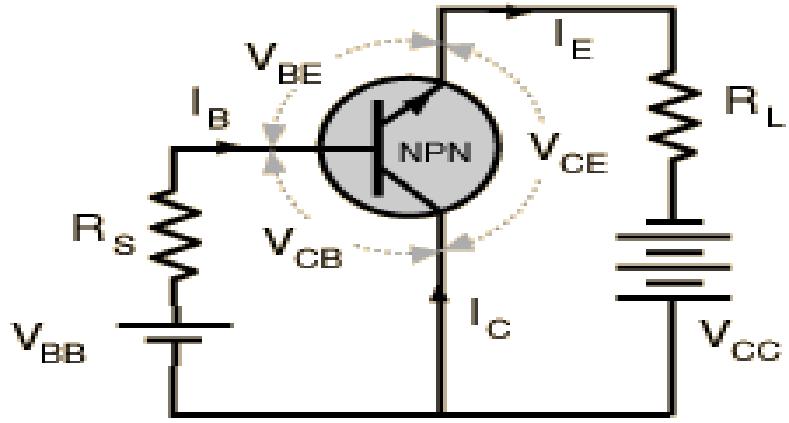
First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (I_C) is taken along y-axis (vertical line) and the output voltage (V_{CE}) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current or base current I_B is kept constant at 0 μA and the output voltage V_{CE} is increased from zero volts to different voltage levels. For each level of output voltage, the corresponding output current (I_C) is recorded.



- i) In saturation region, when the collector to emitter voltage ' V_{CE} ' is increased above zero, the collector current ' I_C ' increases rapidly to a saturation value, depending upon the value of base current.
- * It may be noted that collector current I_C reaches to a Saturation value when V_{CE} is about 0.5V.
- ii) In active region, the collector current is P_{de} times greater than the base current. Thus small I_B current ' I_B ' produces a large o/p current I_C .
- iii) In cutoff region, when base current is zero ($I_B=0$), collector current is not zero ($I_C \neq 0$), a small collector current exists called reverse leakage current ' I_{CEO} '.

Common Collector Configuration



In this configuration, the base terminal of the [transistor](#) serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output. Hence, it is named as common collector configuration. The input is applied between the base and collector while the output is taken from the emitter and collector.

In this configuration, input [current](#) or base current is denoted by I_b and output current or emitter current is denoted by I_e . The common collector amplifier has high input impedance and low output impedance. It has low voltage gain and high current gain.

[Input characteristics](#)

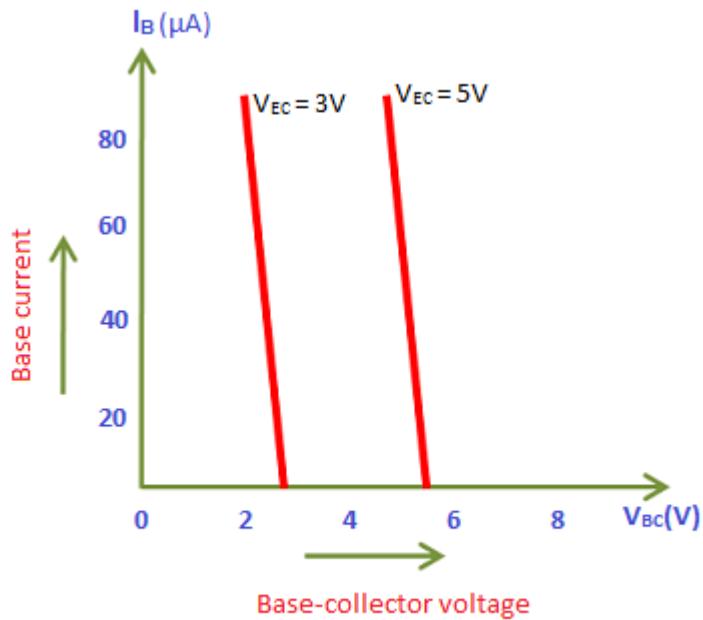
The input characteristics describe the relationship between input current or base current (I_b) and input voltage or base-collector voltage (V_{bc}).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis

The input current or base current (I_b) is taken along y-axis (vertical line) and the input voltage or base-collector voltage (V_{bc}) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{ec} is kept constant at 3V and the input voltage V_{bc} is increased from zero volts to different voltage levels. For each level of input voltage V_{bc} , the

corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (3V).



Input characteristics

Next, the output voltage V_{EC} is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage V_{EC} , the input voltage V_{BC} is kept constant at zero volts.

After we kept the output voltage V_{EC} constant at 5V, the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC} , the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (5V).

This process is repeated for higher fixed values of output voltage (V_{EC}).

Applying KVL from emitter to base ckt.

$$-V_{EC} + V_{EB} + V_{BC} = 0.$$

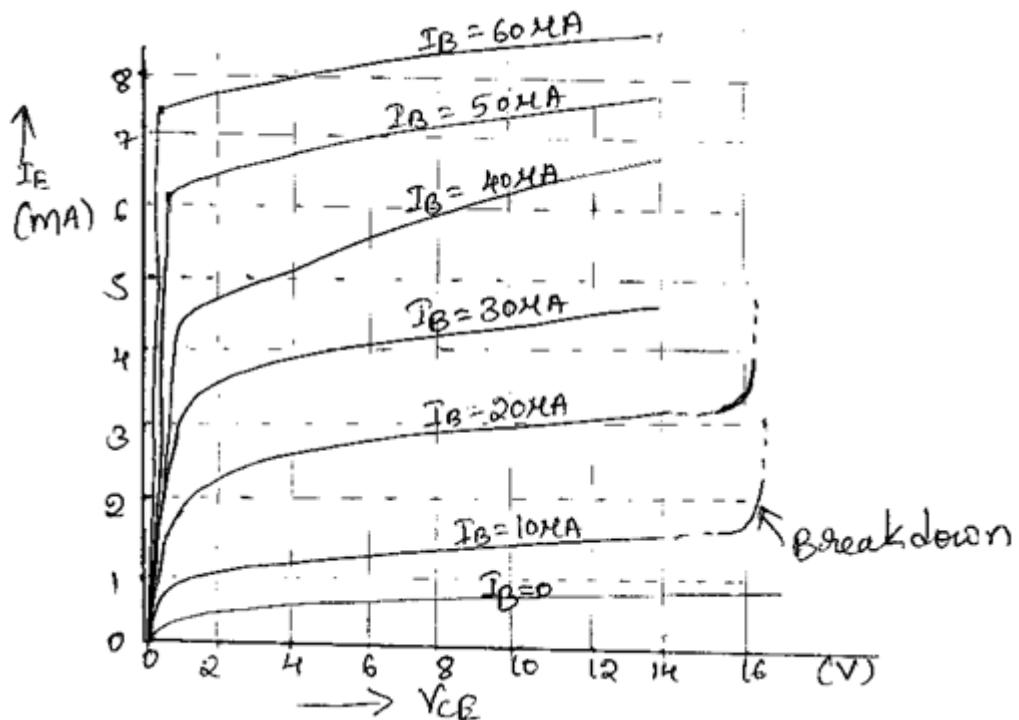
$$V_{BC} = V_{EC} - V_{EB} \rightarrow \textcircled{1}$$

$$V_{EB} = V_{EC} - V_{BC} \rightarrow \textcircled{2}$$

- * At a constant V_{EC} , if V_{BC} is increased, V_{EB} reduces and as a result I_B decreases.

Output characteristics

The output characteristics describe the relationship between output current or emitter current (I_E) and output voltage or emitter-collector voltage (V_{EC}).



- * common-collector o/p characteristic shows the variation of I_E as a function of V_{EC} at a constant I_B .
- * I_B is set to a convenient value, V_{EC} is varied in suitable steps and at each step I_E value is recorded.
The same procedure is repeated for different settings of I_B .
- * the common collector current gain characteristics are I_E plotted versus I_B for several fixed values of V_{CE} .
- * the I_C is approximately equal to I_E , the common collector o/p characteristics & current gain characteristics are - practically identical to those of the common-emitter circuit.

Field Effect Transistors

- 19.1 Types of Field Effect Transistors**
- 19.3 Principle and Working of JFET**
- 19.5 Importance of JFET**
- 19.7 JFET as an Amplifier**
- 19.9 Salient Features of JFET**
- 19.11 Expression for Drain Current (I_D)**
- 19.13 Parameters of JFET**
- 19.15 Variation of Transconductance (g_m or g_{fs}) of JFET**
- 19.17 JFET Biasing by Bias Battery**
- 19.19 JFET with Voltage-Divider Bias**
- 19.21 Practical JFET Amplifier**
- 19.23 D.C. Load Line Analysis**
- 19.25 Voltage Gain of JFET Amplifier (With Source Resistance R_s)**
- 19.27 Metal Oxide Semiconductor FET (MOSFET)**
- 19.29 Symbols for D-MOSFET**
- 19.31 D-MOSFET Transfer Characteristic**
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- 19.35 D-MOSFETs Versus JFETs**
- 19.37 E-MOSFET Biasing Circuits**



INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The FET is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding FET market has led many semiconductor market-

ing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

- (i) Junction field effect transistor (*JFET*)
- (ii) Metal oxide semiconductor field effect transistor (*MOSFET*)

To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET*.

19.2 Junction Field Effect Transistor (*JFET*)

A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier *i.e.*, electrons or holes.

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig. 19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (i) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (ii). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).

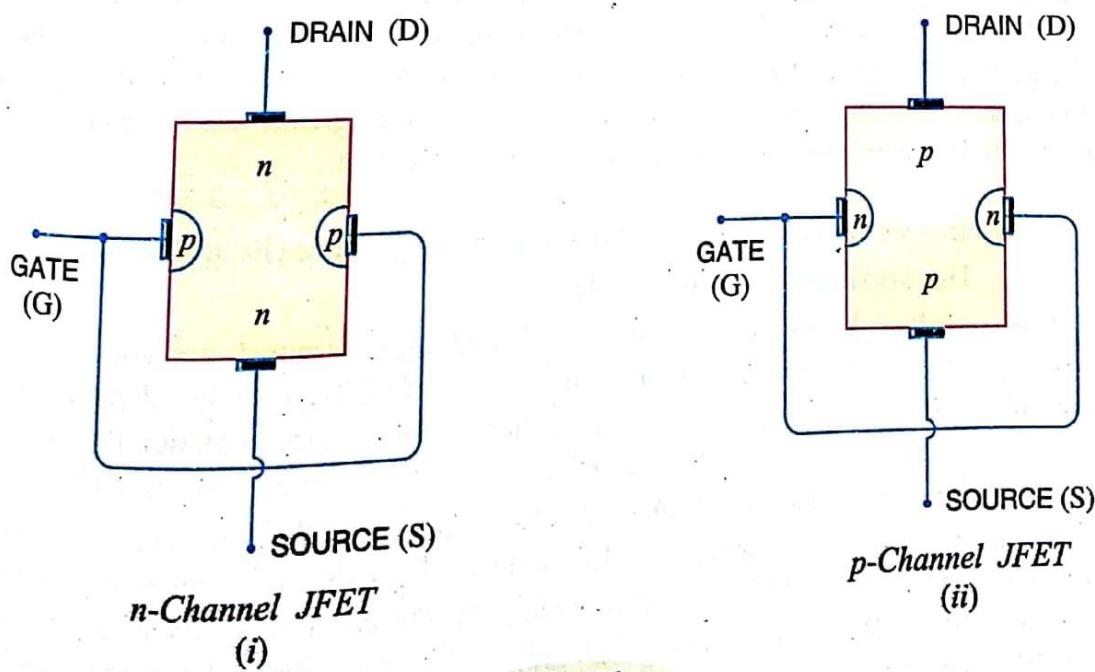


Fig. 19.1

It would seem from Fig. 19.1 that there are three doped material regions. However, this is not the case. The gate material *surrounds* the channel in the same manner as a belt surrounding your waist.

JFET polarities. Fig. 19.2 (i) shows *n*-channel JFET polarities whereas Fig. 19.2 (ii) shows *p*-channel JFET polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of JFET connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

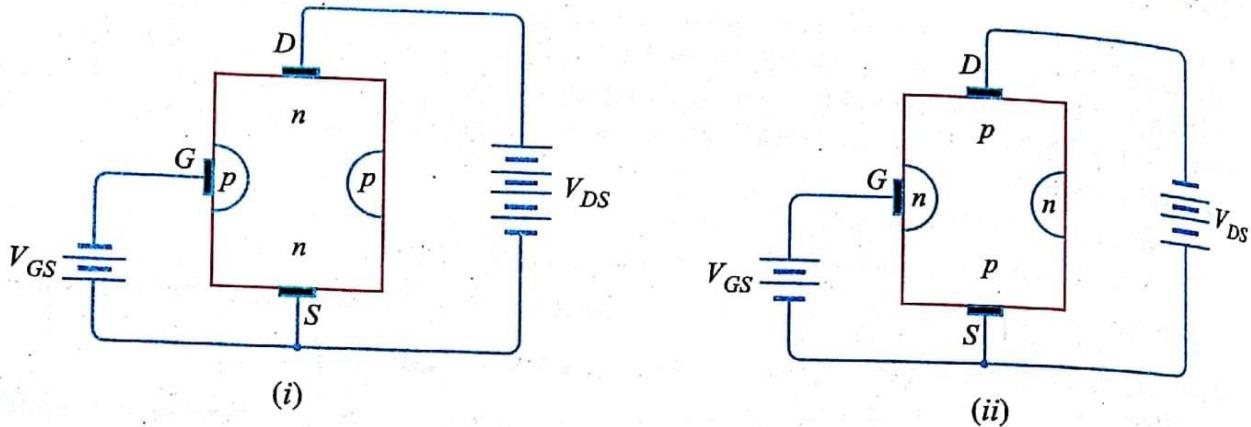


Fig. 19.2

The following points may be noted :

- (i) The input circuit (*i.e.* gate to source) of a JFET is reverse biased. This means that the device has high input impedance.
- (ii) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.
- (iii) In all JFETs, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel JFET with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS} . The greater the reverse voltage V_{GS} , the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS} .* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS} .

Working. The working of JFET is as under :

- (i) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (i)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.
- (ii) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (ii)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

The resistance of the channel depends upon its area of X-section. The greater the X-sectional area of this channel, the lower will be its resistance and the greater will be the current flow through it.

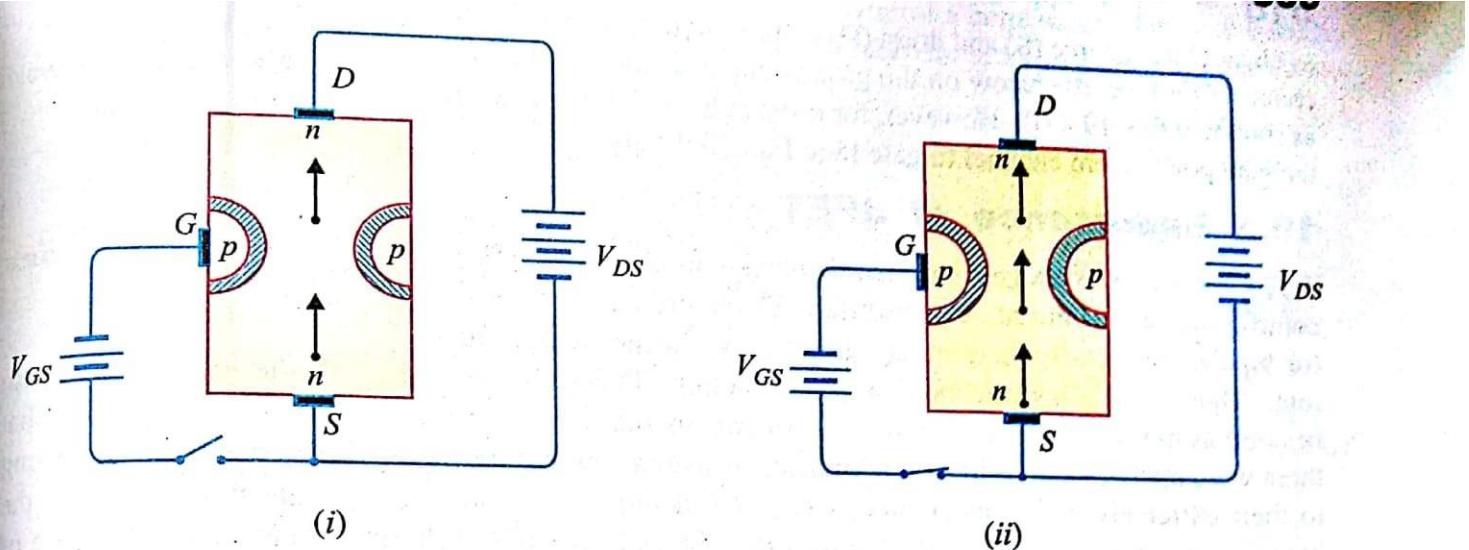


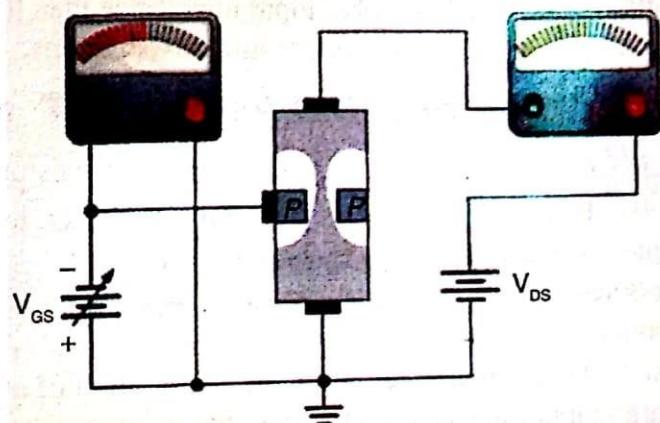
Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n*-channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

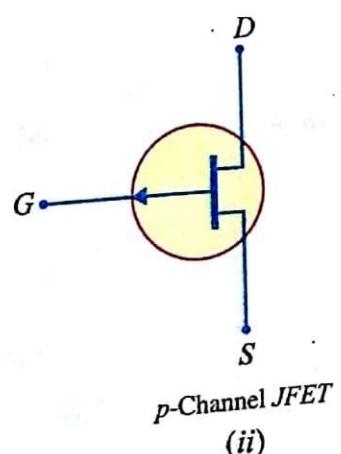
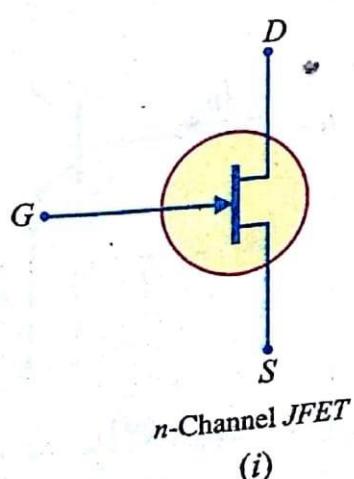
Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.

19.4 Schematic Symbol of JFET

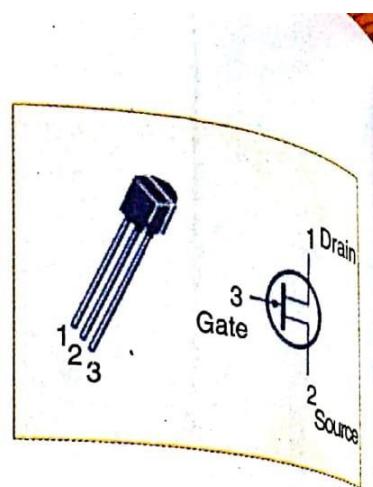
Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought



JFET biased for Conduction



as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (i). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (ii)].



19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(i) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(ii) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(iii) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0A$). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].

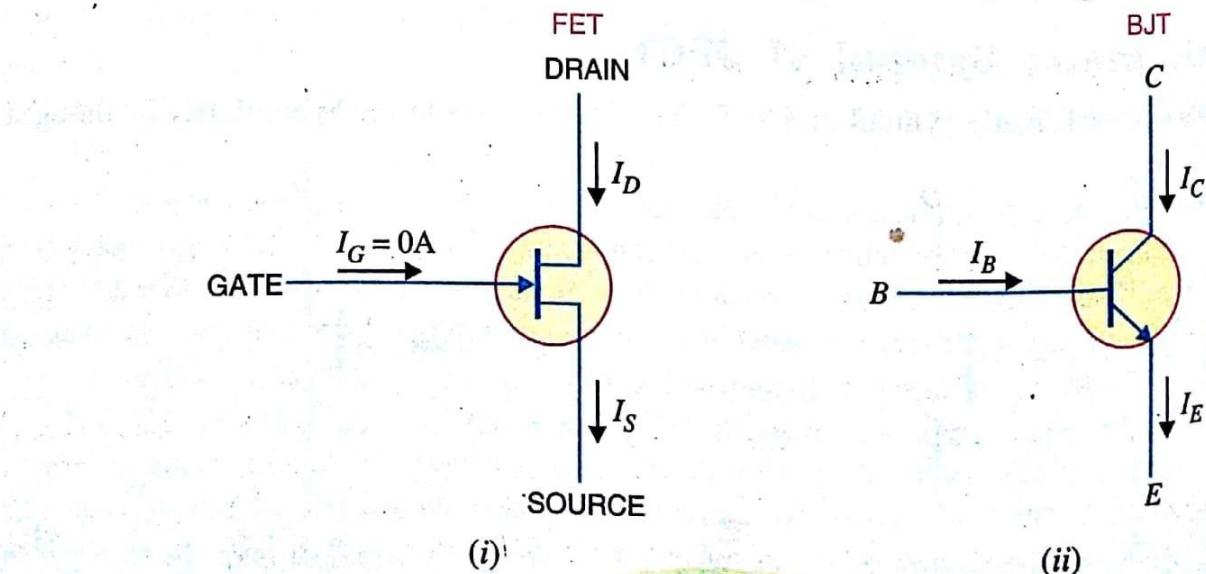


Fig. 19.5

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*-type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG} .

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L . In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drain-source voltage is changed in steps. Corresponding to each value of V_{DS} , the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at $V_{GS} = 1$ V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

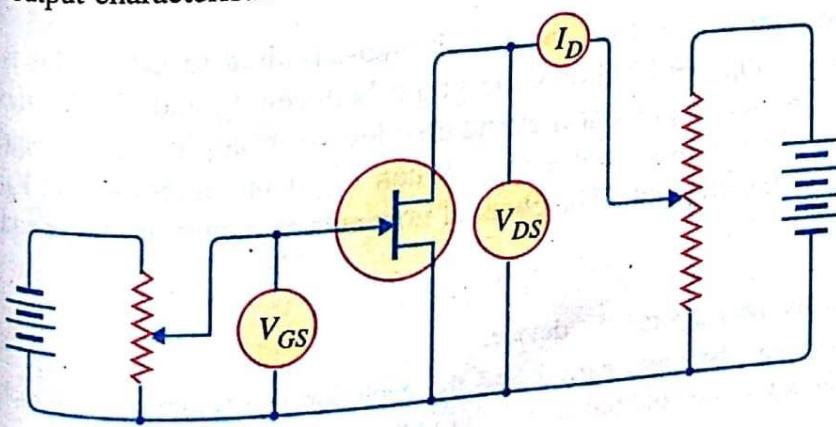


Fig. 19.7

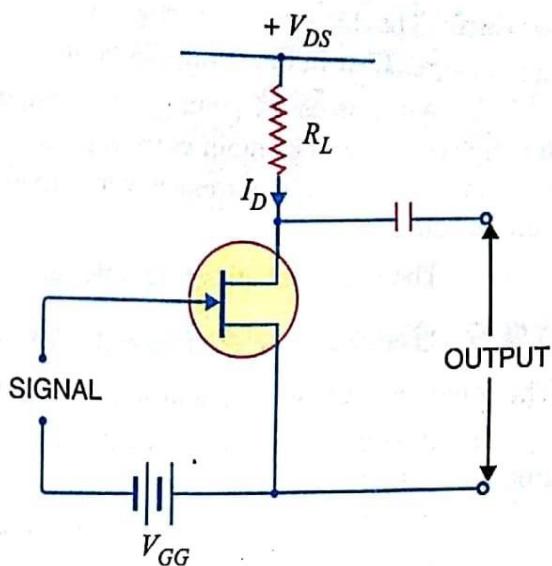


Fig. 19.6

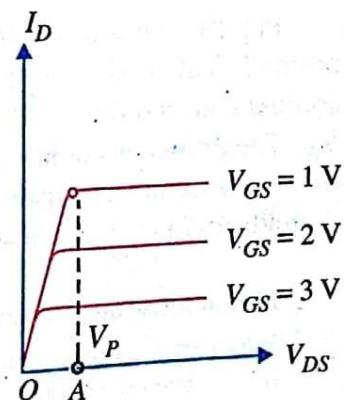


Fig. 19.8

19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device i.e. it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (i.e. decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as **depletion-mode operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) i.e. it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

A field effect transistor (FET) that can be operated in the enhancement-mode is called a MOSFET.

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs* viz.

1. Depletion-type *MOSFET* or *D-MOSFET*. The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.
2. Enhancement-type *MOSFET* or *E-MOSFET*. The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. **D-MOSFET.** Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons (∴ it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (i.e. substrate).

(ii) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals viz *source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.

With gate reverse biased, the channel is depleted (i.e. emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.

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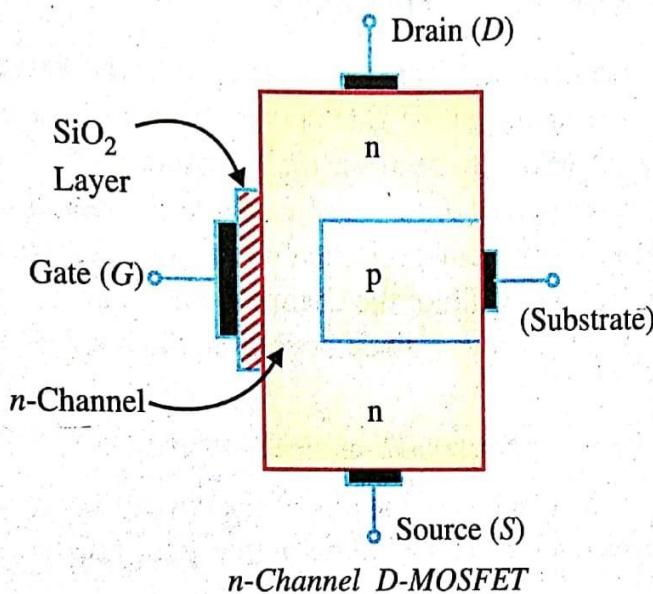


Fig. 19.43

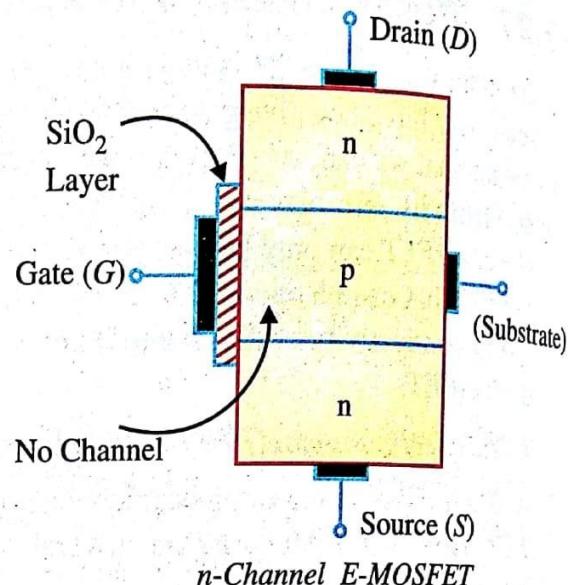


Fig. 19.44

2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET*. Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET*? The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET)*. However, this term is rarely used in place of the term *MOSFET*.

Module-3

OP-AMP's and its Applications

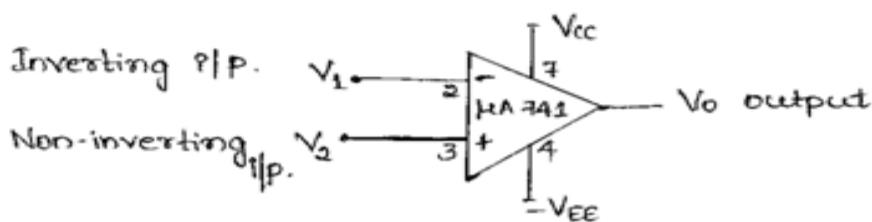
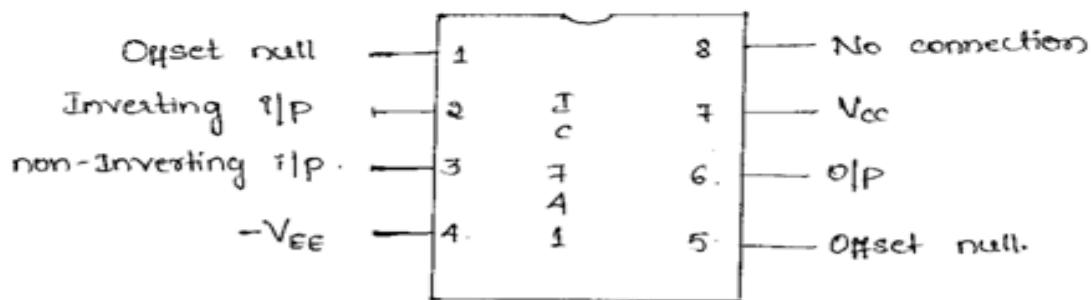
Define op-amp ?.

Op-amp is a directly coupled multistage voltage amplifier with high gain. It has very high input impedance and very low output impedance.

Op-amps are used for performing mathematical operations such as addition, subtraction, multiplication, integration and differentiation.

NOTE:- The op-amp is used to perform various mathematical operations. Thus it is called operational amplifier.

Pin diagram and op-amp symbol.



V_1 is the voltage at the inverting input.

V_2 is the voltage at the non-inverting input.

V_o is the output voltage.

- * The o/p voltage V_o is proportional to the difference between the i/p voltage.

$$\text{i.e. } V_o = A(V_2 - V_1)$$

Where A is the open-loop voltage gain.

Inverting mode :-

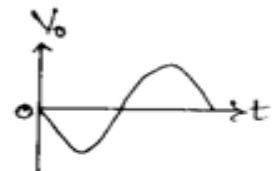
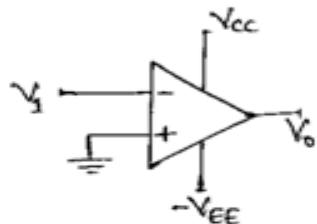
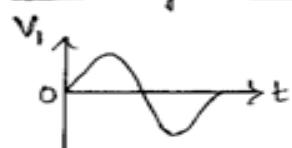


fig 1 : Inverting amplifier.

- * In inverting mode i/p is applied to the inverting terminal and non-inverting terminal is grounded.
- * The amplified voltage is 180° out of phase with respect to applied i/p voltage.
ie $V_o = -AV_1$.

NOTE :- Negative sign indicates that o/p is 180° out of phase.

Non-Inverting mode :-

In non-inverting mode, i/p is applied to the non-inverting terminal and inverting terminal is grounded.

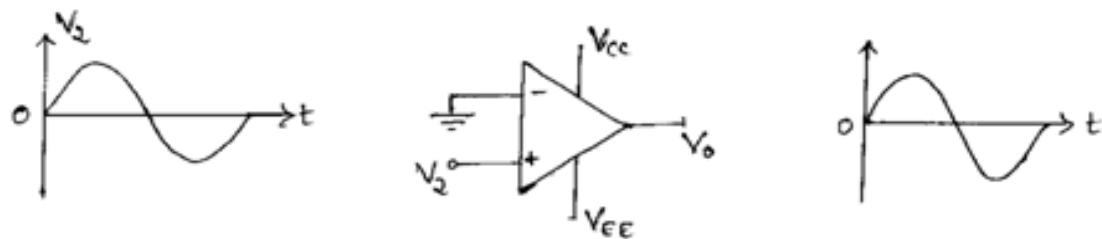


Fig 2 :- Non-Inverting amplifier.

- * The amplified o/p voltage is in phase w.r.t to applied i/p voltage.

$$\text{i.e. } V_o = A V_2.$$

Block-diagram of op-amp :-

Draw the block schematic of an op-amp and explain the function of each stage.

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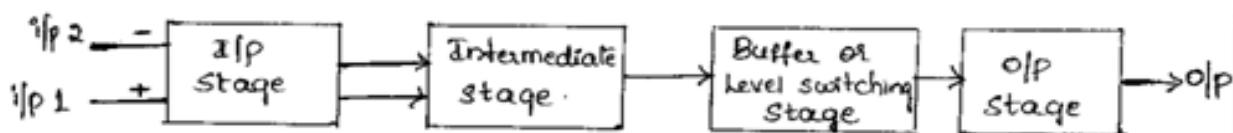


fig 1 : Block diagram of op-amp.

Input stage :-

The op-amp has two i/p terminals. Its o/p stage requires dual i/p terminals with high i/p impedance. These requirements are satisfied by the dual-i/p balanced differential amplifier. [Two i/p's & two o/p's].

Its function is to amplify the difference between the two i/p signals. It provides high differential gain, high i/p impedance and low o/p impedance.

Intermediate stage :-

The overall gain requirement of an op-amp is very high, since the i/p stage alone cannot provide such a high gain. The main function of the intermediate stage is provide such a high gain.

It consist of another differential amplifier with the dual i/p unbalanced o/p (Single ended). Practically the intermediate stage is chain of cascaded amplifiers called as multistage amplifiers are used.

Buffer and Level shifting stage :-

In intermediate stage all amplifiers are directly coupled. In the absence of coupling capacitors, DC voltage level gets amplified. Such a high DC level may drive the transistor into saturation. It causes distortion.

The level shifting stage brings the DC level to ground (zero).

O/p stage :- The o/p stage requires low o/p impedance large voltage swing. This is satisfied by class B push pull emitter follower circuit.

The ideal characteristics of op-amp are:-

1. Infinite voltage gain ($A_{OL} = \infty$) :-

The gain loop voltage gain (A_{OL}) of the ideal op-amp is very large infinity.

$$A_{OL} = \infty.$$

2. Infinite input impedance [$R_i = \infty$] :-

An ideal op-amp does not draw any current from the voltage source connected to its input terminals. Thus its o/p impedance is infinite.

$$\text{i.e. } R_{in} = \infty.$$

3. Zero output impedance [$R_o = 0$] :-

The o/p voltage of an ideal op-amp is independent of the current drawn from it. This means op-amp has zero o/p impedance. ie. infinite.

$$\text{i.e. } R_{out} = \infty, \text{ i.e. } R_o = 0.$$

4. Infinite Bandwidth ($BW = \infty$) :-

An ideal op-amp amplifies signals of any frequency with a constant gain, which implies that op-amp has infinite BW ie. $BW = \infty$.

5) Infinite CMRR [$P = \infty$] :-

[CMRR is defined as the ratio of differential voltage gain to common mode voltage gain]

$$\text{i.e. } \text{CMRR} = P = \frac{A_d}{A_c}$$

The common mode rejection ratio of an ideal op-amp is infinite i.e. $\text{CMRR} = \infty$.

6) Infinite slew rate [$SR = \infty$] :-

An ideal op amp has infinite slew rate this implies that the o/p voltage changes simultaneously with the i/p voltages.

7) The characteristics of an ideal op-amp do not change with temperature.

8) The power supply rejection ratio of an ideal op-amp is zero. i.e. $\text{PSRR} = 0$.

9) Zero offset voltage :-

The presence of small o/p voltage when $V_1 = V_2 = 0$ is called an offset voltage.

For an ideal op-amp offset voltage is zero.

i) CMRR :-

CMRR is defined as the ratio of the differential gain 'Ad' to the common mode gain 'Ac'.

$$\boxed{CMRR = P = \frac{Ad}{Ac}}$$

CMRR is always expressed in decibels as

$$\boxed{(CMRR)_{dB} = 20 \log_{10} \frac{Ad}{Ac}}$$

The typical value of CMRR for μA741 op-amp is 90 dB.

ii) Slew Rate :-

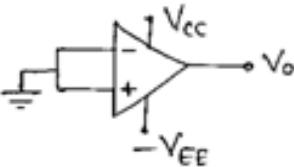
Slew rate of the op-amp is defined as the maximum rate of change of its o/p voltage w.r.t time & is expressed in volts per microsecond.

$$\boxed{SR = \left. \frac{dV_o}{dt} \right|_{\text{max.}} \text{V/μsec.}}$$

For 741, SR = 0.5 V / μsec.

(iii) lop offset voltage :-

When both the lop terminals are shorted and connected to ground, the lop should be ideally zero but practically there exists a small dc lop voltage known as lop offset voltage.



{ To make this lop voltage zero, a small voltage is required to be applied to one of the lop terminals. Such a voltage makes the lop exactly zero. This dc voltage, which makes the lop voltage zero is called lop offset voltage 'Vios'. }

iv) power supply voltage rejection ratio (PSRR) :-

PSRR is defined as the ratio of change in lop offset voltage due to change in the supply voltage producing it, keeping other power supply voltage constant.

* If V_{EE} is constant & due to change in V_{cc} , there is change in lop offset voltage then PSRR is expressed as.

$$\boxed{\text{PSRR} = \frac{\Delta V_{ios}}{\Delta V_{cc}} \mid V_{EE} \text{ constant}}$$

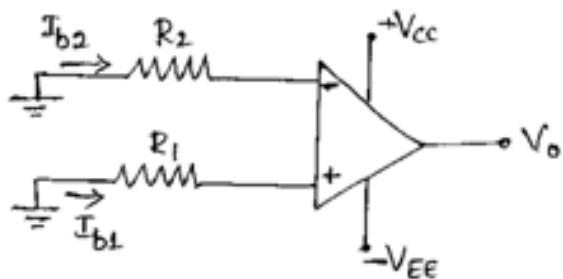
* If V_{cc} is constant & due to change in V_{EE} , there is change in lop offset voltage then PSRR is expressed as

$$\boxed{\text{PSRR} = \frac{\Delta V_{ios}}{\Delta V_{cc}} \mid V_{cc} \text{ constant}}$$

v) I_{IP} offset voltage :-

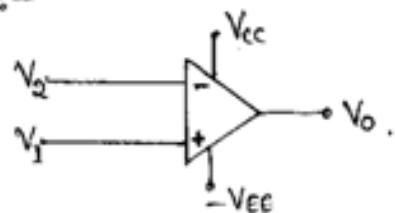
The dc voltage, which makes the o/p voltage zero, when the other terminal is grounded is called I_{IP} offset voltage. It also depends upon temperature.

- * The ideal value of I_{IP} offset voltage is zero but practically this value is small.

vi) I_{IP} bias current :-

It is defined as the average value of the individual current flowing into the INV and Non-INV I_{IP} terminals of the op-amp.

$$I_B = \frac{I_{b1} + I_{b2}}{2}$$

Open-loop amplifier :-

In open loop amplifier, there will be no feedback signal from o/p to I_{IP}.

The o/p voltage is $V_o = A_{OL}(V_1 - V_2)$

Closed loop amplifier :-

- * Explain why closed loop configuration of op-amp is used in all the practical amplifier circuit and bring out the advantages of closed loop operation with negative feedback.

June - 07, 6M

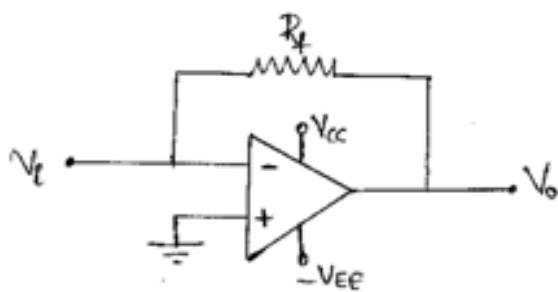


Fig: op-amp with negative feedback.

- * The closed loop amplifier is possible using feedback i.e. feeding some part of the o/p back to the I/p through resistor. Always op-amp is used with negative feedback.

The gain resulting with feedback is called closed loop gain of the op-amp. Due to -ve feedback gain decreases.

Advantages of -ve feedback :-

- 1) It reduces the gain and makes it controllable.
- 2) It reduces the distortion.
- 3) It increases the bandwidth.
- 4) It increases the I/p resistance of the op-amp.
- 5) It decreases the o/p resistance of the op-amp.
- 6) It reduces the effects of temperature and power supply.

Saturation property of op-amp :-

Saturating property of an op-amp in which the op voltage swing is below saturation voltage i.e $\pm V_{sat}$.

Thus if op tries to rise more than $+V_{cc}$ or less than $-V_{ee}$ then it gets clipped & gets saturated at the levels almost equal to $+V_{cc}$ & $-V_{ee}$.

Practically, the saturation voltage levels are about 90% of the supply voltage levels. Thus for an op-amp of supply $\pm 12V$, the saturation voltage levels are 90% of $\pm 12V$ i.e $\pm 10.8V$.

Op-amp Applications :-

The applications of op-amps are :-

- 1) Inverting amplifier.
- 2) Non-Inv amplifier.
- 3) Voltage follower.
- 4) Summer or Adder.
- 5) Subtractor or Difference amplifier
- 6) Integrator & .
- 7) Differentiator etc.

Non - INV amplifier.

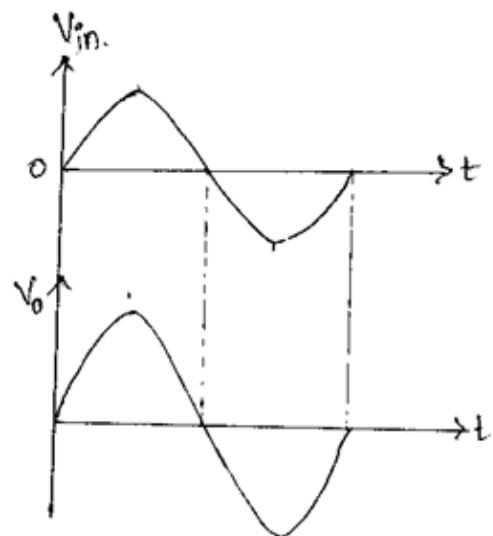
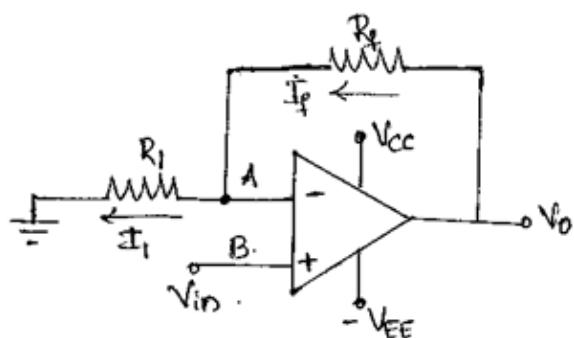


fig 1 @ : Non - INV amplifier.

- * In Non-INV amplifier o/p voltage is amplified & is in-phase with the IIP signal.
- * the potential at node B is V_{in} , hence the potential at node A is same as node B i.e $V_A = V_B = V_{in}$.

From IIP side, the current I is

$$I_1 = \frac{V_A - 0}{R_1}$$

$$\boxed{I_1 = \frac{V_{in}}{R_1}} \rightarrow \textcircled{1}$$

WKT - $\boxed{V_A = V_{in}}$

From OIP side.

$$I_f = \frac{V_o - V_A}{R_f}$$

$$\boxed{I_f = \frac{V_o - V_{in}}{R_f}} \rightarrow \textcircled{2}$$

Equating eq \textcircled{1} & \textcircled{2}

$$\frac{V_{in}}{R_1} = \frac{V_o - V_{in}}{R_f}$$

$$\frac{V_{in}}{R_1} = \underbrace{\frac{V_o}{R_f}}_{V_A} - \frac{V_{in}}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$\frac{V_o}{R_f} = V_{in} \left[\frac{1}{R_1} + \frac{1}{R_f} \right]$$

$$\frac{V_o}{V_{in}} = R_f \left[\frac{R_f + R_1}{R_1 R_f} \right]$$

$$\frac{V_o}{V_{in}} = \left[\frac{R_f}{R_1} + \frac{R_1}{R_f} \right]$$

$$\boxed{\frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right)} \rightarrow \textcircled{3}$$

In eq. ③, +ve sign indicates that the O/P is in-phase with the I/p.

INVERTING AMPLIFIER :-

- * Show how op-amp can be used as an inverting amplifier? Derive an expression for the voltage gain.

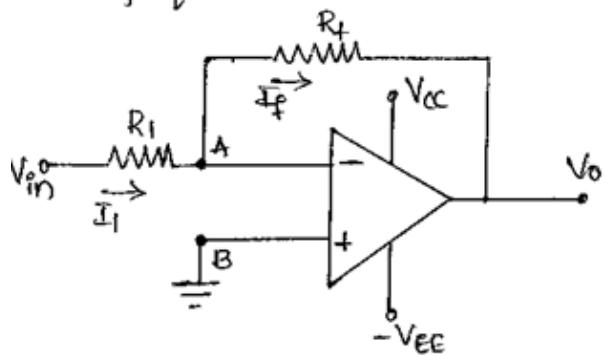
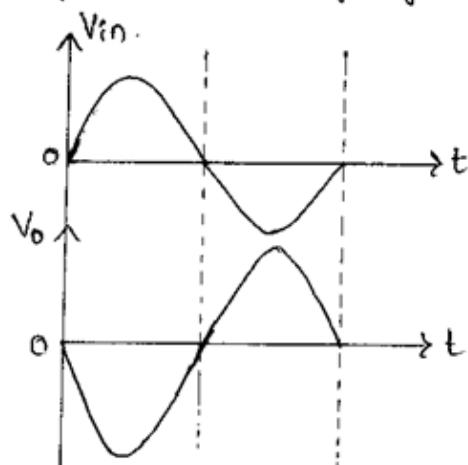


Fig 1 ④ : INV amplifier



- * In INV amplifier o/p voltage is amplified and is 180° out of phase with respect to the I/p Signal.
- * The potential at node B is zero, due to virtual ground concept the potential at node A is also zero.

$$\therefore V_A = V_B = 0$$

From I/p side,

$$I_i = \frac{V_{in} - V_A}{R_1} = \frac{V_{in} - 0}{R_1}$$

$$\boxed{I_i = \frac{V_{in}}{R_1}} \rightarrow \textcircled{1}$$

From o/p side,

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f}$$

$$\boxed{I_f = -\frac{V_o}{R_f}} \rightarrow \textcircled{2}$$

Equating eq \textcircled{1} & \textcircled{2} we get

$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = -\frac{V_{in}}{R_1}$$

$$\boxed{-\frac{V_o}{V_{in}} = -\left(\frac{R_f}{R_1}\right)}$$

Where R_f/R_1 is closed loop gain & -ve sign indicates that the polarity of o/p is opposite to that of i/p.

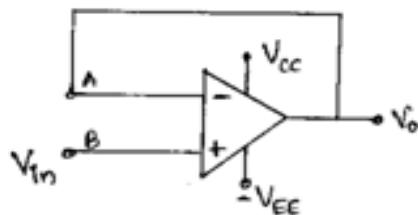
Voltage follower :-

Fig 1 @ : Voltage follower.

- * A ckt in which the op-amp follows.
- * op-amp voltage is called Voltage follower.
- * The potential at node B is V_{in} . Due to virtual ground concept the potential at node A is also V_{in} .

i.e. $V_A = V_B = V_{in}$

- * The node A is directly connected to op-amp terminal.

$$V_o = V_A$$

$$\therefore V_o = V_{in}$$

- * This circuit is also called source follower, unity gain amplifier buffer or isolation amplifier.

SUMMING or ADDER amplifier :-

- * With a neat diagram explain the working of an op-amp as summing amplifier. Jan - 10, 6M

When more than one op signal is applied to the INV or Non-INV amplifier, the op-amp contains addition of the applied op signals. Hence it is called summer or adder amplifier circuit.

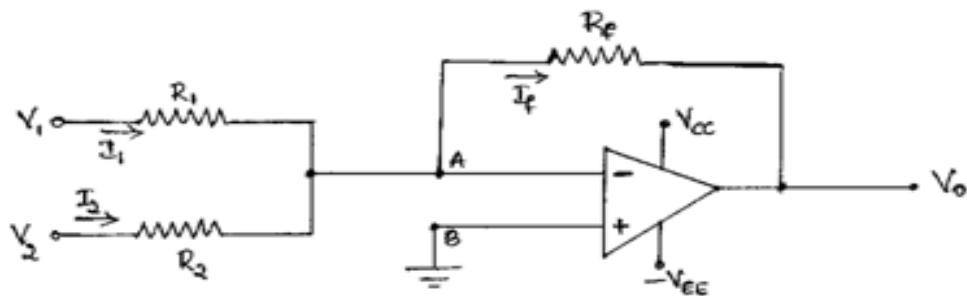
1) INV Summer amplifier ckt :-

Fig ① : INV Summing amplifier.

- * IIP signals which are to be added are applied to the INV IIP of op-amp.
- * As node B is grounded, due to virtual ground concept the node A is also at ground potential ie. $V_A = V_B = 0$.

From IIP side,

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1}$$

$I_1 = \frac{V_1}{R_1}$

 $\rightarrow ①$

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2}$$

$I_2 = \frac{V_2}{R_2}$

 $\rightarrow ②$

From OIP side,

$$I_f = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f}$$

$I_f = -\frac{V_o}{R_f}$

 $\rightarrow ③$

Applying KCL at node A,

$$I_1 + I_2 - I_f = 0.$$

$$I_f = I_1 + I_2$$

Substituting eq ①, ② & ③ in eq ④, we get

$$-\frac{V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2}$$

$$V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right]$$

If $R_1 = R_2 = R_f = R$, then

$$V_o = -R \left[\frac{V_1}{R} + \frac{V_2}{R} \right]$$

$$V_o = -\frac{R}{R} [V_1 + V_2]$$

$V_o = -[V_1 + V_2]$

ii) Non-INV summing amplifier:-

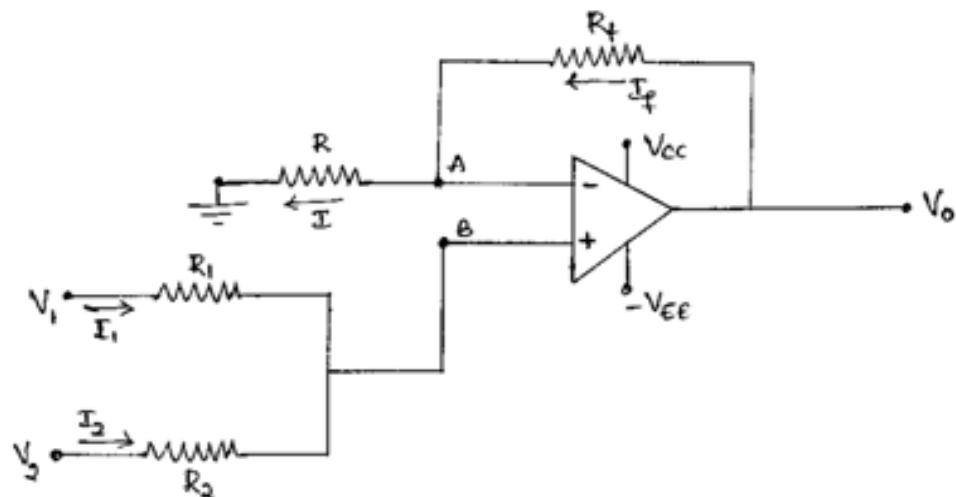


fig ①: Non-INV summing amplifier.

* Due to Virtual ground concept $V_A = V_B$ from zlp side.

$$I_1 = \frac{V_1 - V_B}{R_1} \rightarrow ①$$

$$I_2 = \frac{V_2 - V_B}{R_2} \rightarrow ②$$

WKT zlp current to op-amp is zero.

$$\therefore I_1 + I_2 = 0 \rightarrow ③$$

Substituting eq ① & ② in eq ③ we get

$$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0.$$

$$\frac{V_1}{R_1} - \frac{V_B}{R_1} + \frac{V_2}{R_2} - \frac{V_B}{R_2} = 0.$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_B}{R_1} + \frac{V_B}{R_2}$$

$$V_B \left[\frac{1}{R_1} + \frac{1}{R_2} \right] = \frac{V_1 R_2 + V_2 R_1}{R_1 R_2}$$

$$V_B \left[\frac{R_1 + R_2}{R_1 R_2} \right] = \frac{V_1 R_2 + V_2 R_1}{R_1 R_2}$$

$$V_B = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2} \rightarrow ④$$

Now at node A

$$I = \frac{V_A - 0}{R}$$

WKT $V_A = V_B$

$$I = \frac{V_B}{R} \rightarrow ⑤$$

From o/p side.

$$I = \frac{V_0 - V_A}{R_f} \quad \text{or} \quad V_A = V_B.$$

$$\boxed{I = \frac{V_0 - V_B}{R_f}} \rightarrow \textcircled{5}$$

Equating eq \textcircled{5} & \textcircled{6}, we get

$$\frac{V_B}{R} = \frac{V_0 - V_F}{R_f}$$

$$\frac{V_B}{R} = \frac{V_0}{R_f} - \frac{V_B}{R_f}$$

$$\frac{V_B}{R} + \frac{V_F}{R_f} = \frac{V_0}{R_f}$$

$$V_B \left[\frac{1}{R} + \frac{1}{R_f} \right] = \frac{V_0}{R_f}$$

$$\frac{V_0}{R_f} = V_B \left[\frac{R + R_f}{RR_f} \right]$$

$$\boxed{V_0 = V_B \left[\frac{R + R_f}{R} \right]} \rightarrow \textcircled{6}$$

Substituting eq \textcircled{4} in eq \textcircled{6}, we get

$$V_0 = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2} \left[\frac{R + R_f}{R} \right]$$

$$\text{If } R_1 = R_2 = R_f = R$$

$$V_0 = \frac{V_1 R + V_2 R}{R + R} \left(\frac{R + R}{R} \right)$$

$$= R(V_1 + V_2) \cdot \frac{1}{R}$$

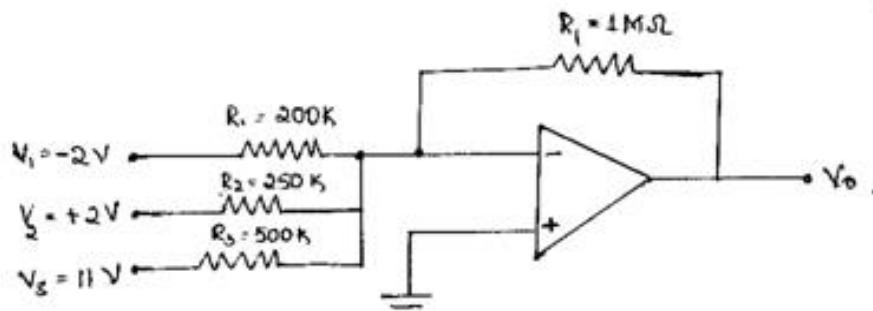
$$\boxed{V_0 = V_1 + V_2}$$

* calculate the output voltage of a three input summing amplifier given :

$$R_1 = 200\text{ k}\Omega, R_2 = 250\text{ k}\Omega, R_3 = 500\text{ k}\Omega, R_f = 1\text{ M}\Omega, V_1 = -2\text{ V},$$

$$V_2 = -2\text{ V}, V_3 = +2\text{ V}, V_s = +1\text{ V}.$$

June - 03, 6M



$$\text{Given : } R_f = 1\text{ M}\Omega, R_1 = 200\text{ k}\Omega, R_2 = 250\text{ k}\Omega, R_3 = 500\text{ k}\Omega \dots$$

$$V_1 = -2\text{ V}, V_2 = +2\text{ V}, V_3 = +1\text{ V}.$$

SOLⁿ: WKT for the summing amplifier.

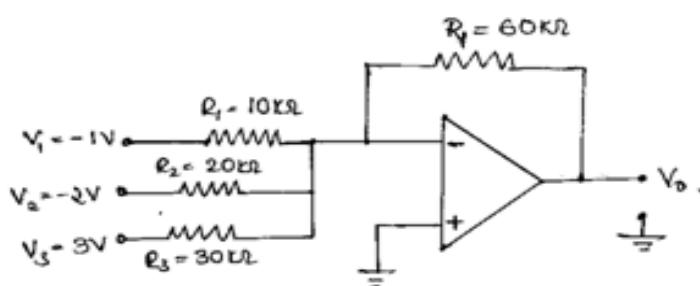
$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$= - \left[\frac{1 \times 10^6}{200 \times 10^3} (-2) + \frac{1 \times 10^6}{250 \times 10^3} (2) + \frac{1 \times 10^6}{500 \times 10^3} (1) \right]$$

$$V_o = - [-10 + 8 + 2]$$

$V_o = 0\text{ V}$

(2) For the circuit shown in fig, calculate the o/p Voltage



July-04, 5M

Given : $V_1 = -1V$, $V_2 = -2V$, $V_3 = 3V$ $R_1 = 10k\Omega$, $R_2 = 20k\Omega$, $R_3 = 30k\Omega$, $R_f = 60k\Omega$, $V_o = ?$

$$\begin{aligned} \text{Sol :- } V_o &= - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right] \\ &= - \left[\frac{60 \times 10^3}{10 \times 10^3} (-1) + \frac{60 \times 10^3}{20 \times 10^3} (-2) + \frac{60 \times 10^3}{30 \times 10^3} (3) \right] \\ &= -[-6 - 6 + 6] = -[-6] \end{aligned}$$

$$\boxed{V_o = 6V}$$

- * An op-amp is used as an inverting amplifier to amplify an input sine wave of amplitude 100mV (peak to peak). The input resistance $R_i = 1k\Omega$ & feedback resistance $R_f = 10k\Omega$. Calculate the voltage gain and sketch the output waveform to scale.

Jan-05, 6M

Given : $V_{in} = 100mV$, $R_f = 10k\Omega$, $R_i = 1k\Omega$

$$V_o = ? \quad A_f = ?$$

* WOKT. $A_f = -\frac{R_f}{R_i}$

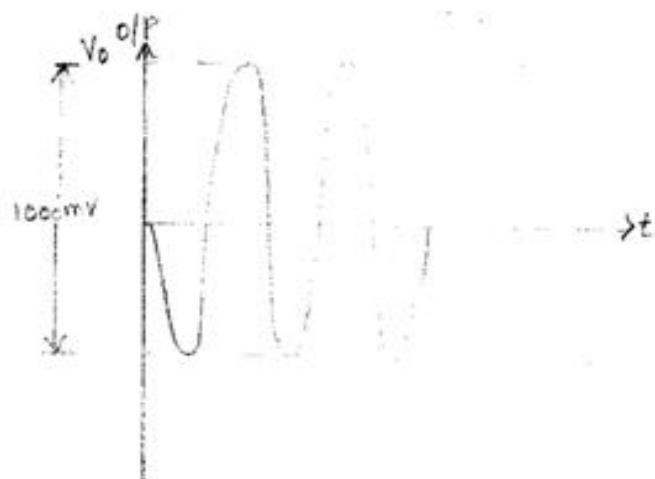
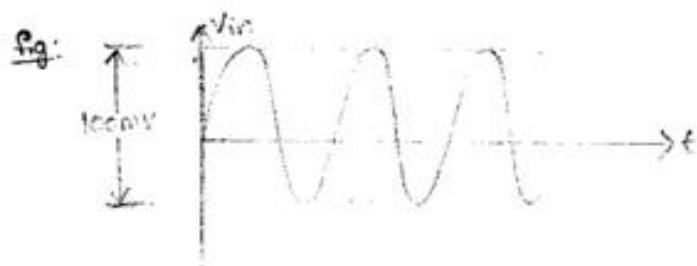
$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

$$V_o = -\frac{R_f}{R_i} \times V_i = -\frac{10 \times 10^3}{1 \times 10^3} \times 100 \times 10^{-3}$$

$V_o = -1V$

* Voltage gain = $A_f = \frac{V_o}{V_{in}} = -\frac{1V}{100 \times 10^{-3}} V$

$A_f = 10$



* Design an adder circuit using an op-amp to obtain an output expression.

$$V_o = 2(0.1V_1 + 0.5V_2 + 20V_3) \text{ where } V_1, V_2 \text{ & } V_3 \text{ are inputs.}$$

Given: $V_o = 2(0.1V_1 + 0.5V_2 + 20V_3)$

June -05, 5M

$$\frac{R_f}{R_1} = 0.2, \quad \frac{R_f}{R_3} = 40, \quad \frac{R_f}{R_2} = 1$$

Sol:- Assuming $R_f = 10\text{ k}\Omega$

* $\frac{R_f}{R_1} = 0.2$

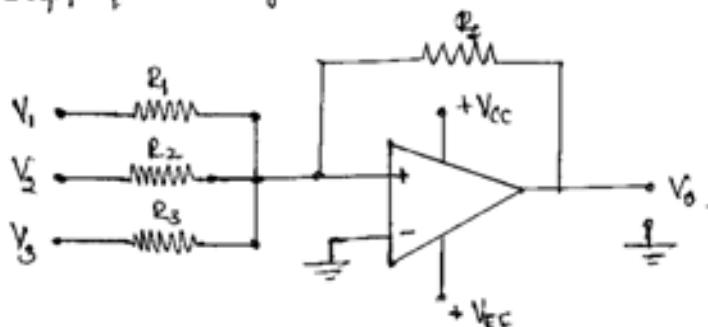
$$R_1 = \frac{R_f}{0.2} = \frac{10\text{ k}\Omega}{0.2} = 50\text{ k}\Omega$$

* $\frac{R_f}{R_2} = 1, \quad R_2 = \frac{R_f}{1} = \frac{10\text{ k}\Omega}{1} = 10\text{ k}\Omega$

* $\frac{R_f}{R_3} = 40, \quad R_3 = \frac{R_f}{40} = \frac{10\text{ k}\Omega}{40} = 250\text{ }\Omega$

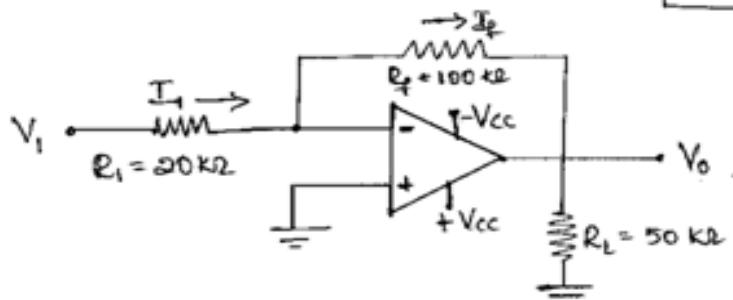
* $\frac{R_f}{R_3} = 40, \quad R_3 = \frac{R_f}{40} = \frac{10\text{ k}\Omega}{40} = 250\text{ }\Omega$

The supply voltages $+V_{CC}$ & $-V_{EE}$ may be $\pm 15\text{ V}$.



- * An inverting amplifier circuit has input series resistor of $20\text{ k}\Omega$, feedback resistor of $100\text{ k}\Omega$ and a load resistor of $50\text{ k}\Omega$. Draw the circuit and calculate the input current, load current and the output voltage when the applied input voltage is equal to $+1.5\text{ V}$.

June - 07, 8M



Given: $R_1 = 20\text{ k}\Omega$, $I_i = ?$, $R_L = 50\text{ k}\Omega$, $V_i = 1.5\text{ V}$.

$R_f = 100\text{ k}\Omega$, $V_o = ?$

$$(i) I_i = \frac{V_i}{R_1} = \frac{1.5}{20 \times 10^3} = \frac{1.5 \times 10^{-3}}{20} = 0.075 \times 10^{-3} \text{ A.}$$

$$(ii) V_o = -\frac{R_f}{R_1} \times V_i = -\frac{100 \times 10^3 \times 1.5}{20 \times 10^3} = -7.5\text{ V.}$$

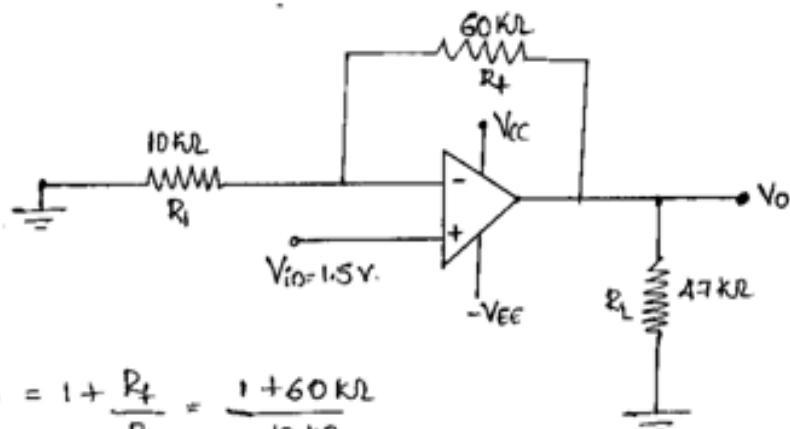
$$(iii) I_L = \frac{V_o}{R_L} = \frac{-7.5}{50 \times 10^3} = -0.15 \times 10^{-3} \text{ A.}$$

- * A non inverting amplifier has input resistance $10\text{ k}\Omega$ and feedback resistance $60\text{ k}\Omega$ with load resistance $47\text{ k}\Omega$. Draw the circuit and calculate output voltage, voltage gain and load current when input voltage is 1.5 V .

Jan - 08, 8M

Given: $R_i = 10\text{ k}\Omega$, $R_f = 60\text{ k}\Omega$, $R_L = 47\text{ k}\Omega$, $V_i = 1.5\text{ V}$.

$V_o = ?$, $I_L = ?$



NKT

$$A_f = 1 + \frac{R_f}{R_i} = \frac{1 + 60 \text{ k}\Omega}{10 \text{ k}\Omega}$$

for Non-inv amp $A_f = 7$.

$$A_f = \frac{V_o}{V_i} = V_o = A_f \cdot V_i = 7 \times 1.5 \text{ V}$$

$V_o = 10.5 \text{ V}$

$$I_L = \frac{V_o}{R_L} = \frac{10.5 \text{ V}}{4.7 \times 10^3} = 0.2234 \text{ mA}$$

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES: CO2
FACULTY NAME:	
DATE:	
LECTURE HOUR: 41	
OBJECTIVES OF THE LECTURE:	
To study and understand the basics of communication.	
To study and understand the Elements of Communication System.	
<h2>Module 4: COMMUNICATION SYSTEMS</h2> <h3>Introduction</h3> <p>Communication is basic process of exchanging information. In today's world, there are number of modern communication system in use, which include radio telephony and telegraphy, broadcasting, point to point and mobile communication etc.</p> <p>a) Broadcasting: It consists of a single powerful transmitter and numerous receivers that are relatively inexpensive to build. Here, information bearing signals flows only in one direction. E.g. AM, FM broadcasts, TV broadcasts etc.</p> <p>b) Point to Point Communication: In this mode, communication process takes place over a link between a single TX and a Rx. In this case there's usually a bidirectional flow of information bearing signals which require the use of a TX and a RX at each end of the link.</p> <p>Primary Communication Resources:</p> <p>In communication system, two primary resources are employed.</p> <ul style="list-style-type: none"> i) Transmitted Power: average power of the transmitting signal ii) Channel Bandwidth: band of frequencies allocated for the transmission of the message signal. <p>Typically, one resource may be important than the other. i.e. Power limited channel (telephone circuit), Band limited channel (satellite channel).</p> <p>Depending upon the mode of transmission channel can also be divided into guided propagation (telephone channels, Coaxial cables and fibers) and free Propagation (broadcast, radio channels, satellite channels).</p>	

Analog and Digital Communication Systems

Analog communication source produces messages that are defined on continuum. Ex: Microphone – the output voltage describes the information in the sound and it is distributed over a continuous range of values.

Digital communication source produces a finite set of possible messages. Ex: Typewriter – there is a finite number of characters (messages) that can be emitted by this source.

Analog communication system transfers information from an analog source to an intended receiver (sink). Analog communication signals, such as AM & FM signals, are analog signal. They are continuous and vary in amplitude, frequency or phase Ex: AM & FM systems. Analog waveform is a function of time that has a continuous range of values. Ex: sinusoidal waveform.

Digital communication system transfers information from a digital source to an intended receiver (sink). They are discrete, discontinuous pulses that have one of M distinct waveforms. If $M = 2$, this is a binary digital system. Ex: pager & mobile. Digital waveform is a function of time that can have only a discrete set of values. Ex: rectangular pulse.

Comparison between Analog Communication System and Digital Communication System

	ADVANTAGES	DISADVANTAGES
ANALOG COMMUNICATION SYSTEM	<ul style="list-style-type: none"> • Smaller bandwidth. • Synchronization problem is relatively easier. 	<ul style="list-style-type: none"> • Expensive analog components. • No privacy. • Cannot merge data from different sources. • No error correction capability.
DIGITAL COMMUNICATION SYSTEM	<ul style="list-style-type: none"> • Inexpensive digital circuits. • Privacy preserved (data encryption). • Can merge different data (voice, video and data) and transmit over a common digital transmission system. • Error correction by coding. 	<ul style="list-style-type: none"> • Larger bandwidth • Synchronization problem is relatively difficult.

Elements of Communication System

Radio communication means the radiation of radio waves by the transmitting station, the propagation of these waves through space and their reception by the radio receiver. Fig. below shows the general principle of radio broadcasting, transmission and reception. It essentially consists of transmitter, transmission of radio waves and radio receiver.

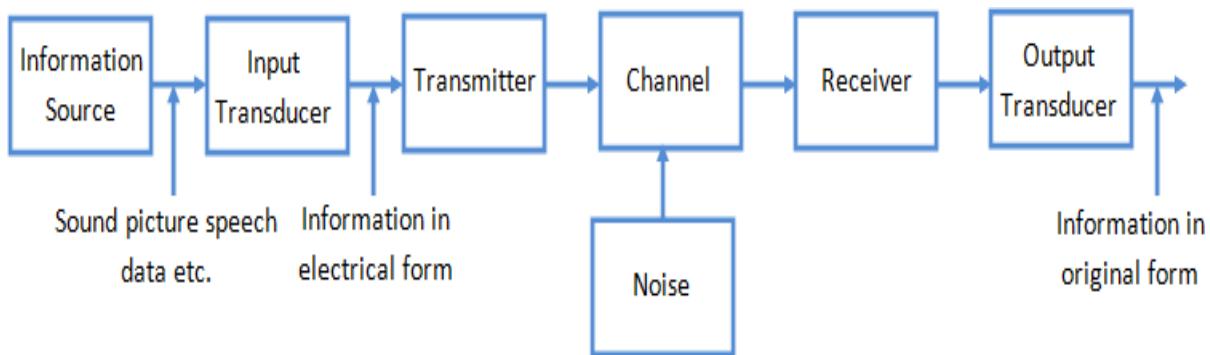


Fig.5.1 Block diagram of communication system

Information Source

- As we know, a communication system serves to communicate a message or information. This information originates in the information source.
- In general, there can be various messages in the form of words, group of words, code, symbols, sound signal etc. However, out of these messages, only the desired message is selected and communicated.
- Therefore, we can say that the function of information source is to produce required message which has to be transmitted.

Input Transducer

- A transducer is a device which converts one form of energy into another form.
- The message from the information source may or may not be electrical in nature. In a case when the message produced by the information source is not electrical in nature, an input transducer is used to convert it into a time-varying electrical signal.
- For example, in case of radio-broadcasting, a microphone converts the information or message which is in the form of sound waves into corresponding electrical signal.

Transmitter

- The function of the transmitter is to process the electrical signal from different aspects.
- For example in radio broadcasting the electrical signal obtained from sound signal, is processed to restrict its range of audio frequencies (upto 5 kHz in amplitude modulation radio broadcast) and is often amplified.
- In wire telephony, no real processing is needed. However, in long-distance radio communication, signal amplification is necessary before modulation.
- Modulation is the main function of the transmitter. In modulation, the message signal is superimposed upon the high-frequency carrier signal.
- In short, we can say that inside the transmitter, signal processing such as restriction of range of audio frequencies, amplification and modulation of are achieved.
- All these processing's of the message signal are done just to ease the transmission of the signal through the channel.

The Channel and the Noise

- The term channel means the medium through which the message travels from the transmitter to the receiver. In other words, we can say that the function of the channel is to provide a physical connection between the transmitter and the receiver.
- There are two types of channels, namely point-to-point channels and broadcast channels.
- Example of point-to-point channels are wire lines, microwave links and optical fibres. Wire-lines operate by guided electromagnetic waves and they are used for local telephone transmission.
- In case of microwave links, the transmitted signal is radiated as an electromagnetic wave in free space. Microwave links are used in long distance telephone transmission.
- An optical fibre is a low-loss, well-controlled, guided optical medium. Optical fibres are used in optical communications.
- Although these three channels operate differently, they all provide a physical medium for the transmission of signals from one point to another point. Therefore, for these channels, the term point-to-point is used.

- On the other hand, the broadcast channel provides a capability where several receiving stations can be

reached simultaneously from a single transmitter.

- An example of a broadcast channel is a satellite in geostationary orbit, which covers about one third of the earth's surface.
- During the process of transmission and reception the signal gets distorted due to noise introduced in the system.
- Noise is an unwanted signal which tends to interfere with the required signal. Noise signal is always random in character. Noise may interfere with signal at any point in a communication system. However, the noise has its greatest effect on the signal in the channel.

Receiver

The main function of the receiver is to reproduce the message signal in electrical form from the distorted received signal. This reproduction of the original signal is accomplished by a process known as the demodulation or detection. Demodulation is the reverse process of modulation carried out in transmitter.

Destination

Destination is the final stage which is used to convert an electrical message signal into its original form. For example in radio broadcasting, the destination is a loudspeaker which works as a transducer i.e. converts the electrical signal in the form of original sound signal.

IMPORTANT POINTS TO REMEMBER:

- Communication is basic process of exchanging information
- Principle of radio broadcasting, transmission and reception.
- A transducer is a device which converts one form of energy into another form

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Define Communication. Explain the elements of communication system.
2. With neat block diagram explain the communication system

REFERENCES:

1. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.1 to 4.
2. http://npteldownloads.iitm.ac.in/downloads_mp4/117102059/lec01.mp4
3. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES: CO2
FACULTY NAME:	
DATE:	
LECTURE HOUR: 42	

OBJECTIVES OF THE LECTURE:

- To study and understand the basic concept of Modulation.
- To study and understand the need for Modulation.

Modulation

It's a process of transmitting information over a medium. It can be defined as the process by which some characteristics/parameter (frequency, amplitude, phase) of high frequency carrier is varied with the low frequency message signal. Modulation occurs at the transmitting end of the system.

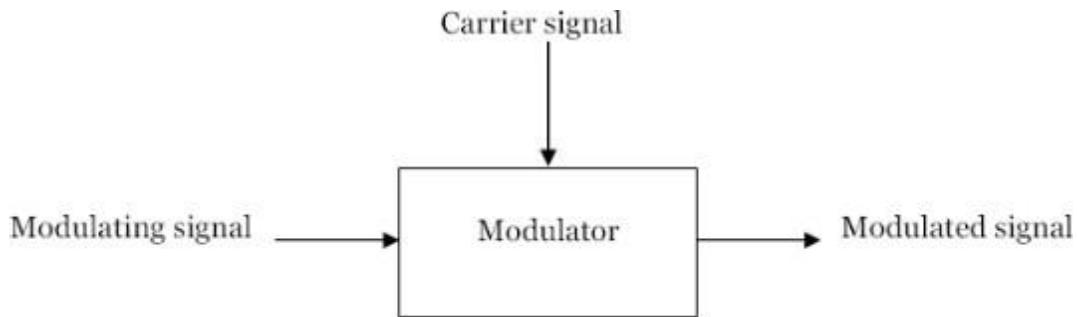


Fig. Block Diagram of a Modulation Process



Fig. Block Diagram of Modulation and Demodulation Process

Demodulation is the reverse process of modulation and converts the modulated carrier back to the original information (that is, extracting the message signal from the carrier).

Need for modulation

The advantages of using modulation technique are given below:

- Reduce the height of the antenna
- Increase the range of communication
- Avoids mixing of signals
- Allows multiplexing of signals
- Improves the signal to noise ratio.
- Avoids interference of the bands by providing guard band
- Improve quality of reception
- Provide possibility for wireless transmission.

1. Practical Antenna length

Theory shows that in order to transmit a wave effectively the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$\text{wavelength} = \frac{\text{Velocity}}{\text{frequency}} = \frac{3 \times 10^8}{\text{frequency (Hz)}} \text{ metres}$$

As the audio frequencies range from 20 Hz to 20Khz, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For example to radiate a frequency of 20 KHz directly into space we would need an antenna length of $3 \times 10^8 / 20 \times 10^3 \approx 15,000$ meters. This is too long to be constructed practically. But instead we operate at higher frequencies, say in MHz range, the antenna dimension comes down. The operation at this frequencies is possible only with modulation techniques.

2. Operating Range

The energy of a wave depends upon its frequency. The greater the frequency of the wave,

the greater the energy possessed by it. As the audio signal frequencies are small, therefore these cannot be transmitted over large distances if radiated directly into space.

3. Avoids mixing of signals:

The transmission band of 20Hz to 20KHz contains many signals generated from different sources. These signals are translated to different portion of the electromagnetic spectrum called channels, having different band widths, by providing different carrier frequencies. These frequencies are separated at the receiver while receiving.

4. Allows multiplexing of signals

The modulation permits multiplexing of signals, meaning simultaneous transmission of more signals on the same channel. Example MW and SW transmission with frequencies allotted to different bands and transmitted on the same channel

5. Improves the signal to noise ratio

The base band signals which are in the audio frequency range are susceptible to noise. The radio frequencies which are used for modulation are immune to noise. Hence modulating the message signals with the carrier helps in improving the signal to noise ratio.

6. Avoids interference of the bands by providing guard band

Special guard bands are provided between bands to guard the interference of adjacent band signals. This is usually around 25KHz.

7. Improve quality of reception

Different techniques of transmission like digital modulation improves the quality of reception by reducing the noise in the system.

8. Wireless communication

Radio transmission should be carried out without wires.

IMPORTANT POINTS TO REMEMBER:

- Modulation is a process of transmission of information over a medium.
- Length of the transmitting antenna should be approximately equal to the wavelength of the wave.
- The radio frequencies which are used for modulation are immune to noise

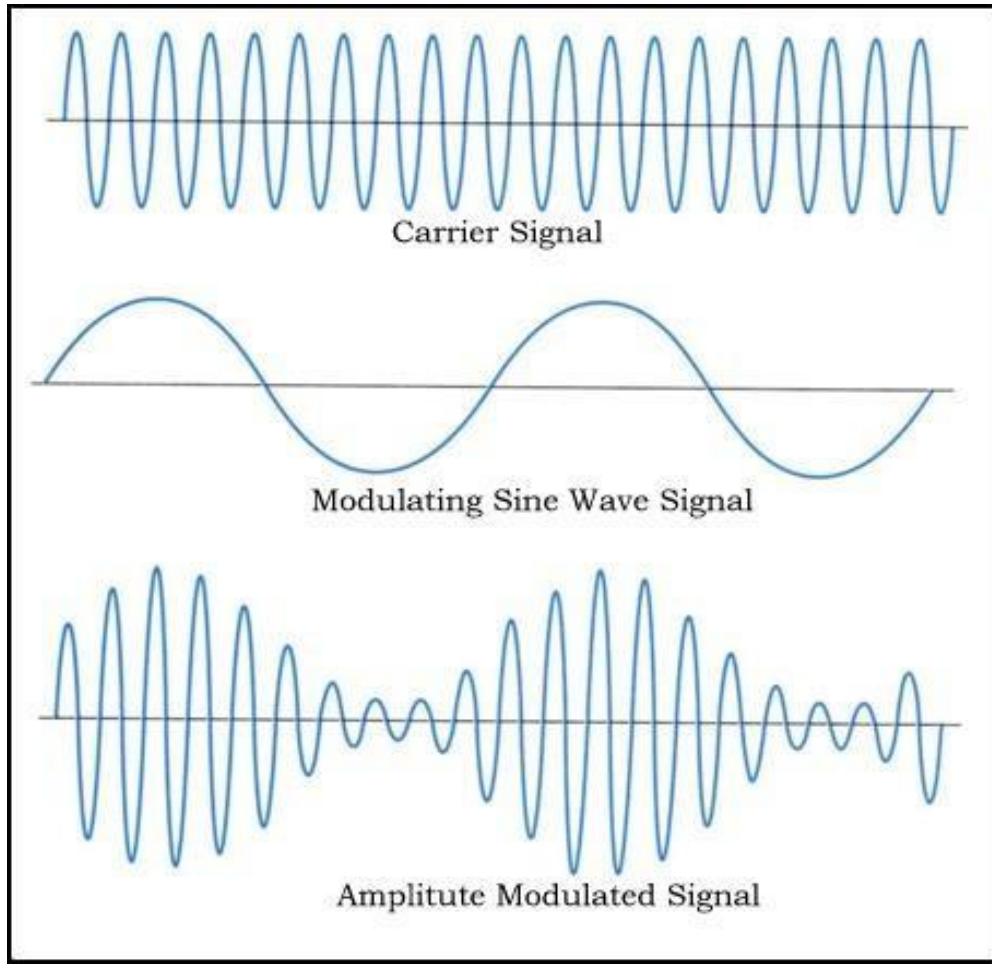
BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. What is modulation? Explain the need for modulation? (May 2009, Jan 2015 ..5Marks)

REFERENCES:

4. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.5 to 6.
5. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES:
FACULTY NAME:	CO2
DATE:	
LECTURE HOUR: 43	
OBJECTIVES OF THE LECTURE:	
<p>To study and understand the principle of Amplitude modulation</p> <p>To derive the equation for instantaneous output voltage of amplitude modulated wave.</p>	
<h3>Types of modulation</h3> <ol style="list-style-type: none"> 1. Amplitude modulation 2. Frequency modulation 3. Phase modulation <p>1. Amplitude modulation</p> <p>When the amplitude of high frequency carrier wave is changed in accordance with the intensity of the signal, it is called amplitude modulation. The following points are to be noted in amplitude modulation .</p> <ol style="list-style-type: none"> 1. The amplitude of the carrier wave changes according to the intensity of the signal. 2. The amplitude variations of the carrier wave is at the signal frequency f_S. 3. The frequency of the amplitude modulated wave remains the same ie.carrier frequency f_C. <ul style="list-style-type: none"> ➤ The carrier signal frequency would be greater than the modulating signal frequency. ➤ Amplitude modulation is first type of modulation used for transmitting messages for long distances by the mankind. ➤ The AM radio ranges in between 535 to 1705 kHz which is great. But when compared to frequency modulation, the Amplitude modulation is weak, but still it is used for transmitting messages. ➤ Bandwidth of amplitude modulation should be twice the frequency of modulating signal or message signal. ➤ If the modulating signal frequency is 10 kHz then the Amplitude modulation frequency should be around 20 kHz. In AM radio broadcasting, the modulating signal or message signal is 15 kHz. Hence the AM modulated signal which is used for broadcasting should be 30 kHz. 	



AM waveforms

Derivation for Amplitude modulated wave

A carrier is described by

$$v = V_c \sin(\omega_c t + \theta)$$

To **amplitude modulate** the carrier its amplitude is changed in accordance with the level of the audio signal, which is described by

$$v = V_m \sin(\omega_m t)$$

The amplitude of the carrier varies sinusoidally about a mean of V_c . When the carrier is modulated its amplitude is varied with the instantaneous value of the modulating signal. The amplitude of the variation

of the carrier amplitude is V_c and the angular frequency of the rate at which the amplitude varies is ω_m . The amplitude of the carrier is then:

$$\text{Carrier amplitude} = V_c + V_m \sin(\omega_m t)$$

and the instantaneous value (value at any instant in time) is

$$\begin{aligned} v &= \{V_c + V_m \sin(\omega_m t)\} * \sin(\omega_c t) \\ &= V_c \sin(\omega_c t) + V_m \sin(\omega_m t) * \sin(\omega_c t) \end{aligned} \quad \text{Eqn. 1}$$

Using $\sin A * \sin B = \frac{1}{2} \cos(A - B) - \frac{1}{2} \cos(A + B)$ this becomes

$$v = V_c \sin(\omega_c t) + \frac{1}{2} V_m \cos((\omega_c - \omega_m)t) - \frac{1}{2} V_m \cos((\omega_c + \omega_m)t) \quad \text{Eqn. 2}$$

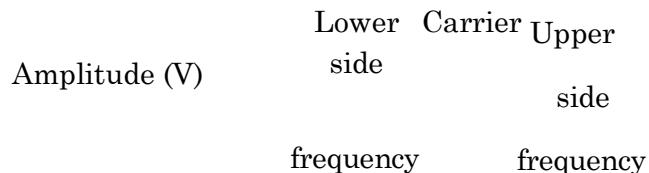
This is a signal made up of 3 signal components

- **carrier** at ω_c (rad/s) Frequency is $f_c = \omega_c / 2\pi$ Hz
- **upper side frequency** $\omega_c + \omega_m$ (rad/s) Frequency is $(\omega_c + \omega_m) / 2\pi = f_m + f_c$ Hz
- **lower side frequency** $\omega_c - \omega_m$ (rad/s) Frequency is $(\omega_c - \omega_m) / 2\pi = f_m - f_c$ Hz

The **bandwidth** (the difference between the highest and the

$$\text{lowest frequency}) \text{ is } \text{BW} = (\omega_c + \omega_m) - (\omega_c - \omega_m) = 2 * \omega_m$$

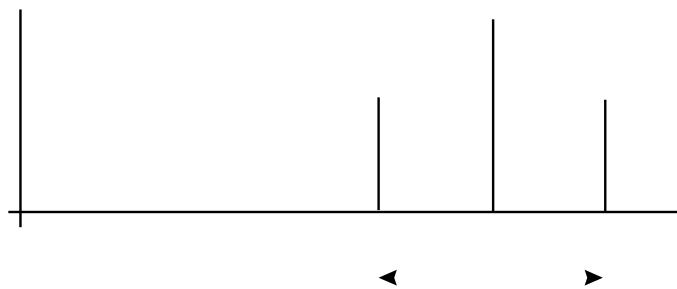
$$\text{Rad/s} \quad (= \omega_m / \pi \text{ Hz})$$

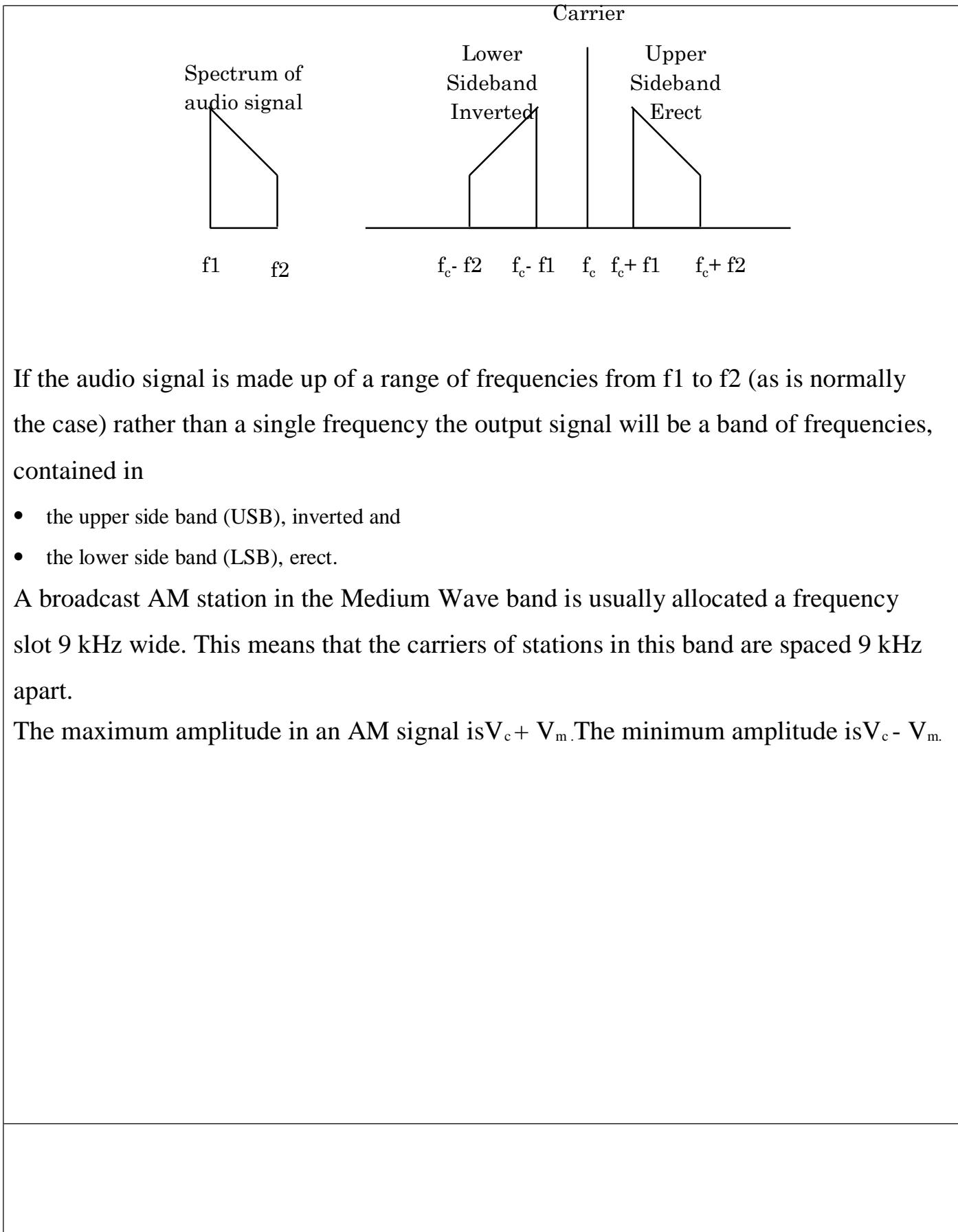


Angular		Angular
$\omega_c - \omega_m$	ω_c	$\omega_c + \omega_m$

$$\frac{\text{Frequency}}{\text{Bandwidth}} = 2 * \omega_m$$

The spectrum of these signals is shown. This is described as the signal in the **frequency domain**, as opposed to the signal in the **time domain**. In this case the audio signal is made up of a single frequency. In this example the **angular frequencies** (expressed in Radians/sec, or kRad/sec, or Mrad/sec) are shown. In most cases however the frequency is shown (expressed in Hz, or kHz, or MHz).





IMPORTANT POINTS TO REMEMBER:

- Amplitude modulation is first type of modulation used for transmitting messages for long distances by the mankind.

- Bandwidth of amplitude modulation should be twice the frequency of modulating signal or message signal.

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Define Amplitude modulation? Explain the principle of AM with suitable wave form. (**Jan2015, Feb 2010 ...10Marks**)

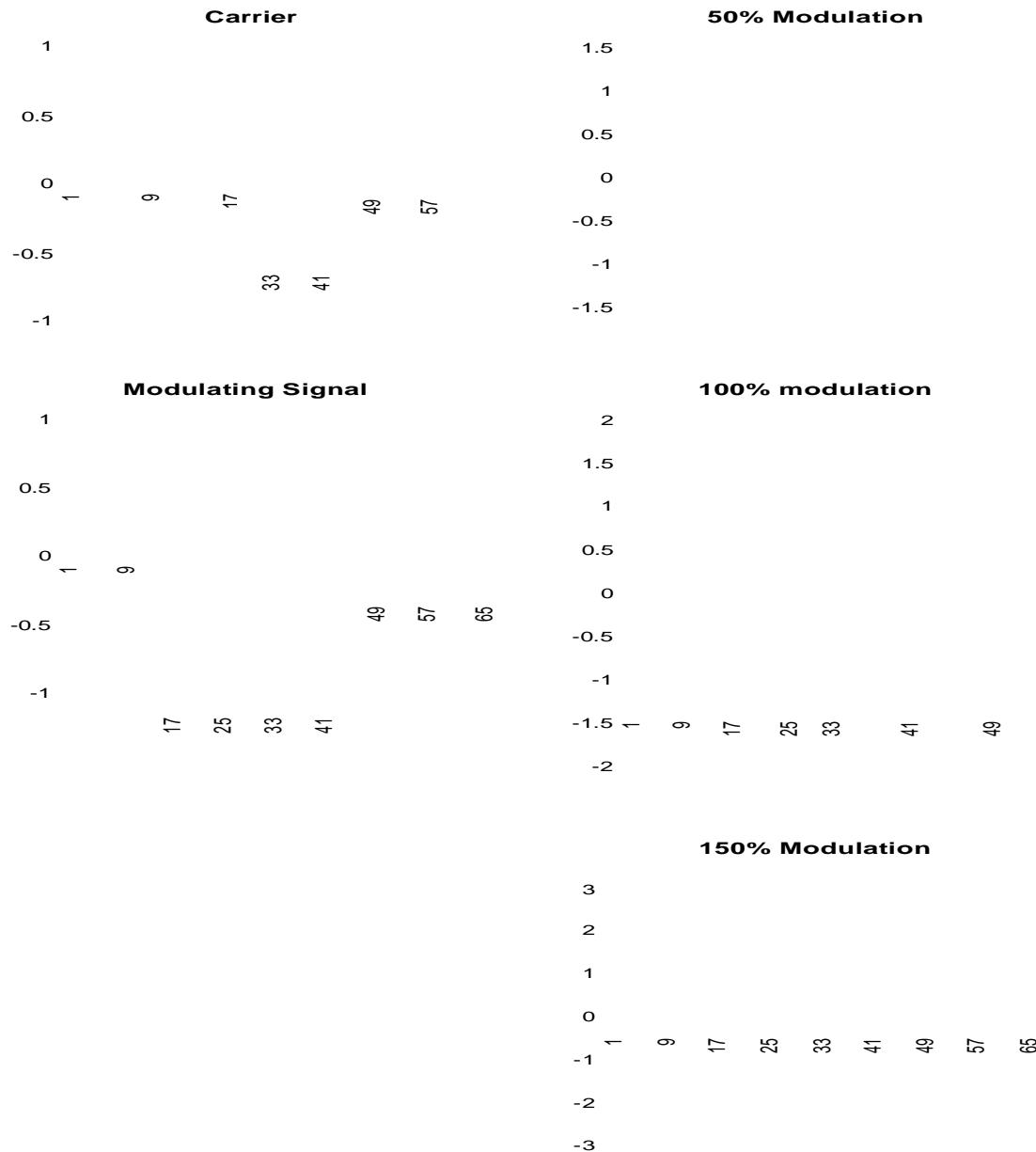
BLOOMS LEVEL-3 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Derive the expression for instantaneous output voltage in AM wave

REFERENCES:

6. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.35 to 37
7. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf
8. http://npteldownloads.iitm.ac.in/downloads_mp4/117102059/lec08.mp4

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES:
FACULTY NAME:	CO2
DATE:	
LECTURE HOUR: 44	
OBJECTIVES OF THE LECTURE:	
<p>To Derive the equation for Modulation Index</p> <p>To derive the equation for Power in AM wave.</p> <p>To study the limitations of Amplitude Modulation.</p>	
<p>Modulation Index (or Modulation Factor or Depth of Modulation)</p> <p>The ratio of change of amplitude of carrier wave to the amplitude of normal carrier wave is called modulation factor.</p> <p>$m = (\text{amplitude change of carrier wave}) / \text{normal carrier wave(unchanged)}$</p> <p>Modulation factor is very important since it determines the strength and quality of the transmitted signal. The greater the degree of modulation, the stronger and clearer will be the audio signal. It should be noted that if the carrier is over modulated (ie $m > 1$) distortion will occur at reception.</p>	
<p>This is defined as $m = \frac{V_m}{V_c}$</p> <p>In AM, this quantity, also called modulation depth, indicates by how much the modulated signal varies around its 'original' level. For AM, it relates to the variations in the carrier amplitude.</p> <p>So if $m = 0.5$, the carrier amplitude varies by 50% above and below its unmodulated level, and for $m = 1.0$ it varies by 100%. Modulation depth greater than 100% is generally to be avoided as it creates distortion.</p> <p>Using this Eqn. 2 can be re-written as</p> $v = V_c \sin(\omega_c t) + \frac{1}{2}(V_m \cos((\omega_c - \omega_m)t) - V_m \cos((\omega_c + \omega_m)t)) * V_c / V_c$ $v = V_c \{ \sin(\omega_c t) + \frac{1}{2} m [\cos((\omega_c - \omega_m)t) + \cos((\omega_c + \omega_m)t)] \} \quad \text{Eqn. 3}$	



The maximum allowed value of m is 1. If this is exceeded the envelope of the output waveform is distorted. This is known as **Over-modulation** and should never occur in practice, because the distorted envelope will result in a distorted output sound signal in the radio receiver. The effect of over-modulation can be examined in the laboratory.

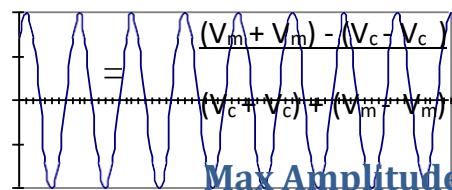
Alternative form for modulation index

If an AM signal is being displayed on an oscilloscope it can be difficult to read V_m and V_c . Instead the form for expressing m can be modified to make it easier to read.

$$\text{Modulation index : } m = \frac{V_m}{V_c} =$$

$$\frac{1}{2} (V_m + V_m) - \frac{1}{2} (V_c - V_c)$$

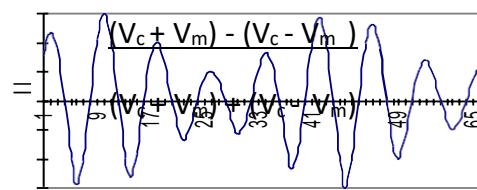
$$\frac{1}{2} (V_c + V_c) + \frac{1}{2} (V_m - V_m)$$



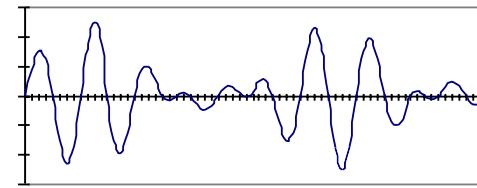
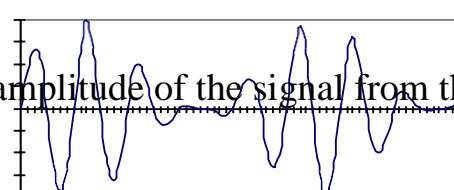
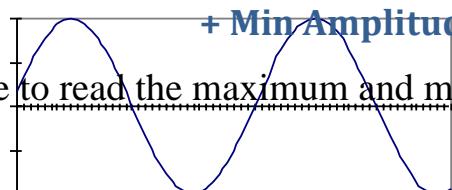
Max Amplitude - Min

Amplitude Max Amplitude

+ Min Amplitude



It is possible to read the maximum and minimum amplitude of the signal from the oscilloscope display.



Power in an AM waveform

Assume that the AM signal is dissipated in a load of $R \Omega$. The total power dissipated will be the sum of the powers in all of the components of the signal.

The power in the carrier will be

$$P_c = \frac{\overline{V_c^2}}{R} \text{ Watts}$$

The power in each of the frequencies is

$$P_s = \frac{\overline{(mV_c/2)^2}}{R} = \frac{\overline{m^2 V_c^2}}{R} = \frac{\overline{m^2}}{R} = 4 P_c$$

The total power is

$$P_t = P_c + P_s + P_s = P_c + 2 P_s = P_c \left(1 + \frac{m^2}{4}\right) = P_c \left(1 + \frac{m^2}{2}\right) \text{ Watts}$$

+

$$\text{The fraction of the power in the carrier is } \frac{P_c}{P_t} = \frac{1}{1 + \frac{m^2}{2}}$$

The maximum value for m is 1.0. This means that at most only 1/3 of the power in the signal will be contained in the sidebands. All of the audio information is contained in either one of the sidebands, so that, in effect, only one sixth of the power (16.7%) is used to carry information. The remainder of the signal can in some respects be considered to be redundant!

Peak Instantaneous Power

The maximum signal voltage is $V_c + V_m = V_c(1 + m)$ so that the maximum instantaneous output power is

$$\frac{\overline{V_c^2}}{R} (1 + m)^2 = P_c (1 + m)^2$$

If the modulation index is 1.0 the maximum output power will be $4 P_c$. The transmitter must be designed to carry this level of output power.

Limitations of Amplitude Modulation

1. Noisy Reception- In an AM wave, the signal is in the amplitude variations of the carrier. Practically all the natural and man-made noises consist of electrical amplitude disturbances. As a radio receiver cannot distinguish between amplitude variations that represent noise and those that contain the desired signal. Therefore reception is very noisy.

2. Low efficiency- In AM useful power is in the sidebands as they contain the signal. An AM wave has low sideband power.

For example even if modulation is 100 % ie $m=1$.

$$\frac{P_S}{P_T} = \frac{m^2}{2+m^2} = \frac{1}{2+1} = 0.33$$

$$P_S = 33\% \text{ of } P_T$$

Sideband power is only one-third of the total power of AM wave. Hence efficiency of this type of modulation is low.

3. Lack of audio quality- In order to attain high fidelity reception, all audio frequencies upto 15 KHz must be reproduced. This necessitates a bandwidth of 30 KHz since both sidebands must be reproduced (2fs). But AM broadcasting stations are assigned with bandwidth of only 10 KHz to minimize the interference from adjacent broadcasting stations. This means that the highest modulating frequency can be 5 KHz which is hardly sufficient to reproduce the music properly.

IMPORTANT POINTS TO REMEMBER:

- Modulation index(m)=(amplitude change of carrier wave) / normal carrier wave(unchanged).
- The maximum allowed value of m is 1.
- In FM signals, the efficiency and bandwidth both depend on both the maximum modulating frequency and the modulation index.
- Compared to AM, the FM signal has a higher efficiency, a larger bandwidth and better immunity to noise.

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Define modulation index in terms of V_{max} and V_{min} .

BLOOMS LEVEL-2 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Derive the expression for modulation index in AM wave?
2. Explain the power relations in AM wave?

BLOOMS LEVEL-3 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. What is over modulation? Sketch AM wave when modulation index $m>1$ and modulation index $m=1$?

BLOOMS LEVEL-4 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

2. A carrier of 1MHz with 400W of its power is amplitude modulated with a sinusoidal signal of 2500Hz. The depth of modulation is 75%. Calculate the sideband frequencies, the bandwidth the power in the sidebands and the total power in the modulated wave?
3. The total power content of an AM wave is 2.64KW at a modulation factor of 80%.Determine the power content of i) carrier ii) each sideband.

REFERENCES:

9. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.39 to 40
10. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES: CO2
FACULTY NAME:	
DATE:	
LECTURE HOUR: 45	

OBJECTIVES OF THE LECTURE:

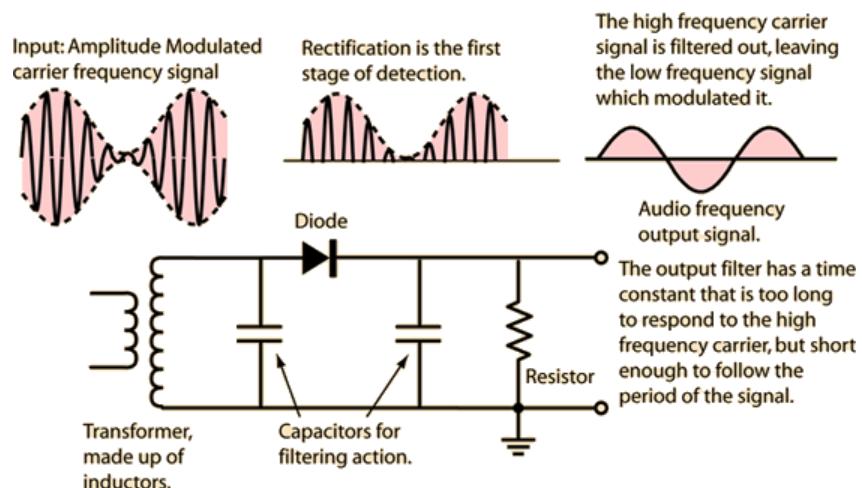
To study and understand the detailed comparison between Amplitude Modulation and Frequency Modulation.

To Solve the numerical problems on Amplitude Modulation.

AM Demodulation

The process of recovering the audio signal from the modulated wave is known as demodulation or detection.

At the broadcasting station, modulation is done to transmit the audio signal over larger distances. When the modulated wave is picked up the receiver, it is necessary to recover the audio signal from it. This process is accomplished in the radio receiver and is called demodulation.



When demodulating a signal, two basic steps may be considered:

- **Create baseband signal:** The main element of AM demodulation is to create the baseband signal.

This can be achieved in a number of ways - one of the easiest is to use a simple diode and rectify the signal. This leaves elements of the original RF signal. When other forms of demodulation are used, they too leave some elements of an RF signal.

- **Filter:** The filtering removes any unwanted high frequency elements from the demodulation process. The audio can then be presented to further stages for audio amplification, etc.

The modulated AM carrier wave is received by the antenna of the radio receiver and is rectified by the action of a detector diode. Then the rectified signal passes through a **low-pass filter** for which the time constant is too long to respond to the high frequency of the AM carrier wave. AM carriers are in the range 600 to 1400 kHz. The signal frequency which modulates it is much lower, 0.02 to 5 kHz, and it can pass through the filter.

The AM detector shown here would be suitable for picking up only one AM radio station for which the values of the **capacitors** and **inductors** were chosen. A practical AM radio uses the process called **heterodyning** to shift the carrier frequency of each radio station to a single frequency called an Intermediate Frequency or IF so that a single sophisticated AM detection circuit can be used to receive all AM radio stations.

Diode detector advantages & disadvantages

The diode detector is widely used, but it has several advantages and disadvantages:

Diode detector advantages

- **Simplicity:** The diode detector is very simple and is easy to construct. The circuit is very straightforward, consisting of a very few components.
- **Low cost:** Requiring so few components, and the fact that the components are not specialised, this form of detector is very cheap. Accordingly it is widely used in AM domestic radios.

Diode detector disadvantages

- **Distortion:** Although the diode detector is able to operate in a reasonably linear fashion over a reasonable range, outside this range high levels of distortion are introduced, and even within the more linear range, distortion levels are not particularly low. It is adequate for small low cost radios.
- **Selective fading:** These detectors are susceptible to the effects of selective fading experienced on short wave broadcast transmissions. Here the ionospheric propagation may be such that certain

small bands of the signal are removed. Under normal circumstances signals received via the ionosphere reach the receiver via a number of different paths. The overall signal is a combination of the signals received via each path and as a result they will combine with each other, sometimes constructively to increase the overall signal level and sometimes destructively to reduce it. It is found that when the path lengths are considerably different this combination process can mean that small portions of the signal are reduced in strength. An AM signal consists of a carrier with two sidebands

- ***Ininsensitive:*** Semiconductor diodes have a certain turn-on voltage. Accordingly the voltage has to reach a certain level before the diode is able to operate reasonably efficiently.

IMPORTANT POINTS TO REMEMBER:

- The process of recovering the audio signal from the modulated wave is known as demodulation or detection.

BLOOMS LEVEL-2 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

- Explain AM Demodulation/ AM Detector.

REFERENCES:

1. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

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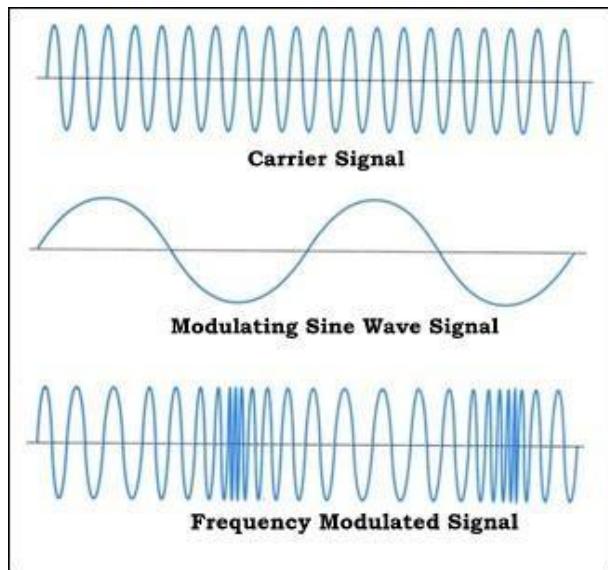
OBJECTIVES OF THE LECTURE:

To study and understand the Principle of Frequency Modulation.

To study the Comparison between AM and FM.

Frequency Modulation

The process of carrier signal frequency is varied according to the message signal or modulation signal frequency by keeping the amplitude constant is called frequency modulation.



that is the ‘frequency’ of a waveform? For a simple wave like a sinewave the answer appears quite obvious, we can define the wave using an expression like

$$S\{t\} = A \cos\{2\pi f t + \phi\}$$

and then identify f as the wave's frequency. An alternative way to represent such a wave would be write

$$S\{t\} = A \cos\{\Theta\{t\}\}$$

where

$$\Theta\{t\} = 2\pi f t + \phi$$

is the wave's *Phase* at any each instant, t . For a simple sine wave f has a constant value and $\Theta\{t\}$

increases steadily with time at the rate

$$\frac{d\Theta\{t\}}{dt} = 2\pi f$$

We can define the FM wave, produced when we modulate a *carrier frequency*, f_c , with a *modulating signal*, $m\{t\}$, to be

$$S\{t\} = A \cos\{2\pi f_i\{t\} t + \phi\}$$

where

$$f_i\{t\} = f_c + k_f m\{t\}$$

is the *instantaneous frequency* of the wave at the instant, t . The term k_f is a constant whose value depends upon the modulating system. It determines "how many Hz of frequency change we get for each volt of modulating signal."

be rewritten as

$$\begin{aligned} S\{t\} &= AJ_0\{\beta\} \cos\{2\pi f_c t\} \\ &+ A \sum_{k=1}^{\infty} J_{2k}\{\beta\} [\sin\{2\pi(f_c + 2kf_m)t\} + \sin\{2\pi(f_c - 2kf_m)t\}] \\ &+ A \sum_{k=0}^{\infty} J_{(2k+1)}\{\beta\} [\cos\{2\pi(f_c + (2k+1)f_m)t\} - \cos\{2\pi(f_c - (2k+1)f_m)t\}] \end{aligned}$$

where $J_n\{\beta\}$ is the *Bessel Function* (first kind, integer order, n) for the value, β .

Advantages of Frequency Modulation:

- Frequency modulation has more noise resistivity when compared to other modulation techniques. That's why they are mainly used in broadcasting and radio communications.

- The frequency modulation is having greater resistance to rapid signal strength variation, which we will use in FM radios even while we are travelling and frequency modulation is also mainly used in mobile communication purposes.
- For transmitting messages in frequency modulation, it does not require special equipments like linear amplifiers or repeaters and transmission levels or higher when compared to other modulation techniques. It does not require any class C or B amplifiers for increasing the efficiency.
- Transmission rate is good for frequency modulation when compared to other modulation that is frequency modulation can transmit around 1200 to 2400 bits per second.
- Frequency modulation has a special effect called capture effect in which high frequency signal will capture the channel and discard the low frequency or weak signals from interference.

Disadvantages of Frequency Modulation:

- In the transmission section, we don't need any special equipment but in the reception, we need more complicated demodulators for demodulating the carrier signal from message or modulating signal.
- Frequency modulation cannot be used to find out the speed and velocity of a moving object. Static interferences are more when compared to phase modulation. Outside interference is one of the biggest disadvantages in the frequency modulation. There may be mixing because of nearby radio stations, pagers, construction walkie-talkies etc.
- To limit the bandwidth in the frequency modulation, we use some filter which will again introduce some distortions in the signal.
- Transmitters and receiver should be in same channel and one free channel must be there between the systems.
- Spectrum space is limit for the frequency modulation and careful controlling the deviation ration.

Applications of Frequency Modulation (FM):

- Frequency modulation is used in radio's which is very common in our daily life.
- Frequency modulation is used in audio frequencies to synthesize sound.
- For recording the video signals by VCR systems, frequency modulation is used for intermediate frequencies.

- Used in applications of magnetic tape storage.

Comparison between Amplitude Modulation and Frequency Modulation

Amplitude modulation and frequency modulation are both methods of modifying a carrier signal in order to transmit data. The **main difference** between amplitude modulation and frequency modulation is that, **in amplitude modulation, the *amplitude* of the carrier wave is modified according to the data** whereas, **in frequency modulation, the *frequency* of the carrier wave is modified according to the data.**

	AM	FM
Stands for	AM stands for Amplitude Modulation	FM stands for Frequency Modulation
Origin	AM method of audio transmission was first successfully carried out in the mid-1870s.	FM radio was developed in the United states in the 1930s, mainly by Edwin Armstrong.
Modulating differences	In AM, a radio wave known as the "carrier" or "carrier wave" is modulated in amplitude by the signal that is to be transmitted. The frequency and phase remain the same.	In FM, a radio wave known as the "carrier" or "carrier wave" is modulated in frequency by the signal that is to be transmitted. The amplitude and phase remain the same.
Pros and cons	AM has poorer sound quality compared with FM, but is cheaper and can be transmitted over long distances. It has a lower bandwidth so it can have more stations available in any frequency range.	FM is less prone to interference than AM. However, FM signals are impacted by physical barriers. FM has better sound quality due to higher bandwidth.
Frequency Range	AM radio ranges from 535 to 1705 KHz (OR) Up to 1200 bits per second.	FM radio ranges in a higher spectrum from 88 to 108 MHz. (OR) 1200 to 2400 bits per second.
Bandwidth Requirements	Twice the highest modulating frequency. In AM radio broadcasting, the modulating signal has bandwidth of 15kHz, and hence the bandwidth of an amplitude-modulated signal is 30kHz.	Twice the sum of the modulating signal frequency and the frequency deviation. If the frequency deviation is 75kHz and the modulating signal frequency is 15kHz, the bandwidth required is 180kHz.
Zero crossing in modulated signal	Equidistant	Not equidistant
Complexity	Transmitter and receiver are simple but synchronization is needed in case of SSBSC AM carrier.	Transmitter and receiver are more complex as variation of modulating signal has to be converted and detected from corresponding variation in

		frequencies.(i.e. voltage to frequency and frequency to voltage conversion has to be done).	
Noise	AM is more susceptible to noise because noise affects amplitude, which is where information is "stored" in an AM signal.	FM is less susceptible to noise because information in an FM signal is transmitted through varying the frequency, and not the amplitude.	

IMPORTANT POINTS TO REMEMBER:

- Compared to AM, the FM signal has a higher efficiency, a larger bandwidth and better immunity to noise.

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Explain the principle of Frequency Modulation and write the expression for instantaneous voltage of Modulated wave.
2. List out the Advantages, Disadvantages and Applications of Frequency Modulation.

BLOOMS LEVEL-2 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Give the comparison between Amplitude Modulation and Frequency Modulation

REFERENCES:

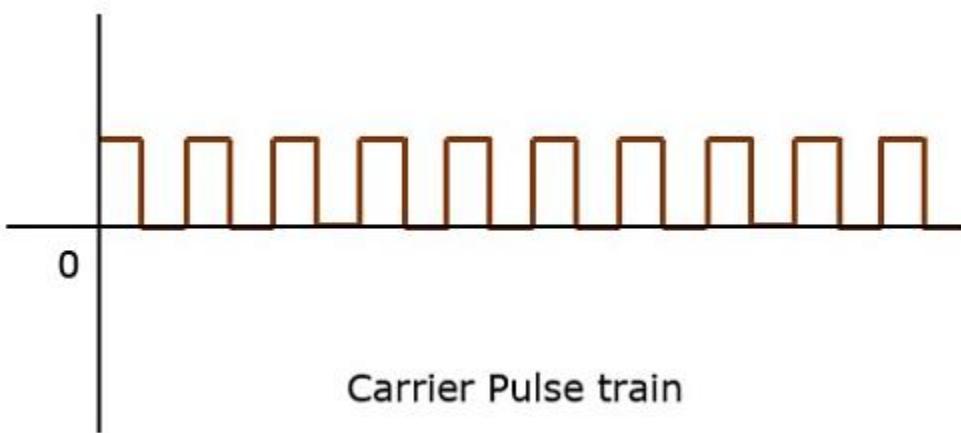
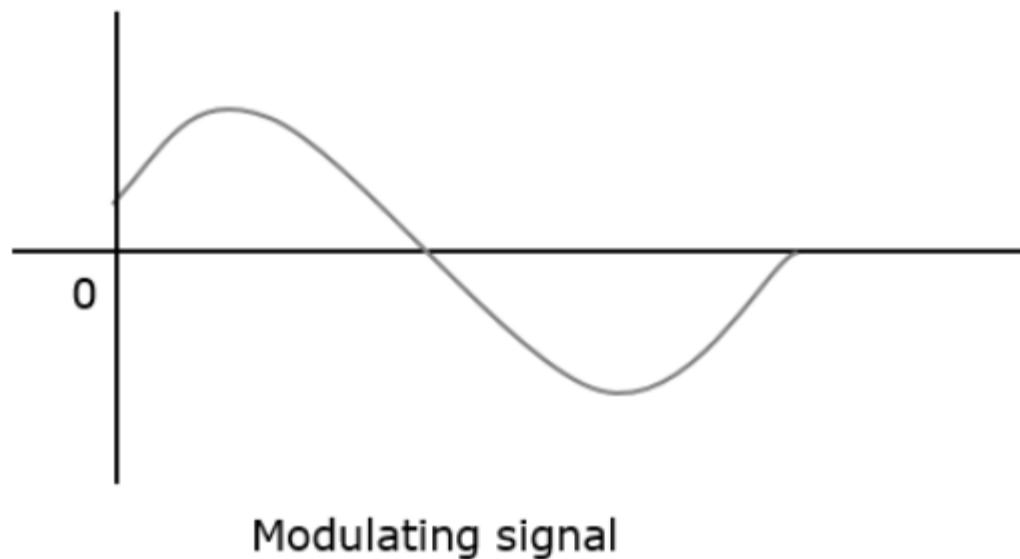
2. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.79 to 80.
3. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

Analog Pulse Modulation

Pulse modulation is further divided into analog and digital modulation. The analog modulation techniques are mainly classified into Pulse Amplitude Modulation, Pulse Duration Modulation/Pulse Width Modulation, and Pulse Position Modulation.

Pulse Amplitude Modulation

Pulse Amplitude Modulation (PAM) is an analog modulating scheme in which the amplitude of the pulse carrier varies proportional to the instantaneous amplitude of the message signal.



Pulse Width Modulation

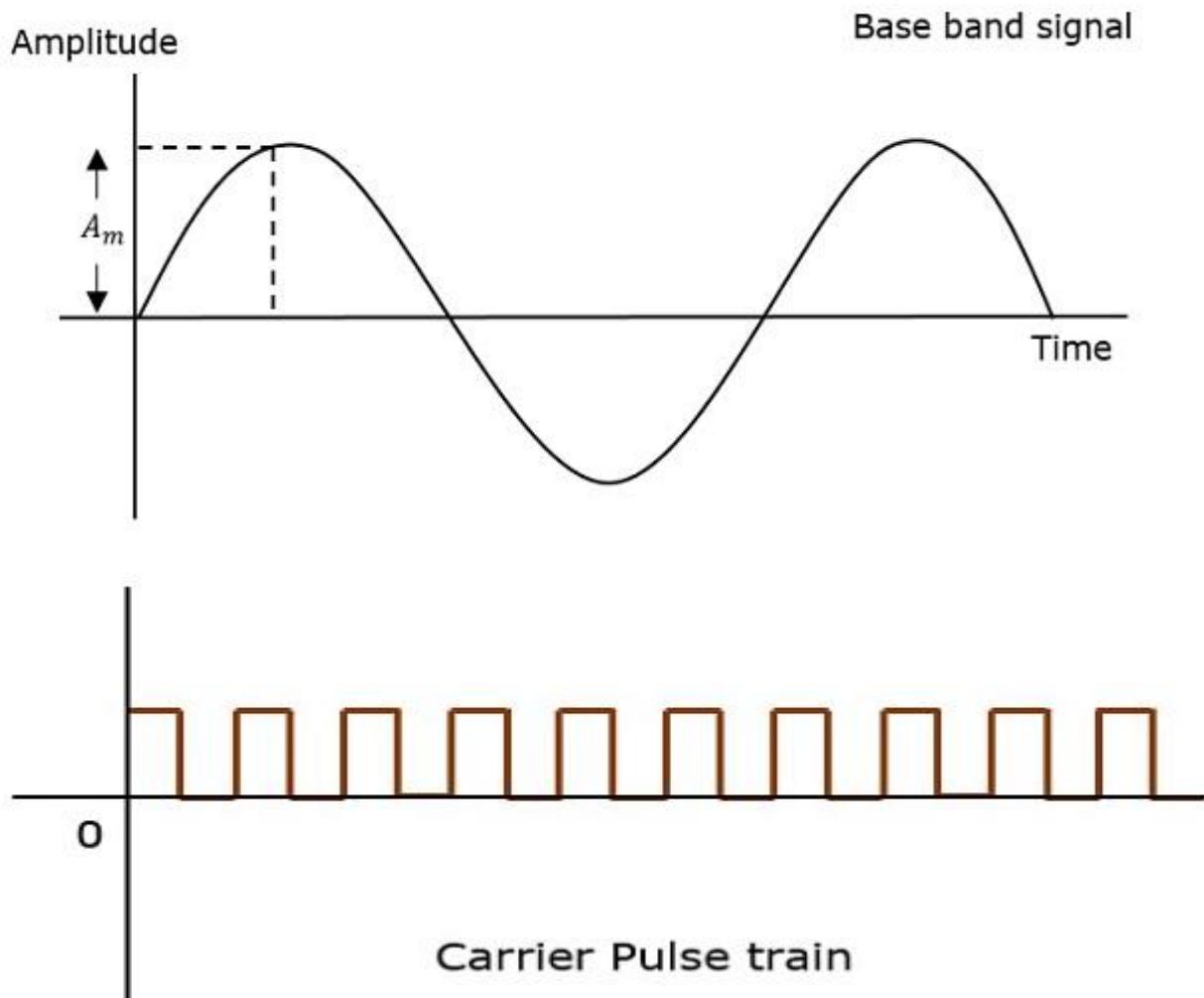
Pulse Width Modulation (PWM) or Pulse Duration Modulation (PDM) or Pulse Time Modulation (PTM) is an analog modulating scheme in which the duration or width or time of the pulse carrier varies proportional to the instantaneous amplitude of the message signal.

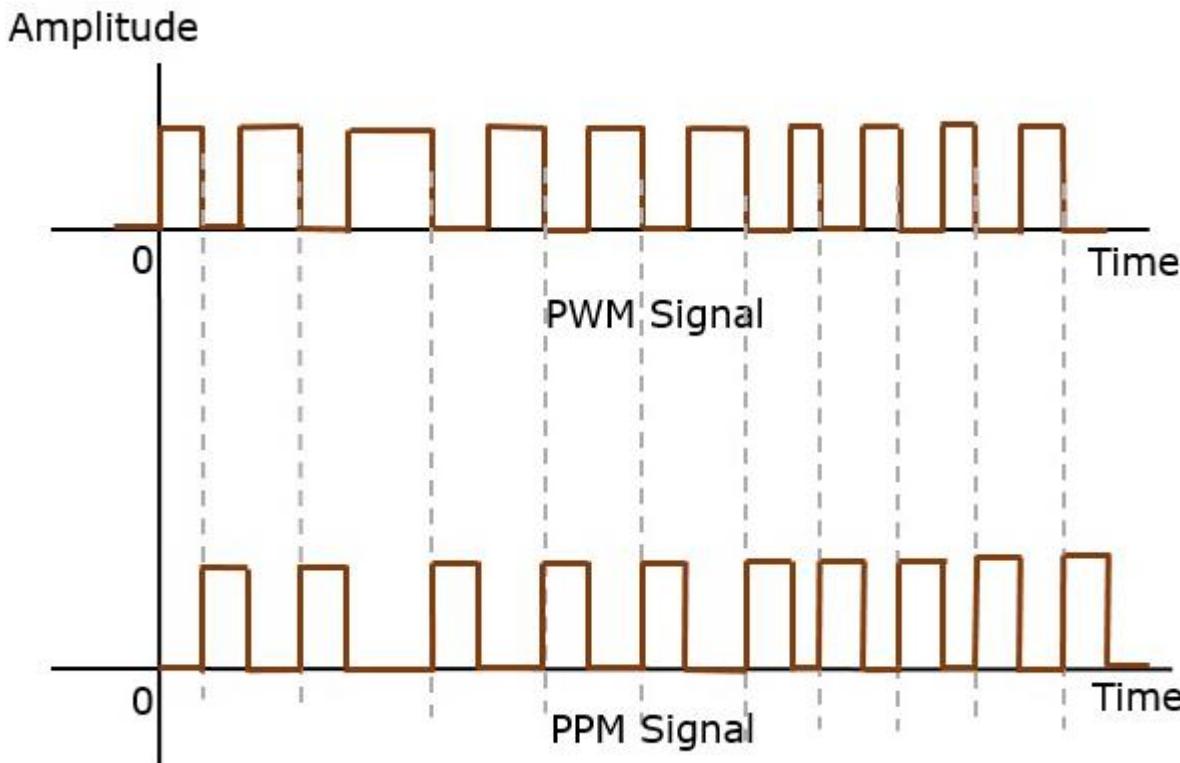
The width of the pulse varies in this method, but the amplitude of the signal remains constant.

Pulse Position Modulation

Pulse Position Modulation (PPM) is an analog modulating scheme in which the amplitude and width of the pulses are kept constant, while the position of each pulse, with reference to the position of a reference pulse varies according to the instantaneous sampled value of the message signal.

The transmitter has to send synchronizing pulses (or simply sync pulses) to keep the transmitter and receiver in synchronism. These sync pulses help maintain the position of the pulses. The following figures explain the Pulse Position Modulation.





Pulse position modulation is done in accordance with the pulse width modulated signal. Each trailing of the pulse width modulated signal becomes the starting point for pulses in PPM signal. Hence, the position of these pulses is proportional to the width of the PWM pulses.

Advantage

As the amplitude and width are constant, the power handled is also constant.

Disadvantage

The synchronization between transmitter and receiver is a must.

Comparison between PAM, PWM, and PPM

The comparison between the above modulation processes is presented in a single table.

PAM	PWM	PPM
Amplitude is varied	Width is varied	Position is varied
Bandwidth depends on the width of the pulse	Bandwidth depends on the rise time of the pulse	Bandwidth depends on the rise time of the pulse
Instantaneous transmitter power varies with the amplitude of the pulses	Instantaneous transmitter power varies with the amplitude and width of the pulses	Instantaneous transmitter power remains constant with the width of the pulses

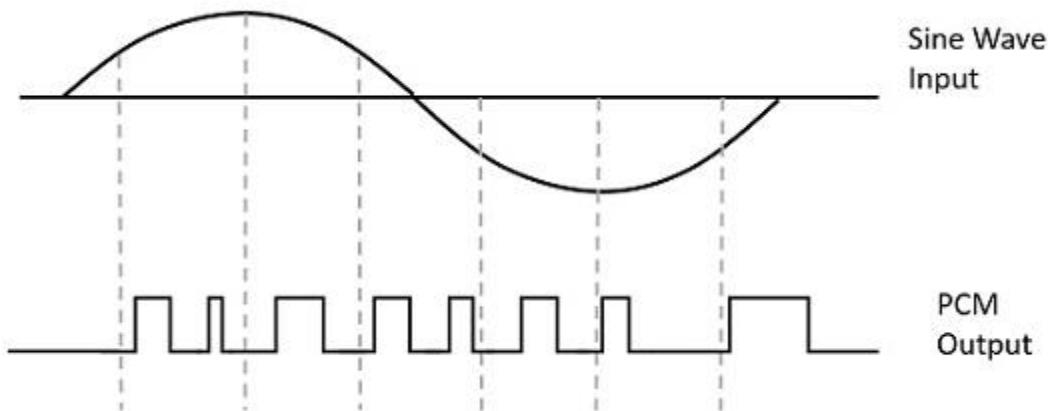
System complexity is high	System complexity is low	System complexity is low
Noise interference is high	Noise interference is low	Noise interference is low
It is similar to amplitude modulation	It is similar to frequency modulation	It is similar to phase modulation

Digital Modulation

Digital modulation has Pulse Code Modulation (PCM) and delta modulation(DM).

Pulse Code Modulation

A signal is Pulse Code modulated to convert its analog information into a binary sequence, i.e., 1s and 0s. The output of a **Pulse Code Modulation (PCM)** will resemble a binary sequence. The following figure shows an example of PCM output with respect to instantaneous values of a given sine wave.



Instead of a pulse train, PCM produces a series of numbers or digits, and hence this process is called as digital. Each one of these digits, though in binary code, represent the approximate amplitude of the signal sample at that instant.

In Pulse Code Modulation, the message signal is represented by a sequence of coded pulses. This message signal is achieved by representing the signal in discrete form in both time and amplitude.

Delta Modulation

In PCM the signaling rate and transmission channel bandwidth are quite large since it transmits all the bits which are used to code a sample. To overcome this problem, Delta modulation is used.

Working Principle

Delta modulation transmits only one bit per sample. Here, the present sample value is compared with the previous sample value and this result whether the amplitude is increased or decreased is transmitted.

Input signal $x(t)$ is approximated to step signal by the delta modulator. This step size is kept fixed.

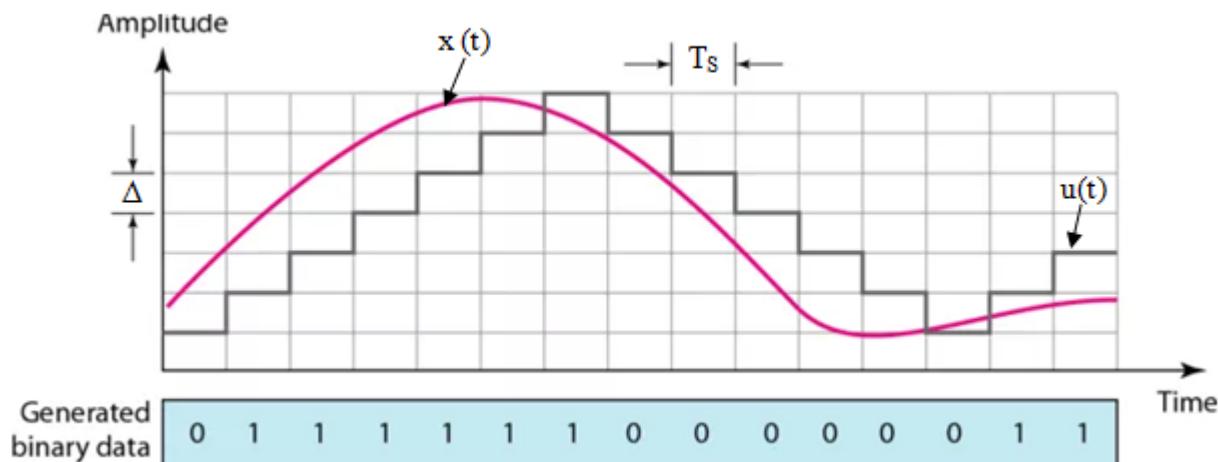
The difference between the input signal $x(t)$ and staircase approximated signal is confined to two levels, i.e., $+\Delta$ and $-\Delta$.

Now, if the difference is positive, then approximated signal is increased by one step, i.e., ' Δ '. If the difference is negative, then approximated signal is reduced by ' Δ '.

When the step is reduced, '0' is transmitted and if the step is increased, '1' is transmitted.

Hence, for each sample, only one binary bit is transmitted.

Fig shows the analog signal $x(t)$ and its staircase approximated signal by the delta modulator.



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OBJECTIVES OF THE LECTURE:

To study and understand the basic principle of Superhetrodyne Receiverwith block diagram representation.

To solve numerical problems on Frequency Modulation.

Superhetrodyne Receiver

A **superheterodyne receiver**uses frequency mixing to convert a received signal to a fixed intermediate frequency (IF) which can be more conveniently processed than the original carrier frequency.

Here the selected radio frequency is converted to a fixed lower value called intermediate frequency (IF). This is achieved by special electronic circuit called mixer circuit. The production of fixed intermediate frequency (455 KHz) is an important feature of super-heterodyne circuit. At this fixed intermediate frequency, the amplifier circuit operates with maximum stability, selectivity and sensitivity.

The block diagram of super-heterodyne receiver is a shown in fig below.

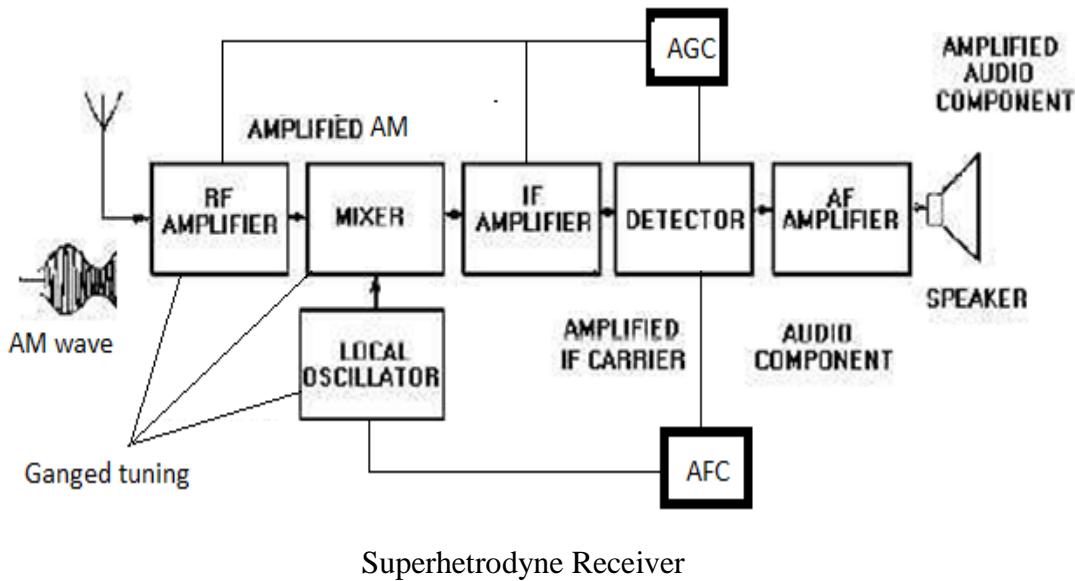
1. RF amplifier stage- The RF amplifier stage uses a tuned parallel circuit L1C1 with a variable capacitor C1. The radio waves from various broadcasting stations are intercepted by the receiving aerial and are coupled to this stage. This stage selects the desired radio wave and raises the strength of the wave to the desired level.

2. Mixer stage- The amplified output of RF amplifier is fed to the mixer stage where it is combined with the output of a local oscillator. The two frequencies beat together and produce an intermediate frequency (IF).

IF= Oscillator frequency –radio frequency

The IF is always 455 KHz regardless of the frequency to which the receiver is tuned. The reason why the mixer will always produce 455KHz frequency above the radio frequency is that oscillator always produces a frequency 455KHz above the selected frequency. In practice, capacitance of C3 is designed to tune the oscillator to a frequency higher than radio frequency by 455KHz.

Receiving antenna



- 3. IF amplifier stage-** The output of mixer is always 455KHz and is fed to fixed tuned IF amplifiers. These amplifiers are tuned to one frequency (ie 455KHz).
- 4. Detector stage-** The output from the last IF amplifier stage is coupled to the input of the detector stage. Here the audio signal is extracted from the IF output. Usually diode detector circuit is used because of its low distortion and excellent audio fidelity.
- 5. AF amplifier stage-** The audio signal output of detector stage is fed to a multistage audio amplifier. Here the signal is amplified until it is sufficiently strong to drive the speaker. The speaker converts the audio signal into sound waves corresponding to the original sound at the broadcasting station.
- 6. Automatic Frequency Control (AFC),** also called **Automatic Fine Tuning (AFT)**, is a method or circuit to automatically keep a resonant circuit tuned to the frequency of an incoming radio signal.
- 7. Automatic gain control (AGC),** also called **automatic volume control(AVC)**, is a closed-loop feedback regulating circuit in an amplifier or chain of amplifiers, the purpose of which is to maintain a suitable signal amplitude at its output, despite variation of the signal amplitude at the input. In a typical receiver the AGC feedback control signal is usually taken from the detector stage and applied to control the gain of the IF or RF amplifier stages.
- 8. GANGED TUNING :**The dotted lines connecting the local oscillator, rf amplifier, and the mixer indicate GANGED TUNING. Ganged tuning is the process used to tune two or more circuits with a single control. When we change the frequency of the receiver, all three stages change by the same amount. There is a fixed difference in frequency between the local oscillator and the rf amplifier at all times. This

difference in **frequency** is the IF. This fixed difference and ganged tuning ensures a constant IF over the frequency range of the receiver.

9. Advantages of Superhetrodyne Circuit –

- 1. High RF amplification**
- 2. Improved selectivity-losses in the tuned circuits are lower at intermediate frequency. Therefore the quality factor Q of the tuned circuits is increased. This makes amplifier circuits to operate with maximum selectivity.**
- 3. Lower cost.**

IMPORTANT POINTS TO REMEMBER:

- A **superheterodyne receiver** uses frequency mixing to convert a received signal to a fixed

intermediate frequency (IF)

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

1. Explain the superheterodyne receiver with neat diagram.

REFERENCES:

4. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.120 to 122.
5. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

COURSE NAME WITH CODE: BASIC ELECTRONICS - ELN15/25	COURSE OUTCOMES: CO2
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OBJECTIVES OF THE LECTURE:

To study and understand the basic principle of optical fiber communication system with block diagram.

To study and understand benefits of optical fiber communication system.

Block diagram and Principle of Optical Fiber Communication:

Since its invention in the early 1970s, the use of and demand for optical fiber have grown tremendously. The uses of optical fiber today are quite numerous. With the explosion of information traffic due to the Internet, electronic commerce, computer networks, multimedia, voice, data, and video, the need for a transmission medium with the bandwidth capabilities for handling such vast amounts of information is paramount. Fiber optics, with its comparatively infinite bandwidth, has proven to be the solution. Companies such as AT&T, MCI, and U.S.

Sprint use optical fiber cable to carry plain old telephone service (POTS) across their nationwide networks. Local telephone service providers use fiber to carry this same service between central office switches at more local levels, and sometimes as far as the neighbourhood or individual home.

Optical fiber is also used extensively for transmission of data signals. Large corporations, banks, universities, Wall Street firms, and others own private networks. These firms need secure, reliable systems to transfer computer and monetary information between buildings, to the desktop terminal or computer, and around the world. The security inherent in optical fiber systems is a major benefit. Cable television or community antenna television (CATV) companies also find fiber useful for video services. The high information-carrying capacity, or bandwidth, of fiber makes it the perfect choice for transmitting signals to subscribers. The fibering of America began in the early 1980s. At that time, systems operated at 90 Mb/s. At this data rate, a single optical fiber could handle approximately 1300 simultaneous voice channels. Today, systems commonly operate at 10 GB/s and beyond. This translates to over 130,000 simultaneous voice channels. Over the past five years, new technologies such as dense wavelength-division multiplexing (DWDM) and erbium-doped fiber amplifiers (EDFA) have been used successfully to further increase data rates to beyond a terabit per second (>1000 Gb/s) over distances in excess of 100

km. This is equivalent to transmitting 13 million simultaneous phone calls through a single hair-size glass fiber. At this speed, one can transmit 100,000 books coast to coast in 1 second!

The growth of the fiber optics industry over the past five years has been explosive. Analysts expect that this industry will continue to grow at a tremendous rate well into the next decade and beyond. Anyone with a vested interest in telecommunication would be all the wiser to learn more about the tremendous advantages of fiber optic communication. With this in mind, we hope this module will provide the student with a rudimentary understanding of fiber optic communication systems, technology, and applications in today's information world.

BENEFITS OF FIBER OPTICS

Optical fiber systems have many advantages over metallic-based communication systems. These advantages include:

- Long-distance signal transmission the low attenuation and superior signal integrity found in optical systems allow much longer intervals of signal transmission than metallic-based systems. While single-line, voice-grade copper systems longer than a couple of kilometres (1.2 miles) require in-line signal for satisfactory performance, it is not unusual for optical systems to go over 100 kilometres (km), or about 62 miles, with no active or passive processing.
- Large bandwidth, light weight, and small diameter Today's applications require an ever-increasing amount of bandwidth. Consequently, it is important to consider the space constraints of many end users. It is commonplace to install new cabling within existing duct systems or conduit. The relatively small diameter and light weight of optical cable make such installations easy and practical, saving valuable conduit space in these environments.
- Non-conductivity Another advantage of optical fibers is their dielectric nature. Since optical fiber has no metallic components, it can be installed in areas with electromagnetic interference (EMI), including radio frequency interference (RFI). Areas with high EMI include utility lines, power-carrying lines, and railroad tracks. All-dielectric cables are also ideal for areas of high lightning-strike incidence.
- Security Unlike metallic-based systems, the dielectric nature of optical fiber makes it impossible to remotely detect the signal being transmitted within the cable. The only way to do so is by accessing the optical fiber. Accessing the fiber requires intervention that is easily detectable by security surveillance. These circumstances make fiber extremely attractive to governmental bodies, banks, and others with major security concerns.

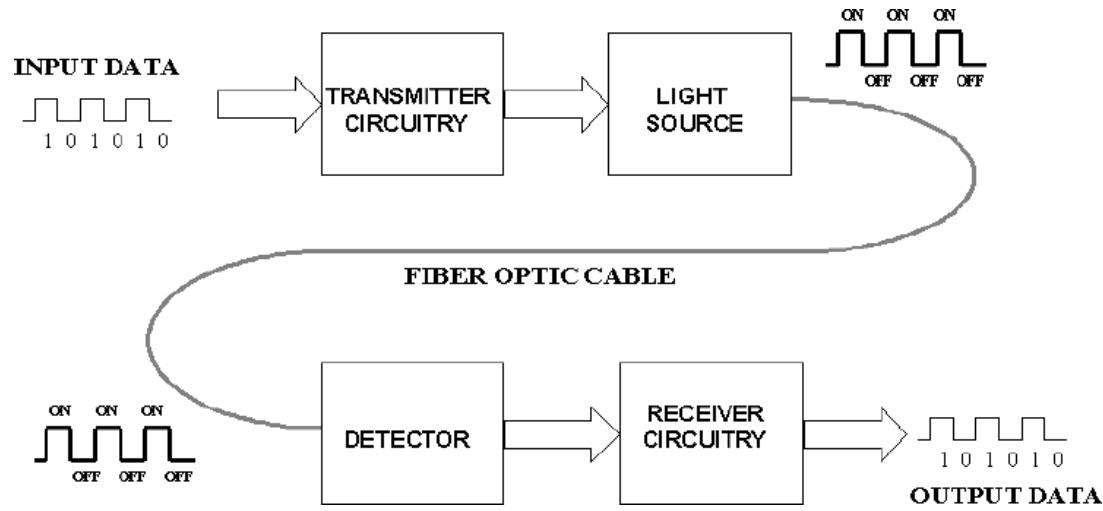
- Designed for future applications needs Fiber optics is affordable today, as electronics prices fall and optical cable pricing remains low. In many cases, fiber solutions are less costly than copper. As bandwidth demands increase rapidly with technological advances, fiber will continue to play a vital role in the long-term success of telecommunication.

BASIC FIBER OPTIC COMMUNICATION SYSTEM

Fiber optics is a medium for carrying information from one point to another in the form of light. Unlike the copper form of transmission, fiber optics is not electrical in nature. A basic fiber optic system consists of a transmitting device that converts an electrical signal into a light signal, an optical fiber cable that carries the light, and a receiver that accepts the light signal and converts it back into an electrical signal. The complexity of a fiber optic system can range from very simple (i.e., local area network) to extremely sophisticated and expensive (i.e., long-distance telephone or cable television trunking). For example, the system shown in Figure 8-1 could be built very

Inexpensively using a visible LED, plastic fiber, a silicon photo detector, and some simple electronic circuitry. The overall cost could be less than \$20. On the other hand, a typical system

used for long-distance, high-bandwidth telecommunication that employs wavelength-division multiplexing, erbium-doped fiber amplifiers, external modulation using DFB lasers with temperature compensation, fiber Bragg gratings, and high-speed infrared photo detectors could cost tens or even hundreds of thousands of dollars. The basic question is “how much information is to be sent and how far does it have to go?” With this in mind we will examine the various components that make up a fiber optic communication system and the considerations that must be taken into account in the design of such systems.

**Fig.Basic fiber optic communication system**

Very simple (i.e., local area network) to extremely sophisticated and expensive (i.e., long-distance telephone or cable television trunking). For example, the system shown in Figure could be built very inexpensively using a visible LED, plastic fiber, a silicon photo detector, and some simple electronic circuitry. On the other hand, a typical system used for long-distance, high-bandwidth telecommunication that employs wavelength-division multiplexing, erbium-doped fiber amplifiers, external modulation using DFB lasers with temperature compensation, fiber Bragg gratings, and high-speed infrared photo detectors could cost tens or even hundreds of thousands of dollars. The basic question is "how much information is to be sent and how far does it have to go?" With this in mind we will examine the various components that make up a fiber Optic communication system and the considerations that must be taken into account in the design of such systems.

IMPORTANT POINTS TO REMEMBER:

- Fiber optics is a medium for carrying information from one point to another in the form of light.

BLOOMS LEVEL-1 ASSIGNMENT QUESTIONS: (VTU/GATE/IES QUESTIONS)

2. Explain the optical fiber communication system with neat diagram.

REFERENCES:

6. George Kennedy, Electronic Communication Systems, TMH, 4th Edition. Page No.120 to 122.
7. http://fpa.hanyang.ac.kr/Lecture/elec/Elec_Chapter19.pdf

Module-5

GSM mobile phone

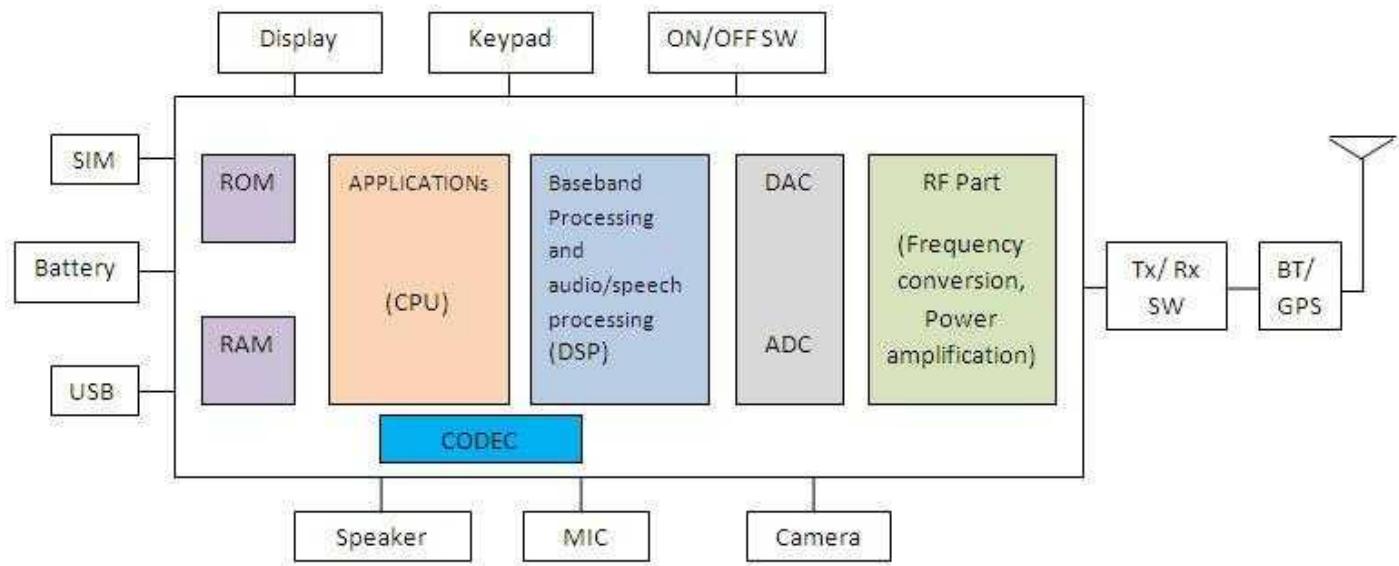


Fig.1 GSM mobile phone block diagram

RF Part

RF part consists of RF frequency up converter and rf frequency down converter. Up converter converts modulated baseband signal either at zero IF(Intermediate frequency) or some IF to RF frequency(890-915 MHz). RF down converter converts RF signal (935 to 960 MHz) to baseband signal.

Baseband Part

This part basically converts voice/data to be carried over GSM air interface to baseband signal. It is ported usually on DSP(Digital Signal Processor) to meet latency and power requirements of mobile phone. For Speech/audio, codec is used to compress and decompress the signal to match the data rate to the frame it has to fit in. CODEC converts speech at 8 KHz sampling rate to 13 kbps rate for full rate speech traffic channel.

ADC and DAC

ADC(Analog to Digital Converter) and DAC(Digital to Analog Converter) is used to convert analog speech signal to digital signal and vice versa in the mobile handset. At Transmit path,

ADC converted digital signal is given to speech coder. AGC(Automatic Gain Control) and AFC(Automatic Frequency Control) is used in the receiver path to control gain and frequency.

Application layer

It also runs on CPU. various applications run in GSM mobile phone. It include audio,video and image/graphics applications. It supports various audio formats such as MP3,MP4,WAV,rm. JPEG image formats are usually available.

Operating system

various operating systems are supported in mobile phone such as Symbian,java,android,RT-Linux,Palm. It runs on CPU of different manufacturers. For time critical applications RTOS (real-time operating system) is used.

Battery

It is the only major source of power to make/to keep mobile phone functional. There are various types of batteries made of Nickel Cadmium(NiCd),Nickel Metal Hydride(NiMH), based on lithium,Li-ion and so on. The major factors for designers is to reduce battery size, last for more talk time,increase battery life. Battery comes usually with 3.6 or 3.7 voltage and 600mAh or 960 mAh ratings. Battery Charger is usually provided with mobile phone to charge the mobile phone battery. Battery charger is AC to DC converter.

Connectivity (WLAN, Bluetooth, USB, GPS)

To make data transfer fast enough between mobile phone and other computing devices(laptop,desktop,tablet) or between mobile and mobile various technologies are evolved which include WLAN,Bluetooth,USB. GPS(global positioning system) is used for location assistance and will enable google map to work efficiently.

Microphone

Microphone or mic converts air pressure variations(result of our speech) to electrical signal to couple on the PCB for further processing.

Speaker

It converts electrical signal to audible signal(pressure vibrations) for human being to hear. This is often coupled with audio amplifier to get required amplification of audio signal.

Camera

It is the major specifications in increasing cost of mobile phone. There are various mega pixel camera for mobile phones are available such as 12 mega pixel, 14 mega pixel and even 41 mega pixel available in smartphones. This has become evident because of advancement in sensor technology. If one wants to buy low cost mobile phone, they usually go for non camera mobile phone.

Display

There are various display devices used in mobile phone such as LCD(liquid crystal display), TFT(Thin-film transistor) screen,OLED(organic light emitting diode),TFD(thin film diode), touch screen of capacitive and resistive type etc.

Keypad

Earlier days keypad was simple matrix type keypad which contains numeric digits(0 to 9), alphabets(a to z),special characters and specific function keys. These has been designed for various applications such as accepting call,rejecting call,cursor movement(left,right,top,down) dialling number, typing name/sms/mms and so on.

Generation of Cellular & Wireless Technologies

<i>Generation (1G,2G,3G,4G,5 G)</i>	<i>Technolo gy</i>	<i>Data Bandwidt h</i>	<i>Standard</i>	<i>Time period</i>	<i>Features</i>
1G	Analog	2 Kbps	AMPS,NMT,TACS	1970 – 1980	During 1G Wireless phones are used for <i>voice only</i> .
2G	Digital Narrow band circuit data	14.4 Kbps	TDMA,CDMA	1990 to 2000	2G capabilities are achieved by allowing <i>multiple users on a single channel via multiplexing</i> . During 2G Cellular phones are used for <i>data also along with voice</i> .
2.5G	Packet Data	16 Kbps	GPRS	2001- 2004	In 2.5G the <i>internet</i> becomes popular and data becomes more relevant.2.5G <i>Multimedia services</i> and streaming starts to show growth. <i>Phones</i>

					<i>start supporting web browsing</i> though limited and very few phones have that.
3G	Digital Broadband Packet Data	2 Mbps	CDMA 2000 UMTS, EDGE	2004-2005	3G has Multimedia services support along with streaming are more popular. In 3G, Universal access and portability across different device types are made possible. (Telephones, PDA's, etc.)
4G	Digital Broadband Packet All IP Very high throughput	200 Mbps	WiMax LTE Wi-Fi	Now	Speeds for 4G are further increased to keep up with data access demand used by various services. High definition streaming is now supported in 4G. New phones with HD capabilities surface. It gets pretty cool. In 4G, Portability is increased further. World-wide roaming is not a distant dream.
5G	Not Yet	Probably gigabits	Not Yet	Soon (probably 2020)	Currently there is no 5G technology deployed. When this becomes available it will provide very high speeds to the consumers. It would also provide efficient use of available bandwidth as has been seen through development of each new technology.

GSM Network Architecture

The GSM network architecture consists of four main parts:

- Mobile station (MS)
- Base-Station Subsystem (BSS)
- Network and Switching Subsystem (NSS)
- Operation and Support Subsystem (OSS)

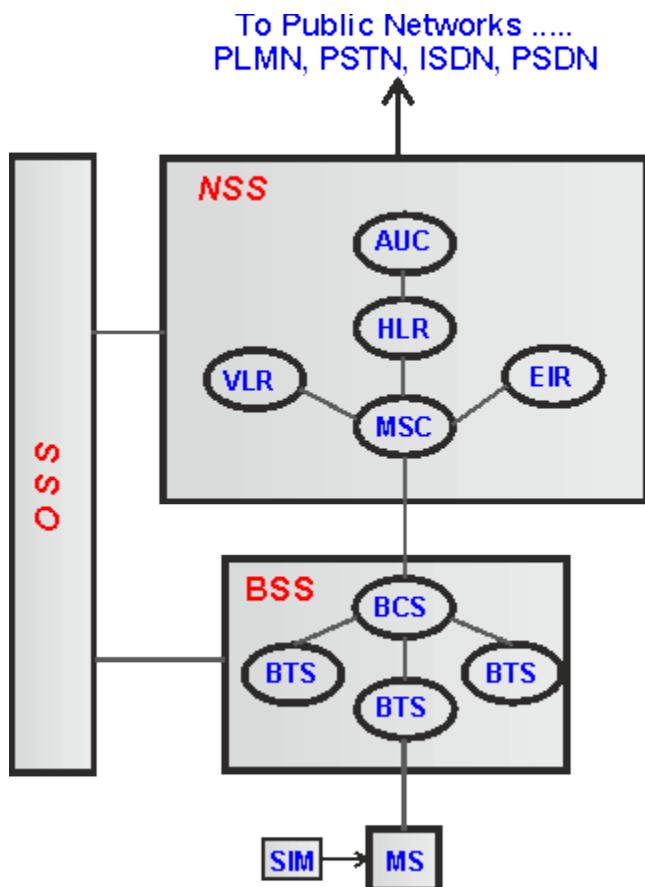


Fig: Simplified GSM Network Architecture Diagram

Mobile station

Mobile station (MS)/mobile equipment (ME)/cell/mobile phone is the section of a GSM cellular network that the user sees and operates. There are number of elements in the cell phone. The two main elements are the main hardware and the SIM.

The hardware itself contains the main elements of the mobile phone including the display, case, battery, and the electronics used to generate the signal, and process the data receiver and to be transmitted. It also contains a number known as the International Mobile Equipment Identity

(IMEI). This is installed in the phone at manufacture and "cannot" be changed. It is accessed by the network during registration to check whether the equipment has been reported as stolen.

The SIM or Subscriber Identity Module contains the information that provides the identity of the user to the network. It contains a variety of information including a number known as the International Mobile Subscriber Identity (IMSI).

Base Station Subsystem (BSS)

The Base Station Subsystem (BSS) section of the GSM network architecture that is fundamentally associated with communicating with the mobiles on the network. It consists of two elements:

- ***Base Transceiver Station (BTS):*** The BTS used in a GSM network comprises the radio transmitter/receivers, and their associated antennas that transmit and receive to directly communicate with the mobiles. The BTS is the defining element for each cell. The BTS communicates with the mobiles and the interface between the two is known as the Um interface with its associated protocols.
- ***Base Station Controller (BSC):*** The BSC forms the next stage back into the GSM network. It controls a group of BTSs, and is often co-located with one of the BTSs in its group. It manages the radio resources and controls items such as handover within the group of BTSs, allocates channels and the like. It communicates with the BTSs over what is termed the Abis interface.

Network Switching Subsystem (NSS)

The GSM system architecture contains a variety of different elements, and is often termed the core network. It provides the main control and interfacing for the whole mobile network. The major elements within the core network include:

- ***Mobile Services Switching Centre (MSC):*** The main element within the core network area of the overall GSM network architecture is the Mobile switching Services Centre (MSC). The MSC acts like a normal switching node within a PSTN or ISDN, but also provides additional functionality to enable the requirements of a mobile user to be supported. These include registration, authentication, call location, inter-MSC handovers and call routing to a mobile subscriber. It also provides an interface to the PSTN so that calls can be routed from the mobile network to a phone connected to a landline. Interfaces to other MSCs are provided to enable calls to be made to mobiles on different networks.
- ***Home Location Register (HLR):*** This database contains all the administrative information about each subscriber along with their last known location. In this way, the GSM network is able to route calls to the relevant base station for the MS. When a user switches on their phone, the phone registers with the network and from this it is possible to determine which BTS it communicates with so that incoming calls can be routed appropriately. Even when the phone is not active (but switched on) it re-registers

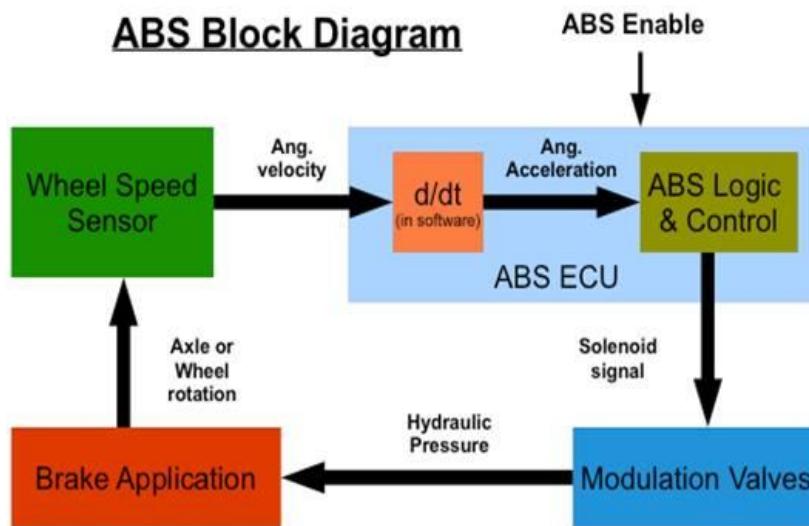
periodically to ensure that the network (HLR) is aware of its latest position. There is one HLR per network, although it may be distributed across various sub-centres to for operational reasons.

- **Visitor Location Register (VLR):** This contains selected information from the HLR that enables the selected services for the individual subscriber to be provided. The VLR can be implemented as a separate entity, but it is commonly realised as an integral part of the MSC, rather than a separate entity. In this way access is made faster and more convenient.
- **Equipment Identity Register (EIR):** The EIR is the entity that decides whether a given mobile equipment may be allowed onto the network. Each mobile equipment has a number known as the International Mobile Equipment Identity. This number, as mentioned above, is installed in the equipment and is checked by the network during registration. Dependent upon the information held in the EIR, the mobile may be allocated one of three states - allowed onto the network, barred access, or monitored in case its problems.
- **Authentication Centre (AuC):** The AuC is a protected database that contains the secret key also contained in the user's SIM card. It is used for authentication and for ciphering on the radio channel.
- **Gateway Mobile Switching Centre (GMSC):** The GMSC is the point to which a ME terminating call is initially routed, without any knowledge of the MS's location. The GMSC is thus in charge of obtaining the MSRN (Mobile Station Roaming Number) from the HLR based on the MSISDN (Mobile Station ISDN number, the "directory number" of a MS) and routing the call to the correct visited MSC. The "MSC" part of the term GMSC is misleading, since the gateway operation does not require any linking to an MSC.
- **SMS Gateway (SMS-G):** The SMS-G or SMS gateway is the term that is used to collectively describe the two Short Message Services Gateways defined in the GSM standards. The two gateways handle messages directed in different directions. The SMS-GMSC (Short Message Service Gateway Mobile Switching Centre) is for short messages being sent to an ME. The SMS-IWMSC (Short Message Service Inter-Working Mobile Switching Centre) is used for short messages originated with a mobile on that network. The SMS-GMSC role is similar to that of the GMSC, whereas the SMS-IWMSC provides a fixed access point to the Short Message Service Centre.

Operation and Support Subsystem (OSS)

The OSS or operation support subsystem is an element within the overall GSM network architecture that is connected to components of the NSS and the BSC. It is used to control and monitor the overall GSM network and it is also used to control the traffic load of the BSS. It must be noted that as the number of BS increases with the scaling of the subscriber population some of the maintenance tasks are transferred to the BTS, allowing savings in the cost of ownership of the system.

Anti-Lock Braking System



Antilock braking system (ABS) prevent brakes from locking during braking. In normal braking situation the driver control the brakes, however during severs braking or on slippery roadways when driver the wheels to approach lockup, the antilock takes over here. The ABS modulates the brake line pressure independent of the pedal force to bring the wheel speed back to the slip level range that necessary to the optimal braking performance. The ABS does not allow full wheel lock under braking. In simple terms, during emergency of braking, the wheel does not get locked even if you push a full auto brake pedal and hence the skidding does not takes place.

Electronic Control Unit (ECU):

1. A micro computer that functions as the ``brain'' of the ABS system.
2. The ECU receives wheel performance data from each wheel sensor.
3. When the wheels try to lock, the ECU delivers commands to the hydraulic valves to control brake pressure.

Hydraulic control unit or modulation valve unit

1. It receives operating signals from the ECU to apply or release the brakes under ABS conditions.
2. Hydraulic control unit controls the brake pressure in each wheel cylinder based on the inputs from the system sensor. This in result controls the wheel speed.

Break application unit

Whenever hard braking situation occur, the system sense the change in the rotation of the speed sensor and decide whether to hold or release pressure to a brake circuit.

Wheel sensor unit

1. It monitors the rotational speed of the wheel and transmits this data to the ABS control module.
2. If a wheel-speed sensor signals a lock up - the ECU sends a current to the hydraulic unit. This stops the braking pressure at that wheel from rising, and keeps it constant. It allows wheel velocity to increase and slip to decrease.

Internet of Things or IoT

BUILDING BLOCKS of IoT

Basic building blocks of IoT system include –sensors, processors, gateways, applications. Each of these nodes has to have their own characteristics in order to form a useful IoT system.

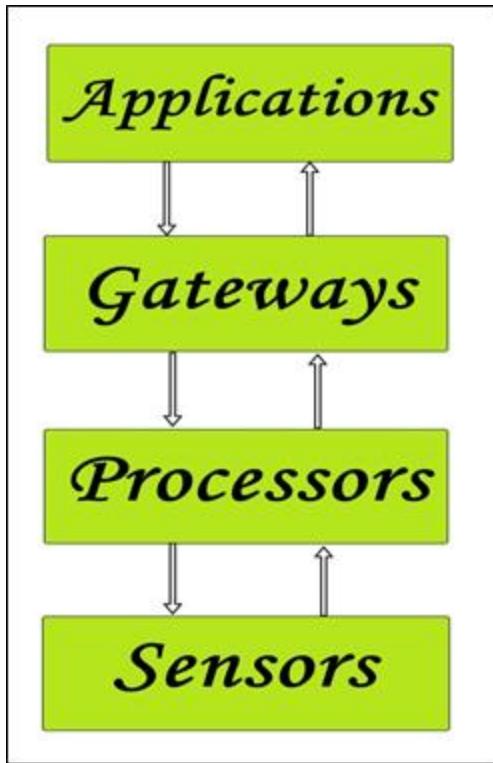


Figure 1: Simplified block diagram of the basic building blocks of the IoT

Sensors:

These form the front end of the IoT devices. These are the so called “Things” of the system. Their main purpose is to collect data from its surrounding (sensors) or give out data to its surrounding (actuators).

These have to be uniquely identifiable devices with a unique IP address so that they can be easily identifiable over a large network.

These have to be active in nature which means that they should be able to collect real time data. These can either work on their own (autonomous in nature) or can be made to work by the user depending on their needs (user controlled).

Examples of sensors are: gas sensor, water quality sensor, moisture sensor etc.

Processors:

Processors are the brain of the IoT system. Their main function is to process the data captured by the sensors and process them so as to extract the valuable data from the enormous amount of raw data collected. In a word, we can say that it gives intelligence to the data.

Processors mostly work on real-time basis and can be easily controlled by applications. These are also responsible for securing the data – that is performing encryption and decryption of data.

Embedded hardware devices, microcontroller etc are the ones that process the data because they have processors attached to it.

Gateways:

Gateways are responsible for routing the processed data and send it to proper locations for its (data) proper utilization.

In other words, we can say that gateway helps in to and fro communication of the data. It provides network connectivity to the data. Network connectivity is essential for any IoT system to communicate.

LAN, WAN, PAN etc are examples of network gateways.

Applications:

Applications form another end of an IoT system. Applications are essential for proper utilization of all the data collected.

Examples of applications are: home automation apps, security systems, industrial control hub etc.

HOW IoT WORKS

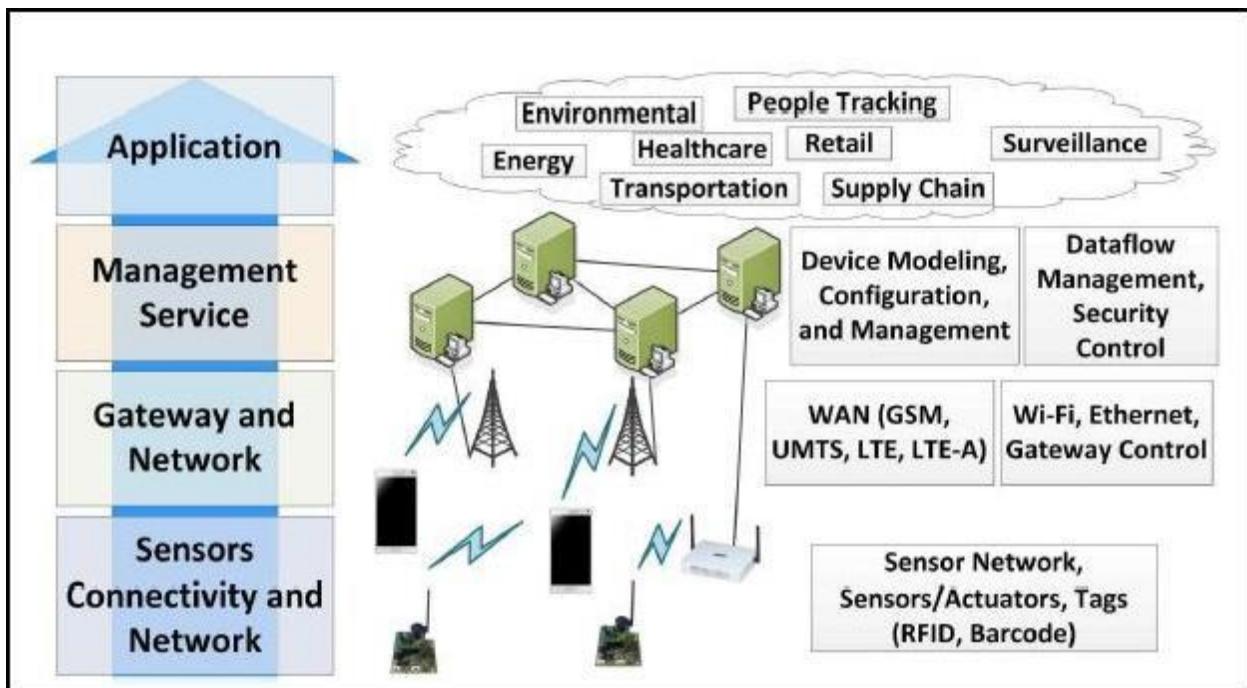
First, it acquires information with respect to basic resources (names, addresses and so on) and related attributes of objects by means of automatic identification and perception technologies such as RFID, wireless sensor and satellite positioning, in other words the sensors, RFID tags and all other uniquely identifiable objects or "things" acquire real-time information (data) with the virtue of a central hub like smartphones.

Second, by virtue of many kinds of communications technologies, it integrates object-related information into the information network and realizes the intelligent indexing and integration of the information related to masses of objects by resorting to fundamental resource services (similar to the resolution, addressing and discovery of the internet).

Finally, utilizing intelligent computing technologies such as cloud computing, fuzzy recognition, data mining and semantic analysis, it analyzes and processes the information related to masses of objects so as to eventually realize intelligent decision and control in the physical world.

IoT ARCHITECTURE

There are four major layers.



Sensor, Connectivity and Network Layer

- This layer consists of RFID tags, sensors (which are essential part of an IoT system and are responsible for collecting raw data). These form the essential “things” of an IoT system.
- Sensors, RFID tags are wireless devices and form the Wireless Sensor Networks (WSN).
- Sensors are active in nature which means that real-time information is to be collected and processed.

- This layer also has the network connectivity (like WAN, PAN etc.) which is responsible for communicating the raw data to the next layer which is the Gateway and Network Layer.

Gateway and Network Layer

- Gateways are responsible for routing the data coming from the **Sensor, Connectivity and Network layer** and pass it to the next layer which is the **Management Service Layer**.
- This layer requires having a large storage capacity for storing the enormous amount of data collected by the sensors, RFID tags etc. Also, this layer needs to have a consistently trusted performance in terms of public, private and hybrid networks.

Management Service Layer

- This layer is used for managing the IoT services. Management Service layer is responsible for Securing Analysis of IoT devices, Analysis of Information, Device Management.
- Data management is required to extract the necessary information from the enormous amount of raw data collected by the sensor devices to yield a valuable result of all the data collected. This action is performed in this layer.

Application Layer

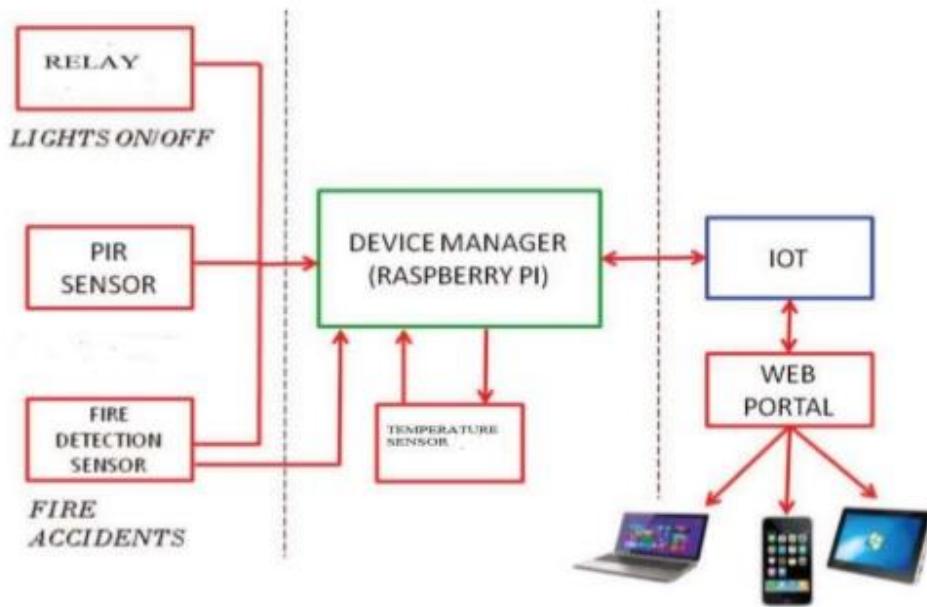
Application layer forms the topmost layer of IoT architecture which are responsible for effective utilization of the data collected.

Various IoT applications include Home Automation, E-health, E-Government etc.

Smart Home automation

Smart Home automation refers to handling and controlling home appliances by using micro-controller or computer technology.

BLOCK DIAGRAM



The home automation using Internet of Things connects devices and control remotely through internet. The system not only monitors the sensor data, like temperature, gas, light, motion sensors, but also actuates a process according to the requirement, for example switching on the light when it gets dark. It also stores the sensor parameters in the cloud (Gmail) in a timely manner. This will help the user to analyze the condition of various parameters in the home anytime anywhere.

The model consists of number of relays to connect various devices. Initially all the devices are connected to the internet through Wi-Fi. When the connection is established in on web page we provide virtual switches to operate the connected devices. If particular device exceeds the threshold set point then server will give notification to the user on web page and that device will automatically turned off.

Passive Infrared Sensor (PIR) is an electronic device which is designed to detect this IR wavelength when a human being is in its proximity. PIR motion sensors are installed at the

entrances of a building. This signal which detects the presence of human beings becomes the input trigger for the micro-controller.

Raspberry Pi: The main processing and controlling unit of the system. It has four USB ports, allowing the connection of different peripherals to it such as keyboard, mouse, memory stick or Wi-Fi dongle, that allows its connection to wireless internet.

The home automation system has the capability to monitor and control the following:

Temperature and humidity

Motion detection

Fire and smoke detection

Light/Fan on/off

ADVANTAGES

(a) Adds Safety Through Appliance and Lighting Control

(b) Secures Home Through web control Increases Convenience through Temperature Adjustment

(c) Save time

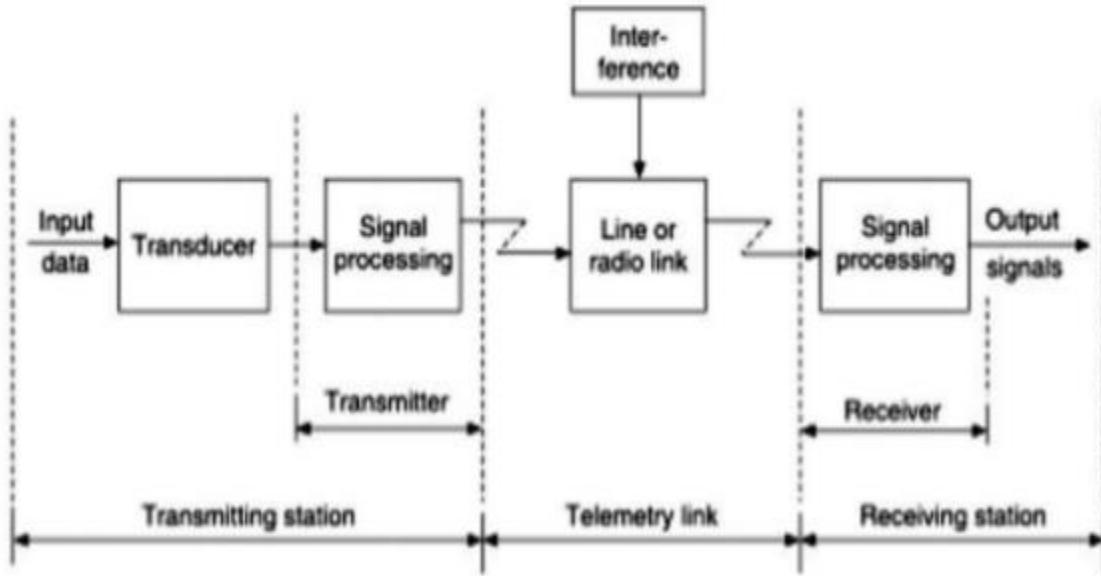
(d) Save money and increase convenience

(e) Allow to appliances control when out of towndraulic pres

Telemetry

Telemetry is an automated communications process by which measurements and other data are collected at remote or inaccessible points and transmitted to receiving equipment for monitoring. The function of Telemetry sub system is to monitor various aircraft parameters and to transmit the measured values to the satellite control centre.

Telemetry involves three steps: a. converting measured quantity to signal b. Transmission of that signal over proper channel c. Its reconversion to actual data for recording, displaying(CRT) for graphical analysis and further computation



1. It refers to the overall operation of generating an electrical signal proportional to the quantity being measured and encoding and transmitting this to a distant station, which for the satellite is one of the earth stations.
2. The telemetry data are analyzed at the control centre is used for routine operation and failure diagnostic purposes.
3. The parameters most commonly monitored are:
 - 1) Voltage, current and Temperatures of all major systems
 - 2) Switch status of communications transponders.
 - 3) Pressure of propulsion tanks
 - 4) Output from attitude sensors
 - 5) Reaction wheel speed
 - 6) Environmental information such as the magnetic field intensity and direction, the frequency of meteorite impact.
4. Several sensors provide analog signals whereas some others provide digital signals.
5. Analog signals are digitally encoded and multiplexed with other signals, forming a continuous digital stream. Typical telemetry data rates are in the range of 150 to 100 bps.
6. The telemetry data are transmitted as FSK, PSK via telemetry antenna. The telemetry signal is commonly used as a beacon by ground stations for tracking purpose

DEMERITS AND MERITS

Merits:

- Effective for short distance measurement

- V and I can be easily transmitted
- Circuitry required is simple
- Wide variety of primary sensing elements are available to measure reqd. variable.

Demerits:

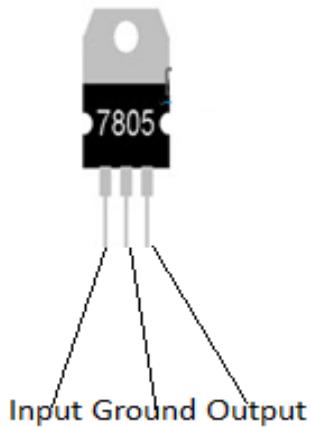
- Demands high S/N ratio that is difficult to calibrate.
- Need to be protected from EMI, noises and distortions in the channel.
- Multiplexing is difficult
- Limited frequency response

7805 Voltage Regulator

7805 is a three terminal linear voltage regulator IC with a fixed output voltage of 5V which is useful in a wide range of applications.

Pin Diagram of 7805 Voltage Regulator IC

As mentioned earlier, 7805 is a three terminal device with the three pins being INPUT, GROUND and OUTPUT.



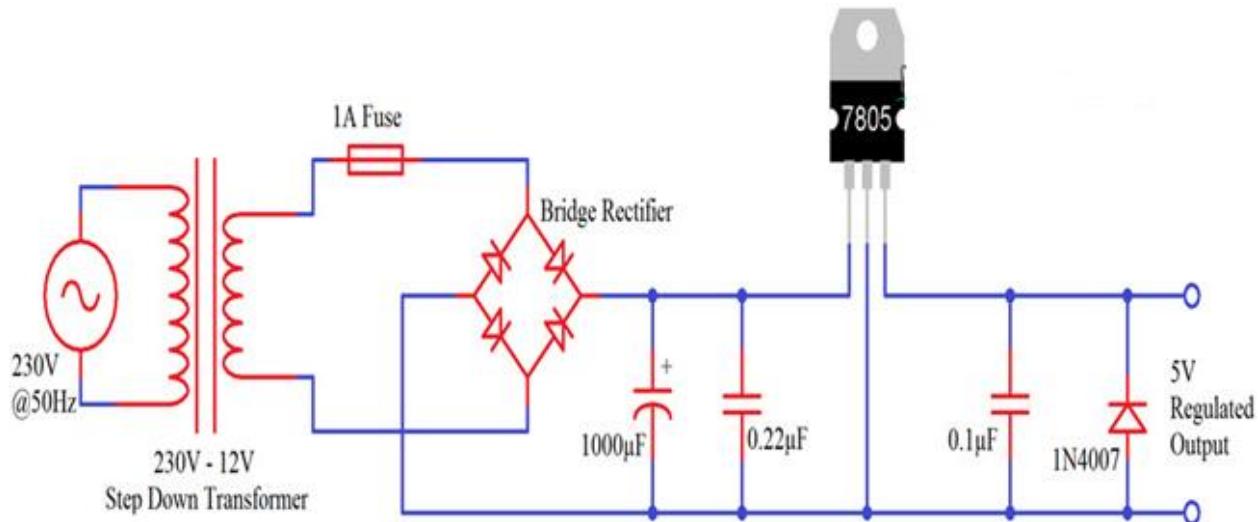
The pin description of the 7805 is described in the following table:

PIN NO.	PIN	DESCRIPTION

PIN NO.	PIN	DESCRIPTION
1	INPUT	Pin 1 is the INPUT Pin. A positive unregulated voltage is given as input to this pin.
2	GROUND	Pin 2 is the GROUND Pin. It is common to both Input and Output.
3	OUTPUT	Pin 3 is the OUTPUT Pin. The output regulated 5V is taken at this pin of the IC.

Circuit Diagram

The following image shows the circuit diagram of producing a regulated 5V from AC Mains supply.



Components Required

- 230V-12V Step Down Transformer
- Bridge Rectifier (or 4 PN Diodes – 1N4007)
- 1A Fuse
- 1000μF Capacitor

- 7805 Voltage Regulator IC
- 0.22 μ F Capacitor
- 0.1 μ F Capacitor
- 1N4007 Diode

Working

The AC power supply from mains first gets converted into unregulated DC and then into a constant regulated DC with the help of this circuit. The circuit is made up of transformer, bridge rectifier made up from diodes, linear voltage regulator 7805 and capacitors.

If you observe, the working of the circuit can be divided into two parts. In the first part, the AC Mains is converted into unregulated DC and in the second part, this unregulated DC is converted into regulated 5V DC. So, let us start discussing the working with this in mind.

Initially, a 230V to 12V Step down transformer is taken and its primary is connected to mains supply. The secondary of the transformer is connected to Bridge rectifier (either a dedicated IC or a combination of 4 1N4007 Diodes can be used).

A 1A fuse is placed between the transformer and the bridge rectifier. This will limit the current drawn by the circuit to 1A. The rectified DC from the bridge rectifier is smoothed out with the help of 1000 μ F Capacitor.

So, the output across the 1000 μ F Capacitor is unregulated 12V DC. This is given as an input to the 7805 Voltage Regulator IC. 7805 IC then converts this to a regulated 5V DC and the output can be obtained at its output terminals.