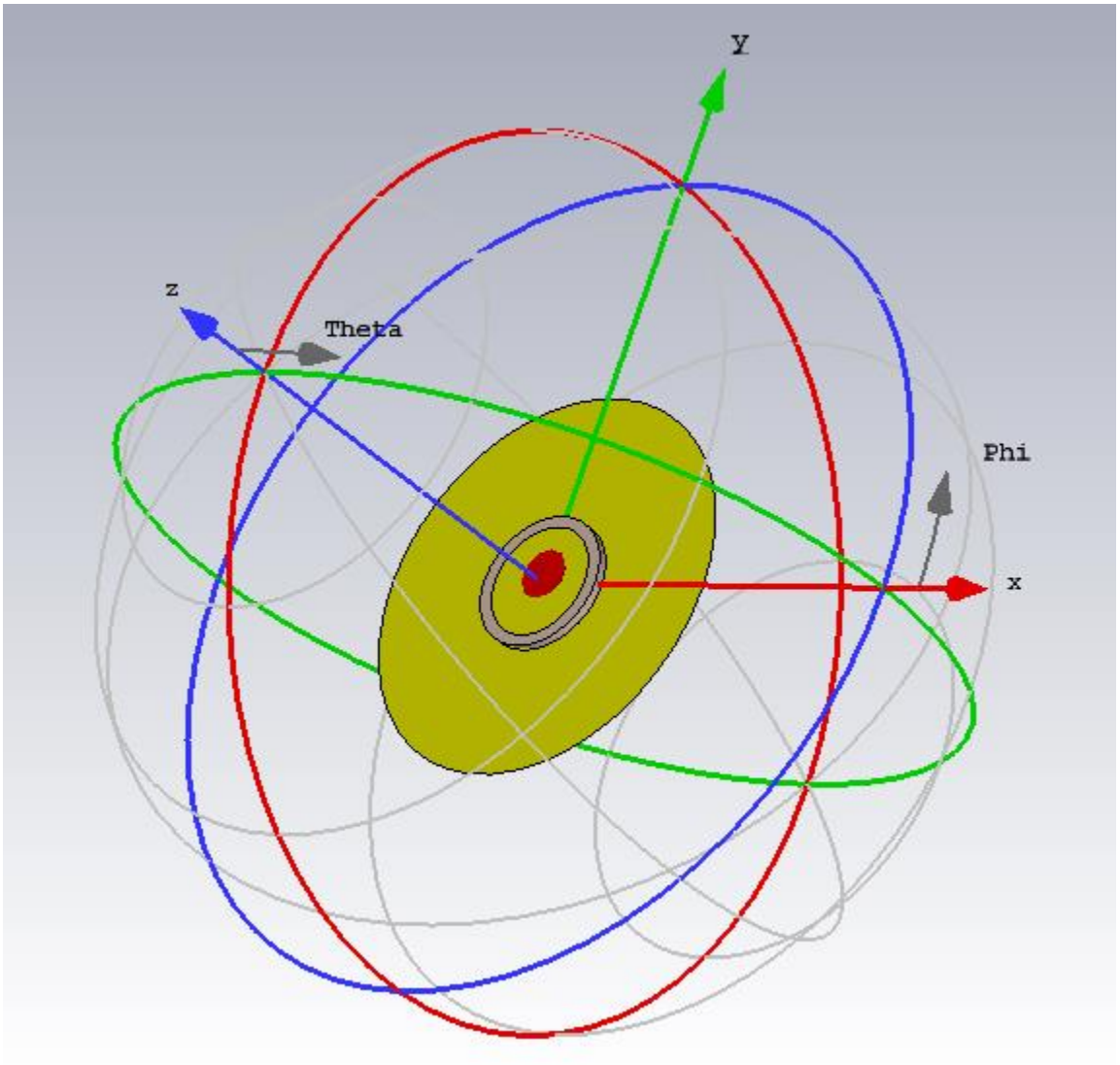
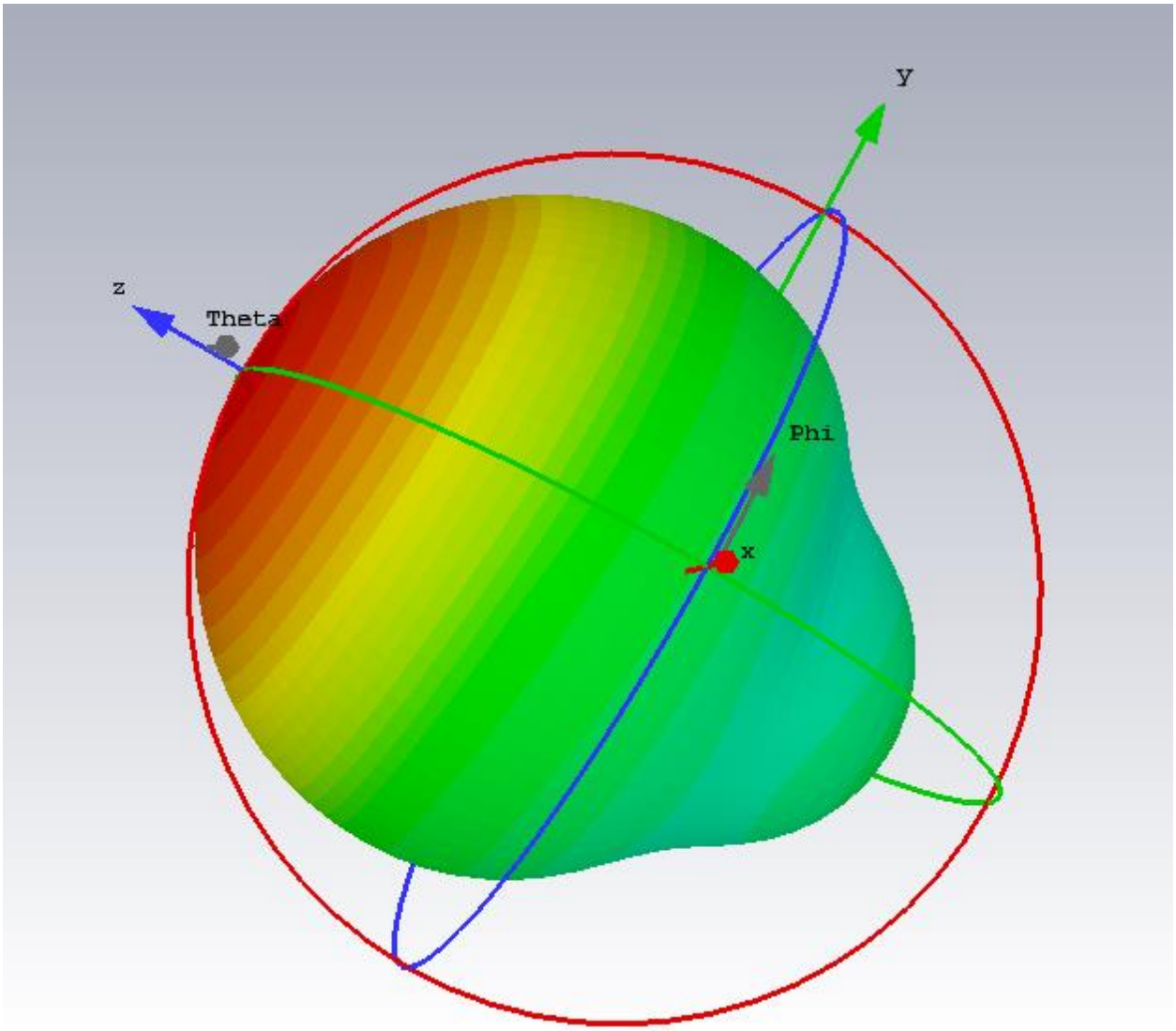
RF Front End Summary:

The RF hardware end of this project is the part where the GPS signal from the satellite constellation is converted from an RF signal into an analog signal, which can then be converted into a digital signal through and A-D converter on the FPGA board, where the data will be processed. The hardware system consists of a tuned antenna to gain the signal of interest while neighboring frequencies are filtered out. The signal then goes to a board, where more filtering and amplification occurs, and the RF signal is demodulated to a baseband analog frequency.

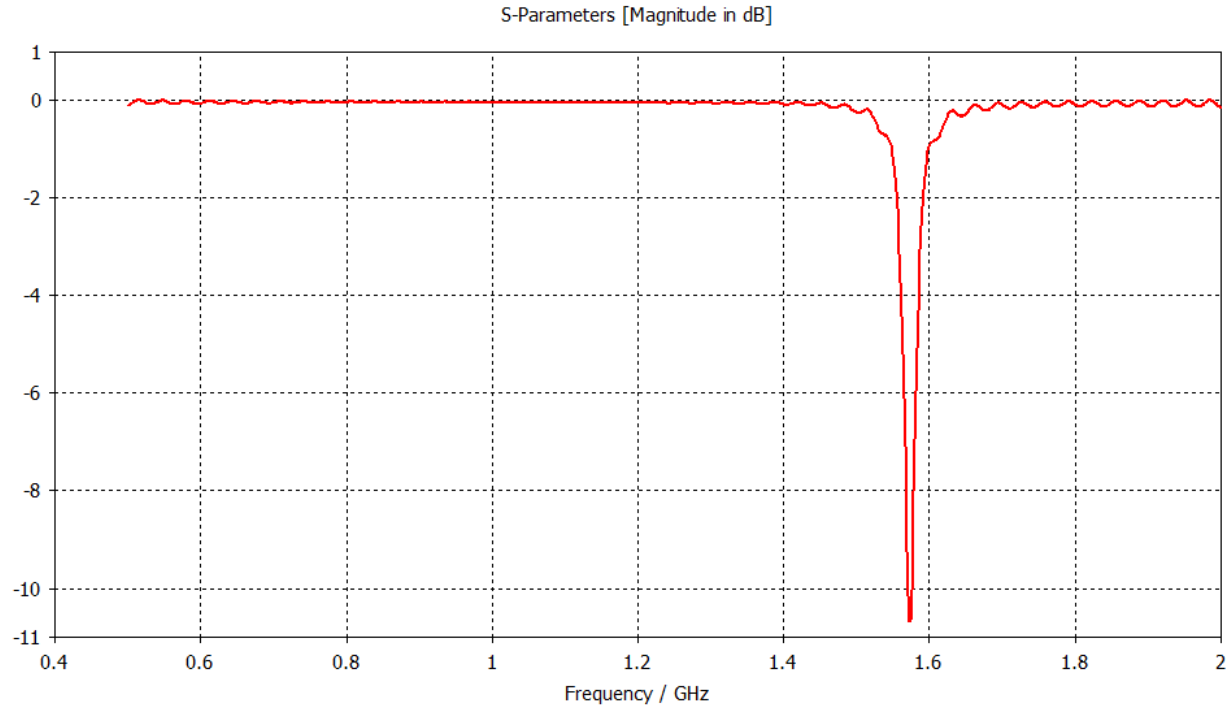
Below is the CAD model of the antenna that was designed using CST Microwave Studio, an electromagnetic simulator that is used to test how the antenna will work to tune the design before building it.



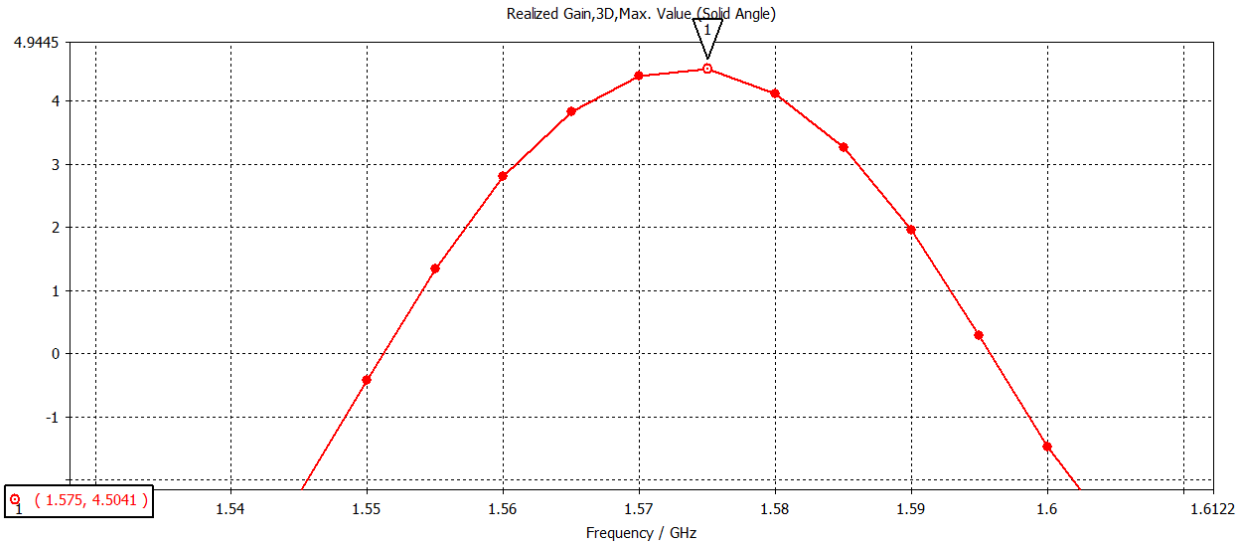
This is the radiation profile of the antenna. It is partially directive in the z-direction to increase the gain in the direction of the satellite constellation, but is also relatively omnidirectional.



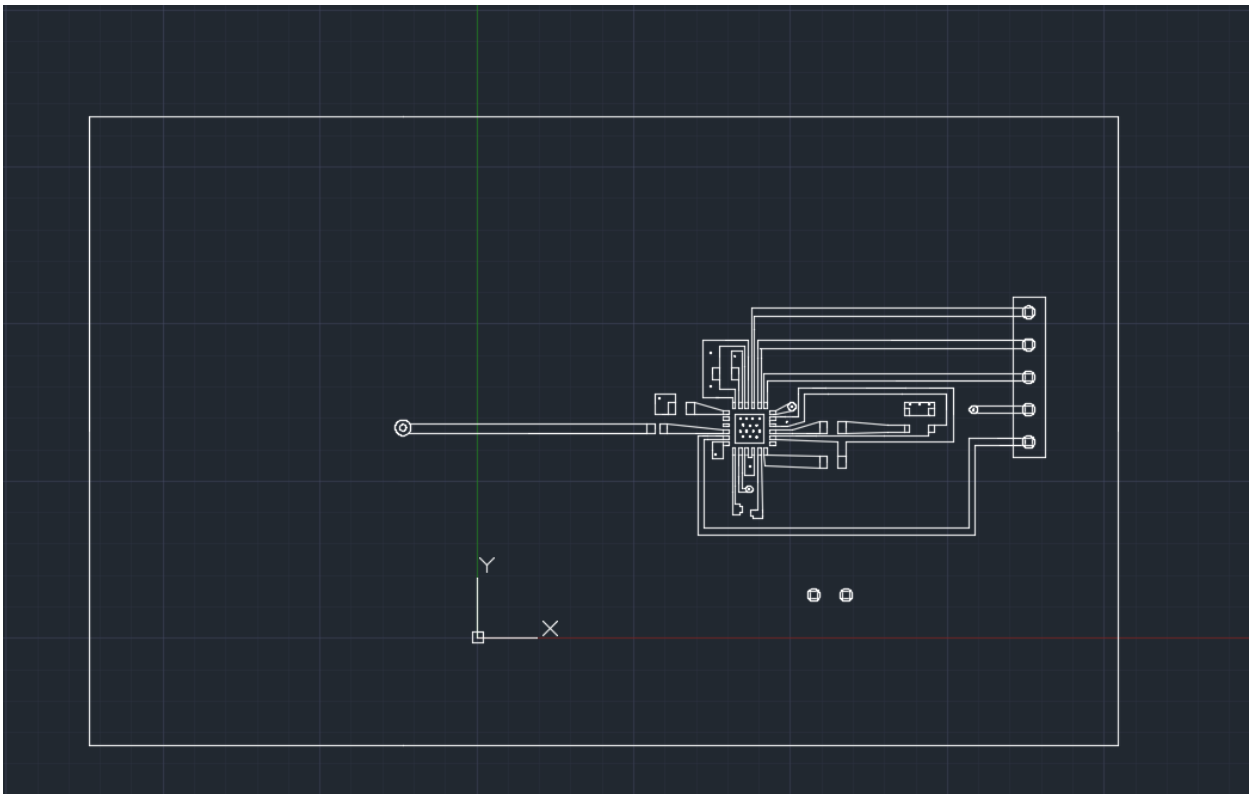
The antenna is very matched to the target frequency, meaning it passes the signal at the GPS frequency and reflects the signals at other frequencies, cutting down on noise.



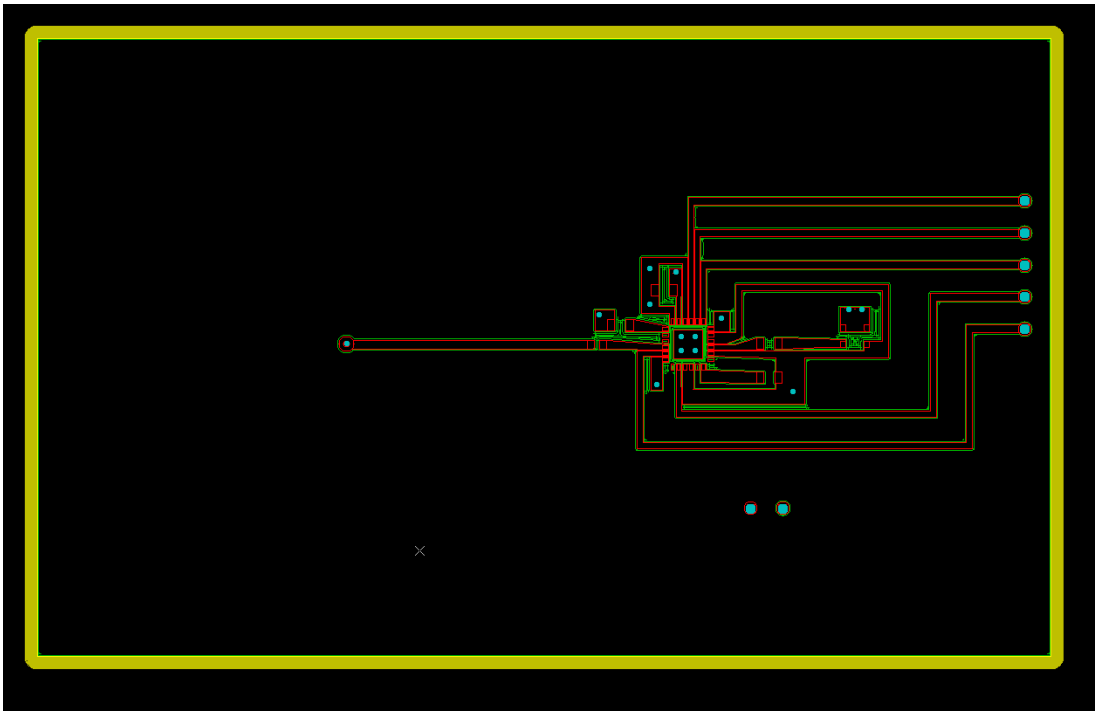
The gain at the target frequency of 1575 MHz is 4.5 dB, which is over 7dB higher than the gain of an off-the-shelf GPS antenna. It also have a very wide gain bandwidth, meaning if the frequency is skewed due to the dielectric constant of materials around it, it can still read the signal.

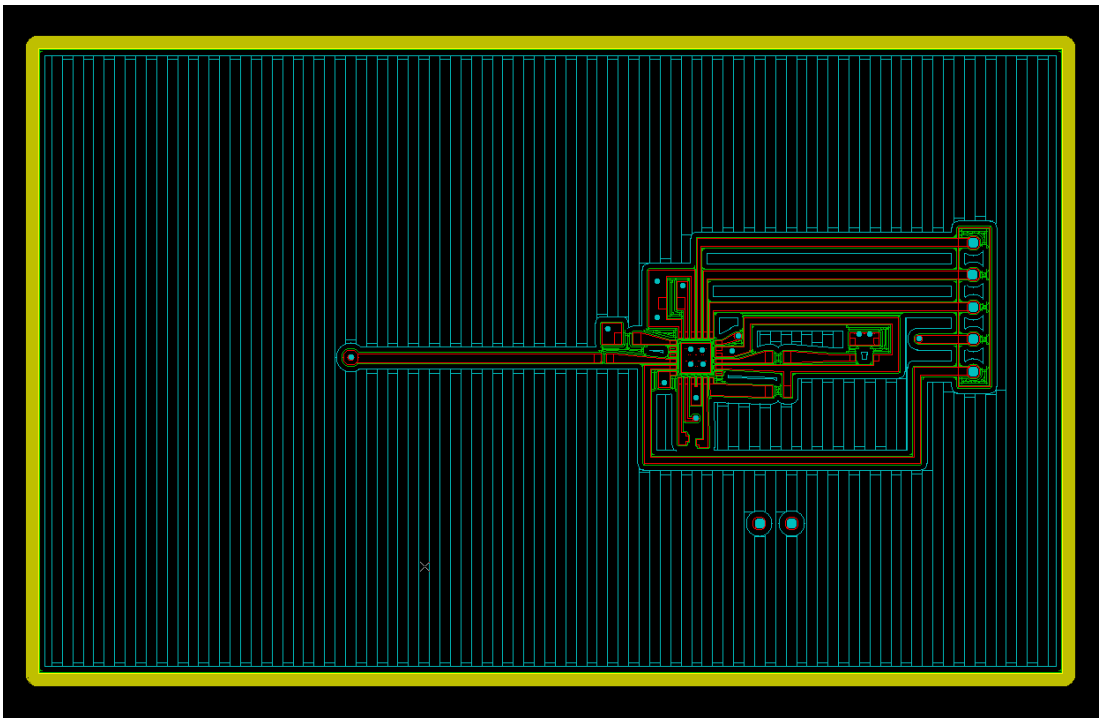


This is the layout of the circuit that contains the GPS chip used to demodulate the signal, IF oscillator used to provide the down-converting frequency, and RF filter to cut away noise. It was designed in AutoCAD instead of a typical circuit layout software, since the components we selected did not have a digital footprint provided, so we had to render the footprints ourselves before actually connecting the pins.



Once the layout was designed, it was pulled into software to cut it out on the milling machine and laser. The 2D layout file was pulled into the LPKF CircuitCam software, where we designed the path for the laser to follow in order to cut out the board by milling away the copper on the board to leave the traces needed place and connect the components. We made 7 boards, due to trouble with either the size of the traces or difficulty soldering onto them. Below are two of the drill traces, the top one simply cutting a gap between the trace and ground layer, and the bottom one cutting away all unneeded copper.





Below are the actual cut out hardware components. The antenna is placed on the top of the board, along with the GPIO pins to communicate with the FPGA. The bottom side of the board is where the signal from the antenna goes to the chip and other components required to demodulate the signal.