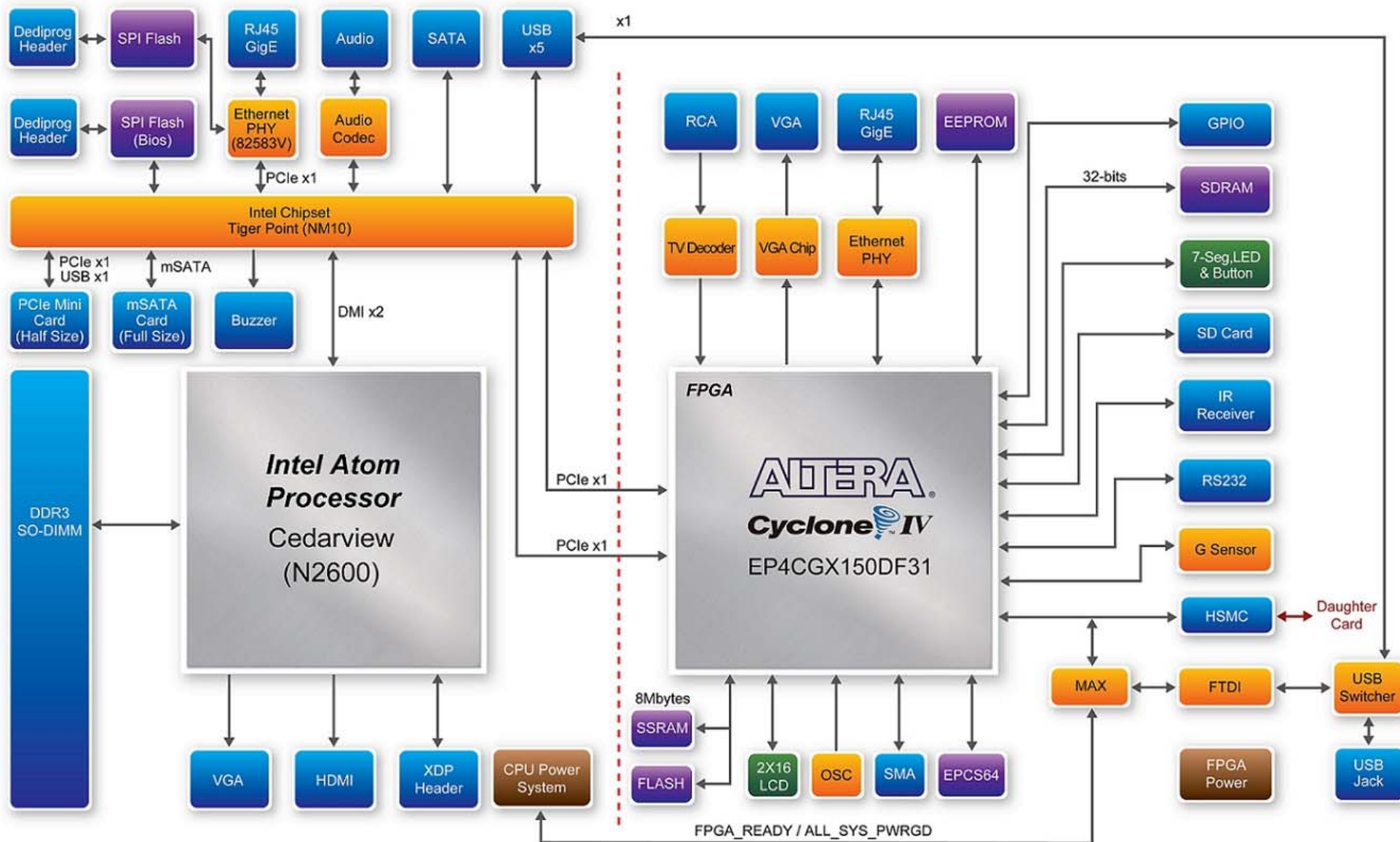



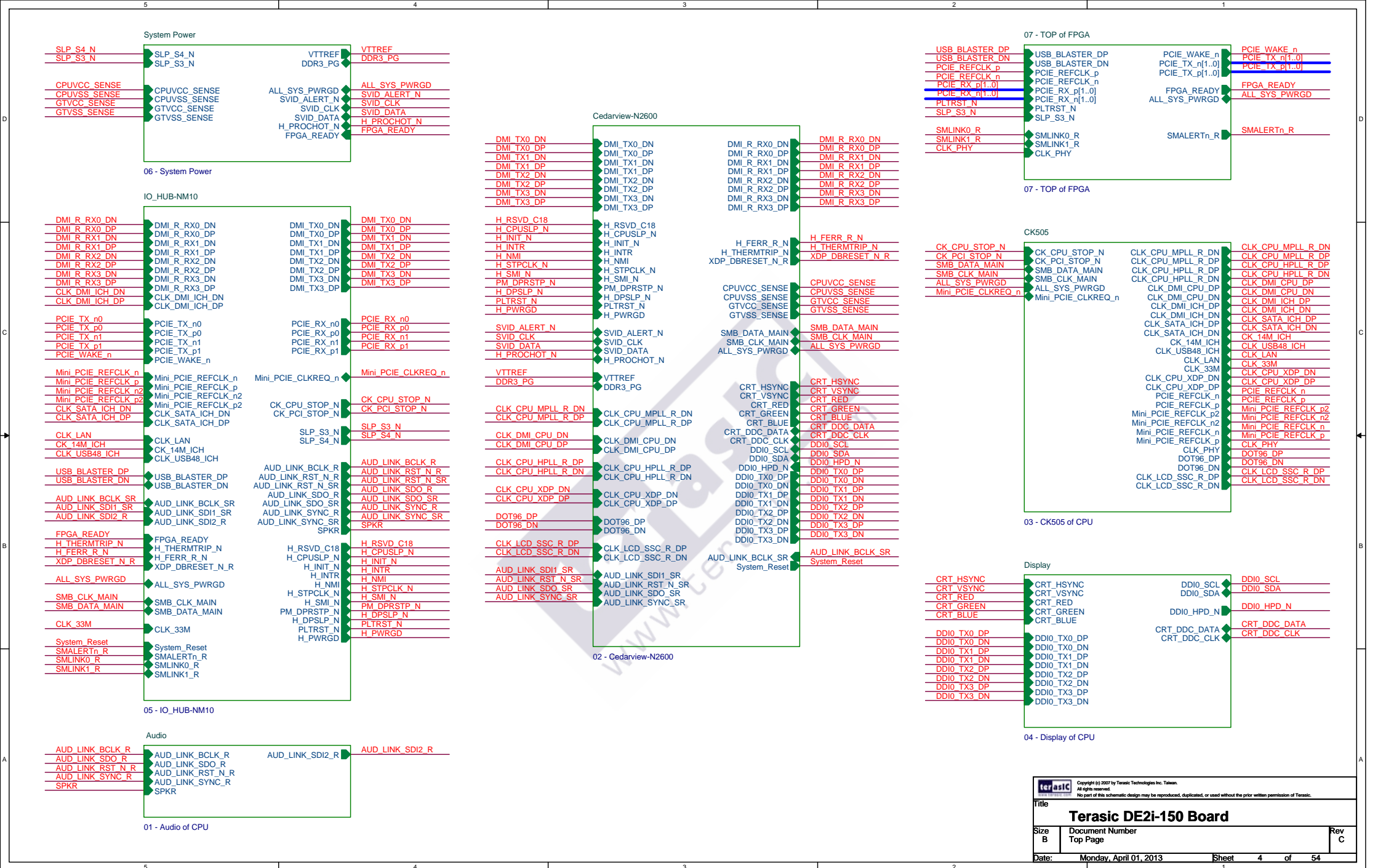
Terasic DE2i-150 Board

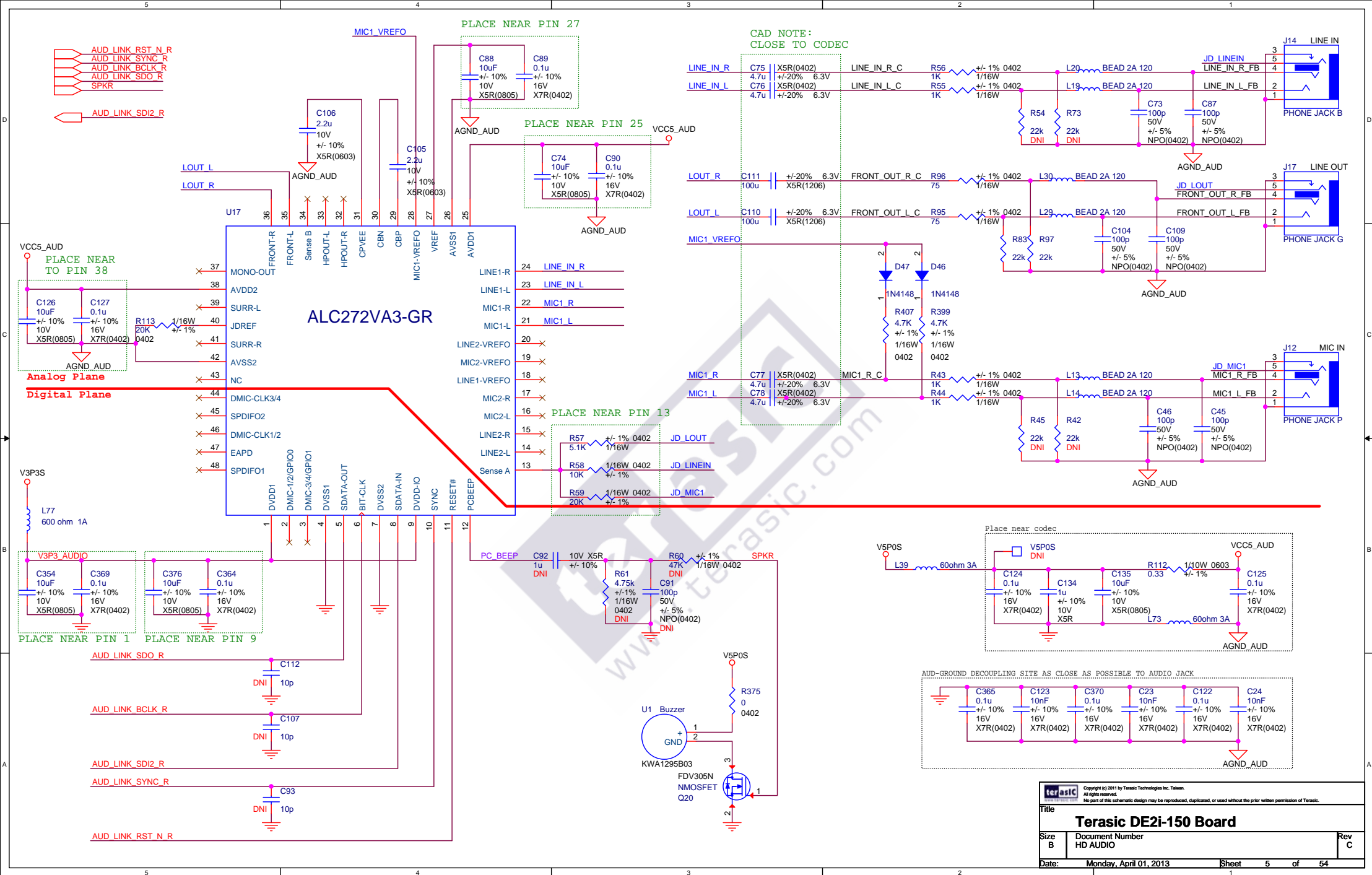
| SCHEMATIC | CONTENT | PAGE |
|---------------------|--|---------|
| 00 Top | Cover Page, Block Diagram,TOP | 00 ~ 03 |
| 01 Audio | Audio | 04 |
| 02 Cedarview-N2600 | Cedarview, DDR3 SO-DIMM, XDP Interface | 05 ~ 12 |
| 03 CK505 of CPU | CK505 | 13 |
| 04 Display of CPU | HDMI, VGA | 14 ~ 15 |
| 05 IO_HUB-NM10 | Tiger Point, LAN, USB, SATA, mSATA, Mini PCIE, SPI Flash(BIOS) | 16 ~ 24 |
| 06 System Power | Power System | 25 ~ 28 |
| | | |
| 07 Top of FPGA | TOP of FPGA Circuit | 29 |
| 08 Memory of FPGA | SDRAM, SSRAM, Flash and SD Card | 30 ~ 32 |
| 09 Display of FPGA | LCD, LED, 7-SEGMENT | 33 ~ 34 |
| 10 IN/OUT of FPGA | CLOCK, IrDA , RS232 , BUTTON , SWITCH , HSMC | 35 ~ 39 |
| 11 Ethernet of FPGA | 88E1111, EEPROM | 40 ~ 41 |
| 12 Video of FPGA | ADV7123, ADV7180 | 42 ~ 43 |
| 13 FPGA Config | USB Blaster | 44 |
| 14 EP4CGX150 FPGA | Cyclone IV EP4CGX150 BANK3..BANK8 , QL0/1,POWER , CONFIG | 45 ~ 52 |
| 15 Sensor of FPGA | G-Sensor | 53 |
| | | |
| | | |
| | | |

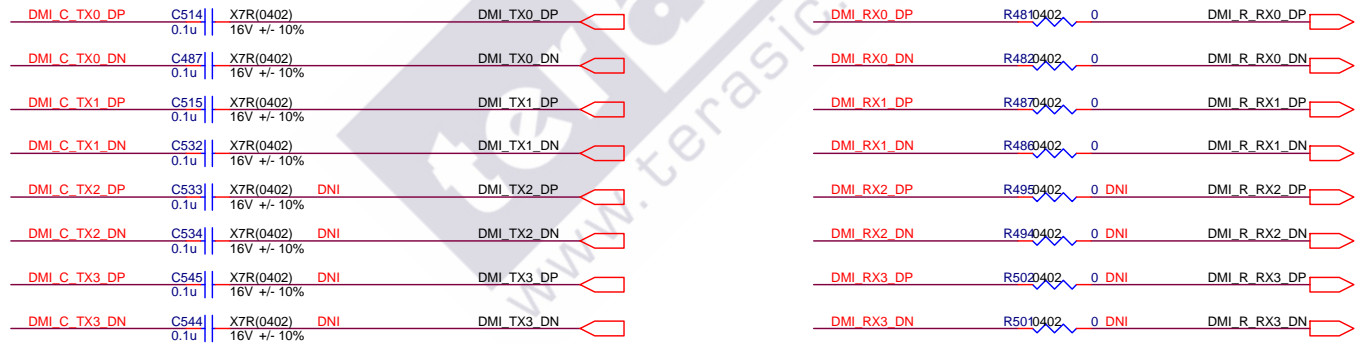


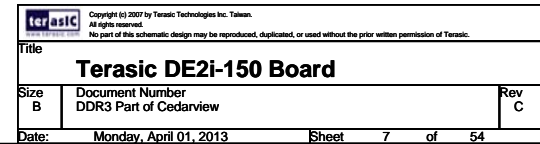
| RAIL | Voltage Level | S0 | S3 | S4 | S5 | PS |
|-------------------|---------------|----|----|----|----|----------------------------------|
| +12V | 12V | Y | Y | Y | Y | Control by HOST_ALERT_MINICARD_N |
| V5P0A | 5V | Y | Y | Y | Y | |
| V5P0S | 5V | Y | N | N | N | |
| V3P3A | 3.3V | Y | Y | Y | Y | |
| V3P3S | 3.3V | Y | N | N | N | |
| V3P3S_PRIME | 3.3V | Y | N | N | N | |
| V3P3_Mini_PCIE | 3.3V | Y | N | N | N | |
| V3P3_AUX(Default) | 3.3V | Y | Y | Y | Y | |
| V1P8S | 1.8V | Y | N | N | N | |
| V1P5C | 1.5V | Y | Y | N | N | |
| V1P5S | 1.5V | Y | Y | N | N | |
| V1P5S_DDR3 | 1.5V | Y | Y | N | N | |
| V1P5S_Mini_PCIE | 1.5V | Y | Y | N | N | |
| V1P05C | 1.05V | Y | N | N | N | |
| VCC_CPU | SVID | Y | N | N | N | |
| VCC_GFX | SVID | Y | N | N | N | Control by J11(HSMC12V_EN) |
| V2P5F | 2.5V | Y | N | N | N | |
| V1P2F | 1.2V | Y | N | N | N | |
| 12V_EXT(Default) | 12V | N | N | N | N | |

| | |
|--|----------------------------------|
|  <small>Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</small> | |
| Title | |
| Terasic DE2i-150 Board | |
| Size B | Document Number Voltage Rails |
| Date: | Monday, April 01, 2013 |
| Sheet | 3 of 54 |
| Rev C | |

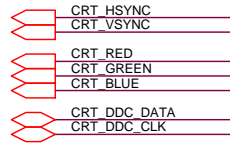




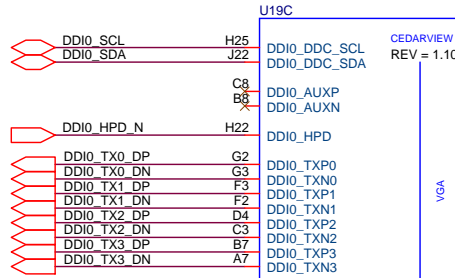




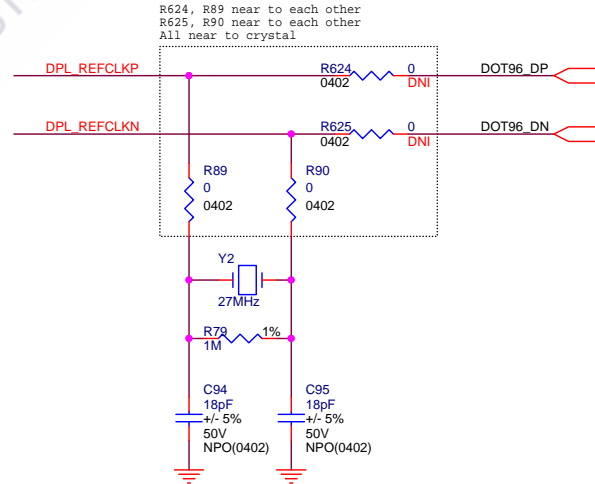
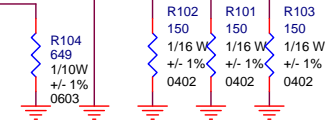
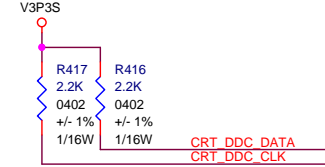
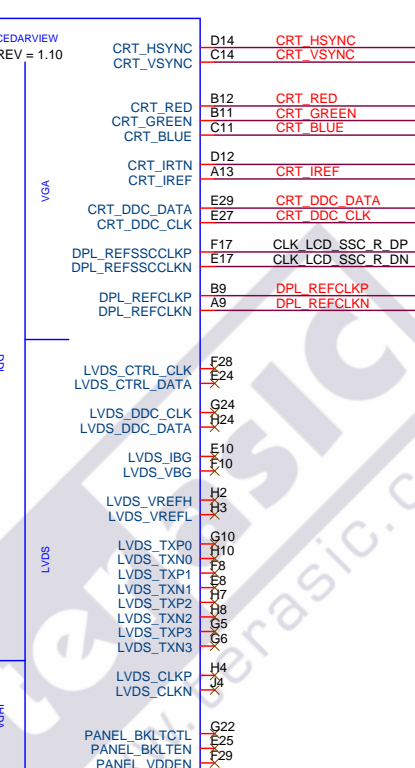
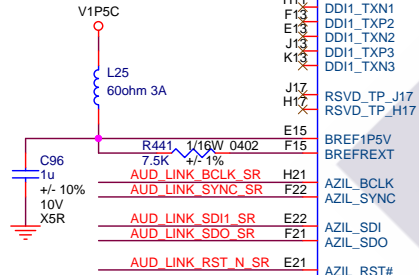
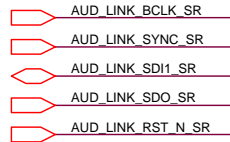
VGA Interface

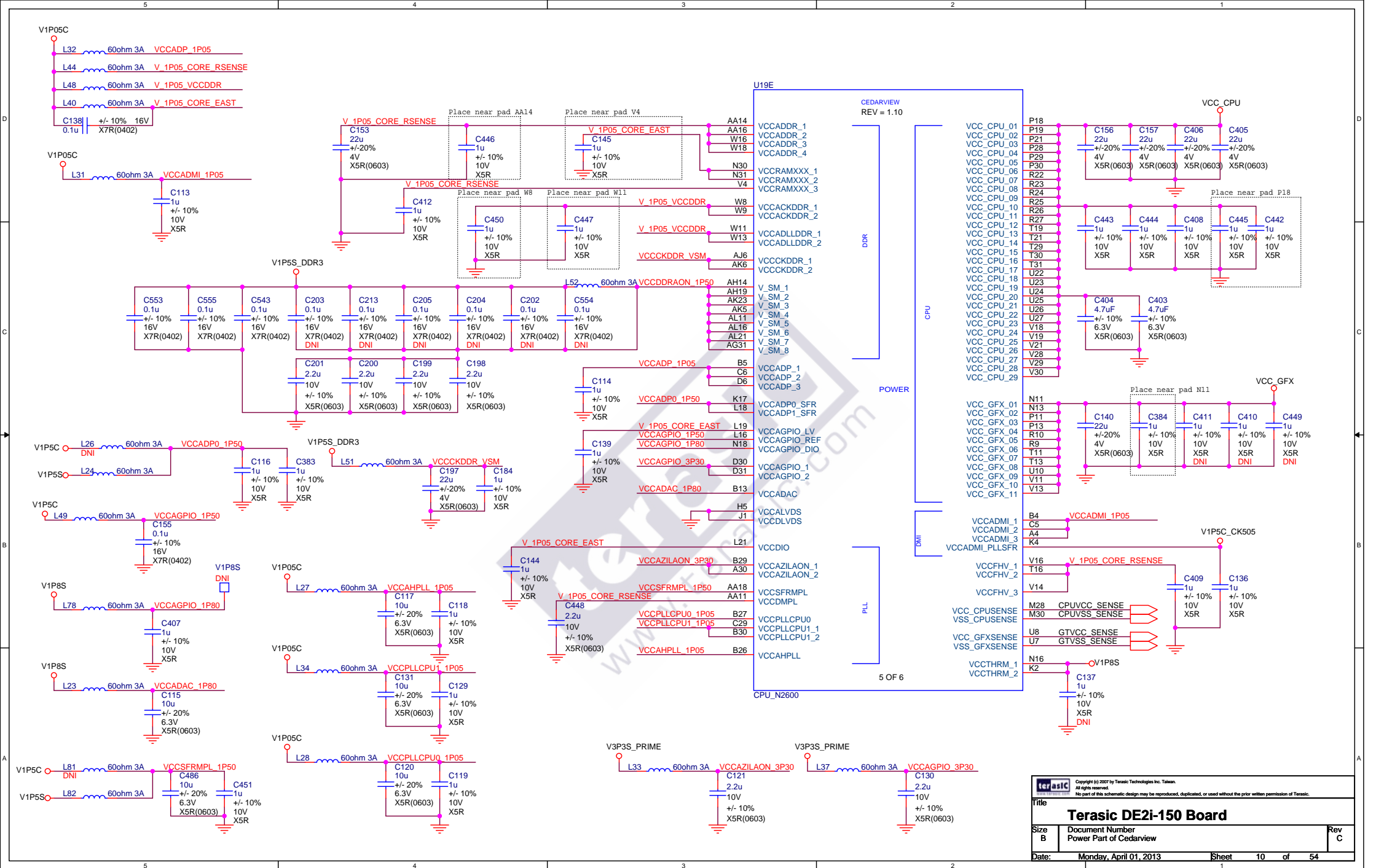


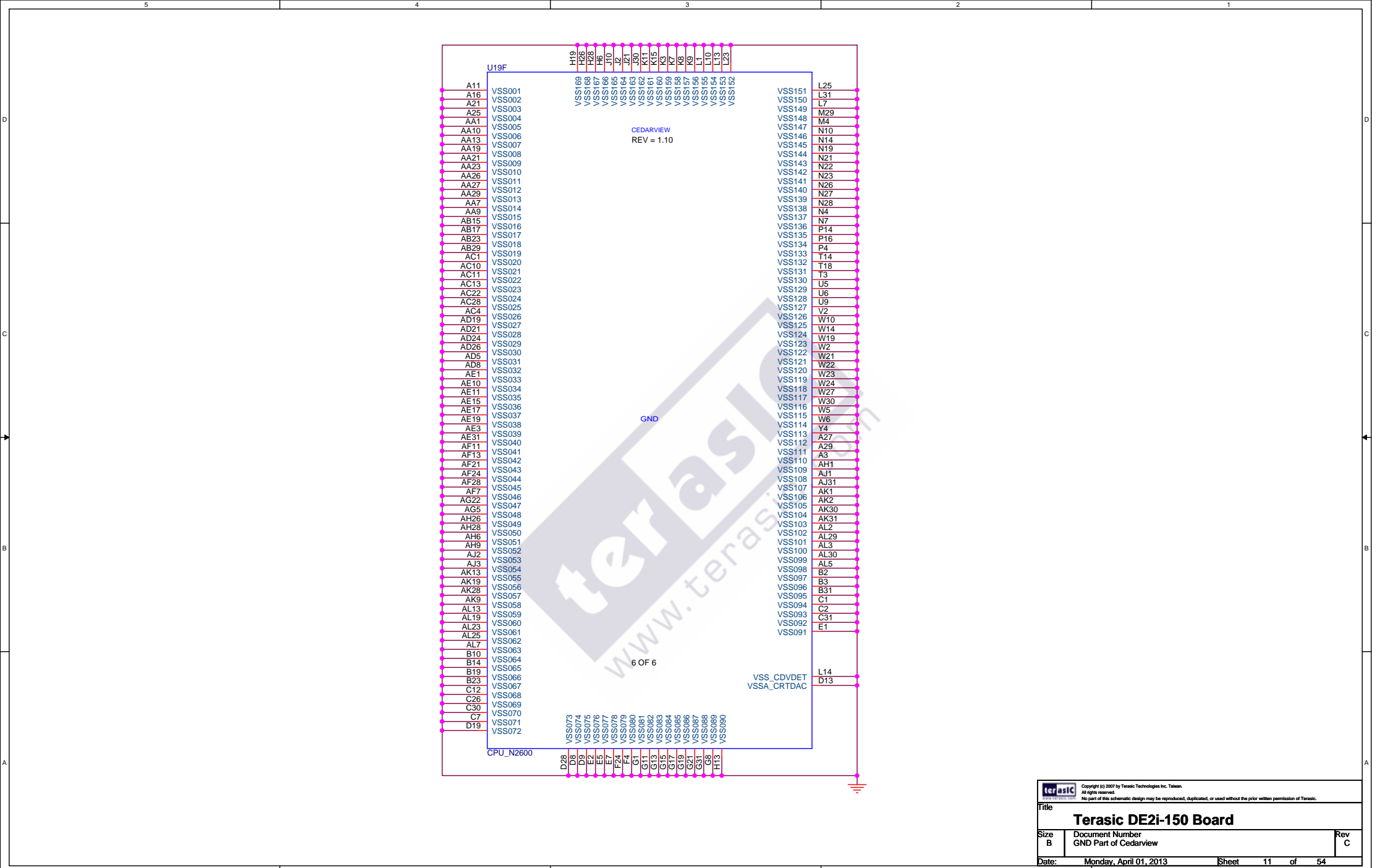
VGA Clock

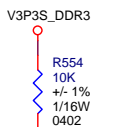
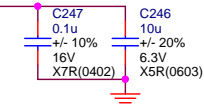
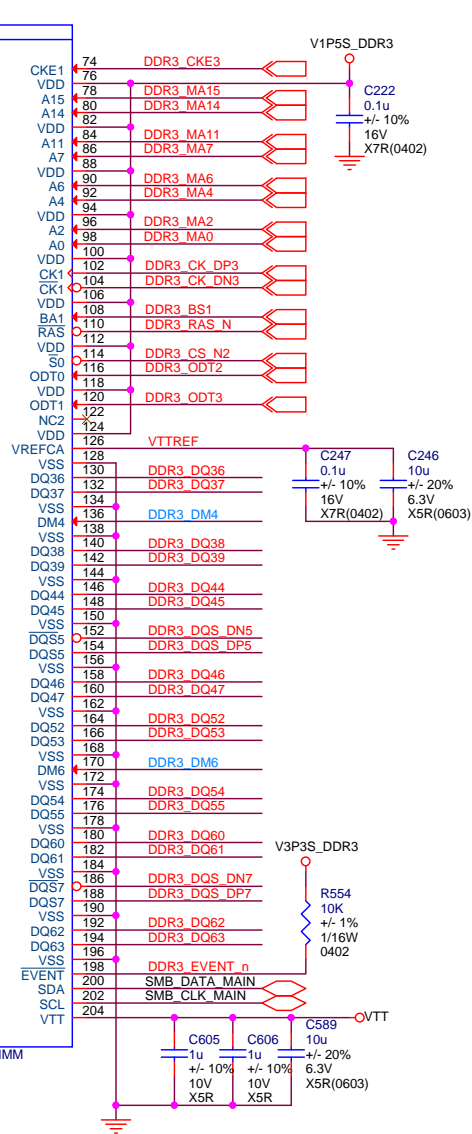
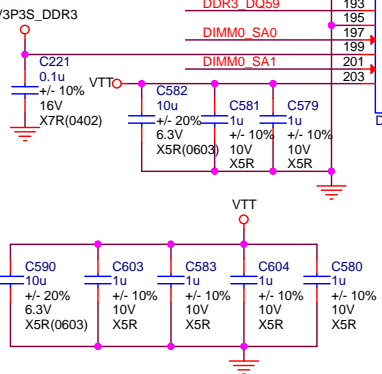
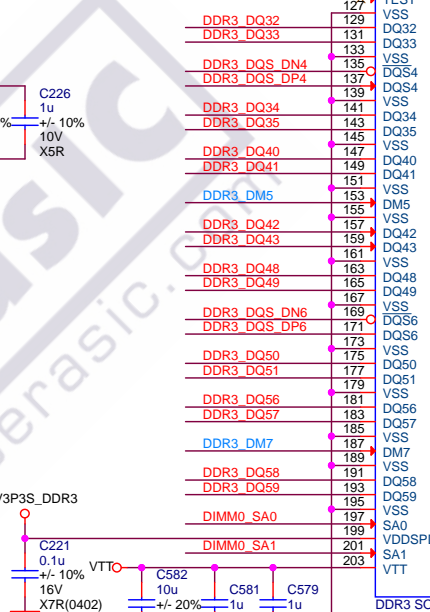
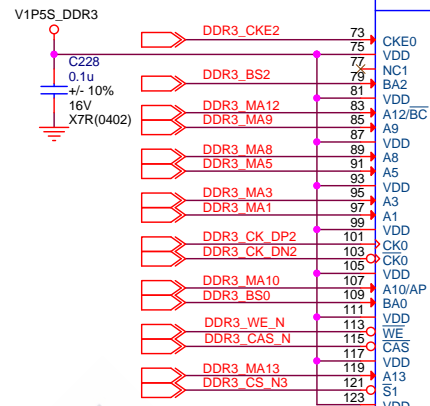
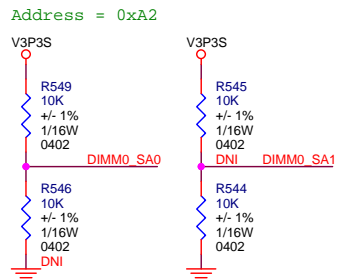
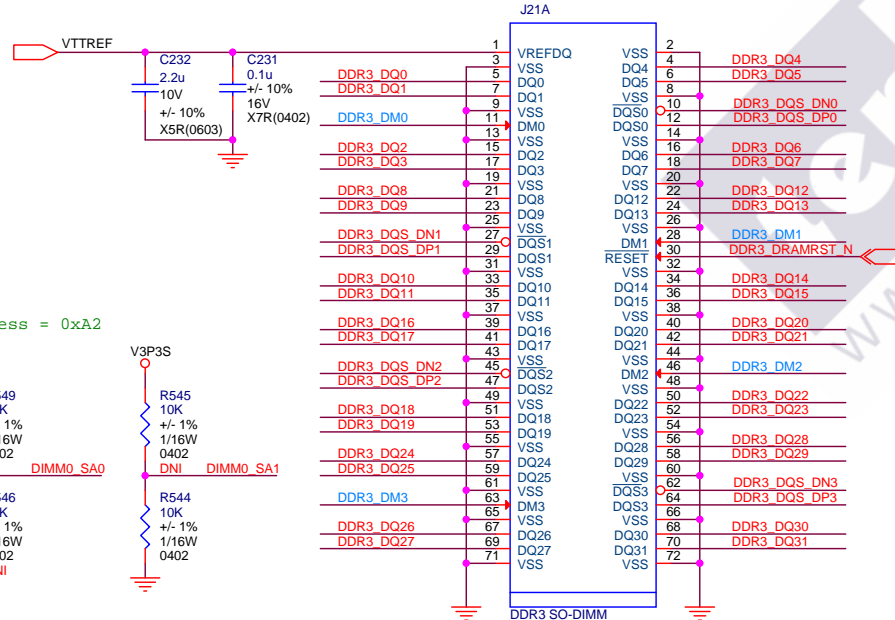
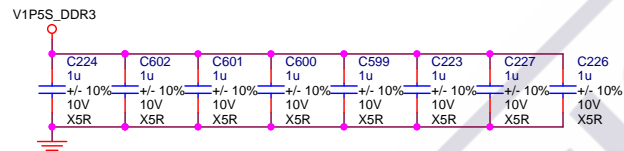
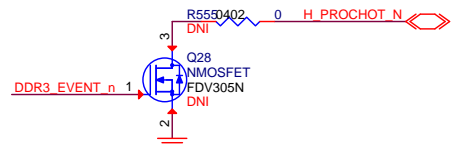
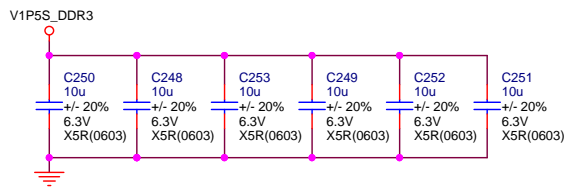
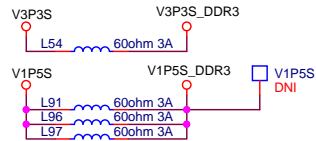
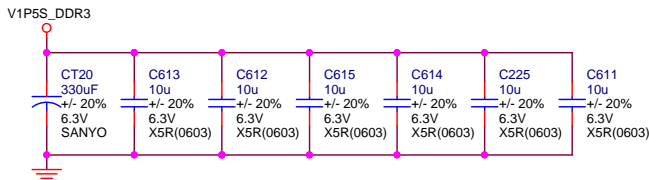
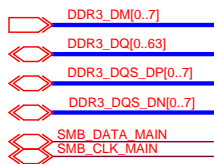


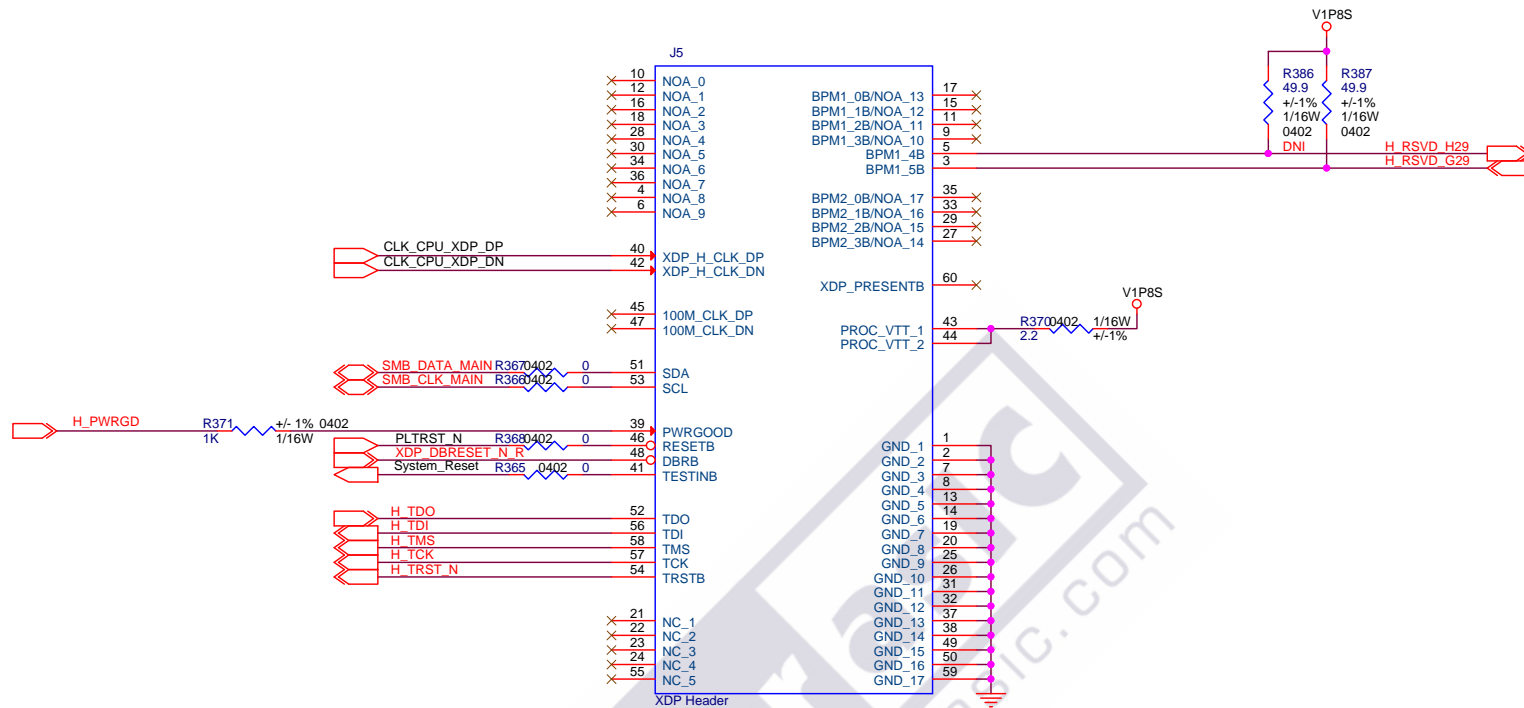
DDI Audio Interface

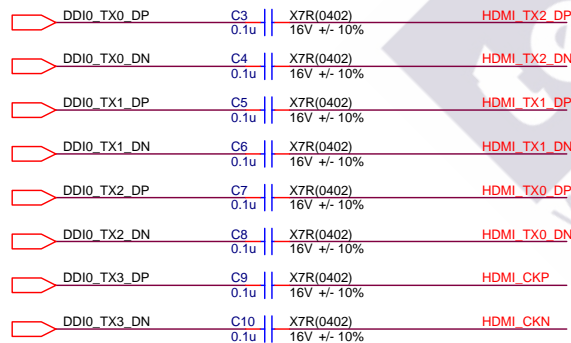
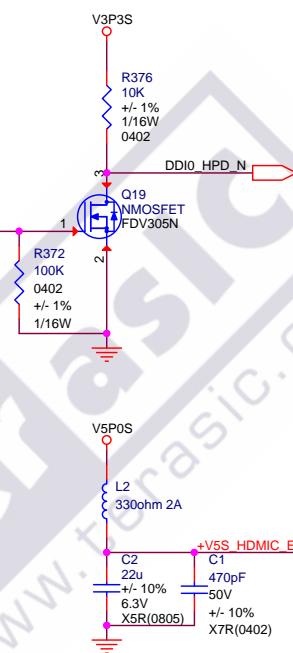




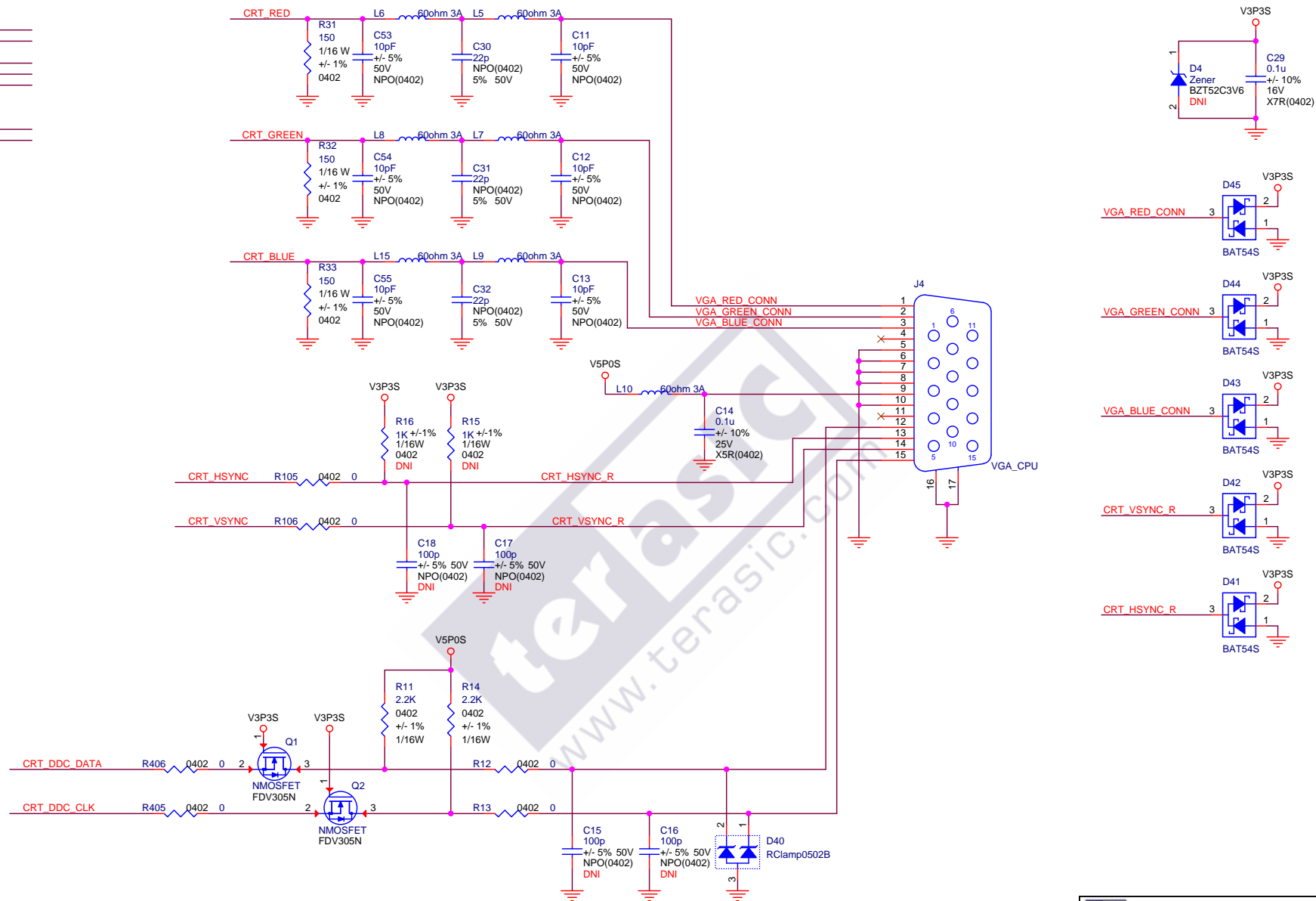
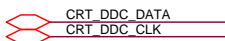
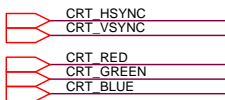




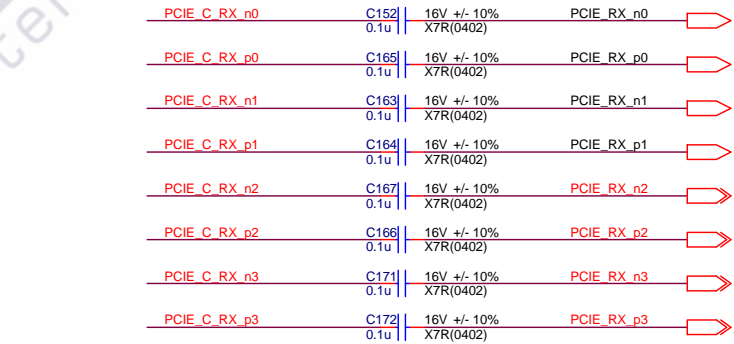
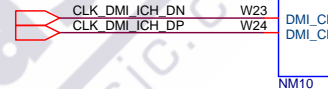
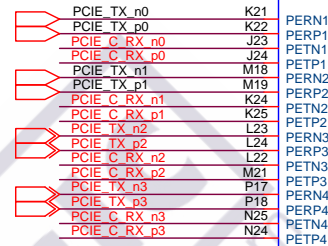
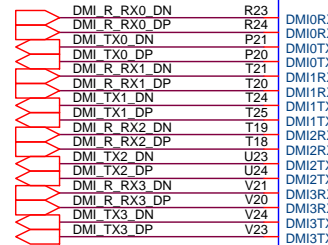
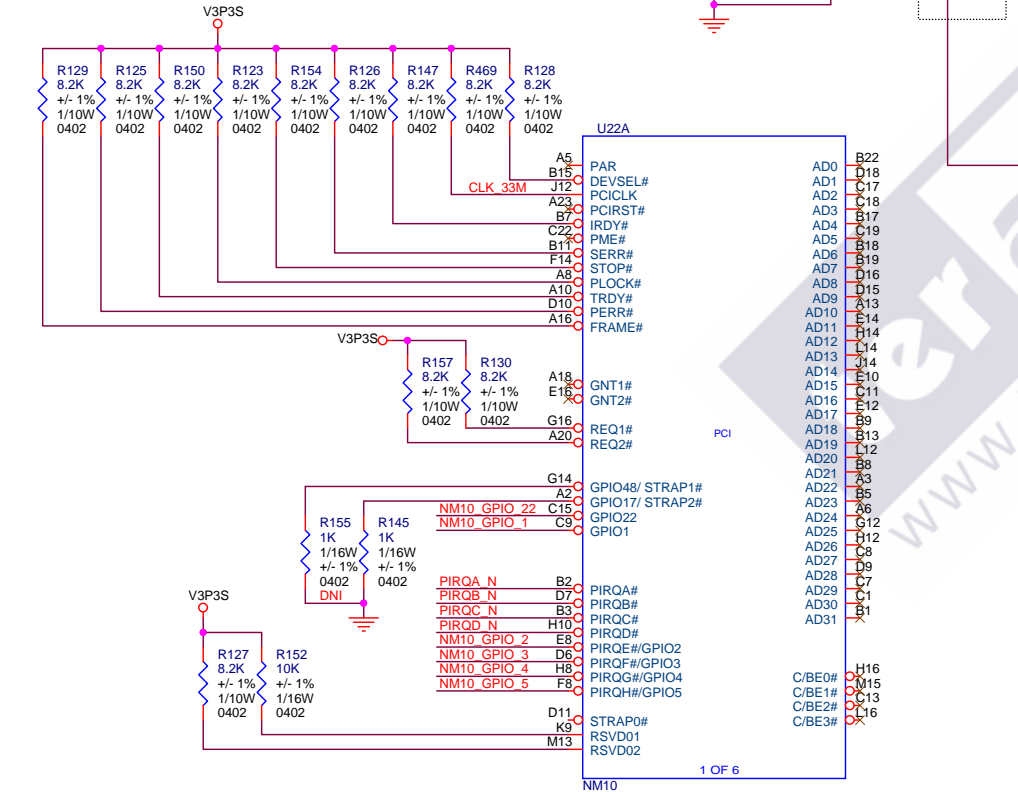
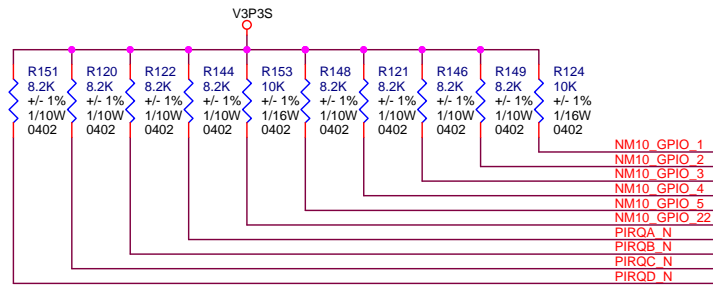


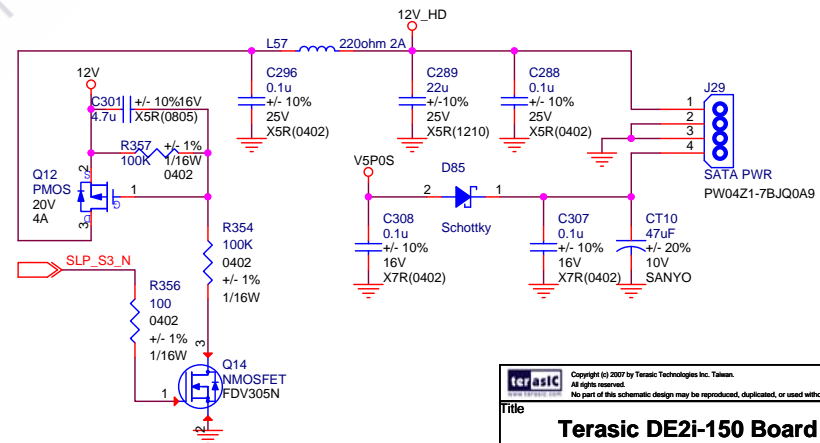
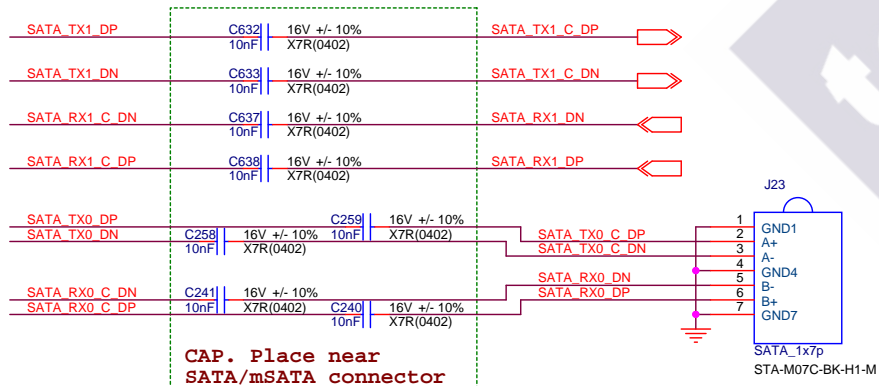
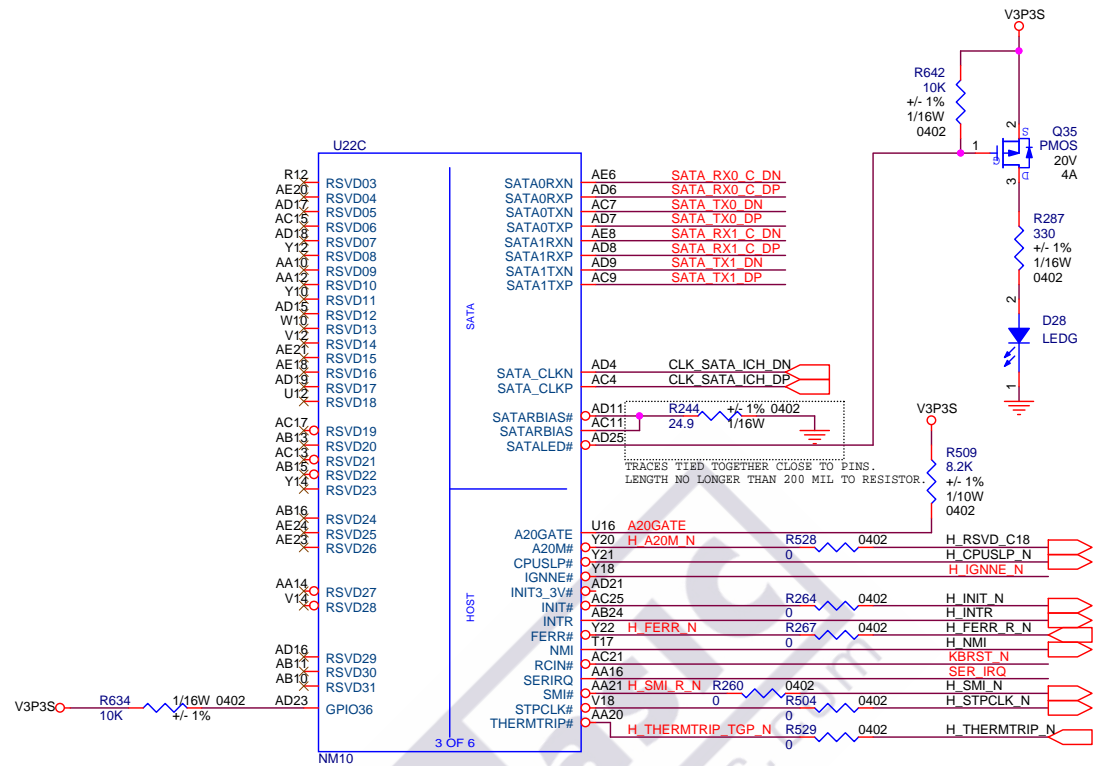


VGA Interface

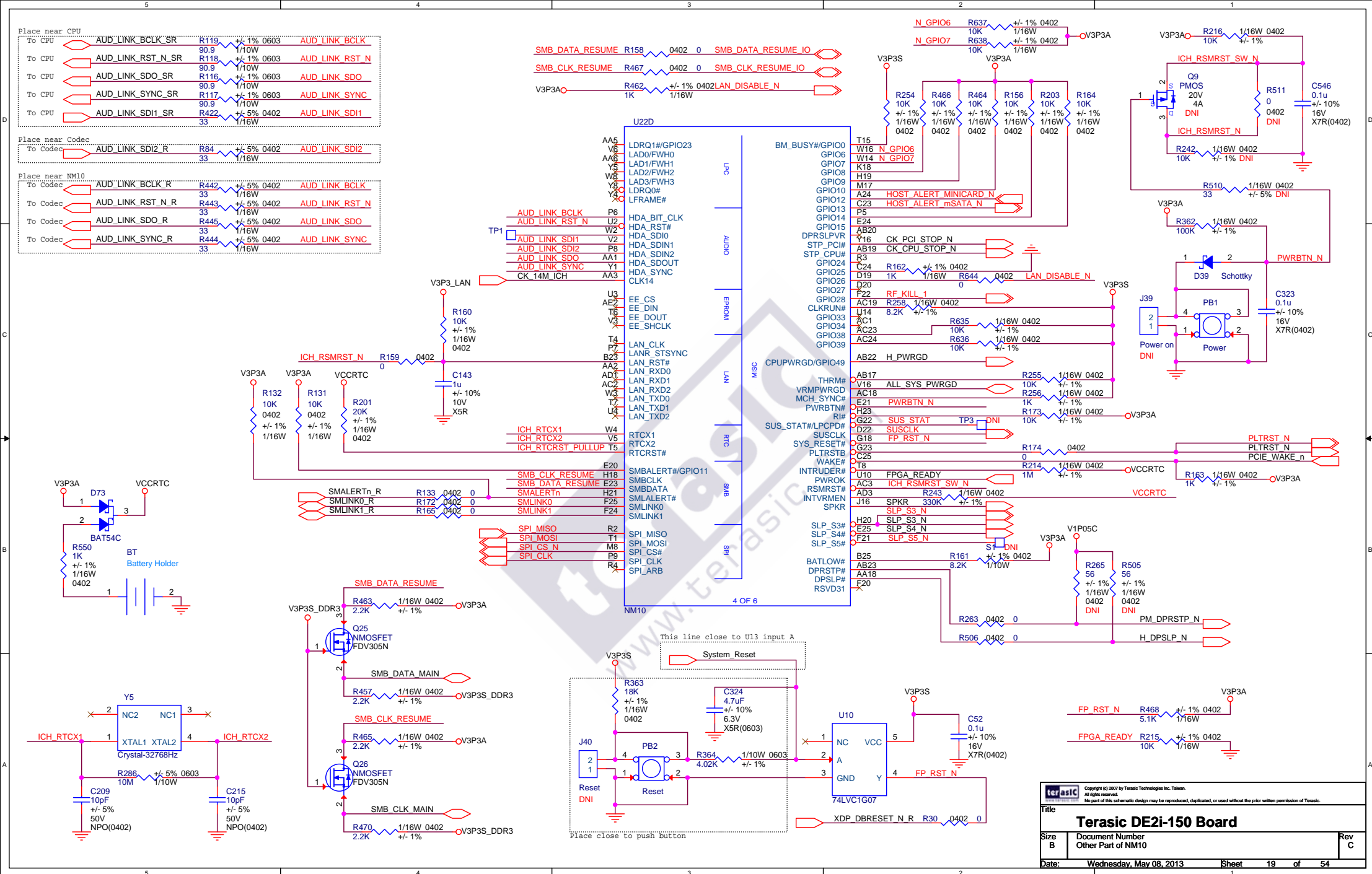


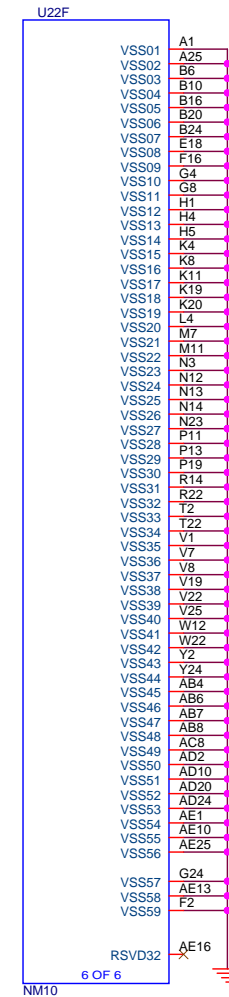
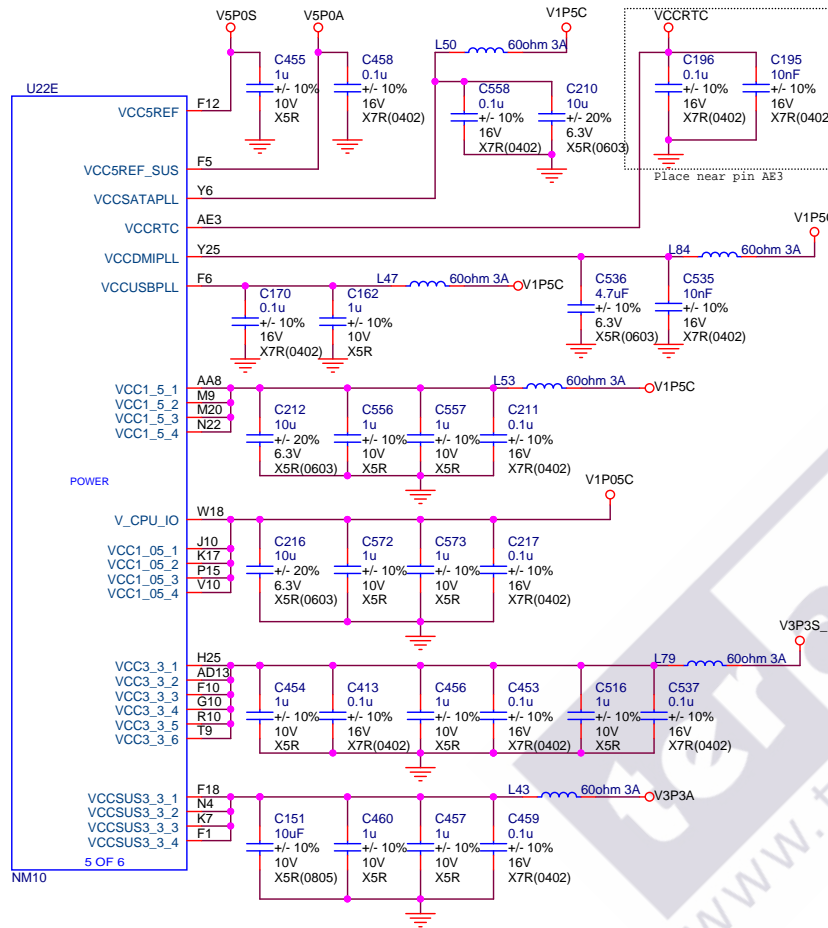
| | | |
|--|------------------------|----------------|
| <div> <div>terasic</div> <div>Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div> | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size | Document Number | Rev |
| B | VGA Part | C |
| Date: | Monday, April 01, 2013 | Sheet 16 of 54 |

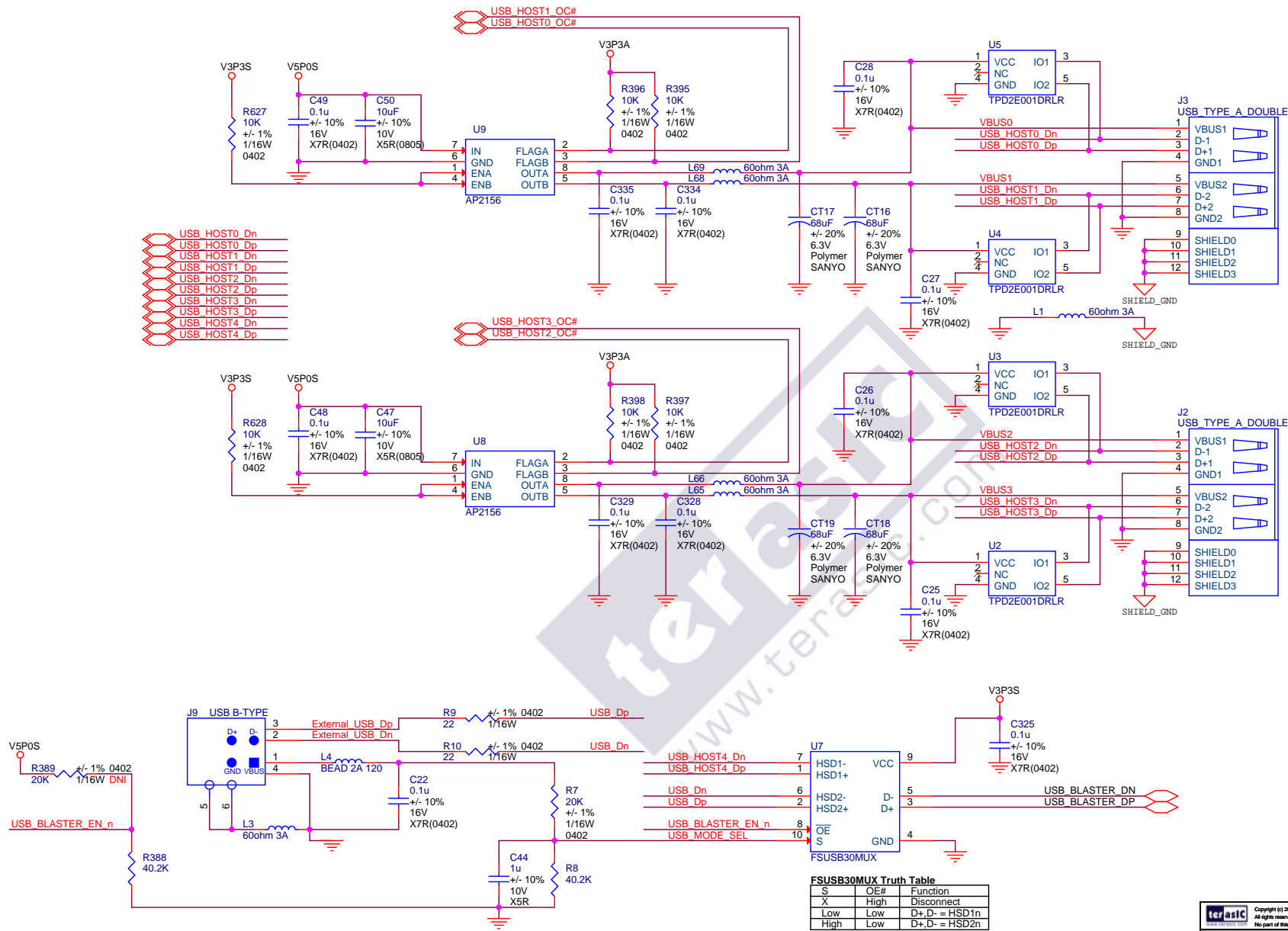




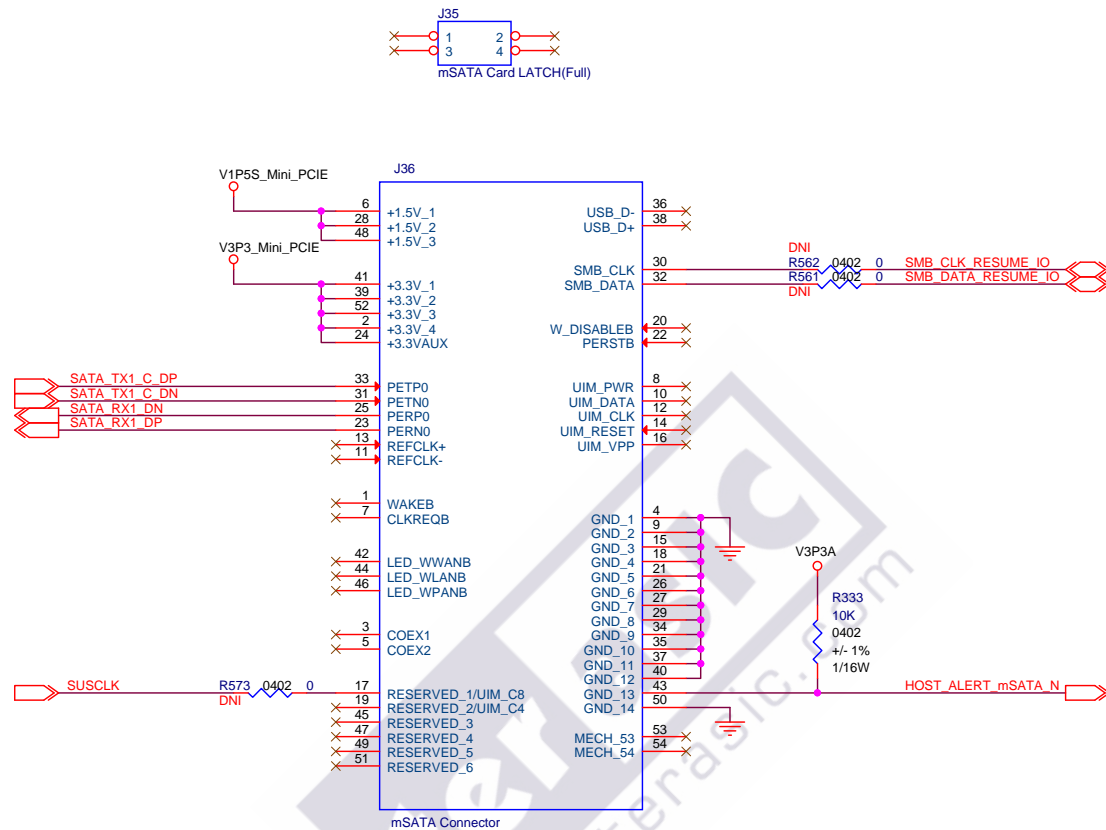
| | | |
|--|------------------------|----------------|
| Terasic Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic. | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size B | Document Number | Rev C |
| SATA Part of NM10 | | |
| Date: | Monday, April 01, 2013 | Sheet 18 of 54 |



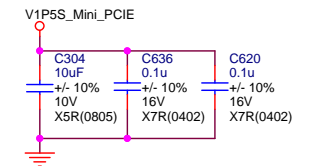
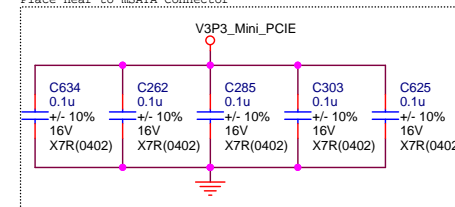




| S | OE# | Function |
|------|------|----------------|
| X | High | Disconnect |
| Low | Low | D+, D- = HSD1n |
| High | Low | D+, D- = HSD2n |

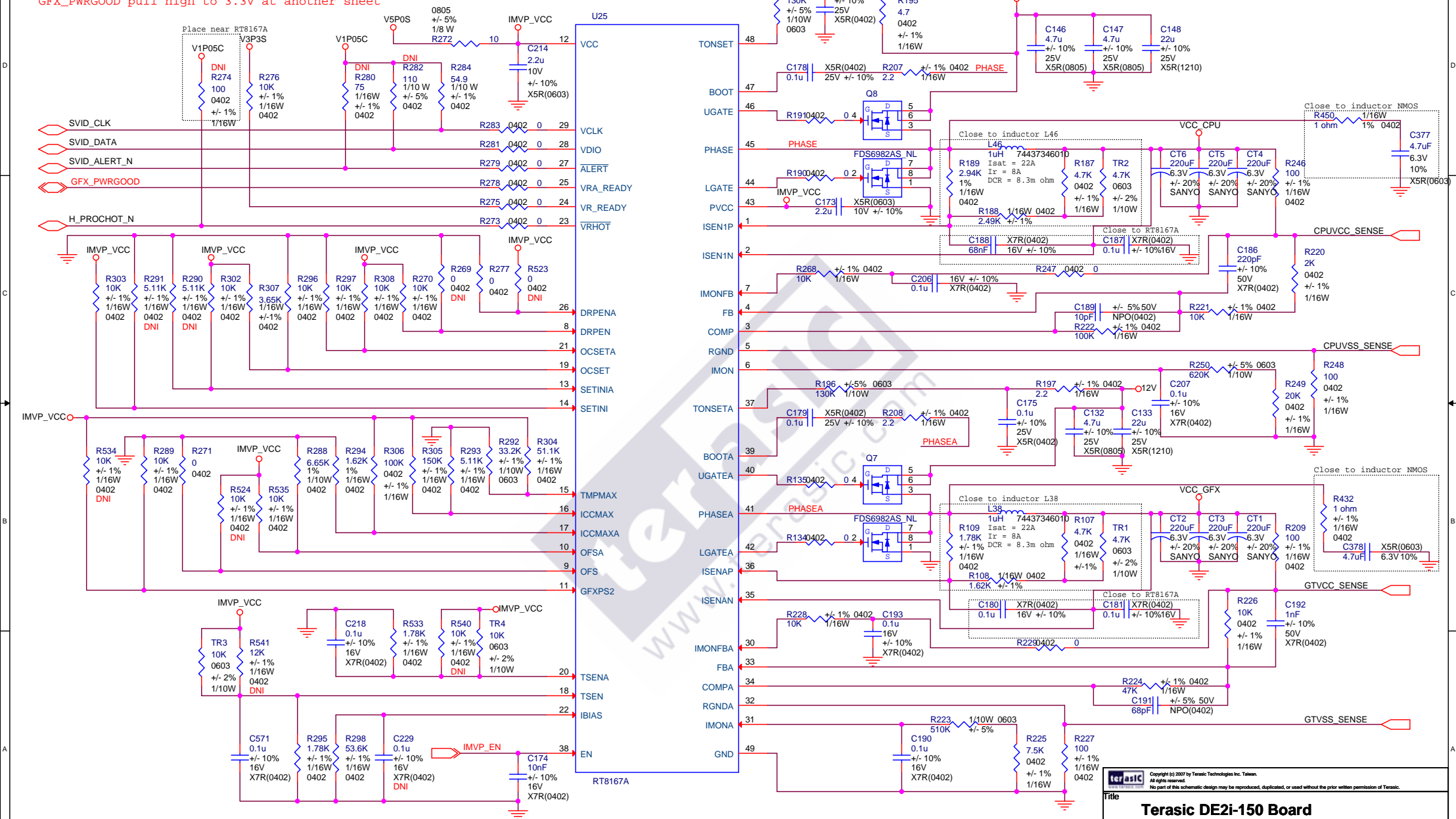


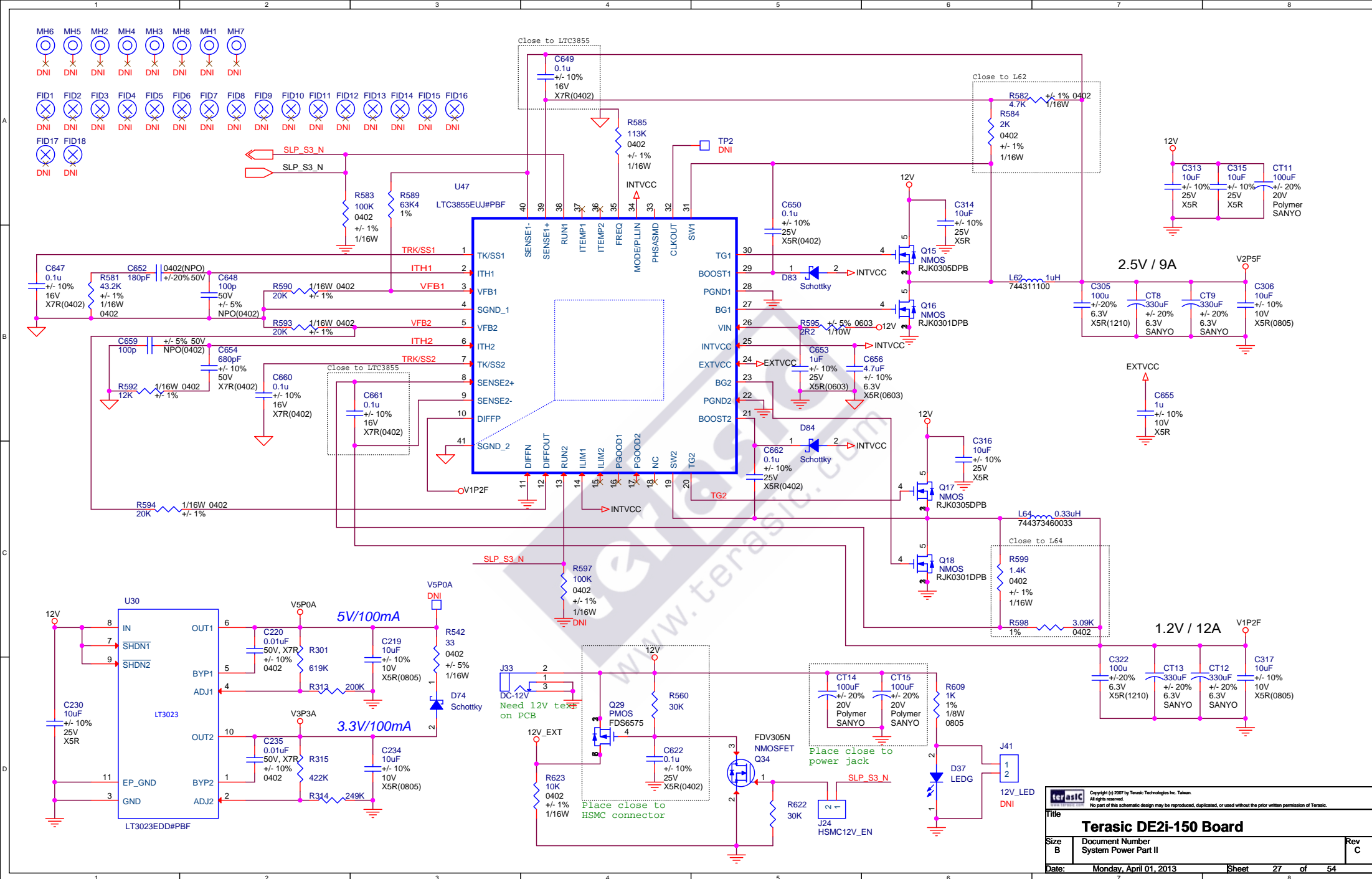
Place near to mSATA Connector

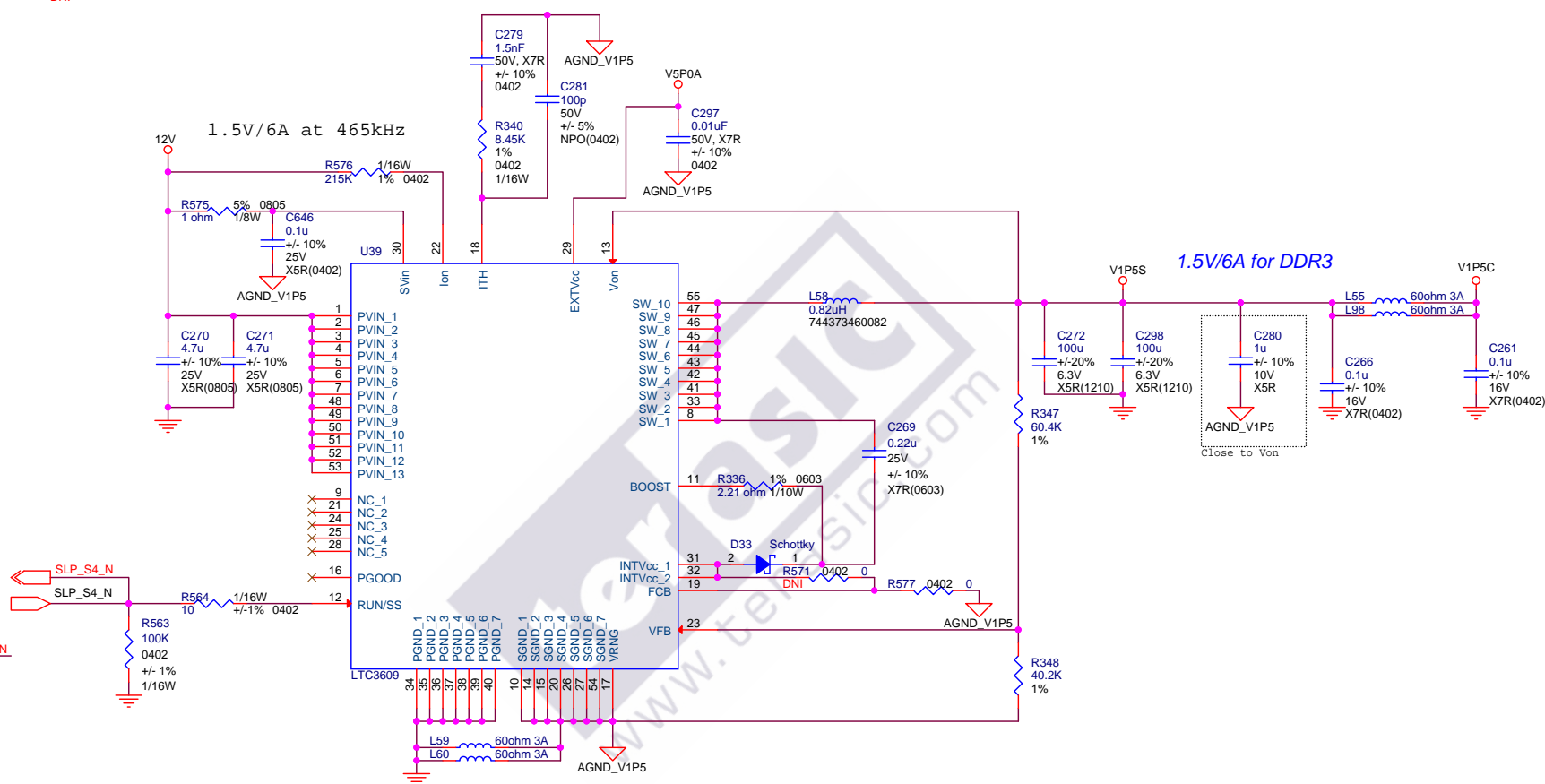


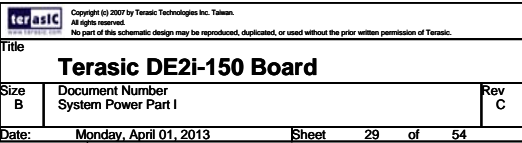
| | | |
|---|------------------------|----------------|
| Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic. | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size | Document Number | Rev |
| B | mSATA Card | C |
| Date: | Monday, April 01, 2013 | Sheet 25 of 54 |

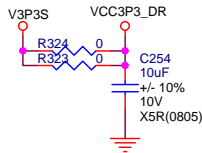
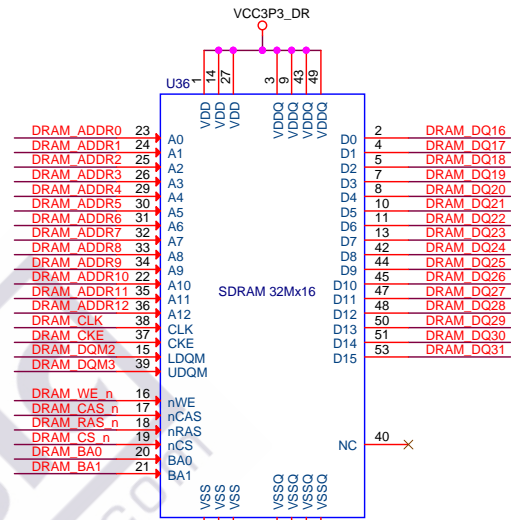
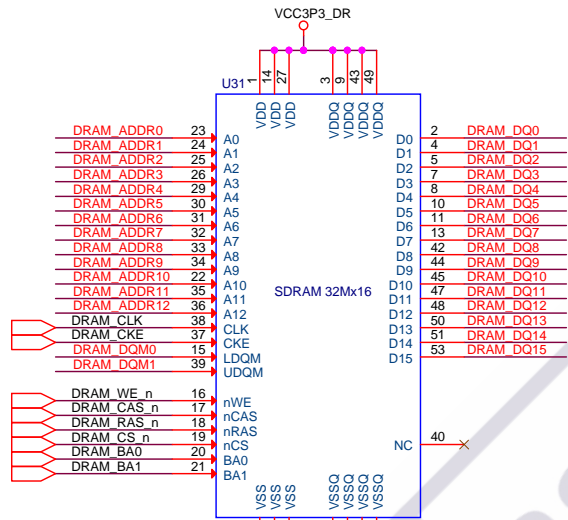
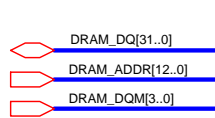
DNI : Do Not Implement (NC Component)
 TR1, TR2 : NTC Resistors (NCP18XM472J03RB)
 TR3, TR4 : NTC Resistors (NCP18XH103F03RB)
 GFX_PWRGOOD pull high to 3.3V at another sheet





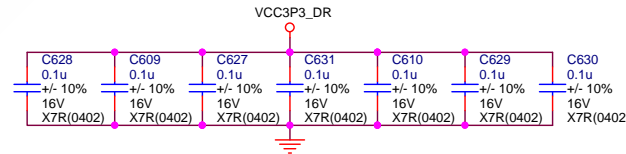
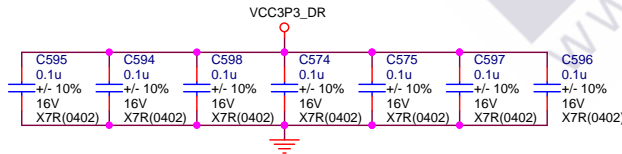
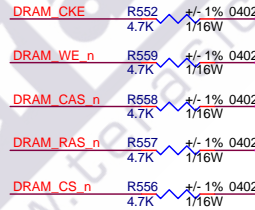


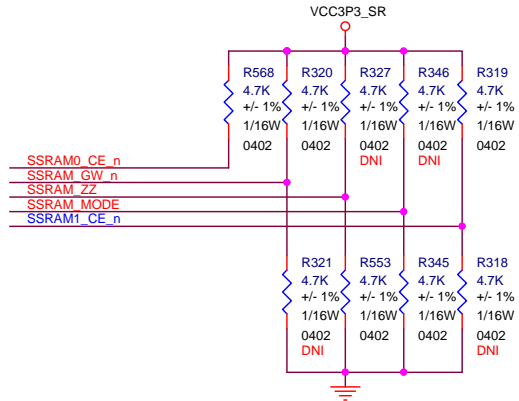
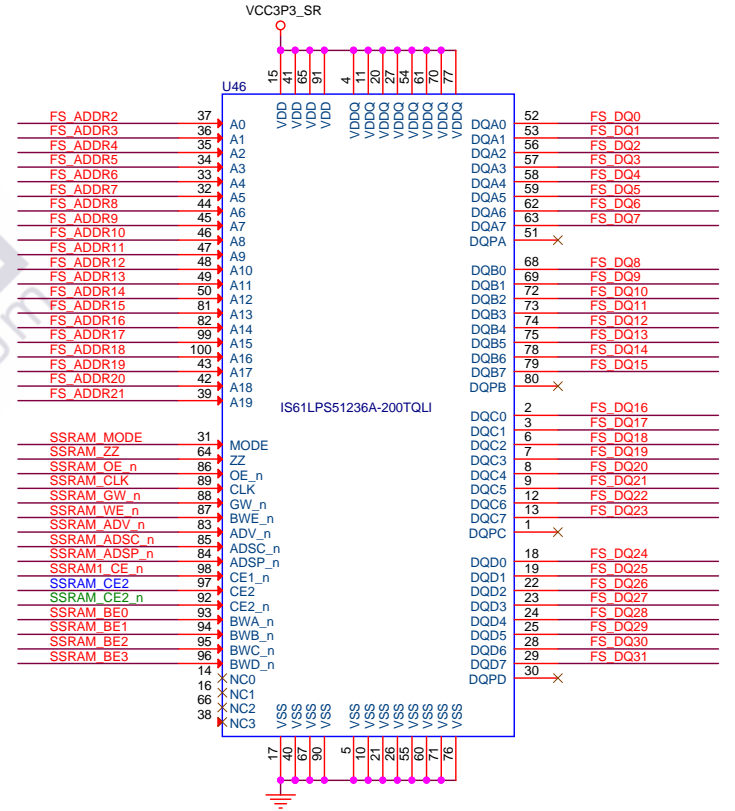
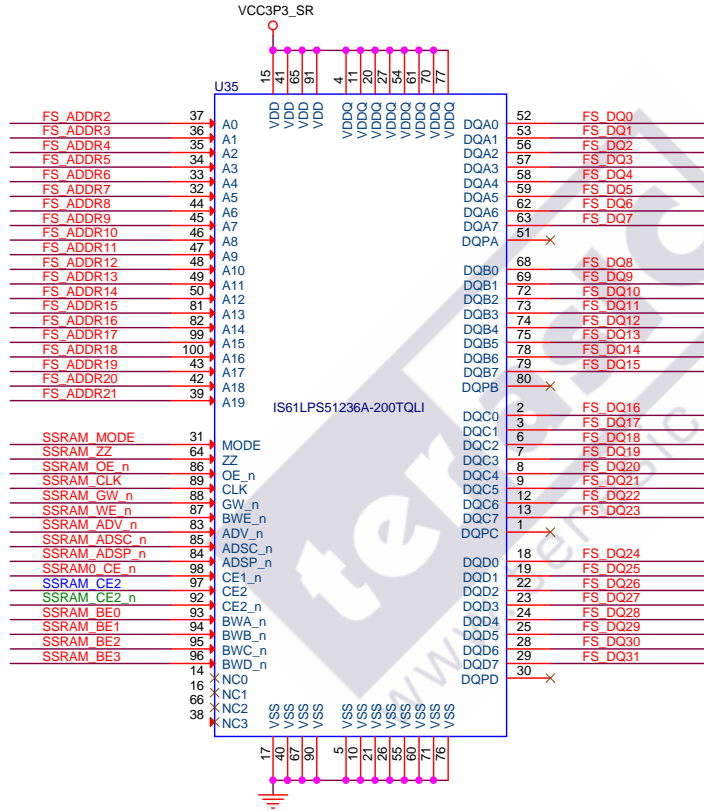
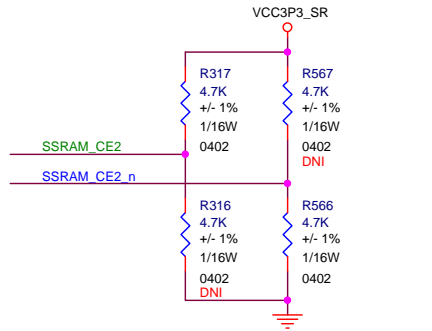
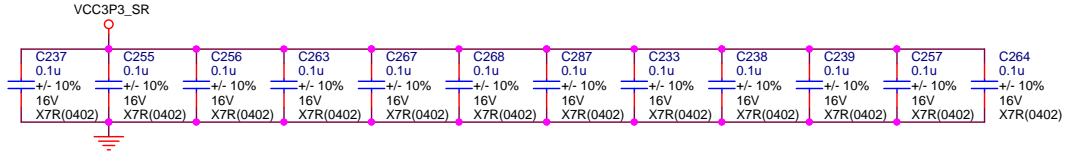
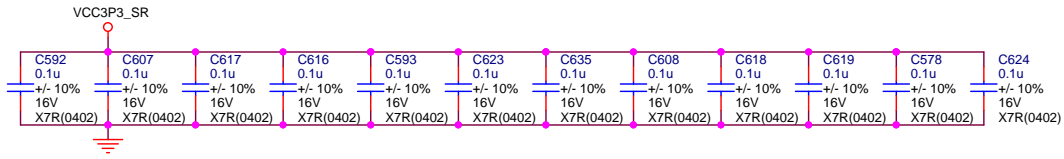
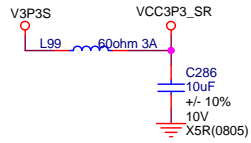
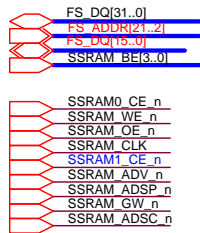




SDRAM 0

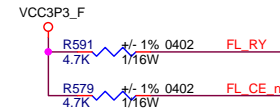
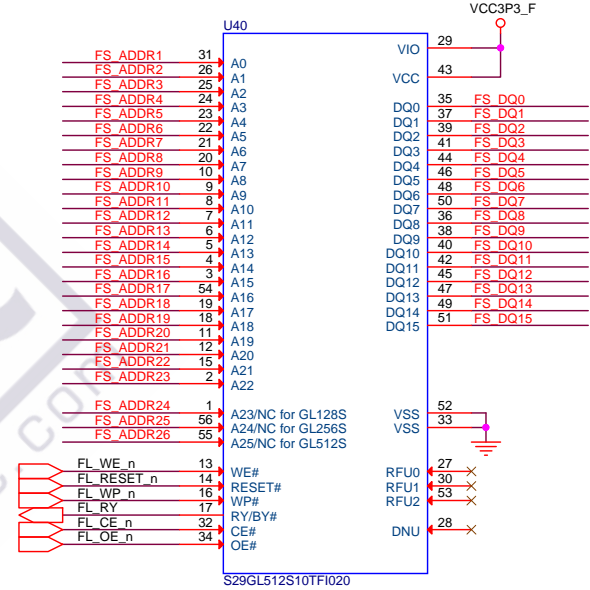
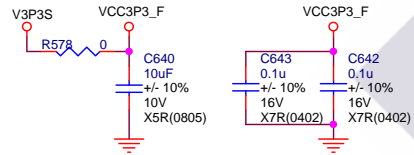
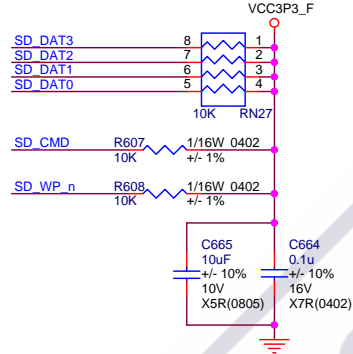
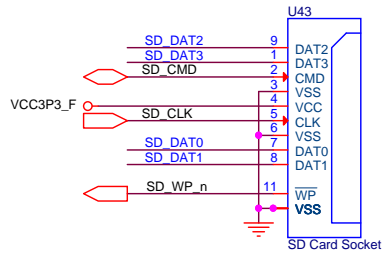
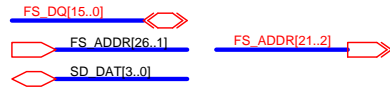
SDRAM 1

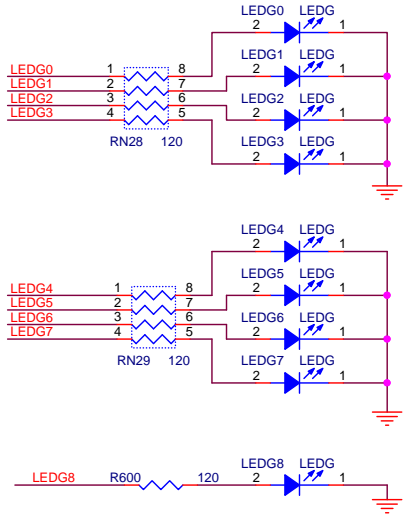
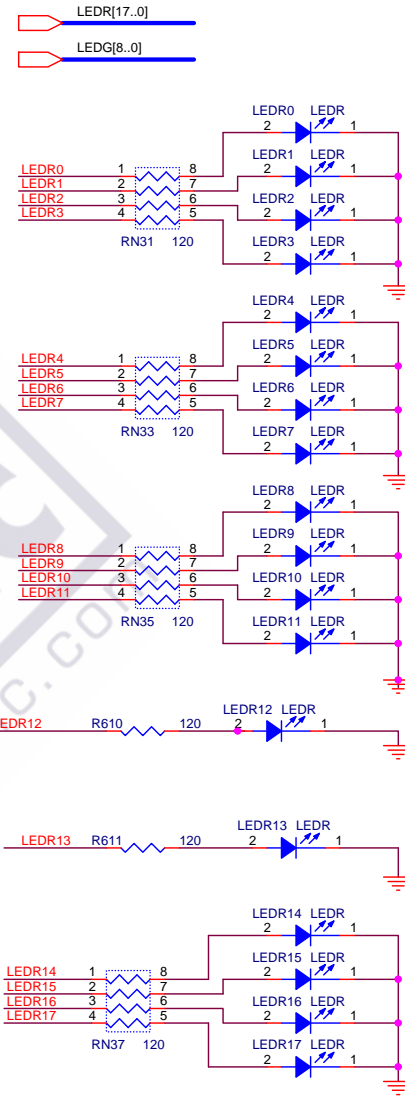
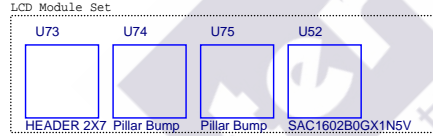
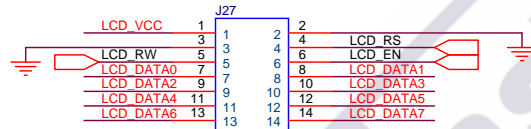
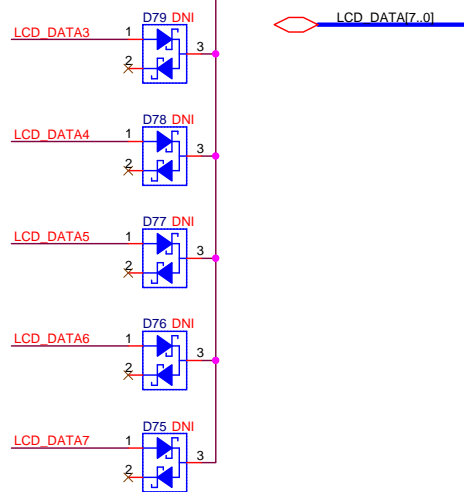
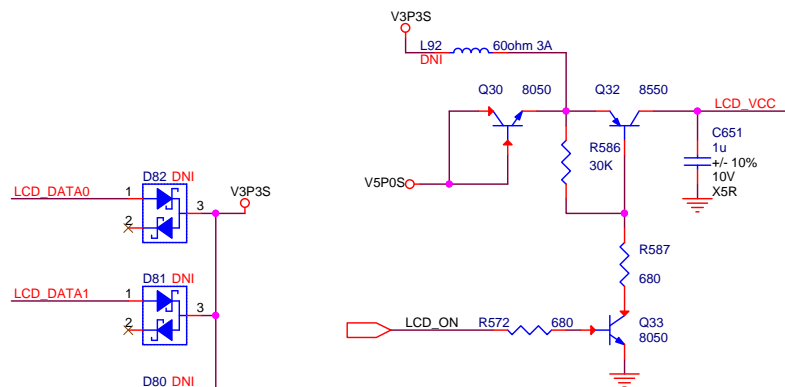


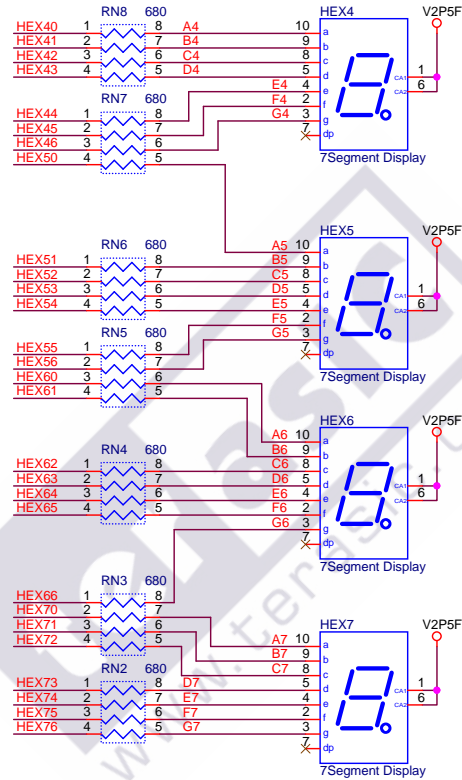
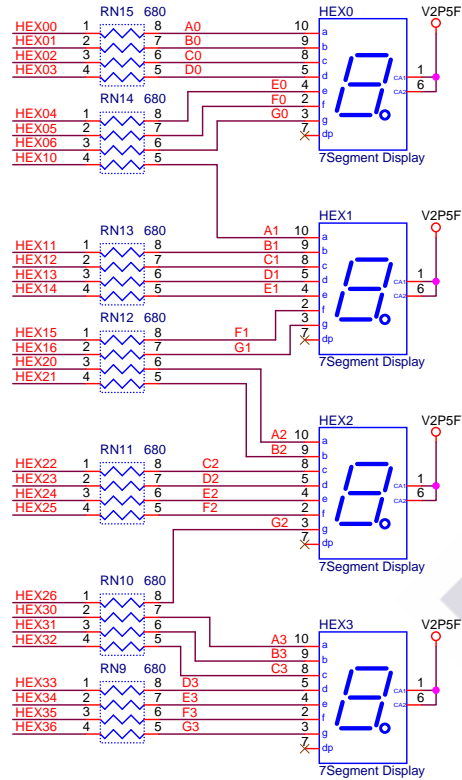
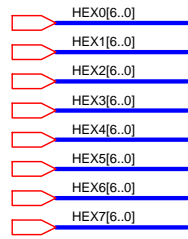


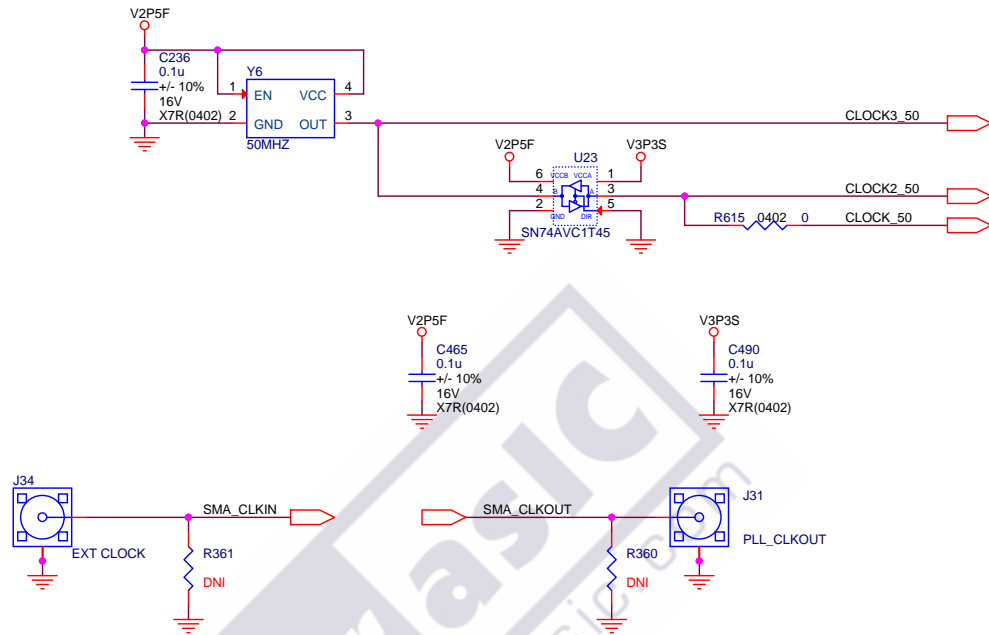
SSRAM 0


SSRAM 1

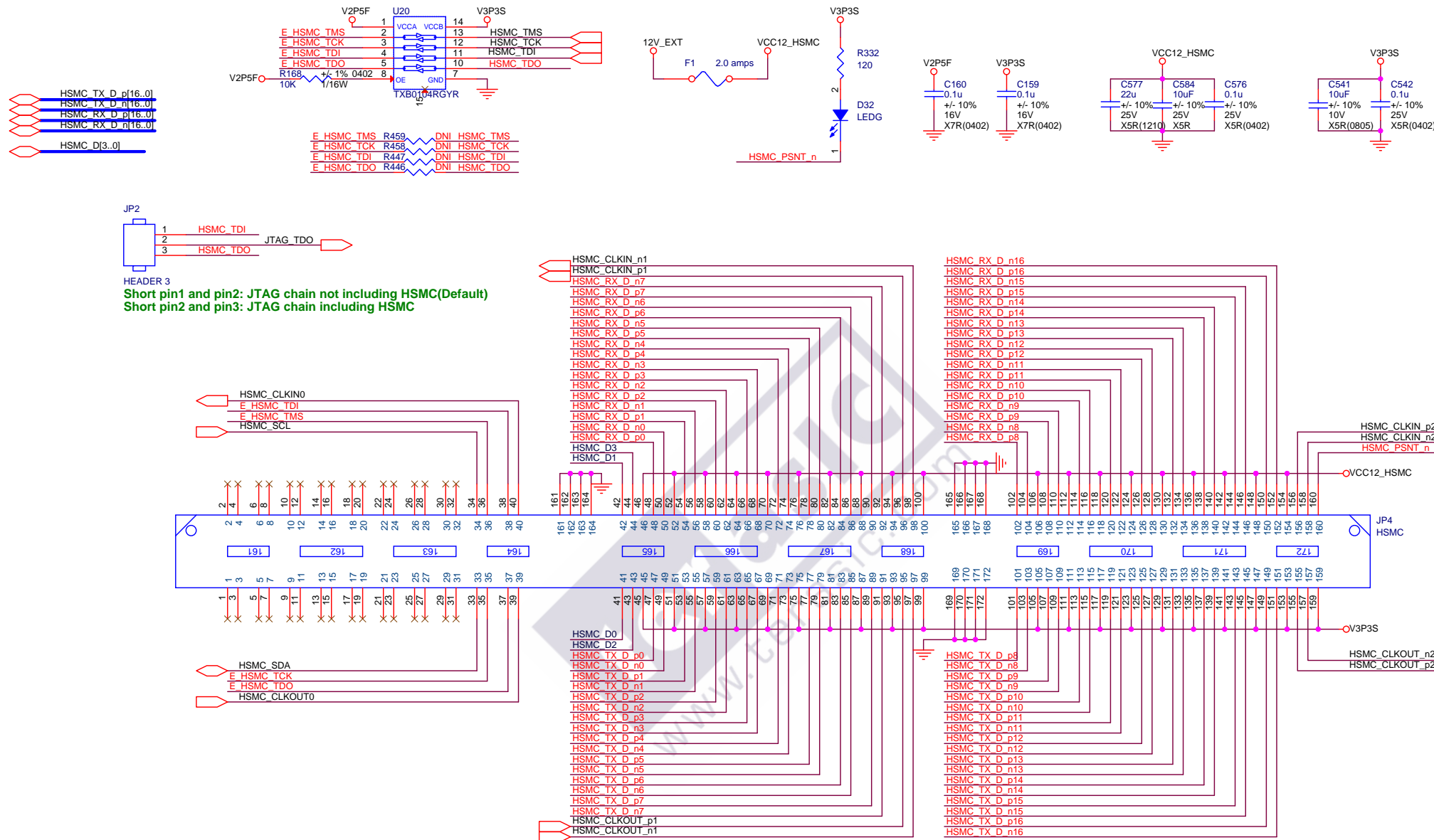


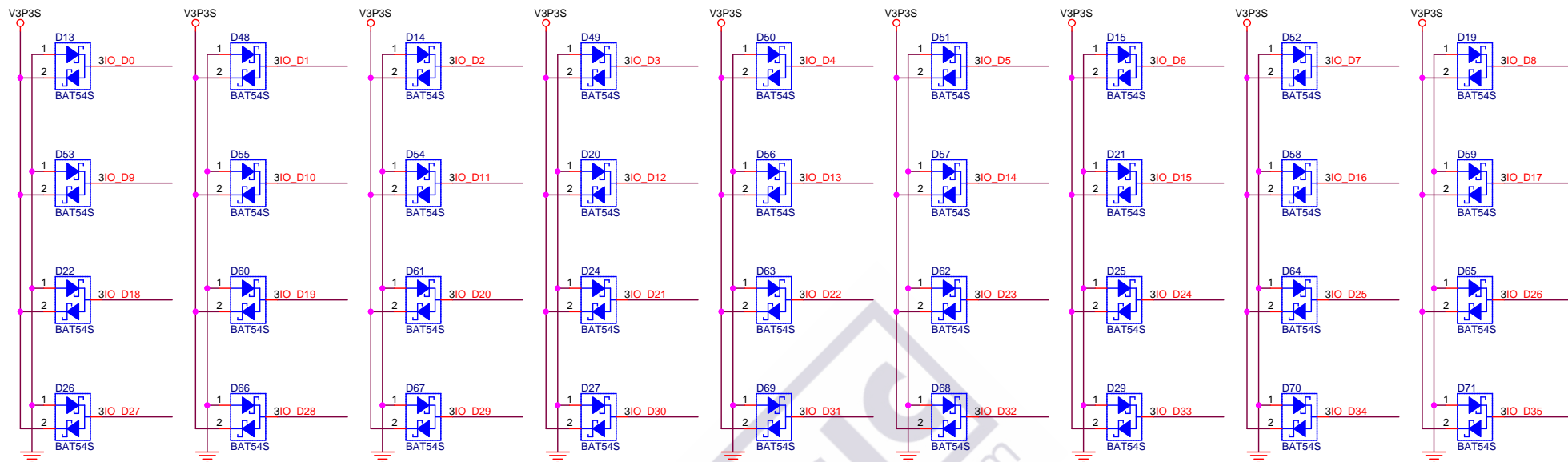




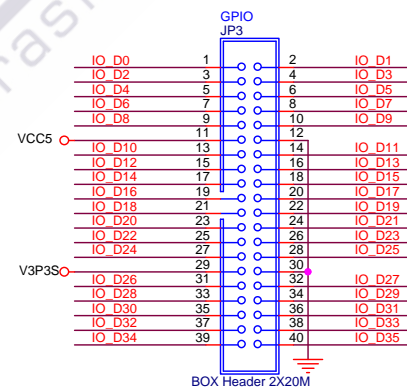
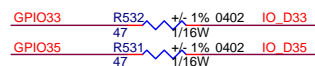
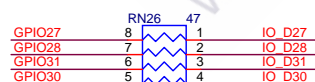
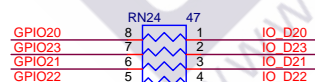
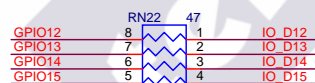
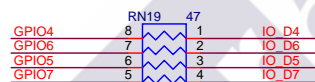
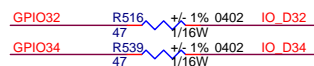
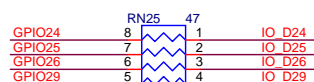
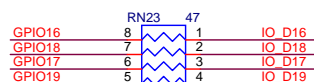
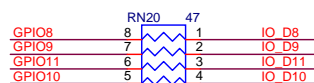
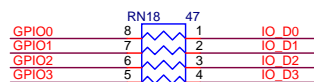


| | | |
|--|------------------------|----------------|
|  <small>Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</small> | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size | Document Number | Rev |
| B | Clock & SMA of FPGA | C |
| Date: | Monday, April 01, 2013 | Sheet 36 of 54 |

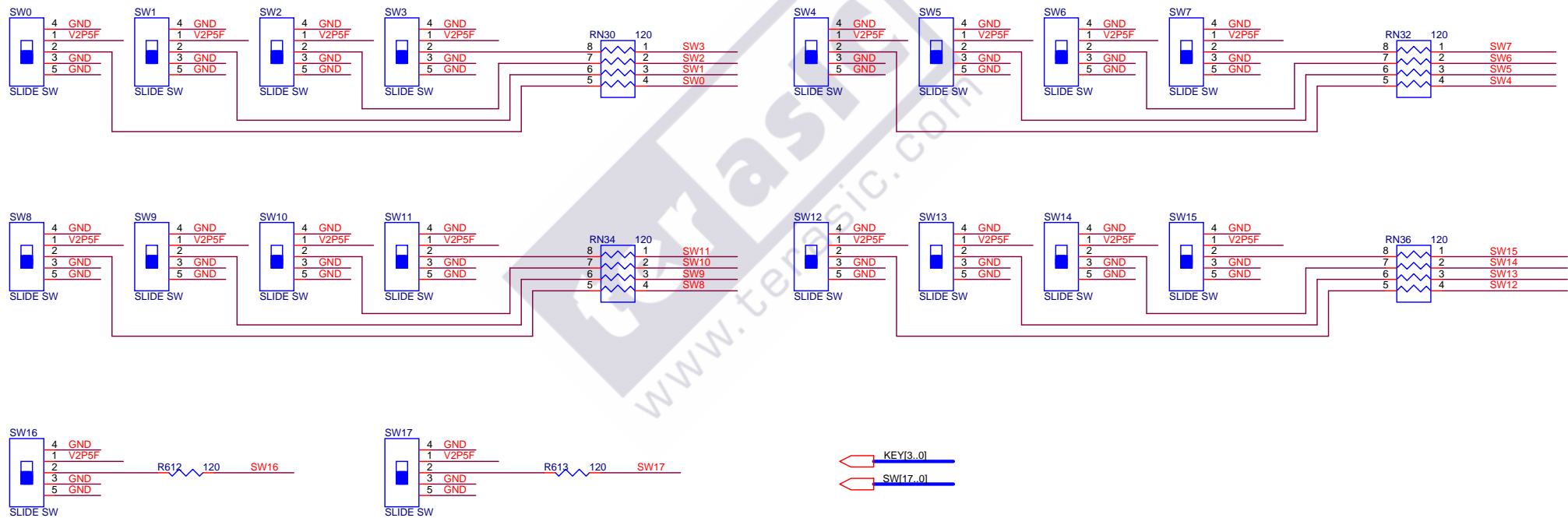


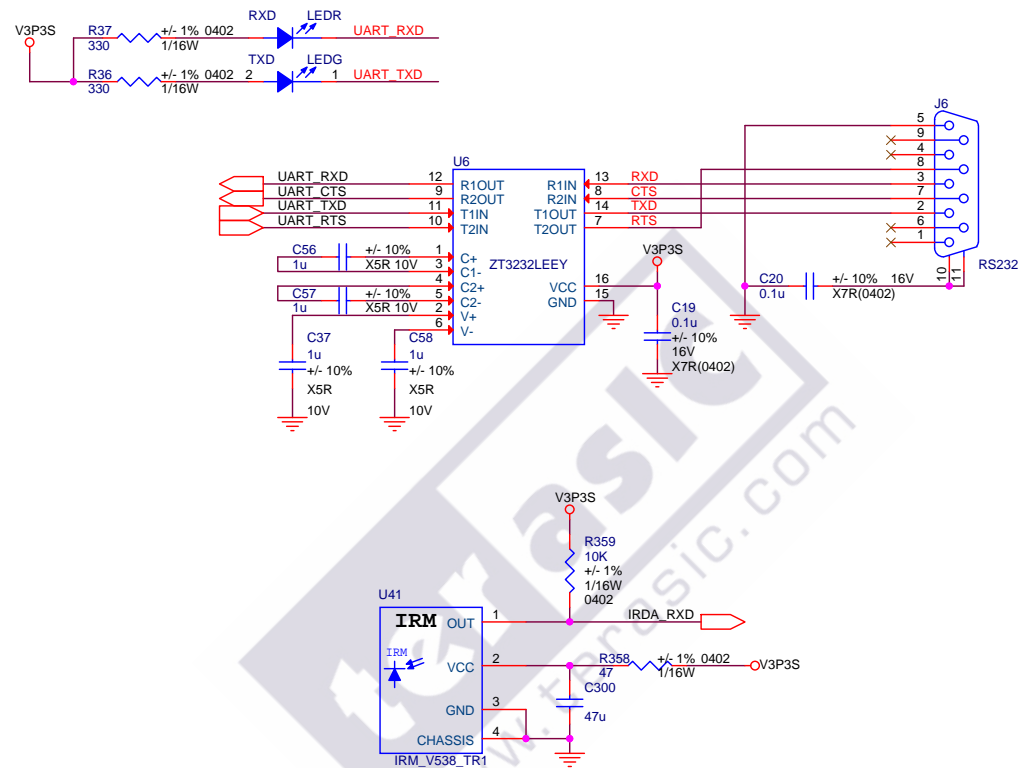



GPIO[35..0]

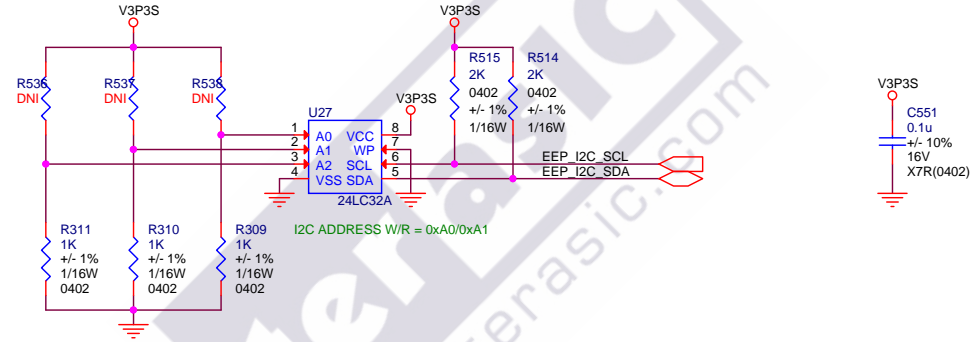



all the resistors close to GPIO connector

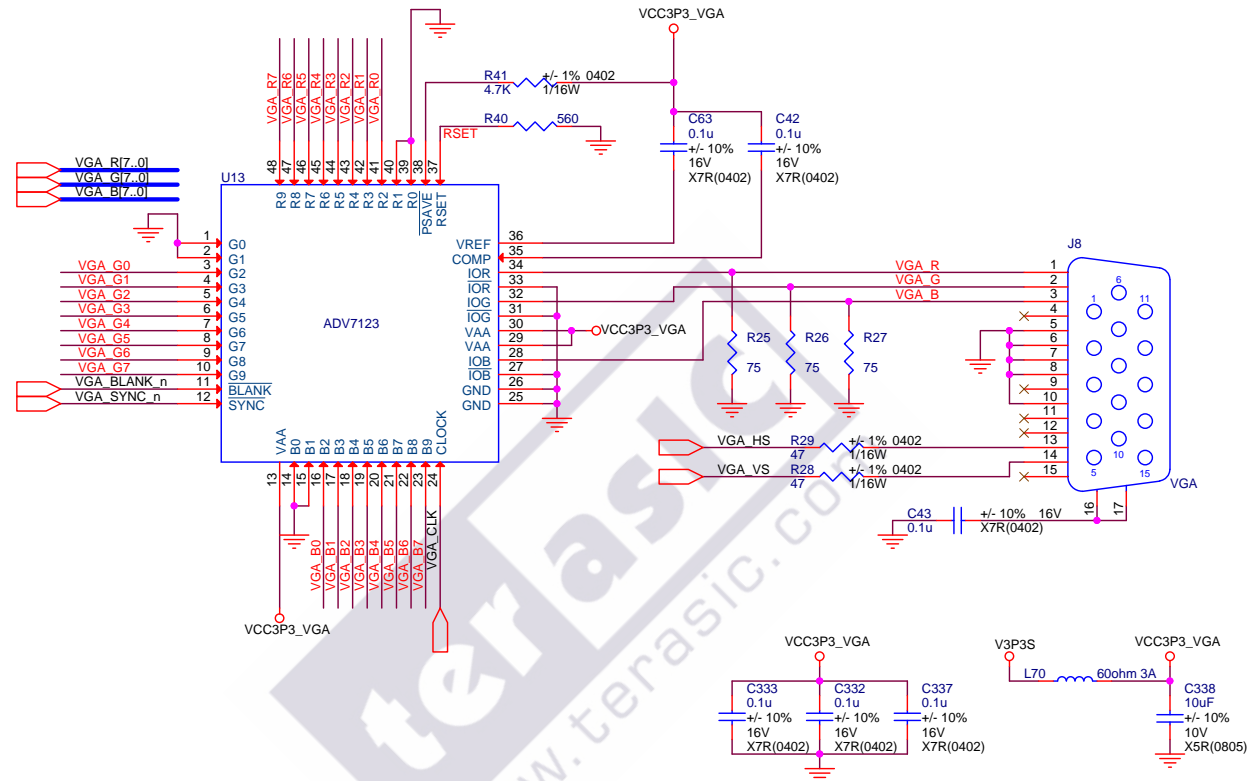


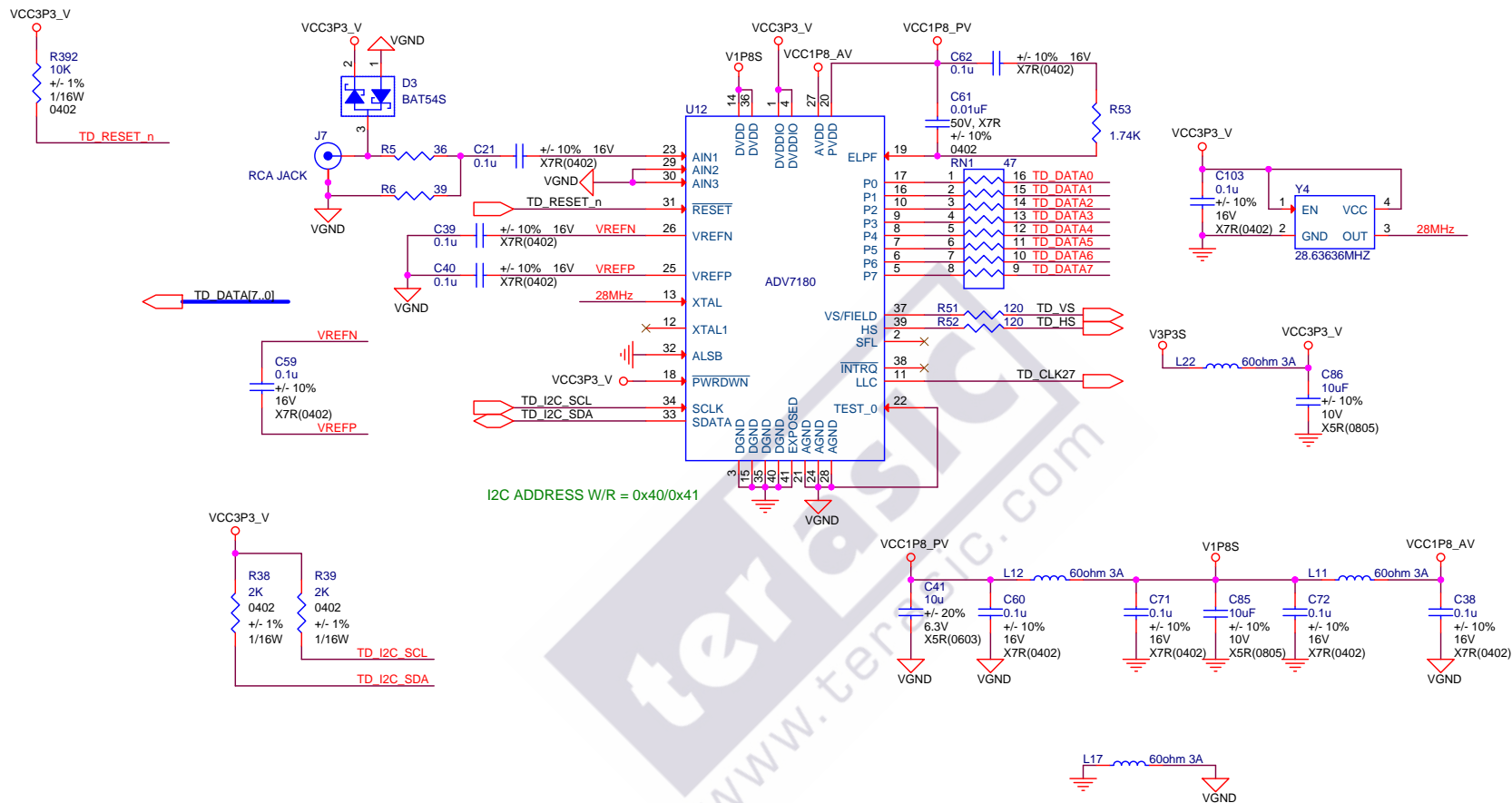


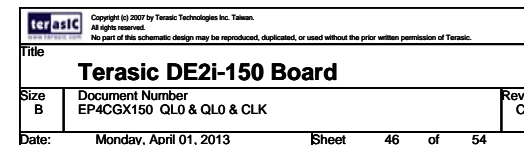
| | | |
|---|------------------------|----------------|
|  Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic. | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size | Document Number | Rev |
| B | RS232 & IRM of FPGA | C |
| Date: | Monday, April 01, 2013 | Sheet 40 of 54 |

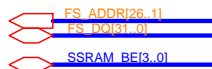
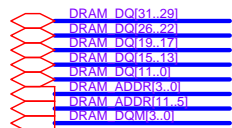


| | | |
|--|-----------------------------------|----------------|
|  <small>Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</small> | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size B | Document Number EEPROM of FPGA | Rev C |
| Date: | Monday, April 01, 2013 | Sheet 41 of 54 |

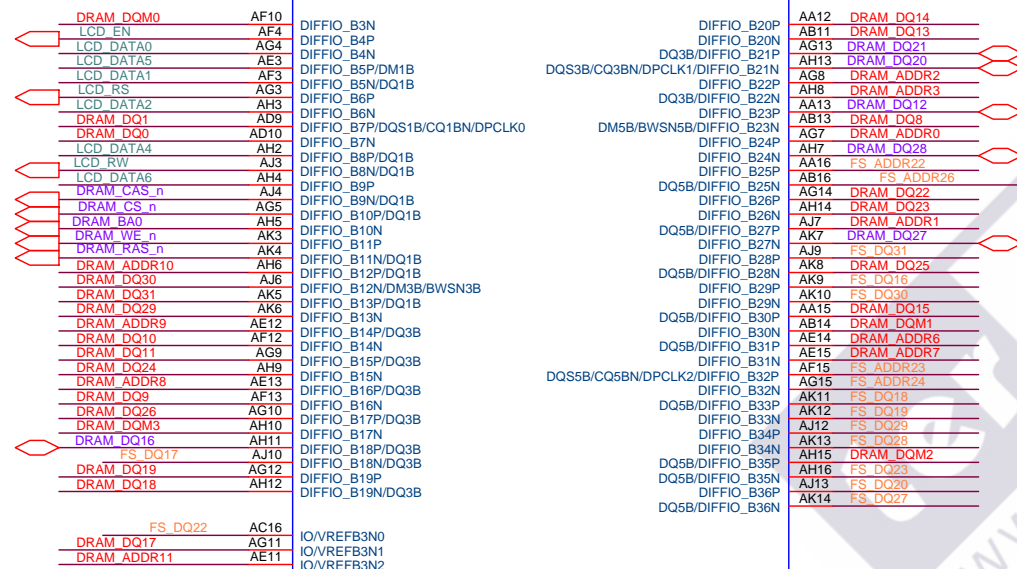






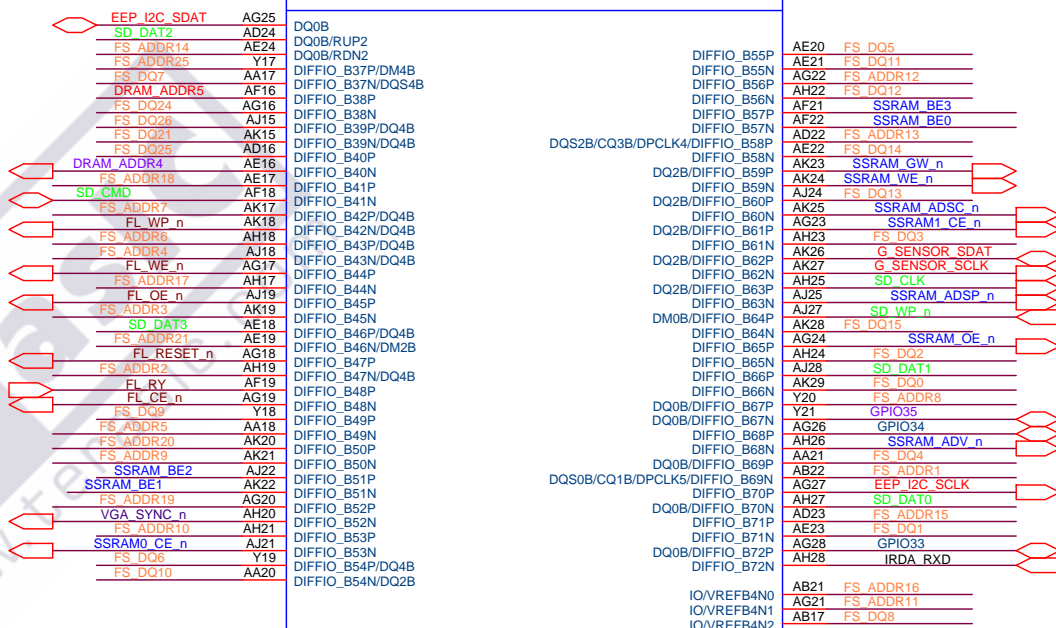


BANK 3

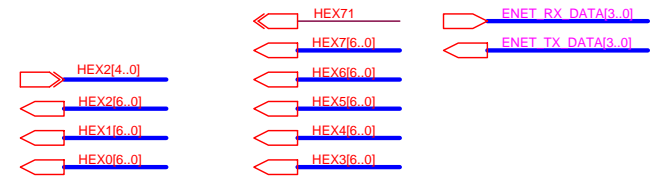
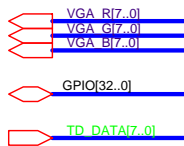


EP4CGX150DF896
Version = 0.1 Preliminary

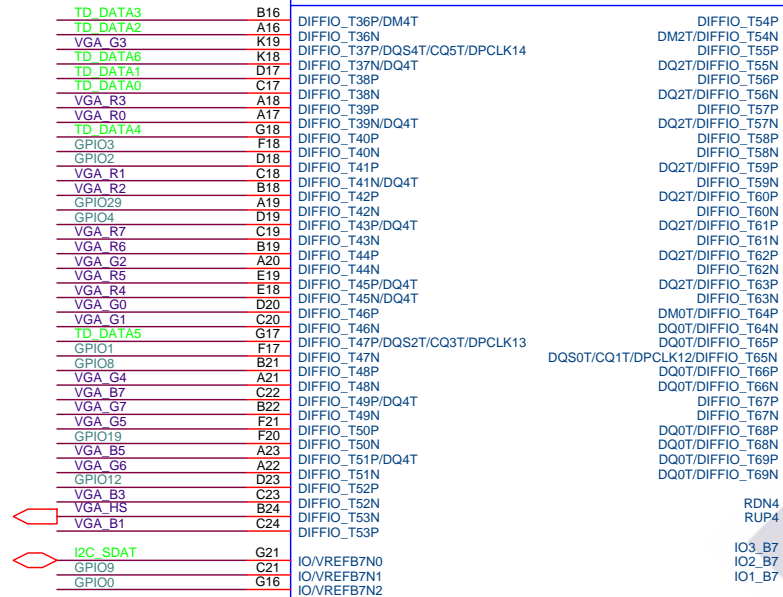
BANK 4



EP4CGX150DF896
Version = 0.1 Preliminary

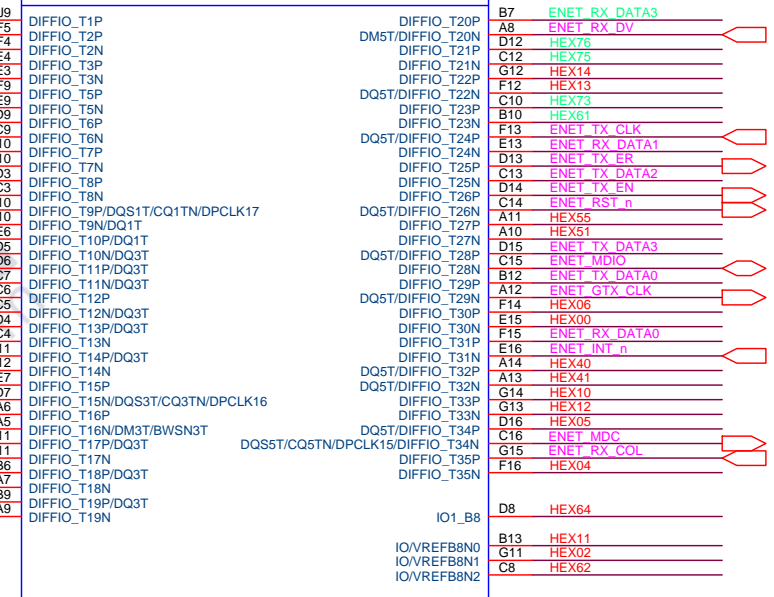


BANK 7



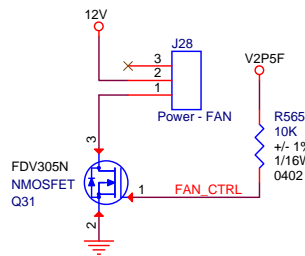
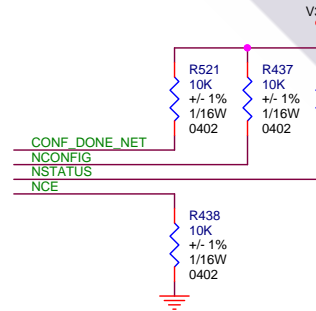
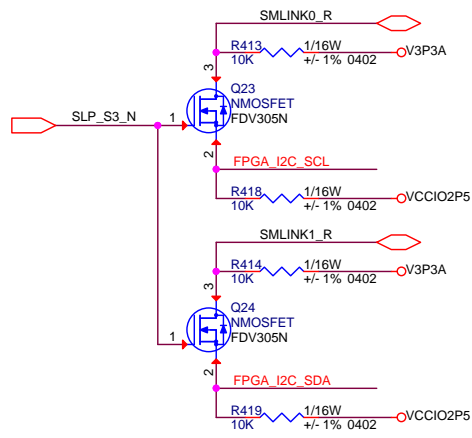
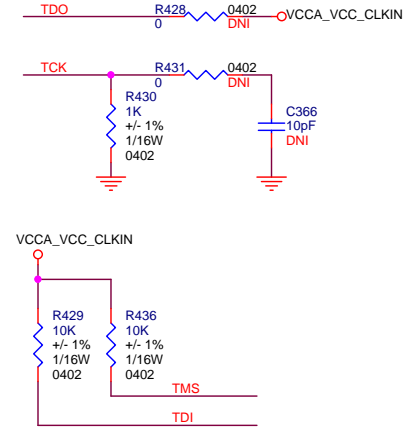
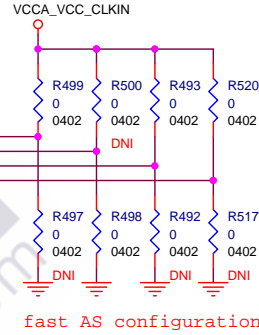
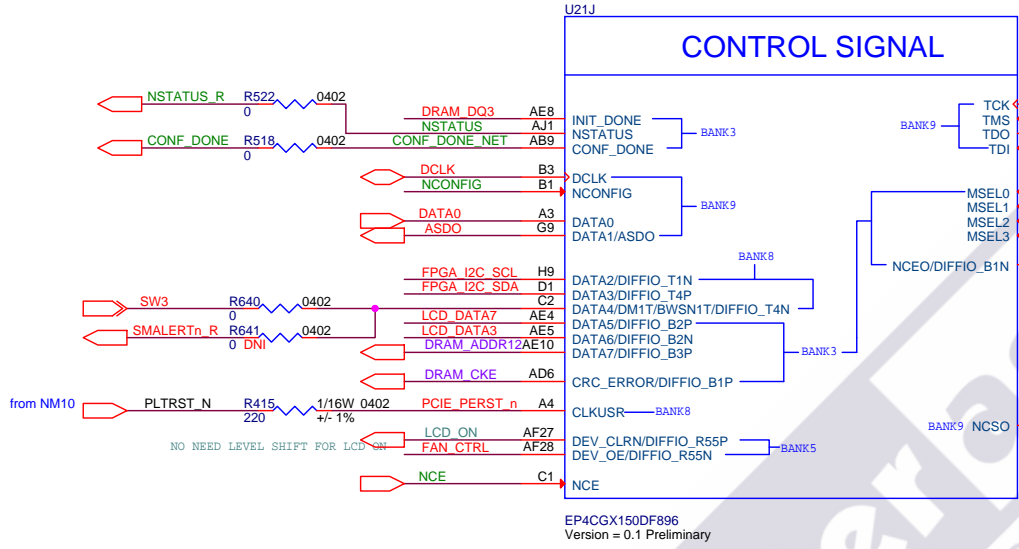
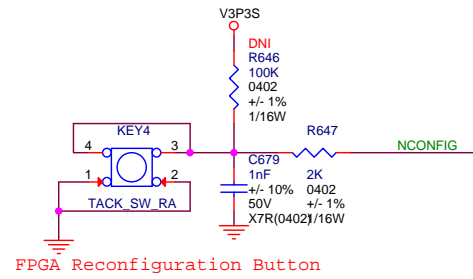
EP4CGX150DF896
Version = 0.1 Preliminary

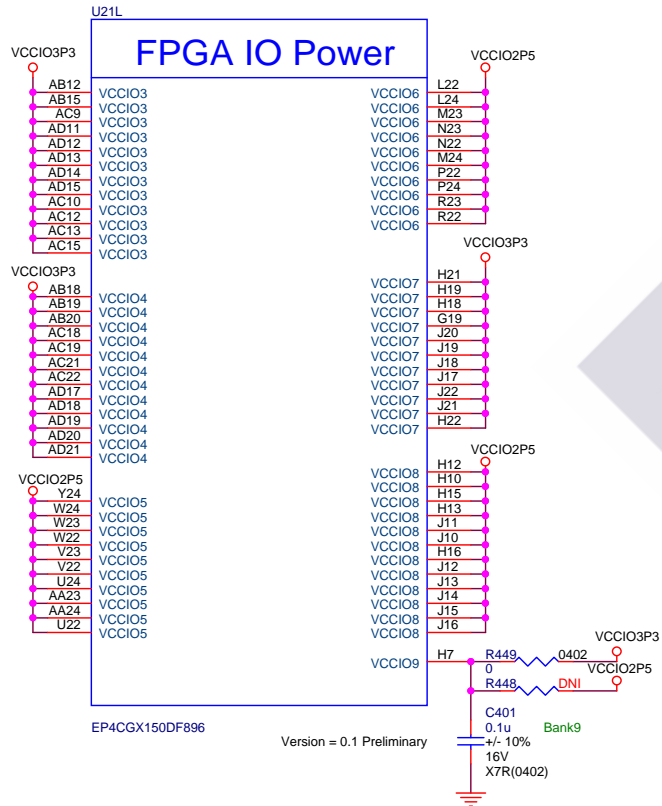
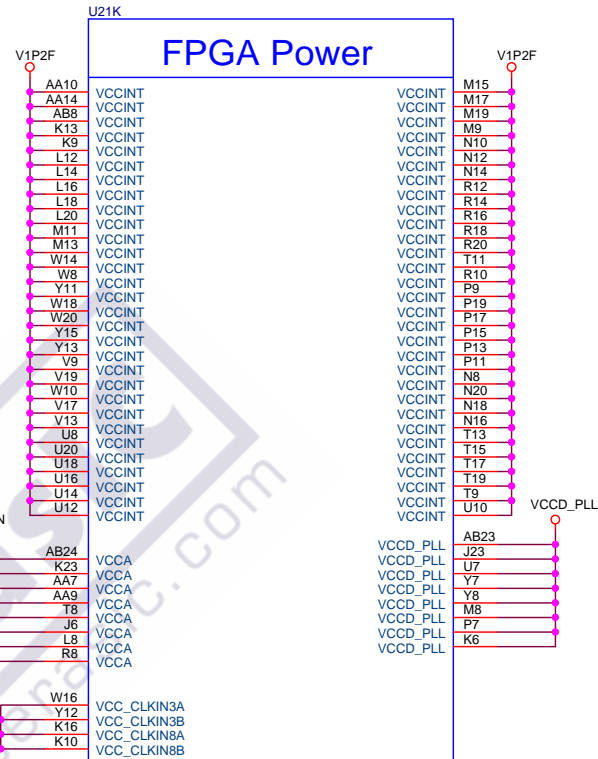
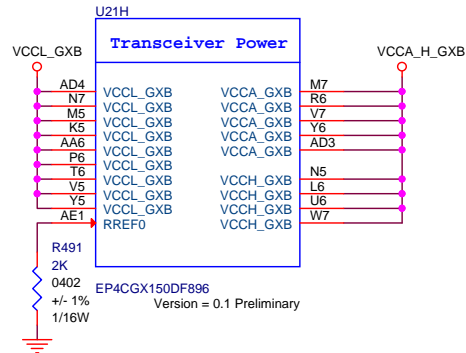
BANK 8

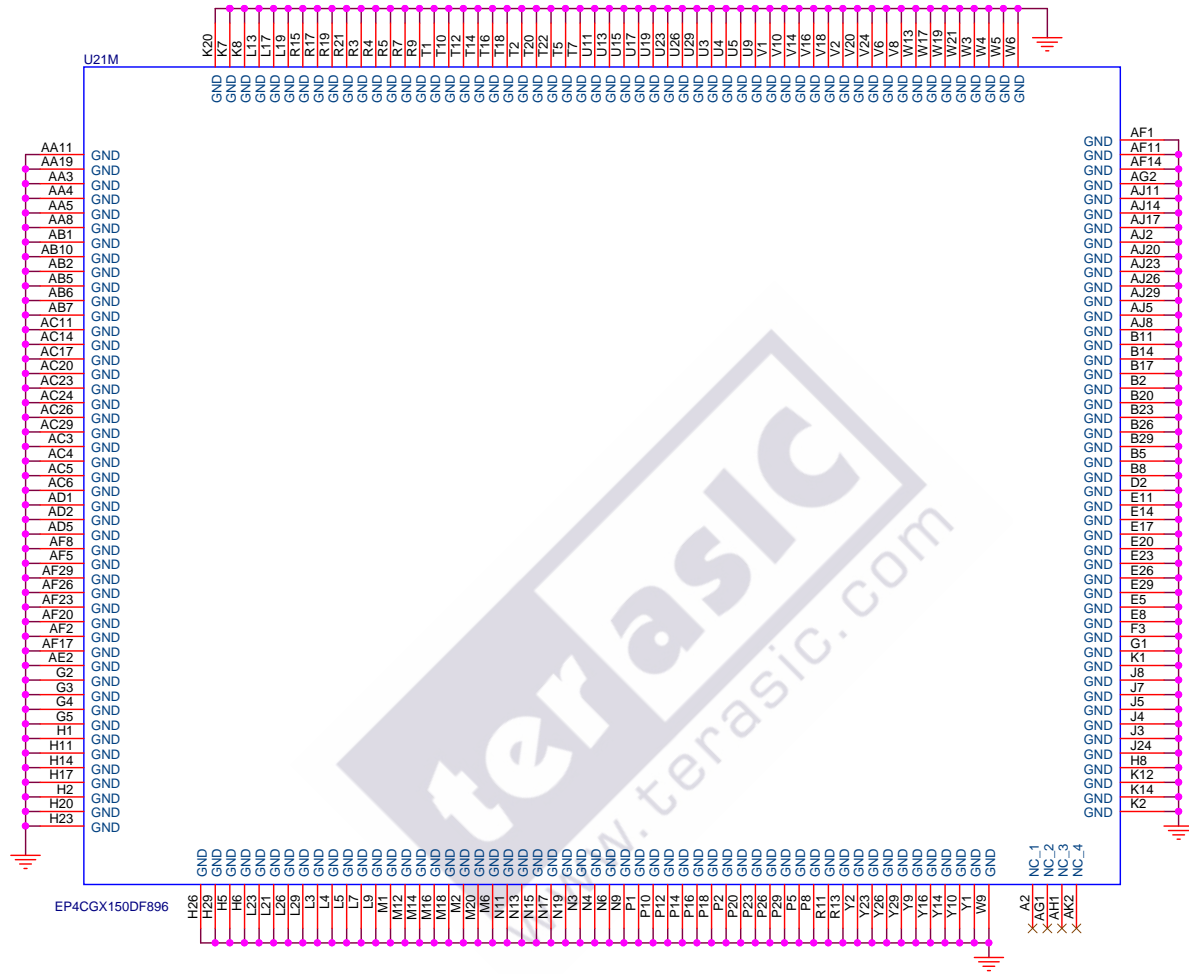


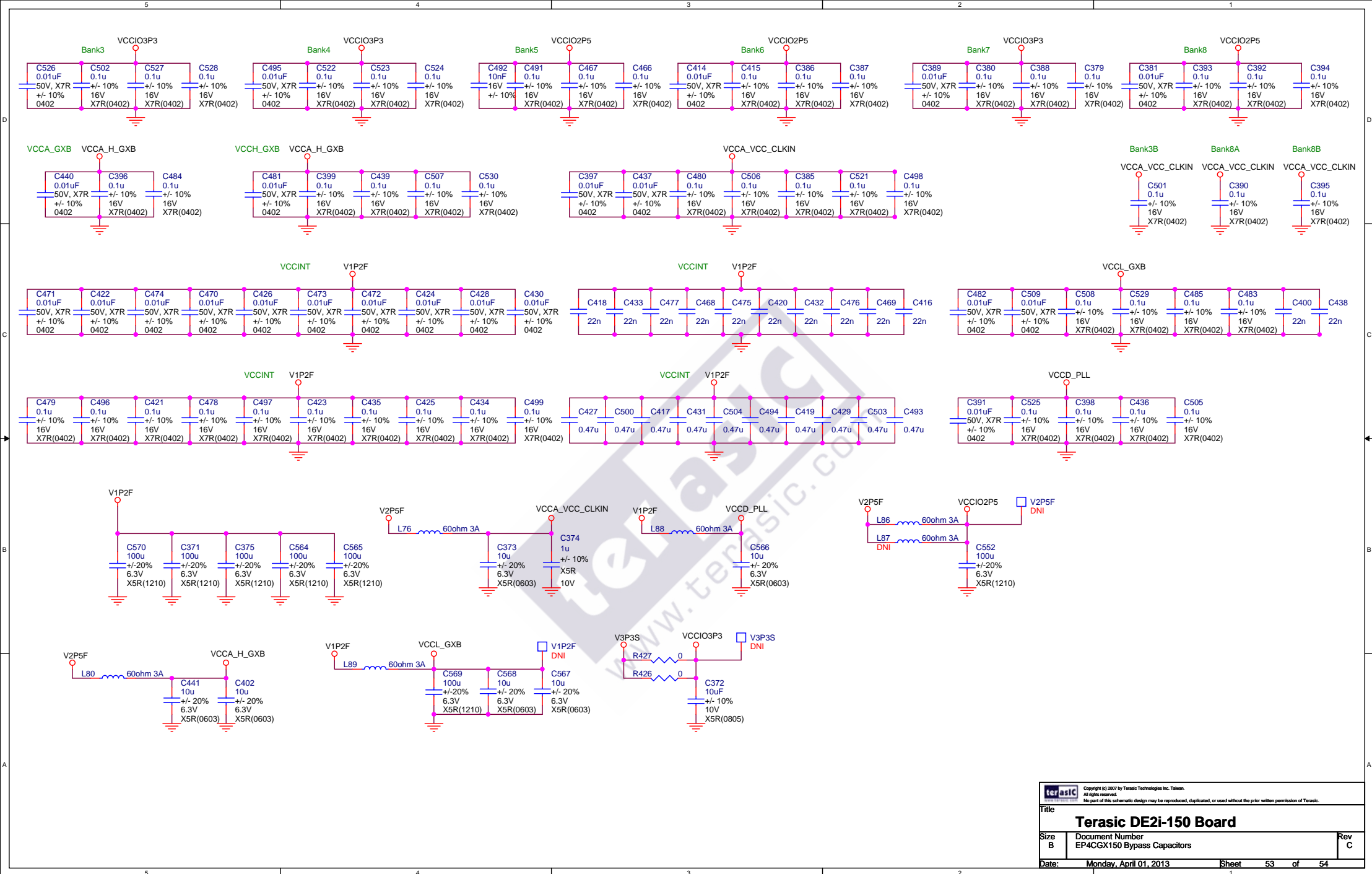
EP4CGX150DF896
Version = 0.1 Preliminary

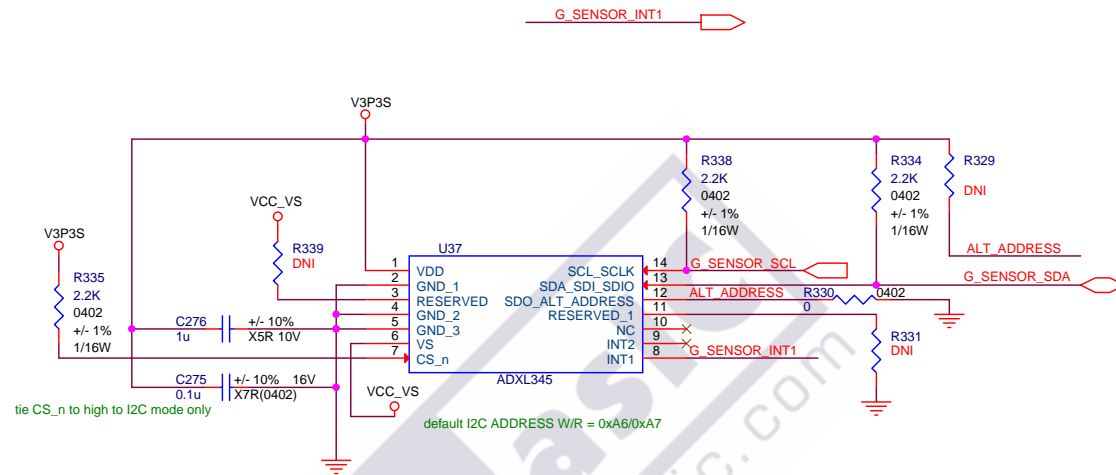
DRAM_DQ[11..0]
LCD_DATA[7..0]











Fitting Component

| | | |
|-------------|-------------|-------------|
| U49 | U50 | U51 |
| GD25Q80BPCP | Battery | GD25Q16BPIG |
| DNI | DNI | DNI |
| U76 | U77 | U78 |
| Fans | 12V Adapter | WiFi Module |
| DNI | DNI | DNI |
| U79 | U80 | |
| Athena | SSD | |
| DNI | DNI | |

| | | |
|---|------------------------|----------------|
| Copyright (c) 2007 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic. | | |
| Title | | |
| Terasic DE2i-150 Board | | |
| Size | Document Number | Rev |
| B | G-SENSOR | C |
| Date: | Monday, April 01, 2013 | Sheet 54 of 54 |