

# 256K x 72, 512K x 36, 1024K x 18 18Mb SYNCHRONOUS PIPELINED, SINGLE CYCLE DESELECT STATIC RAM

**MAY 2010** 

#### **FEATURES**

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- · Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JTAG Boundary Scan for PBGA package
- Power Supply

LPS: VDD  $3.3V \pm 5\%$ , VDDQ  $3.3V/2.5V \pm 5\%$ VPS: VDD  $2.5V \pm 5\%$ , VDDQ  $2.5V \pm 5\%$ 

- JEDEC 100-Pin TQFP, 119-ball PBGA, 165-ball PBGA, and 209-ball (x72) packages
- Lead-free available

#### **DESCRIPTION**

The *ISSI* IS61LPS/VPS51236A, IS61LPS/VPS102418A, and IS61LPS/VPS25672A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS51236A is organized as 524,288 words by 36 bits, the IS61LPS/VPS102418A is organized as 1,048,576 words by 18 bits, and the IS61LPS/VPS25672A is organized as 262,144 words by 72 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable ( $\overline{BWE}$ ) input combined with one or more individual byte write signals ( $\overline{BWx}$ ). In addition, Global Write ( $\overline{GW}$ ) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either  $\overline{\text{ADSP}}$  (Address Status Processor) or  $\overline{\text{ADSC}}$  (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the  $\overline{\text{ADV}}$  (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

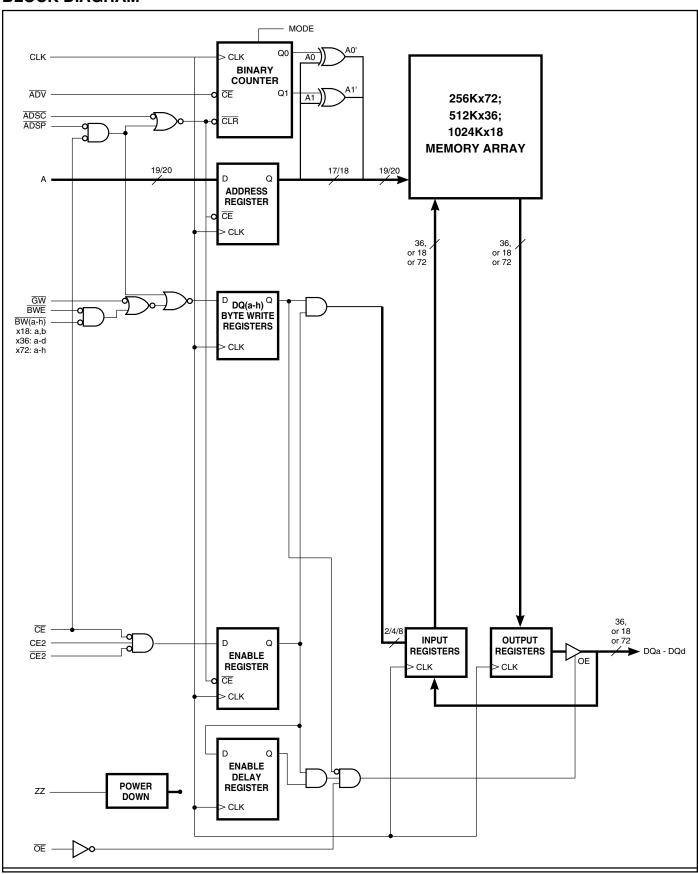
#### **FAST ACCESS TIME**

Symbol	Parameter	250	200	Units
tkQ	Clock Access Time	2.6	3.1	ns
tĸc	Cycle Time	4	5	ns
	Frequency	250	200	MHz

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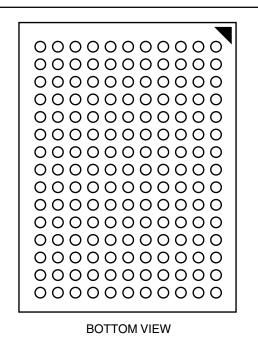
### **BLOCK DIAGRAM**





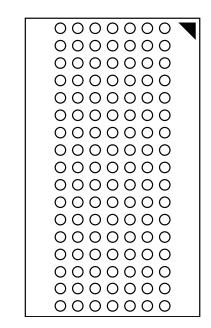
#### **165-PIN BGA**

165-Ball, 13x15 mm BGA 1mm Ball Pitch, 11x15 Ball Array



# 119-PIN BGA

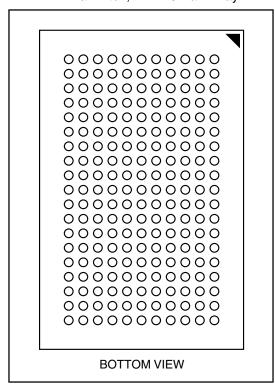
119-Ball, 14x22 mm BGA 1mm Ball Pitch, 7x17 Ball Array



**BOTTOM VIEW** 

#### 209-BALL BGA

209-Ball, 14 mm x 22 mm BGA 1 mm Ball Pitch, 11 x 19 Ball Array





## PIN CONFIGURATION — 256K X 72, 209-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6 `	7	<sup>*</sup> 8	9	10	11
Α	DQg	DQg	Α	CE2	ADSP	ADSC	ADV	CE2	Α	DQb	DQb
В	DQg	DQg	<b>BW</b> c	<b>BW</b> g	NC	BWE	Α	<b>BW</b> b	<b>BW</b> f	DQb	DQb
С	DQg	DQg	<b>BW</b> h	<b>BW</b> d	NC	Œ	NC	<b>BW</b> e	<b>BW</b> a	DQb	DQb
D	DQg	DQg	VSS	NC	NC	ŌĒ	GW	NC	vss	DQb	DQb
Е	DQPg	DQPc	<b>V</b> DDQ	VDDQ	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	VDDQ	VDDQ	DQPf	DQPb
F	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
G	DQc	DQc	VDDQ	VDDQ	V <sub>DD</sub>	NC	V <sub>DD</sub>	VDDQ	VDDQ	DQf	DQf
Н	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
J	DQc	DQc	VDDQ	VDDQ	V <sub>DD</sub>	NC	V <sub>DD</sub>	VDDQ	VDDQ	DQf	DQf
K	NC	NC	CLK	NC	VSS	NC	VSS	NC	NC	NC	NC
L	DQh	DQh	VDDQ	VDDQ	V <sub>DD</sub>	NC	V <sub>DD</sub>	VDDQ	VDDQ	DQa	DQa
М	DQh	DQh	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQa	DQa
Ν	DQh	DQh	VDDQ	VDDQ	V <sub>DD</sub>	NC	VDD	VDDQ	VDDQ	DQa	DQa
Р	DQh	DQh	VSS	VSS	VSS	ZZ	VSS	VSS	VSS	DQa	DQa
R	DQPd	DQPh	VDDQ	VDDQ	V <sub>DD</sub>	V <sub>DD</sub>	VDD	VDDQ	VDDQ	DQPa	DQPe
Т	DQd	DQd	VSS	NC	NC	MODE	NC	NC	VSS	DQe	DQe
U	DQd	DQd	NC	Α	Α	Α	Α	Α	NC	DQe	DQe
V	DQd	DQd	Α	Α	Α	A1	Α	Α	Α	DQe	DQe
W	DQd	DQd	TMS	TDI	Α	A0	Α	TDO	TCK	DQe	DQe

<sup>11</sup> x 19 Ball BGA—14 x 22 mm<sup>2</sup> Body—1 mm Ball Pitch

Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE, CE2, CE2	Synchronous Chip Select
BWx (x=a,b,c,d e,f,g,h)	Synchronous Byte Write Controls

Symbol	Pin Name
BWE	Byte Write Enable
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground



## **119 BGA PACKAGE PIN CONFIGURATION-**512K x 36 (TOP VIEW)

	1	2	3	4	5	6	7
Α	VDDQ	Α	Α	ADSP	Α	Α	VDDQ
В	NC	Α	Α	ADSC	Α	Α	NC
С	NC	Α	Α	<b>V</b> DD	Α	Α	NC
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	CE	Vss	DQb	DQb
F	VDDQ	DQc	Vss	ŌĒ	Vss	DQb	VDDQ
G	DQc	DQc	BWc	ADV	BWb	DQb	DQb
Н	DQc	DQc	Vss	GW	Vss	DQb	DQb
J	VDDQ	VDD	NC	V <sub>DD</sub>	NC	Vdd	VDDQ
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	BWd	NC	BWa	DQa	DQa
М	VDDQ	DQd	Vss	BWE	Vss	DQa	VDDQ
N	DQd	DQd	Vss	A <sub>1</sub> *	Vss	DQa	DQa
P	DQd	DQPd	Vss	<b>A</b> 0*	Vss	DQPa	DQa
R	NC	Α	MODE	<b>V</b> DD	NC	Α	NC
Т	NC	NC	Α	Α	Α	NC	ZZ
U	<b>V</b> DDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note: \* Ao and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE	Synchronous Chip Select
<b>BW</b> x (x=a-d)	Synchronous Byte Write Controls
BWE	Byte Write Enable

Symbol	Pin Name
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO	JTAG Pins
TMS, TDI	
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Output Power Supply
VDD	Power Supply
VDDQ	Output Power Supply
Vss	Ground



## 119 BGA PACKAGE PIN CONFIGURATION

1Mx18 (TOP VIEW)

	1	2	3	4	5	6	7
Α	VDDQ	Α	Α	ADSP	Α	Α	VDDQ
В	NC	Α	Α	ADSC	Α	Α	NC
С	NC	Α	Α	VDD	Α	Α	NC
D	DQb	NC	Vss	NC	Vss	DQPa	NC
Е	NC	DQb	Vss	Œ	Vss	NC	DQa
F	VDDQ	NC	Vss	ŌĒ	Vss	DQa	VDDQ
G	NC	DQb	BWb	ADV	Vss	NC	DQa
Н	DQb	NC	Vss	GW	Vss	DQa	NC
J	VDDQ	Vdd	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	VDDQ
K	NC	DQb	Vss	CLK	Vss	NC	DQa
L	DQb	NC	Vss	NC	BWa	DQa	NC
М	VDDQ	DQb	Vss	BWE	Vss	NC	VDDQ
N	DQb	NC	Vss	A1*	Vss	DQa	NC
Р	NC	DQPb	Vss	<b>A</b> o*	Vss	NC	DQa
R	NC	Α	MODE	VDD	NC	Α	NC
Т	NC	Α	Α	NC	Α	Α	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

 $\textbf{Note:} \ \ ^{\star} Ao \ and \ A_{1} \ are \ the \ two \ least \ significant \ bits \ (LSB) \ of \ the \ address \ field \ and \ set \ the \ internal \ burst \ counter \ if \ burst \ is \ desired.$ 

Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE	Synchronous Chip Select
<b>BW</b> x (x=a,b)	Synchronous Byte Write Controls
BWE	Byte Write Enable

Symbol	Pin Name
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO	JTAG Pins
TMS, TDI	
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Output Power Supply
VDD	Power Supply
VDDQ	Output Power Supply
Vss	Ground



## **165 PBGA PACKAGE PIN CONFIGURATION**

512K x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
Α	NC	Α	CE	BWc	BWb	CE2	BWE	ADSC	ADV	Α	NC
В	NC	Α	CE2	BWd	BWa	CLK	Ğ₩	ŌĒ	ADSP	Α	NC
С	DQPc	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
Е	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	V <sub>DD</sub>	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
Н	NC	Vss	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	$V_{DD}$	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
М	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	Vss	NC	Α	Vss	Vss	VDDQ	NC	DQPa
Р	NC	NC	Α	Α	TDI	A1*	TDO	Α	Α	Α	Α
R	MODE	NC	Α	Α	TMS	A0*	TCK	Α	Α	Α	Α

Note: \* Ao and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE, CE2, CE2	Synchronous Chip Select
BWx (x=a,b,c,d)	Synchronous Byte Write Controls

Symbol	Pin Name
BWE	Byte Write Enable
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground



## **165 PBGA PACKAGE PIN CONFIGURATION**

1M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
Α	NC	Α	CE	BWb	NC	CE2	BWE	ADSC	ADV	Α	Α
В	NC	Α	CE2	NC	BWa	CLK	Ğ₩	ŌĒ	ADSP	Α	NC
С	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	NC	DQa
Н	NC	Vss	NC	VDD	Vss	Vss	Vss	V <sub>DD</sub>	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
М	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	V <sub>DD</sub>	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	Α	Vss	Vss	VDDQ	NC	NC
Р	NC	NC	Α	Α	TDI	A1*	TDO	Α	Α	Α	Α
R	MODE	NC	Α	Α	TMS	A0*	TCK	Α	Α	Α	А

Note: \* Ao and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

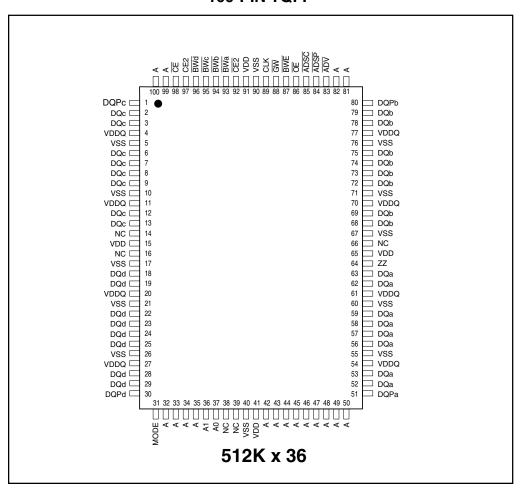
Symbol	Pin Name
Α	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance
ADSP	Address Status Processor
ADSC	Address Status Controller
GW	Global Write Enable
CLK	Synchronous Clock
CE, CE2, CE2	Synchronous Chip Select
BWx (x=a,b)	Synchronous Byte Write Controls

Symbol	Pin Name
BWE	Byte Write Enable
ŌĒ	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
V <sub>DD</sub>	3.3V/2.5V Power Supply
VDDQ	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground



#### **PIN CONFIGURATION**

#### 100-PIN TQFP



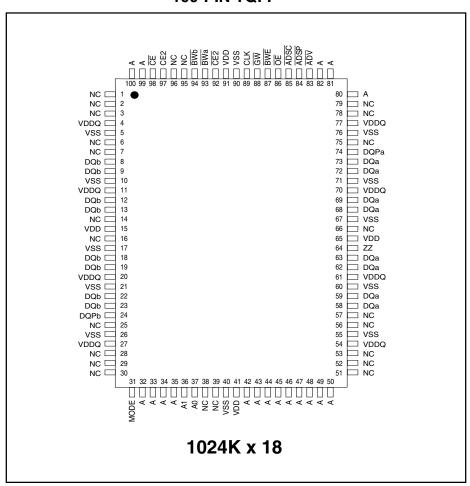
A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.							
Α	Synchronous Address Inputs							
ADSC	Synchronous Controller Address Status							
ADSP	Synchronous Processor Address Status							
ADV	Synchronous Burst Address Advance							
BWa-BWd	Synchronous Byte Write Enable							
BWE	Synchronous Byte Write Enable							
CE, CE2, CE2	Synchronous Chip Enable							
CLK	Synchronous Clock							

DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data Input/Output
GW	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
ŌĒ	Output Enable
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable



### **PIN CONFIGURATION**

#### 100-PIN TQFP



A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
Α	Synchronous Address Inputs
ADSC	Synchronous Controller Address Status
ADSP	Synchronous Processor Address Status
ADV	Synchronous Burst Address Advance
BWa-BWb	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
CE, CE2, CE2	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Input/Output

DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
GW	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
ŌĒ	Output Enable
VDD	3.3V/2.5V Power Supply
VDDQ	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable



## TRUTH TABLE<sup>(1-8)</sup> (3CE option)

OPERATION	ADDRESS	Œ	CE2	CE2	ZZ	<b>ADSP</b>	<b>ADSC</b>	<b>ADV</b>	WRITE	ŌĒ	CLK	DQ
Deselect Cycle, Power-Down	None	Н	Х	Х	L	Χ	L	Х	Х	Х	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Χ	L	L	L	Х	Χ	Х	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Н	Χ	L	L	Χ	Χ	Χ	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Χ	L	L	Н	L	Χ	Χ	Χ	L-H	High-Z
Deselect Cycle, Power-Down	None	L	Н	Х	L	Н	L	Χ	Х	Χ	L-H	High-Z
Snooze Mode, Power-Down	None	Χ	Χ	Χ	Н	Χ	Χ	Χ	Χ	Χ	Χ	High-Z
Read Cycle, Begin Burst	External	L	L	Н	L	L	Χ	Χ	Χ	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	Н	L	L	Х	Χ	Х	Н	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	L	Χ	L-H	D
Read Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	Н	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	Н	L	Н	L	Χ	Н	Н	L-H	High-Z
Read Cycle, Continue Burst	Next	Χ	Х	Х	L	Н	Н	L	Н	L	L-H	Q
Read Cycle, Continue Burst	Next	Χ	Χ	Χ	L	Н	Н	L	Н	Н	L-H	High-Z
Read Cycle, Continue Burst	Next	Н	Х	Х	L	Χ	Н	L	Н	L	L-H	Q
Read Cycle, Continue Burst	Next	Н	Х	Х	L	Χ	Н	L	Н	Н	L-H	High-Z
Write Cycle, Continue Burst	Next	Χ	Χ	Χ	L	Н	Н	L	L	Χ	L-H	D
Write Cycle, Continue Burst	Next	Н	Х	Х	L	Χ	Н	L	L	Х	L-H	D
Read Cycle, Suspend Burst	Current	Χ	Х	Х	L	Н	Н	Н	Н	L	L-H	Q
Read Cycle, Suspend Burst	Current	Χ	Χ	Χ	L	Н	Н	Н	Н	Н	L-H	High-Z
Read Cycle, Suspend Burst	Current	Н	Χ	Χ	L	Χ	Н	Н	Н	L	L-H	Q
Read Cycle, Suspend Burst	Current	Н	Х	Χ	L	Χ	Н	Н	Н	Н	L-H	High-Z
Write Cycle, Suspend Burst	Current	Х	Х	Χ	L	Н	Н	Н	L	Х	L-H	D
Write Cycle, Suspend Burst	Current	Н	Х	Χ	L	Χ	Н	Н	L	Х	L-H	D

#### NOTE:

- 1. X means "Don't Care." H means logic HIGH. L means logic LOW.
- 2. For WRITE, L means one or more byte write enable signals (BWa-h) and BWE are LOW or GW is LOW. WRITE = H for all BWx, BWE, GW HIGH.
- 3. BWa enables WRITEs to DQa's and DQPa. BWb enables WRITEs to DQb's and DQPb. BWc enables WRITEs to DQc's and DQPc. BWd enables WRITEs to DQd's and DQPd. BWe enables WRITEs to DQe's and DQPe. BWf enables WRITEs to DQf's and DQPf. BWg enables WRITEs to DQg's and DQPg. BWh enables WRITEs to DQh's and DQPh. DQPa-DQPh are available on the x72 version. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
- 4. All inputs except OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- 5. Wait states are inserted by suspending burst.
- 6. For a WRITE operation following a READ operation, **OE** must be HIGH before the input data setup time and held HIGH during the input data hold time.
- 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- 8. ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.



## **TRUTH TABLE**<sup>(1-8)</sup> (1CE option)

NEXT CYCLE	ADDRESS	CE	ADSP	ADSC	ADV	WRITE	ŌĒ	DQ
Deselected	None	Н	Х	L	Χ	Х	Х	High-Z
Read, Begin Burst	External	L	L	Х	Х	Х	L	Q
Read, Begin Burst	External	L	L	Х	Χ	Х	Н	High-Z
Write, Begin Burst	External	L	Н	L	Х	L	Х	D
Read, Begin Burst	External	L	Н	L	Х	Н	L	Q
Read, Begin Burst	External	L	Н	L	Χ	Н	Н	High-Z
Read, Continue Burst	Next	Х	Н	Н	L	Н	L	Q
Read, Continue Burst	Next	Х	Н	Н	L	Н	Н	High-Z
Read, Continue Burst	Next	Н	Х	Н	L	Н	L	Q
Read, Continue Burst	Next	Н	Х	Н	L	Н	Н	High-Z
Write, Continue Burst	Next	Х	Н	Н	L	L	Х	D
Write, Continue Burst	Next	Н	Х	Н	L	L	Х	D
Read, Suspend Burst	Current	Х	Н	Н	Н	Н	L	Q
Read, Suspend Burst	Current	Х	Н	Н	Н	Н	Н	High-Z
Read, Suspend Burst	Current	Н	Х	Н	Н	Н	L	Q
Read, Suspend Burst	Current	Н	Х	Н	Н	Н	Н	High-Z
Write, Suspend Burst	Current	Х	Н	Н	Н	L	Х	D
Write, Suspend Burst	Current	Н	Х	Н	Н	L	Χ	D

#### NOTE:

- 1. X means "Don't Care." H means logic HIGH. L means logic LOW.
- 2. For WRITE, L means one or more byte write enable signals (BWa-h) and BWE are LOW or GW is LOW. WRITE = H for all BWx, BWE, GW HIGH.
- 3. BWa enables WRITEs to DQa's and DQPa. BWb enables WRITEs to DQb's and DQPb. BWc enables WRITEs to DQc's and DQPc. BWd enables WRITEs to DQd's and DQPd. BWe enables WRITEs to DQe's and DQPe. BWf enables WRITEs to DQf's and DQPf. BWg enables WRITEs to DQg's and DQPg. BWh enables WRITEs to DQh's and DQPh. DQPa-DQPh are available on the x72 version. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
- All inputs except OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- 5. Wait states are inserted by suspending burst.
- 6. For a WRITE operation following a READ operation,  $\overline{\text{OE}}$  must be HIGH before the input data setup time and held HIGH during the input data hold time.
- 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- 8. ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

#### **PARTIAL TRUTH TABLE**

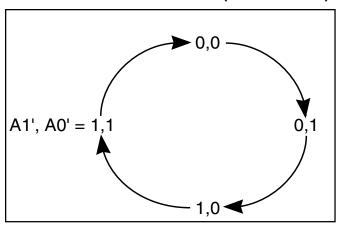
Function	GW	BWE	BWa	BWb	BWc	BWd	BWe	BWf	BWg	BWh
Read	Н	Н	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х
Read	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
Write Byte 1	Н	L	L	Н	Н	Н	Н	Н	Н	Н
Write All Bytes	Н	L	L	L	L	L	L	L	L	L
Write All Bytes	L	Χ	Х	Х	Х	Х	Х	Х	Χ	Х



## INTERLEAVED BURST ADDRESS TABLE (MODE = VDD or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

## LINEAR BURST ADDRESS TABLE (MODE = VSS)



#### ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Тѕтс	Storage Temperature	-55 to +150	°C
Po	Power Dissipation	1.6	W
Іоит	Output Current (per I/O)	100	mA
VIN, VOUT	Voltage Relative to Vss for I/O Pins	-0.5 to VDDQ + 0.5	V
VIN	Voltage Relative to Vss for for Address and Control Inputs	-0.5 to V <sub>DD</sub> + 0.5	V
VDD	Voltage on VDD Supply Relative to Vss	-0.5 to 4.6	V

#### Notes:

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
- 3. This device contains circuitry that will ensure the output devices are in High-Z at power up.



## **OPERATING RANGE (IS61LPSXXXXX)**

Range	Ambient Temperature	V <sub>DD</sub>	VDDQ
Commercial	0°C to +70°C	3.3V <u>+</u> 5%	3.3V / 2.5V <u>+</u> 5%
Industrial	–40°C to +85°C	3.3V <u>+</u> 5%	3.3V / 2.5V <u>+</u> 5%

## **OPERATING RANGE (IS61VPSXXXXX)**

Range	Ambient Temperature	<b>V</b> DD	<b>V</b> DDQ
Commercial	0°C to +70°C	2.5V <u>+</u> 5%	2.5V <u>+</u> 5%
Industrial	–40°C to +85°C	2.5V <u>+</u> 5%	2.5V <u>+</u> 5%

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			3	.3V	2	2.5V	
Symbol	Parameter	<b>Test Conditions</b>	Min.	Max.	Min.	Max.	Unit
Vон	Output HIGH Voltage	IOH = -4.0  mA  (3.3V) IOH = -1.0  mA  (2.5V)	2.4	_	2.0	_	V
VoL	Output LOW Voltage	IoL = 8.0 mA (3.3V) IoL = 1.0 mA (2.5V)	_	0.4	_	0.4	V
ViH	Input HIGH Voltage		2.0	V <sub>DD</sub> + 0.3	1.7	VDD + 0.3	V
VIL	Input LOW Voltage		-0.3	0.8	-0.3	0.7	V
ILI	Input Leakage Current	$Vss \leq V_{IN} \leq V_{DD}^{(1)}$	-5	5	-5	5	μΑ
ILO	Output Leakage Current	$\frac{Vss \le Vout \le VddQ,}{\overline{OE}} = ViH$	-5	5	-5	5	μΑ

## POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

					-250 MAX			-200 MAX		
Symbol	Parameter	Test Conditions	Temp.range	x18	x36	x72	x18	x36	x72	Unit
Icc	AC Operating	Device Selected,	Com.	450	450	600	425	425	550	mA
	Supply Current	$\overline{\text{OE}} = \text{V}_{\text{IH}}, ZZ \leq \text{V}_{\text{IL}},$ All Inputs $\leq 0.2\text{V}$ or $\geq \text{V}_{\text{DD}}$ Cycle Time $\geq \text{tkc}$ min.	Ind. – 0.2V,	500	500	650	475	475	600	
ISB	Standby Current TTL Input	Device Deselected, $V_{DD} = Max.$ , All Inputs $\leq V_{IL}$ or $\geq V_{IH}$ , $ZZ \leq V_{IL}$ , $f = Max$ .	Com. Ind.	150 150	150 150	150 150	150 150	150 150	150 150	mA
İsbi	Standby Current CMOS Input	Device Deselected, $V_{DD} = Max.$ , $V_{IN} \le V_{SS} + 0.2V \text{ or } \ge V_{DD} - 6$	Com. Ind. 0.2V	110 125	110 125	110 125	110 125	110 125	110 125	mA
ISB2	Sleep Mode	ZZ>VIH	Com. Ind.	60 75	60 75	60 75	60 75	60 75	60 75	mA

#### Note:

<sup>1.</sup> MODE pin has an internal pullup and should be tied to  $V_{DD}$  or  $V_{SS}$ . It exhibits  $\pm 100 \mu A$  maximum leakage current when tied to  $\leq V_{SS} + 0.2 V$  or  $\geq V_{DD} - 0.2 V$ .



### CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	VIN = 0V	6	pF
Соит	Input/Output Capacitance	Vout = 0V	8	pF

#### Notes:

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions:  $T_A = 25^{\circ}C$ , f = 1 MHz,  $V_{DD} = 3.3V$ .

### 3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

### **AC TEST LOADS**

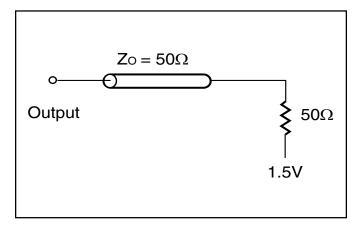


Figure 1

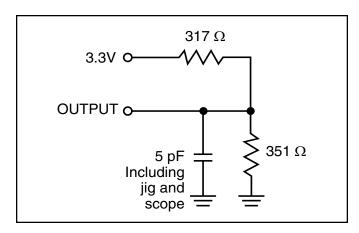


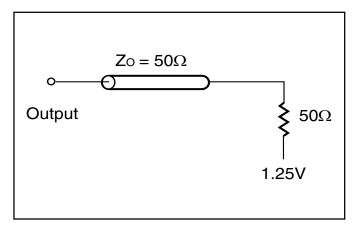
Figure 2



## 2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

## 2.5 I/O OUTPUT LOAD EQUIVALENT



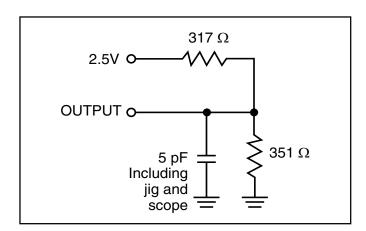


Figure 3 Figure 4



# READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-2!	50	-200	0		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
fmax	Clock Frequency	_	250	_	200	MHz	
tĸc	Cycle Time	4.0	_	5	_	ns	
tкн	Clock High Time	1.7	_	2	_	ns	
tĸL	Clock Low Time	1.7	_	2	_	ns	
tka	Clock Access Time	_	2.6	_	3.1	ns	
tkqx <sup>(2)</sup>	Clock High to Output Invalid	0.8	_	1.5	_	ns	
tkqlz(2,3)	Clock High to Output Low-Z	0.8	_	1	_	ns	
tkqhz(2,3)	Clock High to Output High-Z	_	2.6	_	3.0	ns	
toeq	Output Enable to Output Valid	_	2.8	_	3.1	ns	
toelz(2,3)	Output Enable to Output Low-Z	0	_	0	_	ns	
toehz(2,3)	Output Disable to Output High-Z	_	2.6	_	3.0	ns	
tas	Address Setup Time	1.2	_	1.4	_	ns	
tws	Read/Write Setup Time	1.2	_	1.4	_	ns	
tces	Chip Enable Setup Time	1.2	_	1.4	_	ns	
tavs	Address Advance Setup Time	1.2	_	1.4	_	ns	
tos	Data Setup Time	1.2	_	1.4	_	ns	
tah	Address Hold Time	0.3	_	0.4	_	ns	
twн	Write Hold Time	0.3	_	0.4	_	ns	
tceh	Chip Enable Hold Time	0.3	_	0.4	_	ns	
tavh	Address Advance Hold Time	0.3	_	0.4	_	ns	
ton	Data Hold Time	0.3	_	0.4	_	ns	
tpds	ZZ High to Power Down	_	2	_	2	сус	
tpus	ZZ Low to Power Down	_	2	_	2	сус	

#### Note:

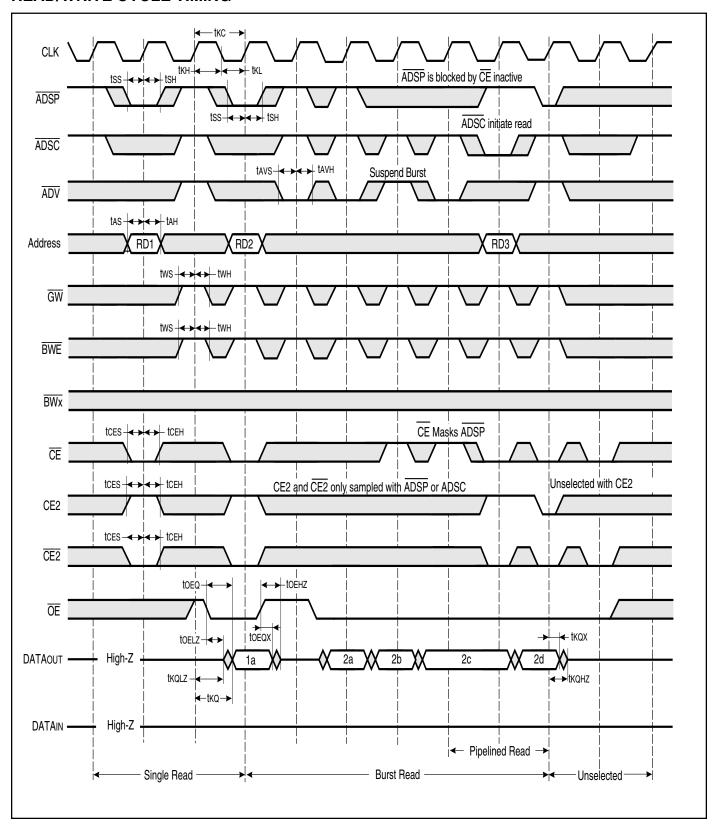
<sup>1.</sup> Configuration signal MODE is static and must not change during normal operation.

<sup>2.</sup> Guaranteed but not 100% tested. This parameter is periodically sampled.

 $<sup>{\</sup>it 3. \ Tested with load in Figure 2.}\\$ 

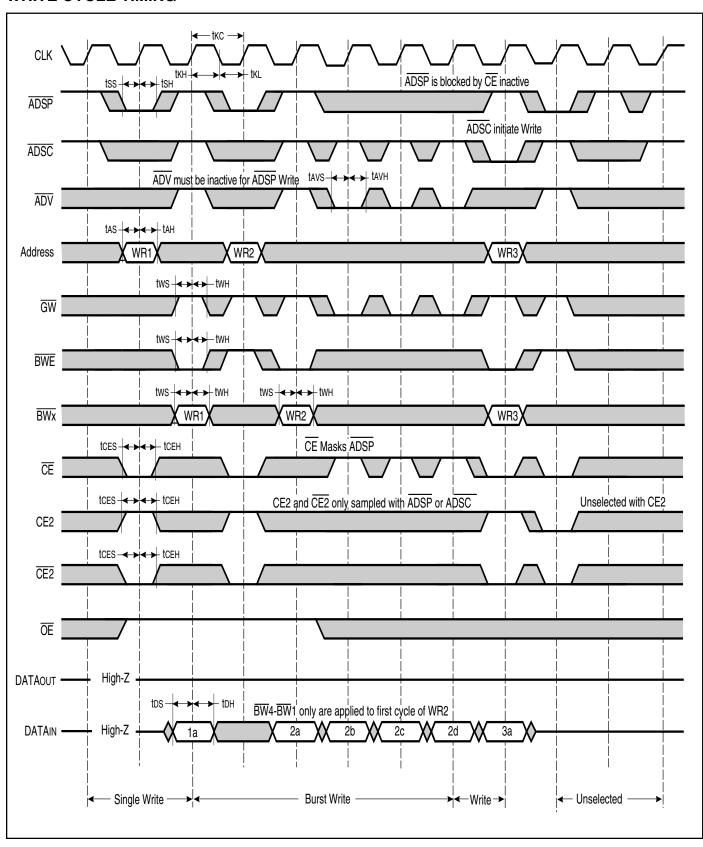


### **READ/WRITE CYCLE TIMING**





### WRITE CYCLE TIMING



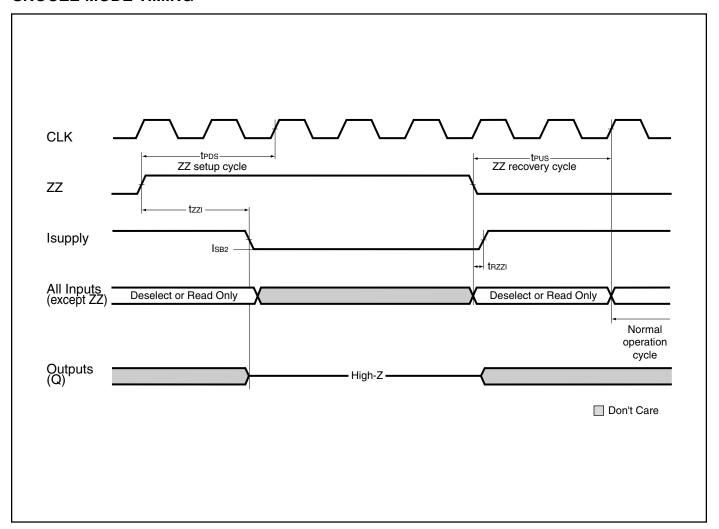


## **SNOOZE MODE ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Max.	Unit
ISB2	Current during SNOOZE MODE	$ZZ \ge Vih$	_	60	mA
tpds	ZZ active to input ignored		_	2	cycle
tpus	ZZ inactive to input sampled		2	_	cycle
tzzı	ZZ active to SNOOZE current		_	2	cycle
trzzi	ZZ inactive to exit SNOOZE current		0	_	ns

### **SNOOZE MODE TIMING**

20





#### IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The IS61LPS/VPSxxxxxx products have a serial boundary scan Test Access Port (TAP) in the PBGA package only. (The TQFP package not available.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

#### **DISABLING THE JTAG FEATURE**

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

### TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

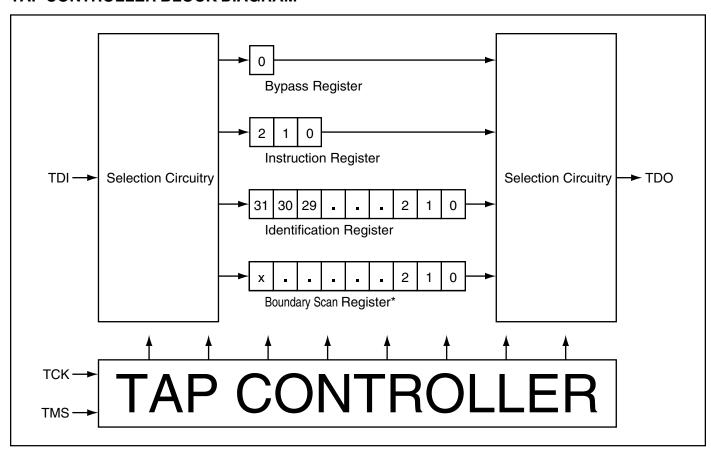
## TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

## **TEST DATA-IN (TDI)**

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

#### TAP CONTROLLER BLOCK DIAGRAM





## **TEST DATA OUT (TDO)**

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

#### PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

#### TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

## **Instruction Register**

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

## **Bypass Register**

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register

is set LOW (Vss) when the BYPASS instruction is executed.

## **Boundary Scan Register**

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

### Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan	75	75	TBD

## Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

#### **IDENTIFICATION REGISTER DEFINITIONS**

Instruction Field	Description	256K x 72	512Kx36	1M x 18
Revision Number (31:28)	Reserved for version number.	xxxx	XXXX	xxxx
Device Depth (27:23)	Defines depth of SRAM. 512K, 1M or 256K	00110	00111	01000
Device Width (22:18)	Defines width of the SRAM. x72, x36 or x18	00101	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	XXXX	XXXXX	xxxxx
ISSIJEDECID (11:1)	Allows unique identification of SRAM vendor.	0011010101	00011010101	00011010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1	1



#### TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

#### **EXTEST**

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

#### **IDCODE**

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### SAMPLE-Z

The SAMPLE-Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (tcs and tch). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

### **BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### **RESERVED**

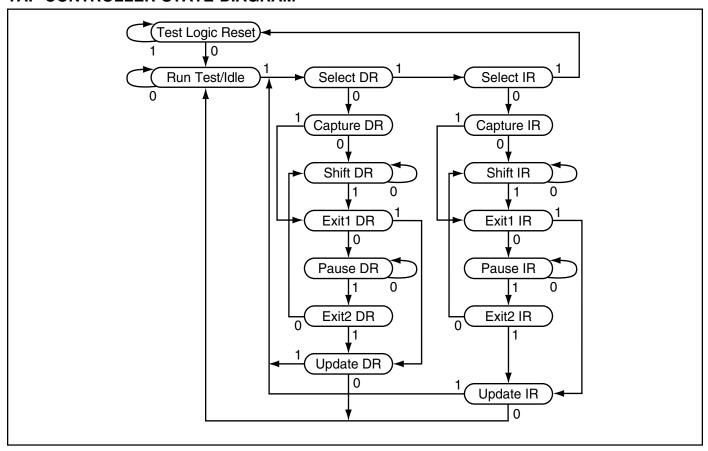
These instructions are not implemented but are reserved for future use. Do not use these instructions.



### **INSTRUCTION CODES**

Code	Instruction	Description
000	EXTEST	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
001	IDCODE	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
010	SAMPLE-Z	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
011	RESERVED	Do Not Use: This instruction is reserved for future use.
100	SAMPLE/PRELOAD	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
101	RESERVED	Do Not Use: This instruction is reserved for future use.
110	RESERVED	Do Not Use: This instruction is reserved for future use.
111	BYPASS	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

### TAP CONTROLLER STATE DIAGRAM





## TAP Electrical Characteristics Over the Operating Range<sup>(1,2)</sup>

Symbol	Parameter	<b>Test Conditions</b>	Min.	Max.	Units
V <sub>OH1</sub>	Output HIGH Voltage	lон = −2.0 mA	1.7	_	V
V <sub>OH2</sub>	Output HIGH Voltage	Іон = −100 μА	2.1	_	V
V <sub>OL1</sub>	Output LOW Voltage	IoL = 2.0 mA	_	0.7	V
V <sub>OL2</sub>	Output LOW Voltage	IoL = 100 μA	_	0.2	V
VIH	Input HIGH Voltage		1.7	VDD +0.3	V
VIL	Input LOW Voltage		-0.3	0.7	V
lx	Input Leakage Current	$V_{\text{SS}} \leq V \; I \leq V_{\text{DDQ}}$	-10	10	μA

#### Notes:

1. All Voltage referenced to Ground.

2. Overshoot: ViH (AC) ≤ VDD +1.5V for t ≤ trcyc/2, Undershoot: ViL (AC) ≤ 0.5V for t ≤ trcyc/2,

Power-up:  $V_{IH} < 2.6 \text{V}$  and  $V_{DD} < 2.4 \text{V}$  and  $V_{DDQ} < 1.4 \text{V}$  for t < 200 ms.

## TAP AC ELECTRICAL CHARACTERISTICS(1,2) (OVER OPERATING RANGE)

Symbol	Parameter	Min.	Max.	Unit
trcyc	TCK Clock cycle time	100	_	ns
ftF	TCK Clock frequency	_	10	MHz
tтн	TCK Clock HIGH	40	_	ns
tτι	TCK Clock LOW	40	_	ns
tтмss	TMS setup to TCK Clock Rise	10	_	ns
ttdis	TDI setup to TCK Clock Rise	10	_	ns
tcs	Capture setup to TCK Rise	10	_	ns
tтмsн	TMS hold after TCK Clock Rise	10	_	ns
tтын	TDI Hold after Clock Rise	10	_	ns
tсн	Capture hold after Clock Rise	10	_	ns
troov	TCK LOW to TDO valid	_	20	ns
troox	TCK LOW to TDO invalid	0	_	ns

#### Notes:

<sup>1.</sup> Both tcs and tch refer to the set-up and hold time requirements of latching data from the boundary scan register.

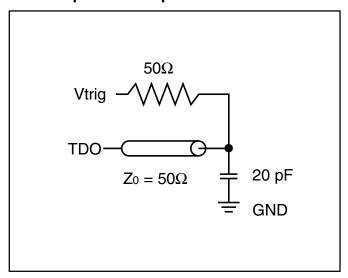
<sup>2.</sup> Test conditions are specified using the load in TAP  $\dot{AC}$  test conditions. tR/tF = 1 ns.



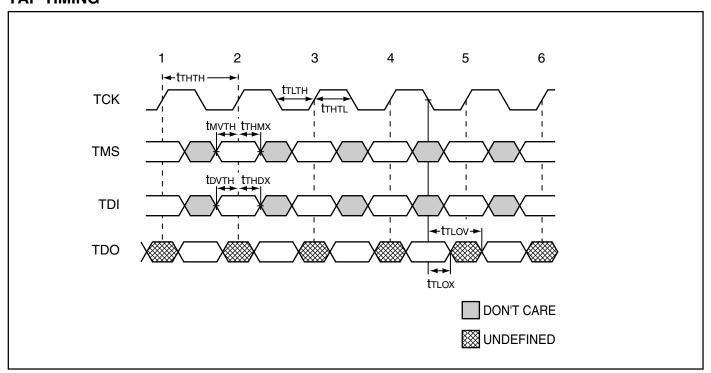
# **TAP AC TEST CONDITIONS** (2.5V/3.3V)

Input pulse levels	0 to 2.5V/0 to 3.0V
Input rise and fall times	1ns
Input timing reference levels	1.25V/1.5V
Output reference levels	1.25V/1.5V
Test load termination supply volta	age 1.25V/1.5V
Vtrig	1.25V/1.5V

# **TAP Output Load Equivalent**



## **TAP TIMING**





209 BOUNDARY SCAN ORDER (256K X 72)





# 165 PBGA BOUNDARY SCAN ORDER (x 36)

Bit #	Signal Name	Bump ID	Bit#	Signal Name	Bump ID	Bit#	Signal Name	Bump ID	Bit#	Signal Name	Bump ID
1	MODE	1R	21	DQb	11G	41	NC	1A	61	DQd	1J
2	Α	6N	22	DQb	11F	42	CE2	6A	62	DQd	1K
3	Α	11P	23	DQb	11E	43	<b>BW</b> a	5B	63	DQd	1L
4	Α	8P	24	DQb	11D	44	<b>BW</b> b	5A	64	DQd	1M
5	Α	8R	25	DQb	10G	45	<b>BW</b> c	4A	65	DQd	2J
6	Α	9R	26	DQb	10F	46	<b>BW</b> d	4B	66	DQd	2K
7	Α	9P	27	DQb	10E	47	CE2	3B	67	DQd	2L
8	Α	10P	28	DQb	10D	48	CE	ЗА	68	DQd	2M
9	Α	10R	29	DQb	11C	49	Α	2A	69	DQd	1N
10	Α	11R	30	NC	11A	50	Α	2B	70	Α	3P
11	ZZ	11H	31	Α	10A	51	NC	1B	71	Α	3R
12	DQa	11N	32	Α	10B	52	DQc	1C	72	А	4R
13	DQa	11M	33	ADV	9A	53	DQc	1D	73	Α	4P
14	DQa	11L	34	ADSP	9B	54	DQc	1E	74	A1	6P
15	DQa	11K	35	ADSC	8A	55	DQc	1F	75	A0	6R
16	DQa	11J	36	ŌĒ	8B	56	DQc	1G			
17	DQa	10M	37	BWE	7A	57	DQc	2D			
18	DQa	10L	38	GW	7B	58	DQc	2E			
19	DQa	10K	39	CLK	6B	59	DQc	2F			
20	DQa	10J	40	NC	11B	60	DQc	2G			



## 165 PBGA BOUNDARY SCAN ORDER (x 18)

Bit#	Signal Name	Bump ID	Bit#	Signal Name	Bump ID	Bit#	Signal Name	Bump ID	Bit#	Signal Name	Bump ID
1	MODE	1R	21	DQa	11G	41	NC	1A	61	DQb	1J
2	Α	6N	22	DQa	11F	42	<b>CE</b> 2	6A	62	DQb	1K
3	Α	11P	23	DQa	11E	43	<del>BW</del> a	5B	63	DQb	1L
4	Α	8P	24	DQa	11D	44	NC	5A	64	DQb	1M
5	Α	8R	25	DQa	11C	45	<b>BW</b> b	4A	65	DQb	1N
6	Α	9R	26	NC	10F	46	NC	4B	66	NC	2K
7	Α	9P	27	NC	10E	47	CE2	3B	67	NC	2L
8	Α	10P	28	NC	10D	48	CE	ЗА	68	NC	2M
9	Α	10R	29	NC	10G	49	Α	2A	69	NC	2J
10	Α	11R	30	Α	11A	50	Α	2B	70	Α	3P
11	ZZ	11H	31	Α	10A	51	NC	1B	71	Α	3R
12	NC	11N	32	Α	10B	52	NC	1C	72	Α	4R
13	NC	11M	33	ADV	9A	53	NC	1D	73	Α	4P
14	NC	11L	34	ADSP	9B	54	NC	1E	74	A1	6P
15	NC	11K	35	ADSC	8A	55	NC	1F	75	A0	6R
16	NC	11J	36	ŌĒ	8B	56	NC	1G			
17	DQa	10M	37	BWE	7A	57	DQb	2D			
18	DQa	10L	38	GW	7B	58	DQb	2E			
19	DQa	10K	39	CLK	6B	59	DQb	2F			
20	DQa	10J	40	NC	11B	60	DQb	2G			



## ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package
512Kx36			
	250	IS61LPS51236A-250TQ IS61LPS51236A-250TQL IS61LPS51236A-250B2 IS61LPS51236A-250B3	100 TQFP 100 TQFP, Lead-free 119 PBGA 165 PBGA
	200	IS61LPS51236A-200TQ IS61LPS51236A-200B2 IS61LPS51236A-200B3	100 TQFP 119 PBGA 165 PBGA
1Mx18			
	250	IS61LPS102418A-250TQ IS61LPS102418A-250B2 IS61LPS102418A-250B3	100 TQFP 119 PBGA 165 PBGA
	200	IS61LPS102418A-200TQ IS61LPS102418A-200B2 IS61LPS102418A-200B3	100 TQFP 119 PBGA 165 PBGA
256Kx72	250	IS61LPS25672A-250B1 IS61LPS25672A-250B1L	209 PBGA 209 PBGA, Lead-free

## Industrial Range: -40°C to +85°C

Configuration	Frequency	Order Part Number	Package
512Kx36			
	250	IS61LPS51236A-250TQI IS61LPS51236A-250B2I	100 TQFP 119 PBGA
		IS61LPS51236A-250B3I IS61LPS51236A-250B3LI	165 PBGA 165 PBGA, Lead-free
	200	IS61LPS51236A-200TQI IS61LPS51236A-200TQLI IS61LPS51236A-200B2I IS61LPS51236A-200B2LI IS61LPS51236A-200B3I IS61LPS51236A-200B3LI	100 TQFP 100 TQFP, Lead-free 119 PBGA 119 PBGA, Lead-free 165 PBGA 165 PBGA, Lead-free
1Mx18			,
	250	IS61LPS102418A-250TQI IS61LPS102418A-250TQLI IS61LPS102418A-250B2I IS61LPS102418A-250B3I	100 TQFP 100 TQFP, Lead-free 119 PBGA 165 PBGA
	200	IS61LPS102418A-200TQI IS61LPS102418A-200TQLI IS61LPS102418A-200B2I IS61LPS102418A-200B3I	100 TQFP 100 TQFP, Lead-free 119 PBGA 165 PBGA
256Kx72	250	IS61LPS25672A-250B1I	209 PBGA



# ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package
512Kx36			
	250	IS61VPS51236A-250TQ IS61VPS51236A-250B2	100 TQFP 119 PBGA
		IS61VPS51236A-250B3 IS61VPS51236A-250B3L	165 PBGA 165 PBGA, Lead-free
	200	IS61VPS51236A-200TQ IS61VPS51236A-200B2	100 TQFP 119 PBGA
		IS61VPS51236A-200B3	165 PBGA
1Mx18			
	250	IS61VPS102418A-250TQ IS61VPS102418A-250TQL IS61VPS102418A-250B2	100 TQFP 100 TQFP, Lead-free 119 PBGA
	200	IS61VPS102418A-250B3 IS61VPS102418A-200TQ IS61VPS102418A-200B2	165 PBGA 100 TQFP 119 PBGA
		IS61VPS102418A-200B3	165 PBGA
256Kx72	250	IS61VPS25672A-250B1	209 PBGA

# Industrial Range: -40°C to +85°C

Configuration	Frequency	Order Part Number	Package
512Kx36			
	250	IS61VPS51236A-250TQI IS61VPS51236A-250B2I	100 TQFP 119 PBGA
		IS61VPS51236A-250B3I	165 PBGA
	200	IS61VPS51236A-200TQI IS61VPS51236A-200TQLI IS61VPS51236A-200B2I	100 TQFP 100 TQFP, Lead-free 119 PBGA
		IS61VPS51236A-200B3I	165 PBGA
1Mx18			
	250	IS61VPS102418A-250TQI IS61VPS102418A-250B2I IS61VPS102418A-250B3I	100 TQFP 119 PBGA 165 PBGA
	200	IS61VPS102418A-200TQI IS61VPS102418A-200B2I IS61VPS102418A-200B3I	100 TQFP 119 PBGA 165 PBGA
256Kx72	250	IS61VPS25672A-250B1I	209 PBGA



