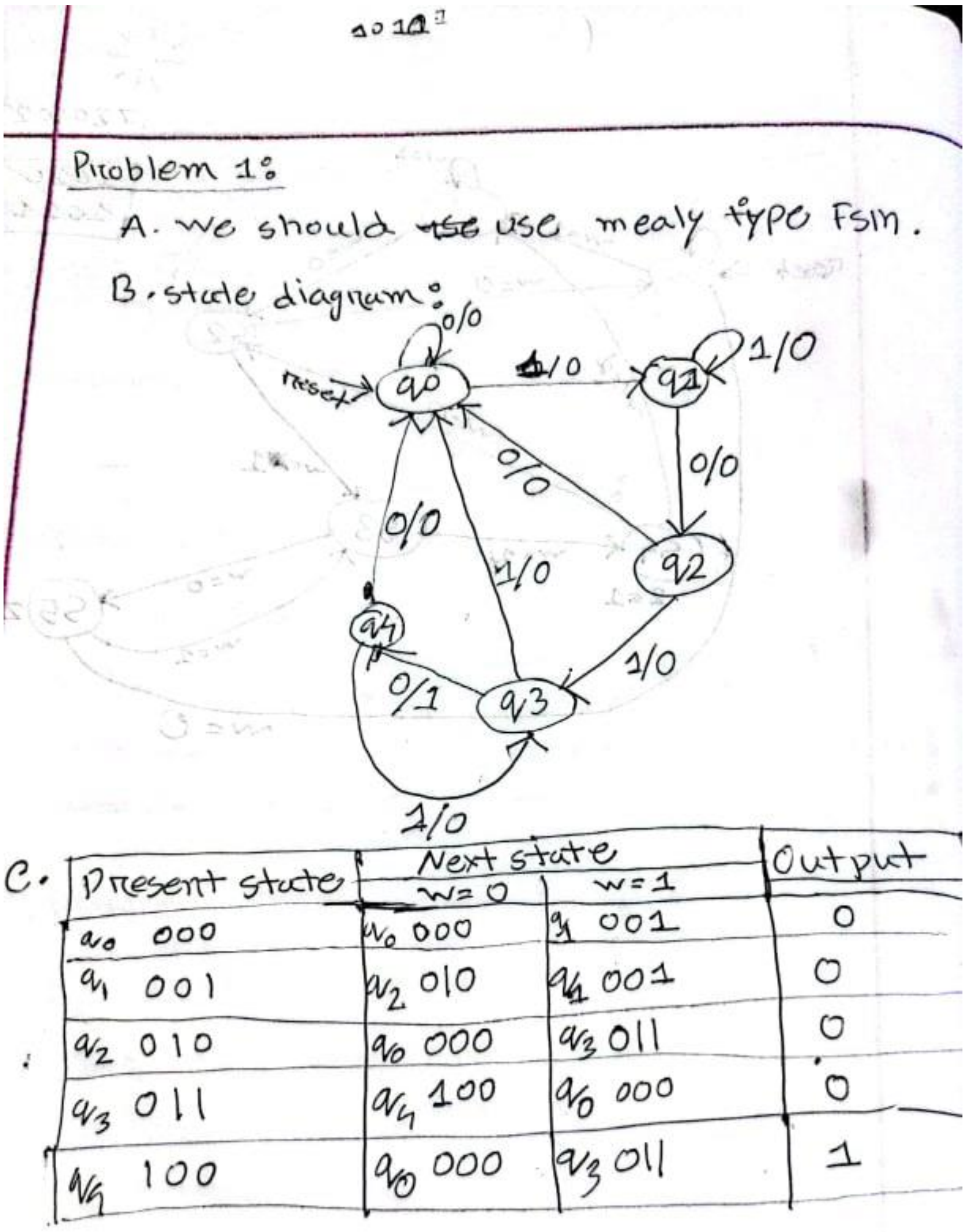
Task 1:

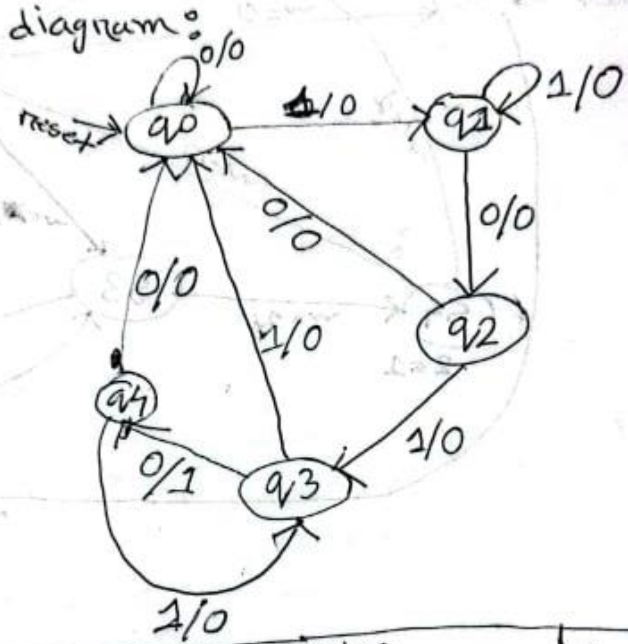


1010

Problem 1:

A. We should ~~use~~ use mealy type Fsm.

B. state diagram:



C.

Present state	Next state w=0	Next state w=1	Output
q0 000	q0 000	q1 001	0
q1 001	q2 010	q1 001	0
q2 010	q0 000	q3 011	0
q3 011	q4 100	q0 000	0
q4 100	q0 000	q3 011	1

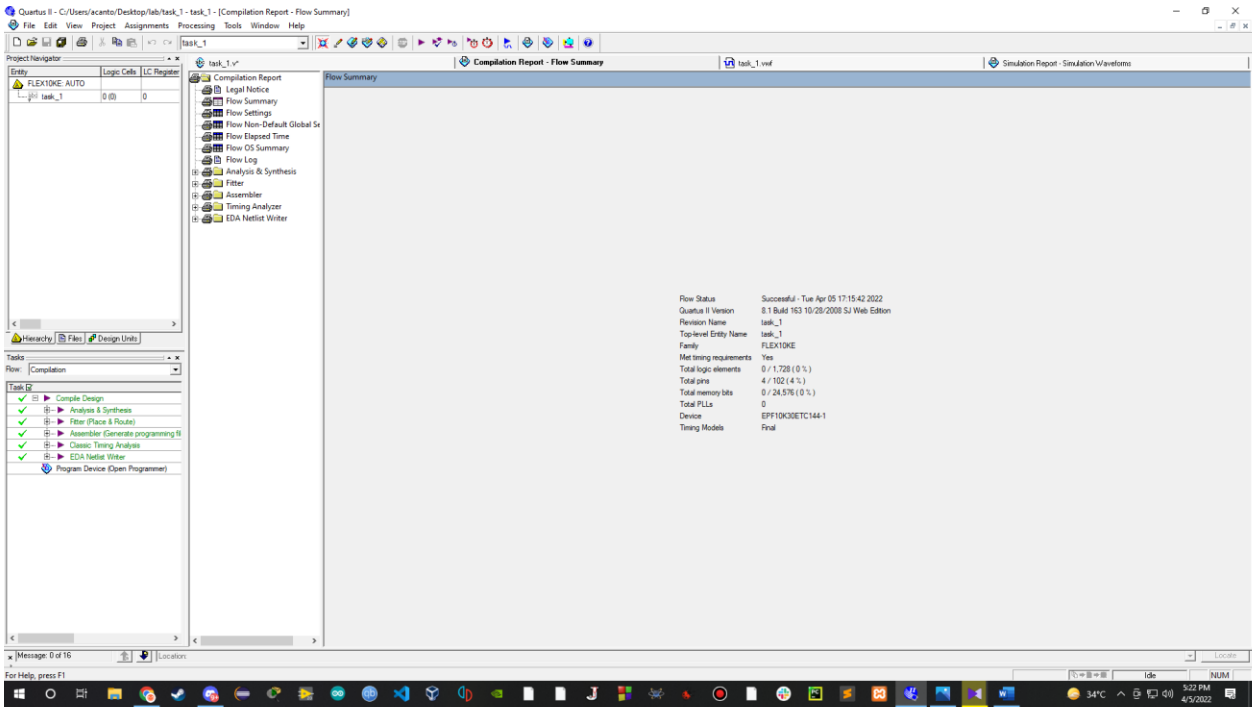
Code:

```
module task_1(clk,resetn,w,z);


input clk,resetn,w;

output reg z;

reg y, Y;

parameter [3:1] q0=3'b000,

                                        q1=3'b001,

                                        q2=3'b010,

                                        q3=3'b011,

                                        q4=3'b100;

always@(w,y)

          case (y)

                    q0: if (w)

                    begin

                    z = 0;

                    Y = q1;

                    end

                    else

                    begin

                    z = 0;

                    Y = q0;

                    end

                    q1: if (w)

                    begin

                    z = 0;

                    Y = q1;

                    end

                    else

                    begin
```

```
z = 0;
Y = q2;
end
q2: if (w)
begin
z = 0;
Y = q3;
end
else
begin
z = 0;
Y = q0;
end
q3: if (w)
begin
z = 0;
Y = q0;
end
else
begin
z = 1;
Y = q4;
end
q4: if (w)
begin
z = 0;
Y = q3;
end
else
```

```
                begin
                z = 0;
                Y = q0;
                end
        endcase

always @ (negedge resetn, posedge clk)
        if (resetn == 0) y <= q0;
        else y<=Y;
endmodule
```

compilation report:

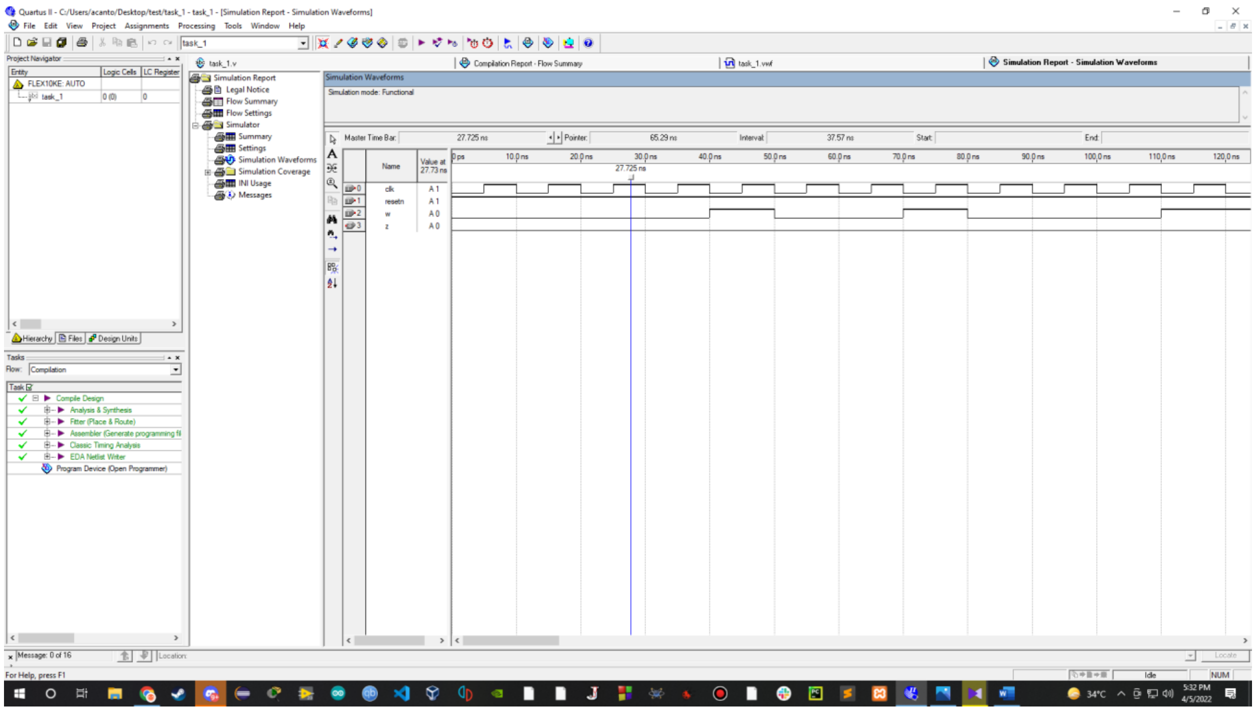


Quartus II - C:/Users/acanto/Desktop/lab/task_1 - task_1 - [Compilation Report - Flow Summary]

Flow Summary

```
Flow Status                 Successful - Tue Apr 05 17:15:42 2022
Quartus II Version          8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name               task_1
Top-level Entity Name       task_1
Family                      FLEX10KE
Met timing requirements     Yes
Total logic elements        0 / 1,728 ( 0 % )
Total pins                  4 / 102 ( 4 % )
Total memory bits           0 / 24,576 ( 0 % )
Total PLLs                  0
Device                      EPF10K30ETC144-1
Timing Models               Final
```

simulation report:


Quartus II - C:/Users/acanto/Desktop/test/task_1 - task_1 - [Simulation Report - Simulation Waveforms]

Simulation Waveforms

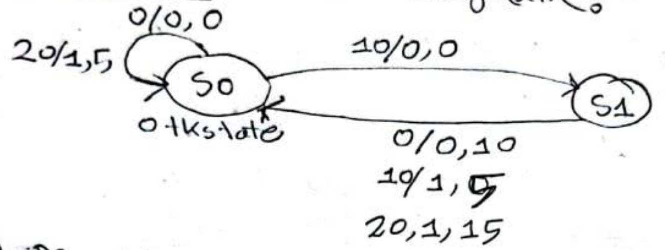
Simulation mode: Functional

Master Time Bar: 27.725 ns   Pointer: 65.29 ns   Interval: 37.57 ns   Start: End:

	Name	Value at 27.73 ns
0	clk	A 1
1	resetn	A 1
2	w	A 0
3	z	A 0

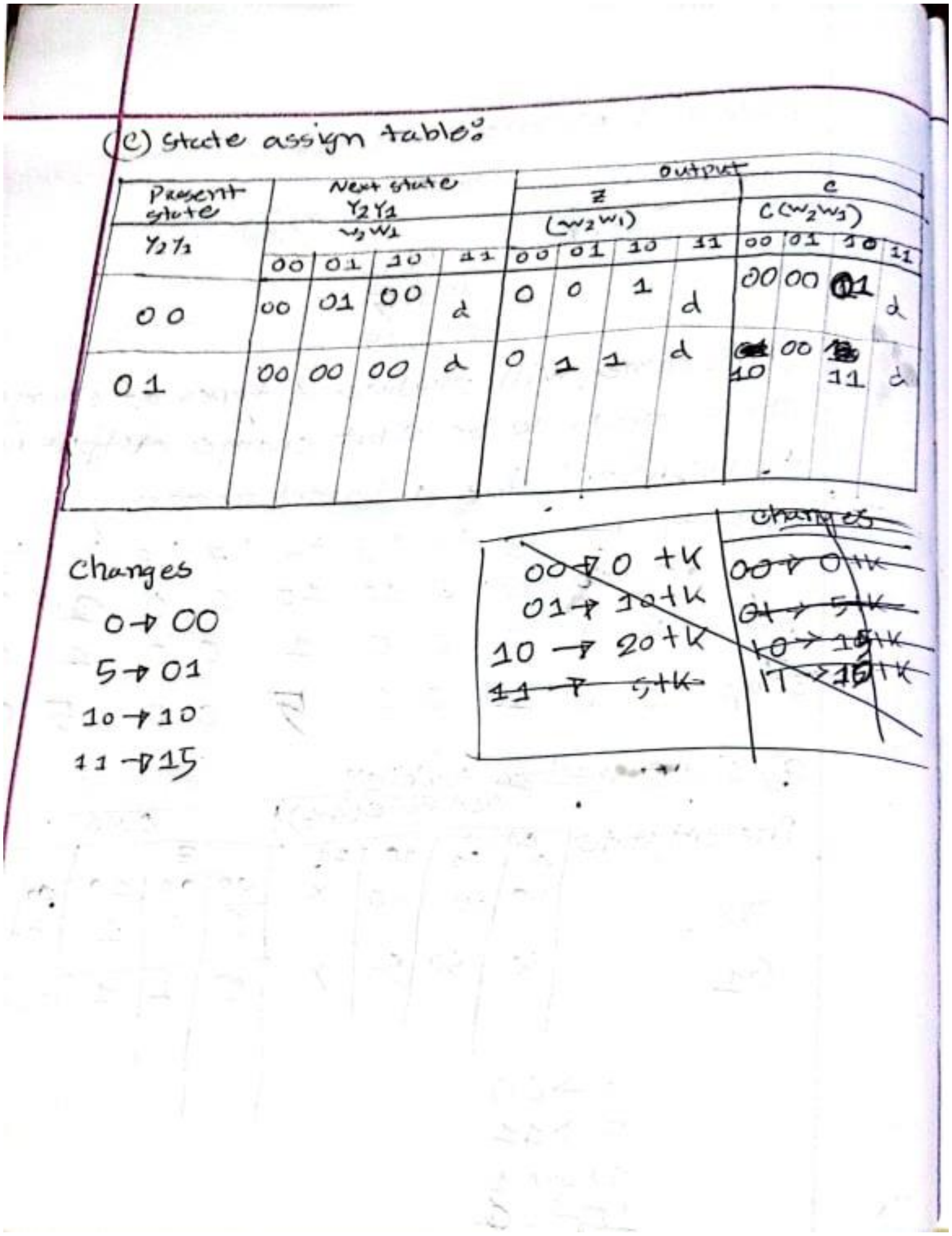
Task 2:

Problem 2: A) State diagram:



B) Machine will produce 4 types of changes. There needs to be 2 bit change output required to represent the returned money.

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
mny	0	10	0	0	10	10	0	0	10	0
buy	0	0	0	0	0	1	0	0	1	0
chang	0	0	10	0	0	5	0	0	5	0



(c) State assign table:

Present state	Next state Y_2Y_1				Output							
					Z				C			
	w_2w_1				(w_2w_1)				$C(w_2w_1)$			
y_2y_1	00	01	10	11	00	01	10	11	00	01	10	11
00	00	01	00	d	0	0	1	d	00	00	01	d
01	00	00	00	d	0	1	1	d	10	00	11	d

Changes

0	00
5	01
10	10
11	15

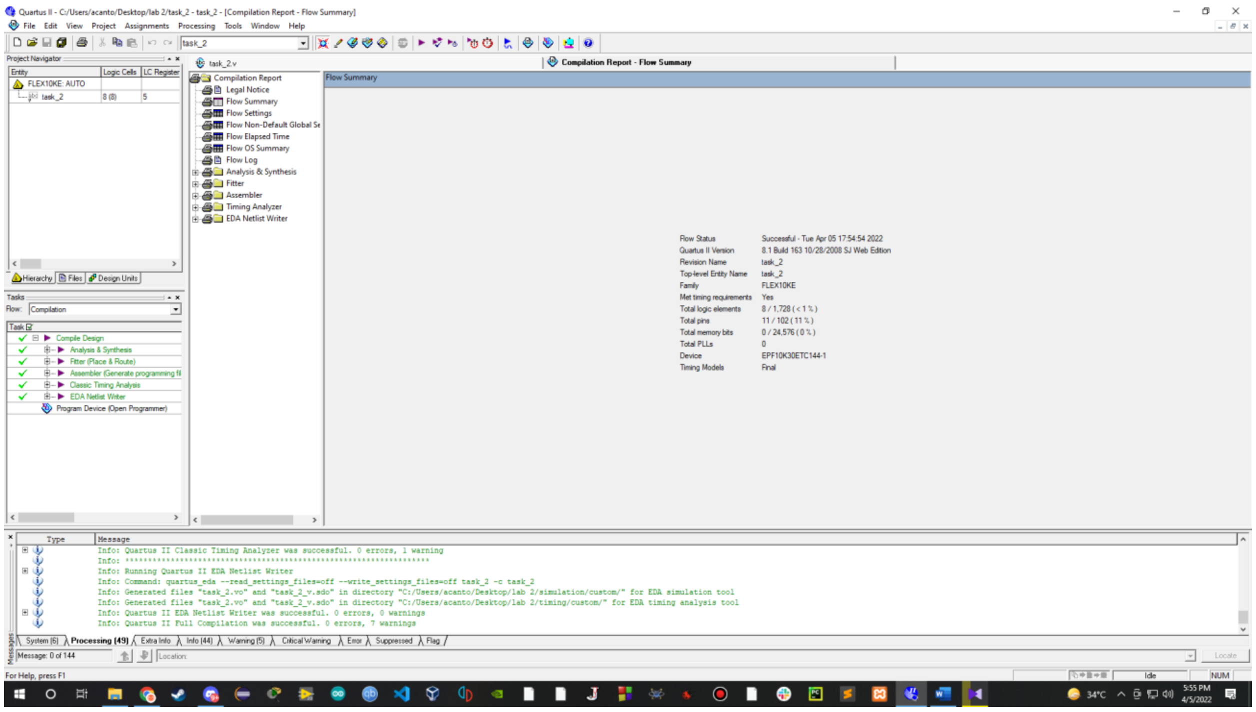
	changes
~~00 → 0 +K~~	~~00 → 0 +K~~
~~01 → 10+K~~	~~01 → 5+K~~
~~10 → 20+K~~	~~10 → 15+K~~
~~11 → 5+K~~	~~11 → 15+K~~

Code:

```
module task_2(clock, reset, cash_in, purchase, present_state, next_state, cash_return);
        input clock, reset;
input [1:0] cash_in;
output reg purchase;
output reg [1:0] cash_return, present_state, next_state;
parameter       state0= 2'b00,
                    state1= 2'b01,
                    n = 15,
                    R0= 2'b00,
                    R5= 2'b01,
                    R10= 2'b10,
                    R15= 2'b11;

always@(posedge clock)
begin
        if(reset==1)
        begin
            present_state = state0;
            next_state = state0;
        end
        else
        begin
            present_state = next_state;

            case(present_state)
            state0: if(cash_in == 2'b00)
                        begin
                            next_state = state0;
                            purchase =0;
                            cash_return = R0;
                        end
                    else if(cash_in == 2'b01)
                        begin
                            next_state = state1;
                            purchase = 0;
                            cash_return = R0;
                        end
                    else if(cash_in == 2'b10)
                        begin
                            next_state = state0;
                            purchase = 1;
                            cash_return = R5;
                        end

            state1: if(cash_in == 2'b00)
                        begin
                            next_state = state0;
                            purchase =0;
                            cash_return = R10;
                        end
                    else if(cash_in == 2'b01)
                        begin
                            next_state=state0;
                            purchase = 1;
                            cash_return = R5;
                        end
                    else if(cash_in == 2'b10)
                        begin
                            next_state=state0;
                            purchase=1;
```

```
                                                            cash_return = R15;
                                                      end
                                    endcase
                              end
                  end
                  endmodule
```

compilation report:

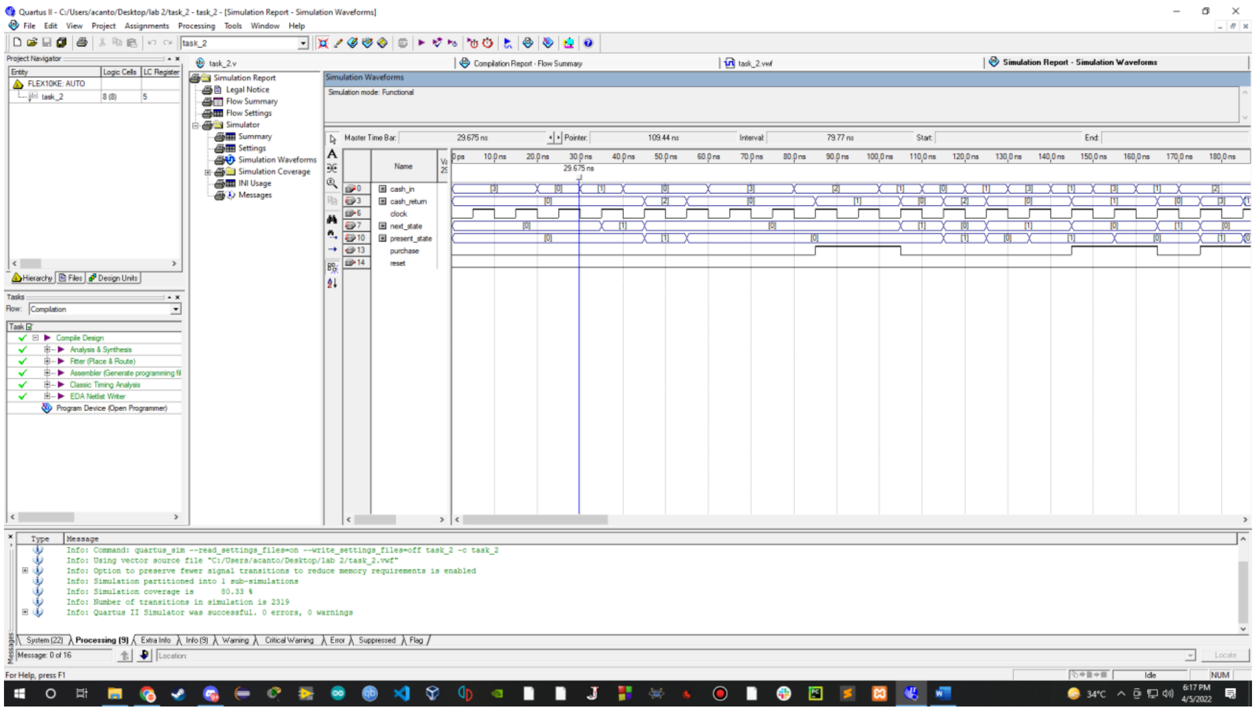


Quartus II - C:/Users/acanto/Desktop/lab 2/task_2 - task_2 - [Compilation Report - Flow Summary]

```
Flow Status                 Successful - Tue Apr 05 17:54:54 2022
Quartus II Version          8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name               task_2
Top-level Entity Name       task_2
Family                      FLEX10KE
Met timing requirements     Yes
Total logic elements        8 / 1,728 ( < 1 % )
Total pins                  11 / 102 ( 11 % )
Total memory bits           0 / 24,576 ( 0 % )
Total PLLs                  0
Device                      EPF10K30ETC144-1
Timing Models               Final
```

```
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info: *******************************************************************
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off task_2 -c task_2
Info: Generated files "task_2.vo" and "task_2_v.sdo" in directory "C:/Users/acanto/Desktop/lab 2/simulation/custom/" for EDA simulation tool
Info: Generated files "task_2.vo" and "task_2_v.sdo" in directory "C:/Users/acanto/Desktop/lab 2/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 7 warnings
```

simulation report:



```
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off task_2 -c task_2
Info: Using vector source file "C:/Users/acanto/Desktop/lab 2/task_2.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      80.33 %
Info: Number of transitions in simulation is 2319
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```