



VOLTAGE-DIVIDER

JFET DC BIASING

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TOPIC OUTLINE

Voltage-Divider Bias

- Gate-to-Source Loop
- Drain-to-Source Loop
- Transconductance Curve



VOLTAGE-DIVIDER BIAS



GENERAL RELATIONSHIPS

Gate Current

$$i_G \cong 0$$

Drain Current

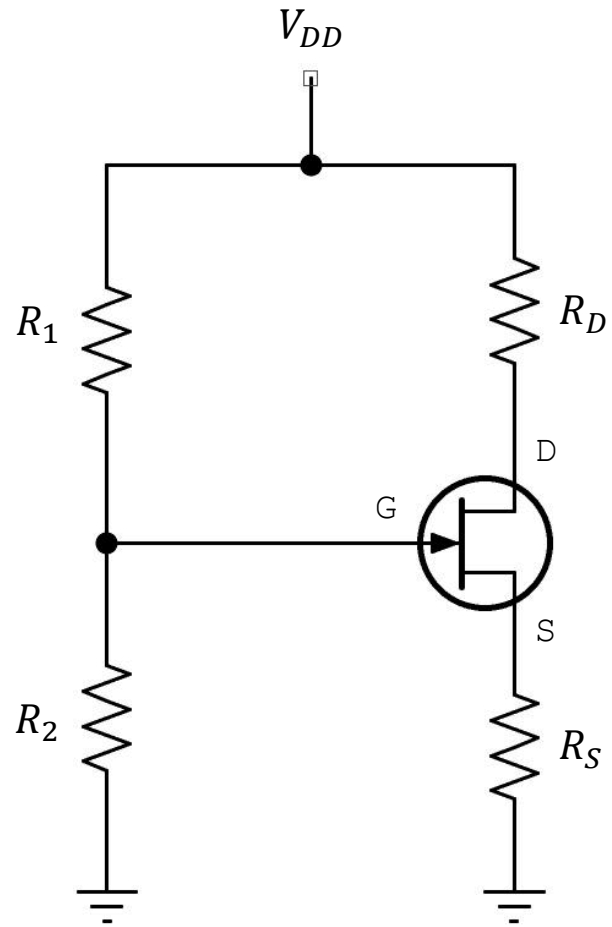
$$i_D = I_{DSS} \left(1 - \frac{v_{GS}}{V_P} \right)^2$$

Source Current

$$i_D = i_S$$

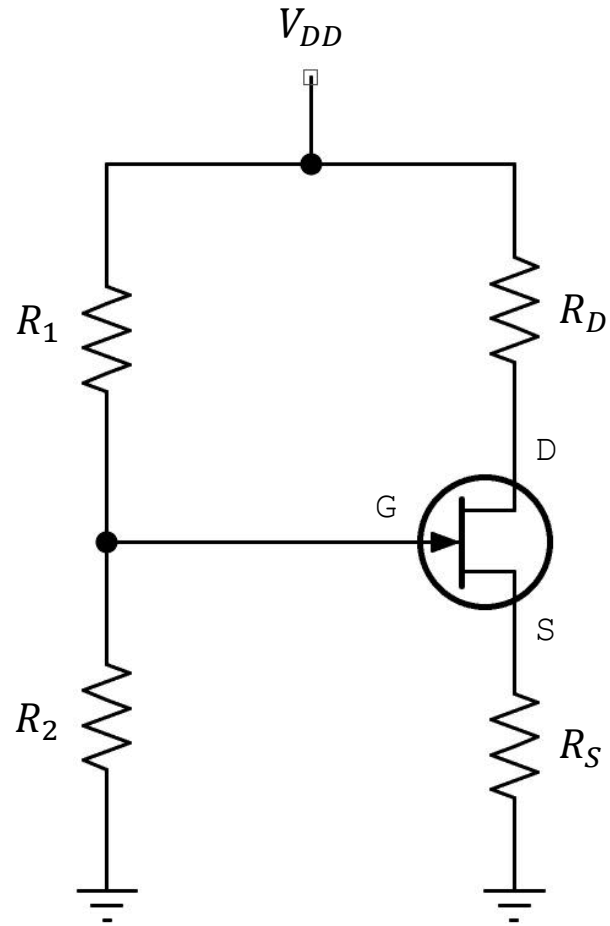


VOLTAGE-DIVIDER BIAS CONFIGURATION



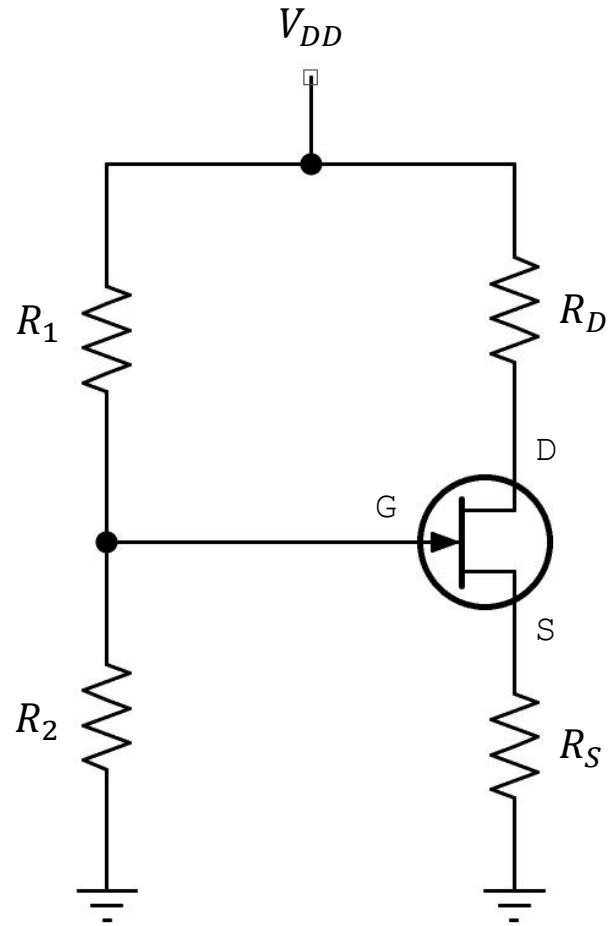
GATE-TO-SOURCE

KVL @ G-S

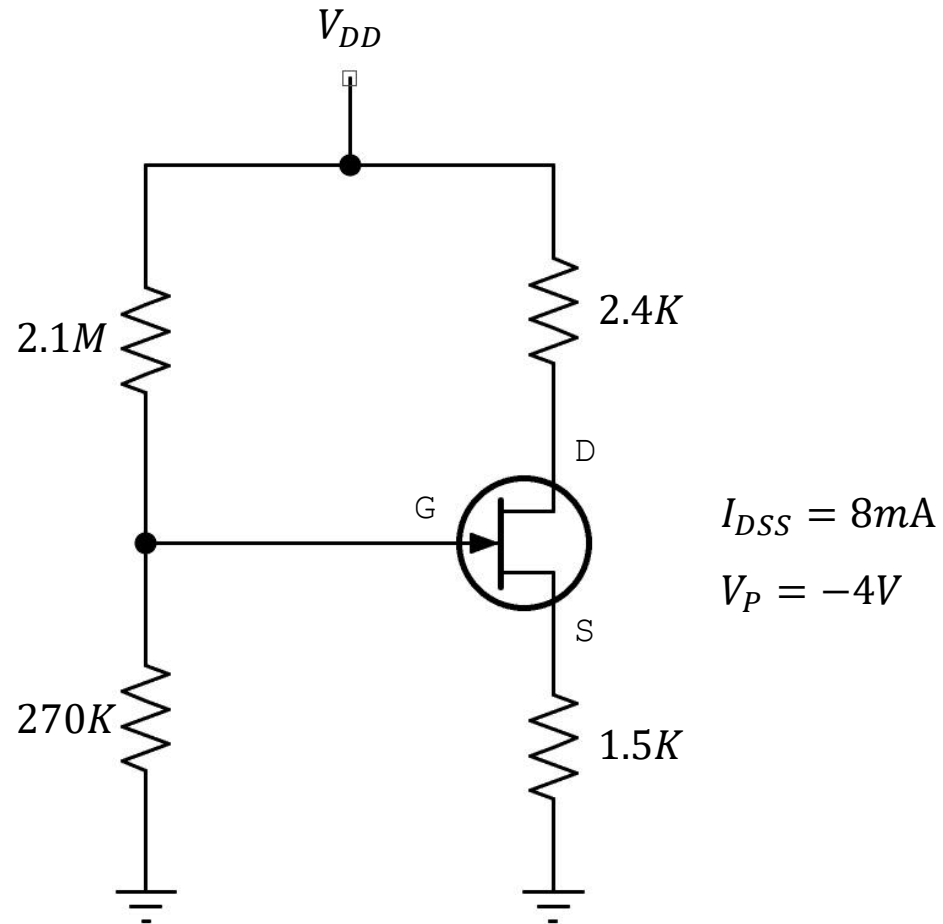


DRAIN-TO-SOURCE

KVL @ D-S



EXERCISE



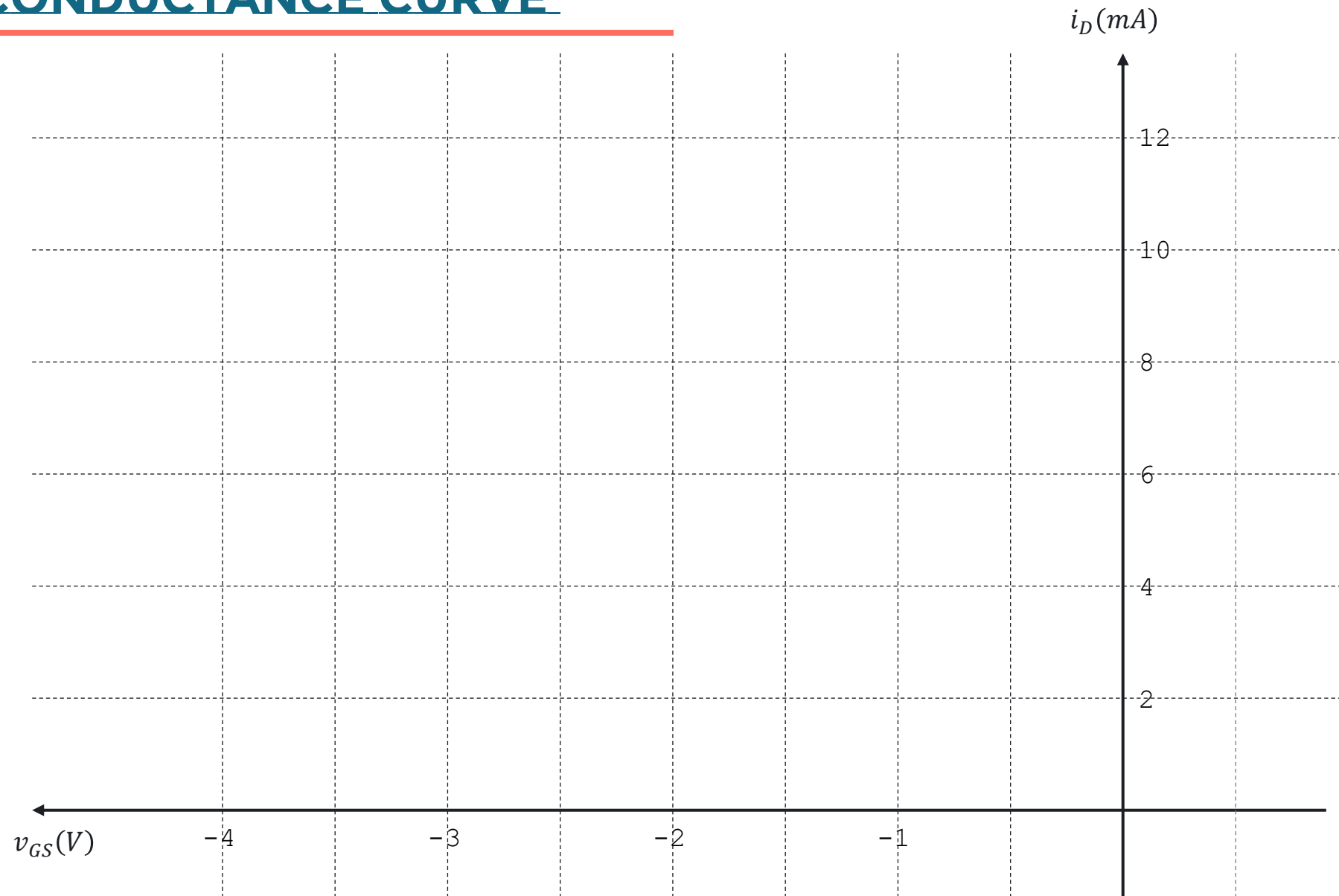
For the given network, determine the following :

- Gate voltage (v_G)
- Source voltage (v_S)
- Gate-source voltage (v_{GSQ})
- Drain current (i_{DQ})
- Drain-source voltage (v_{DS})
- Source voltage (v_S)

and sketch the transconductance curve.



TRANSCONDUCTANCE CURVE



LABORATORY

