FIXED-BIAS CIRCUIT

BJT DC BIASING

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TOPIC OUTLINE

Fixed-Bias Circuit

- Base-Emitter Loop
- Collector-Emitter Loop
- Load Line Analysis

FIXED-BIAS CIRCUIT

CURRENT GAIN

The **current gain** parameters **alpha** (α) and **beta** (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

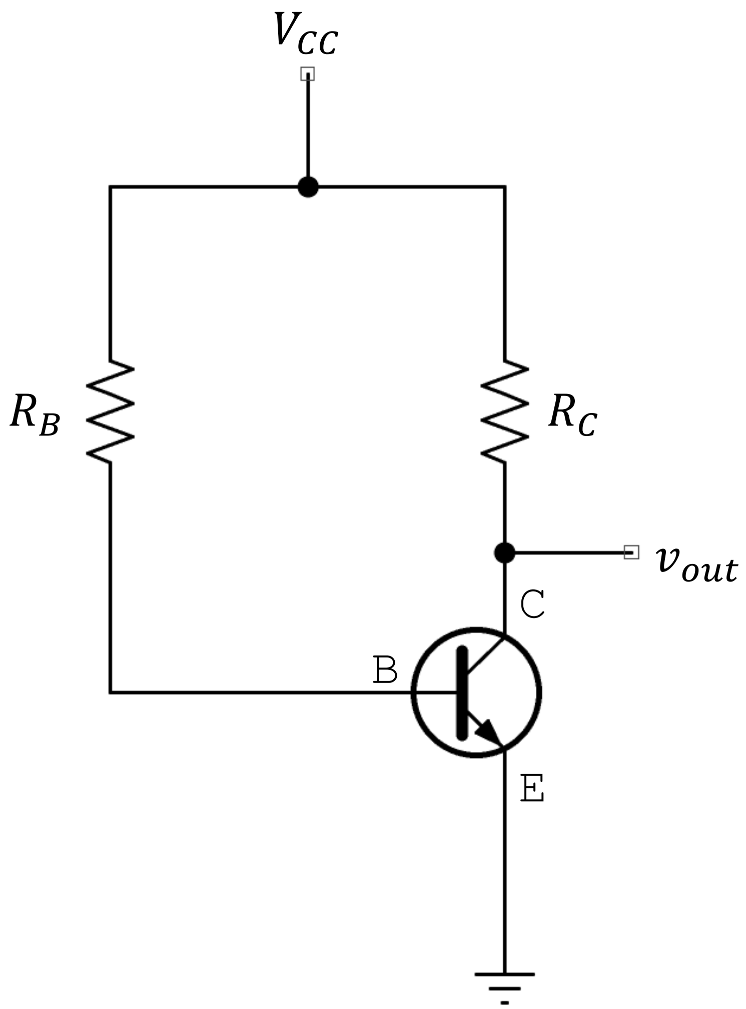
α is always less than 1 (typically 0.95 to 0.995)

Beta (β) is the ratio of the collector current to the base current.

Formula

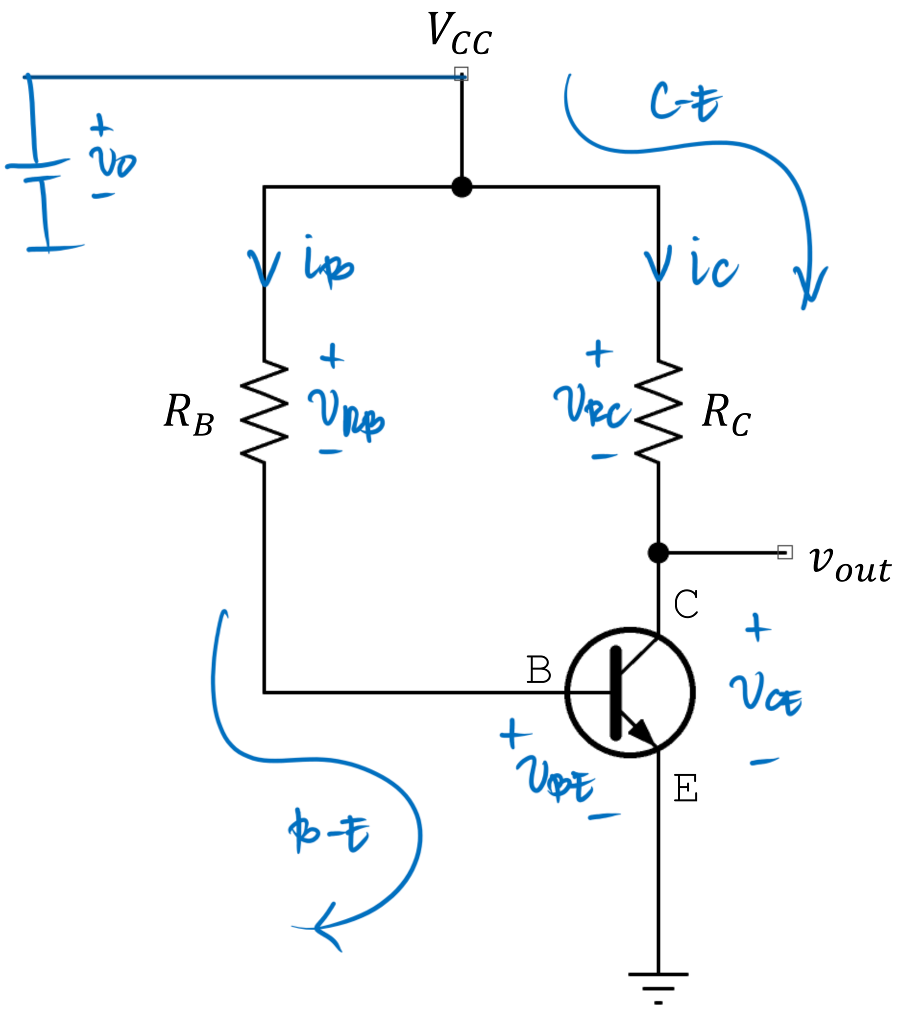
$$\beta = \frac{i_C}{i_B}$$

FIXED-BIAS CIRCUIT



Fixed-bias configuration is the simplest method – the biasing voltage applied to the base of the BJT is fixed by a single resistor (R_B) connected directly to the power supply (v_{CC}).

BASE-EMITTER LOOP



KVL @B-E

$$-\overset{V_{cc}}{\cancel{v_o}} + \underline{v_{RB}} + v_{BE} = 0$$

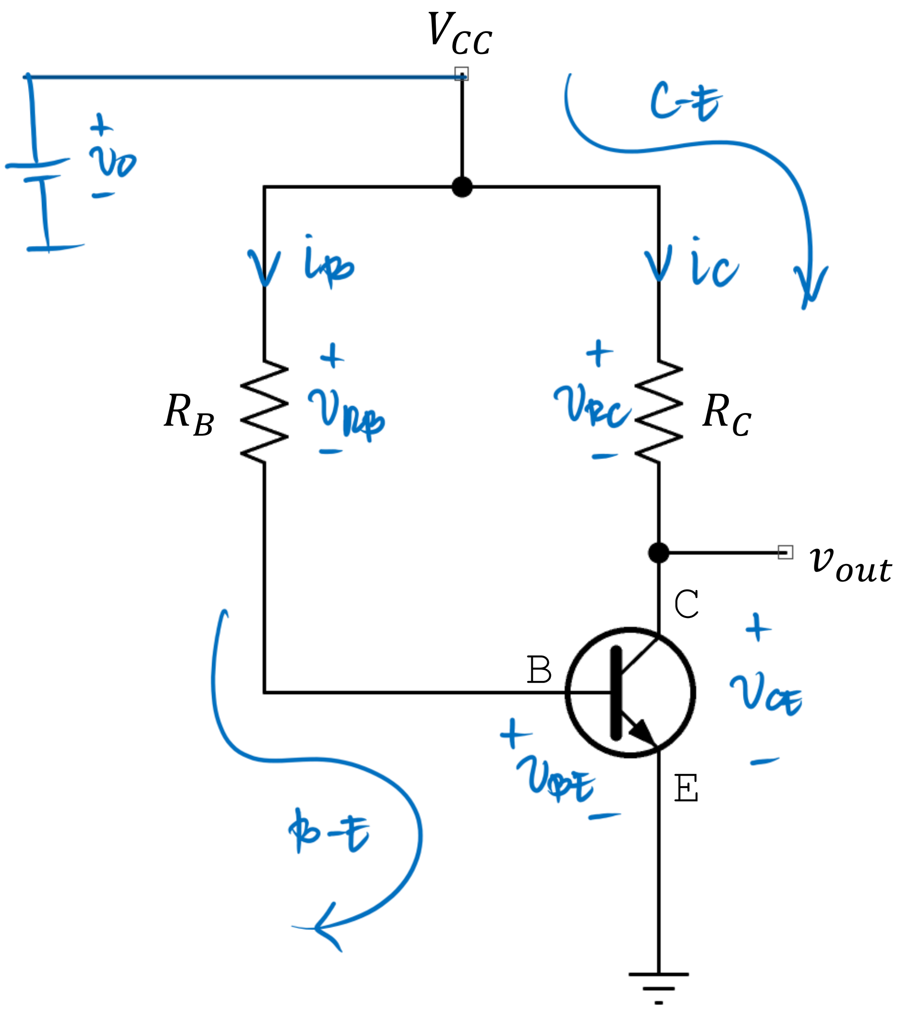
$$v_{RB} = V_{cc} - v_{BE}$$

$$\frac{i_B \cancel{R_B}}{\cancel{R_B}} = \frac{V_{cc} - v_{BE}}{R_B}$$

$$\boxed{i_B = \frac{V_{cc} - v_{BE}}{R_B}}$$

Fixed-Bias

COLLECTOR-EMITTER LOOP



KVL @C-E

$$\xcancel{-v_o}^{\;V_{CC}} + v_{RC} + \underline{v_{CE}} = 0$$

$$v_{CE} = V_{CC} - v_{RC}$$

$$\boxed{v_{CE} = V_{CC} - i_C R_C}$$

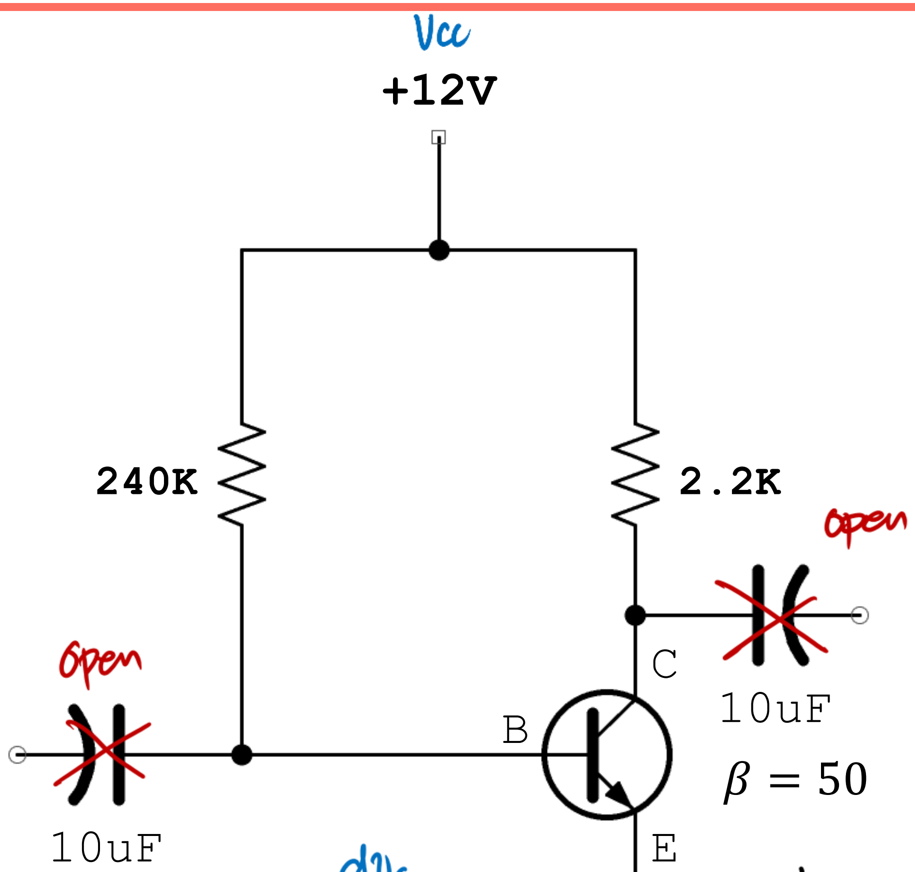
Fixed-bias

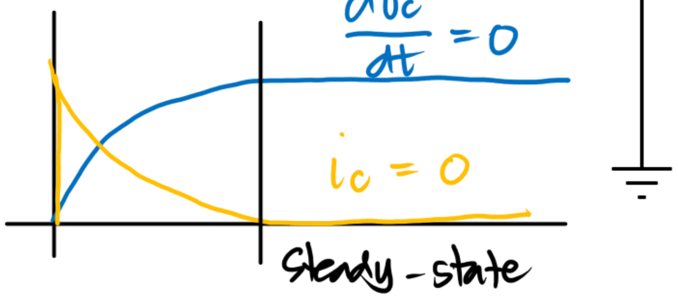
Current Gain

$$\beta = \frac{i_C}{i_B}$$

$$\underline{i_C = \beta i_B}$$

EXERCISE



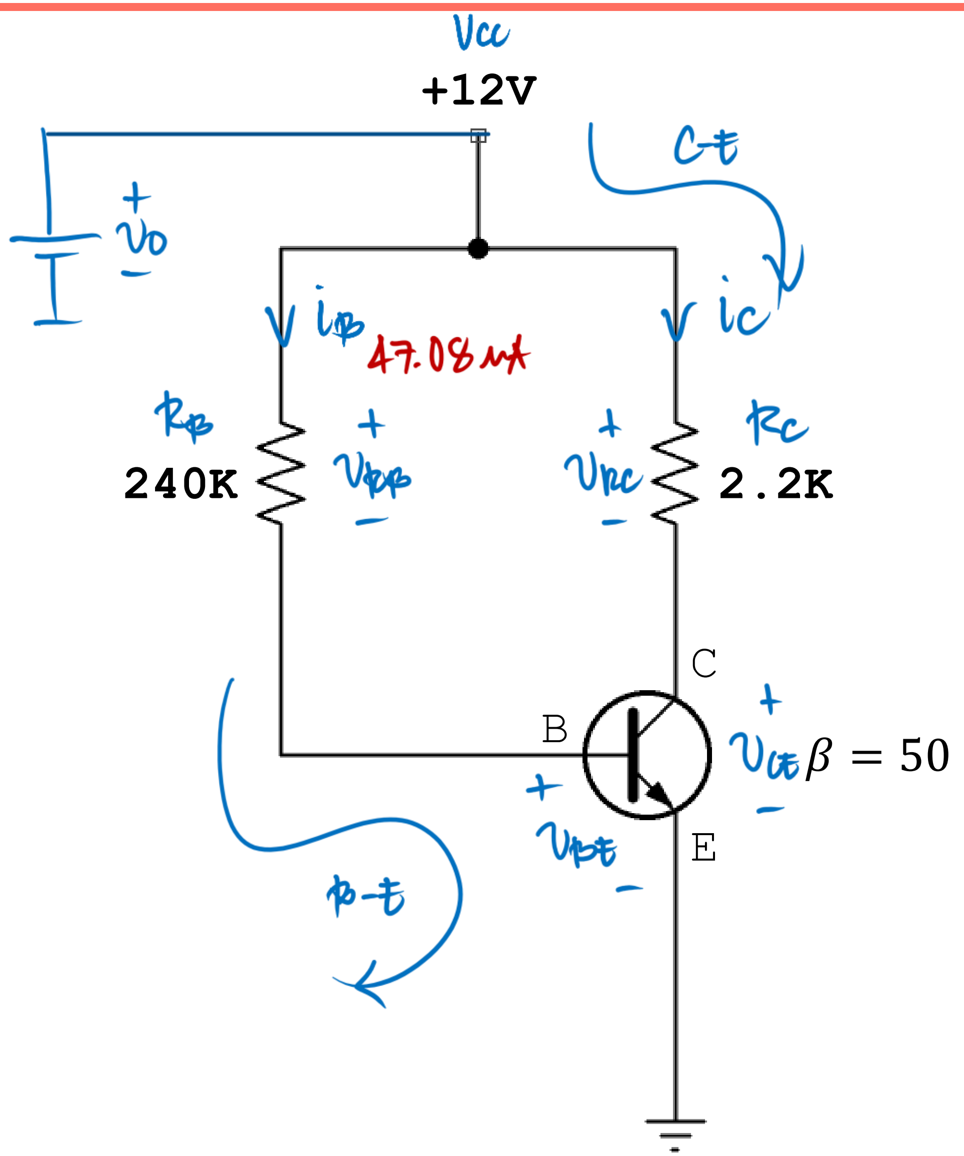


Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})
- Base voltage (v_B)
- Base-Collector voltage (v_{BC})

In DC analysis,
Replace capacitors w/
open ckt. equivalent.

EXERCISE



Solution

KVL @ b-E

$$-\cancel{V_0}^{V_{CC}} + \underline{V_{Rb}} + V_{bE} = 0$$

$$V_{Rb} = V_{CC} - V_{bE}$$

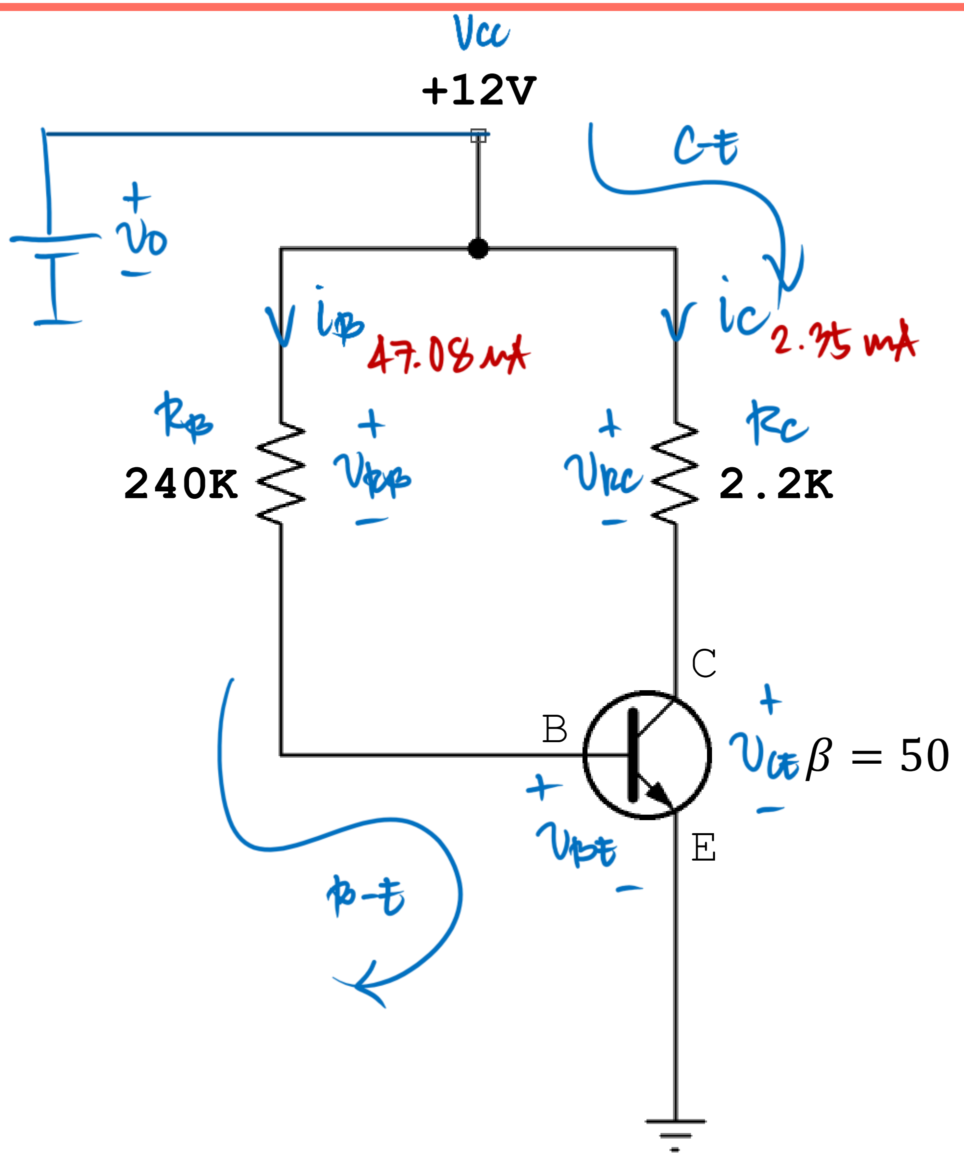
$$\frac{i_b \cancel{R_b}}{\cancel{R_b}} = \frac{V_{CC} - V_{bE}}{R_b}$$

$$i_b = \frac{12 - 0.7}{240k}$$

$$\boxed{i_b = 47.08\,\mu A}$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_C}{i_B}$$

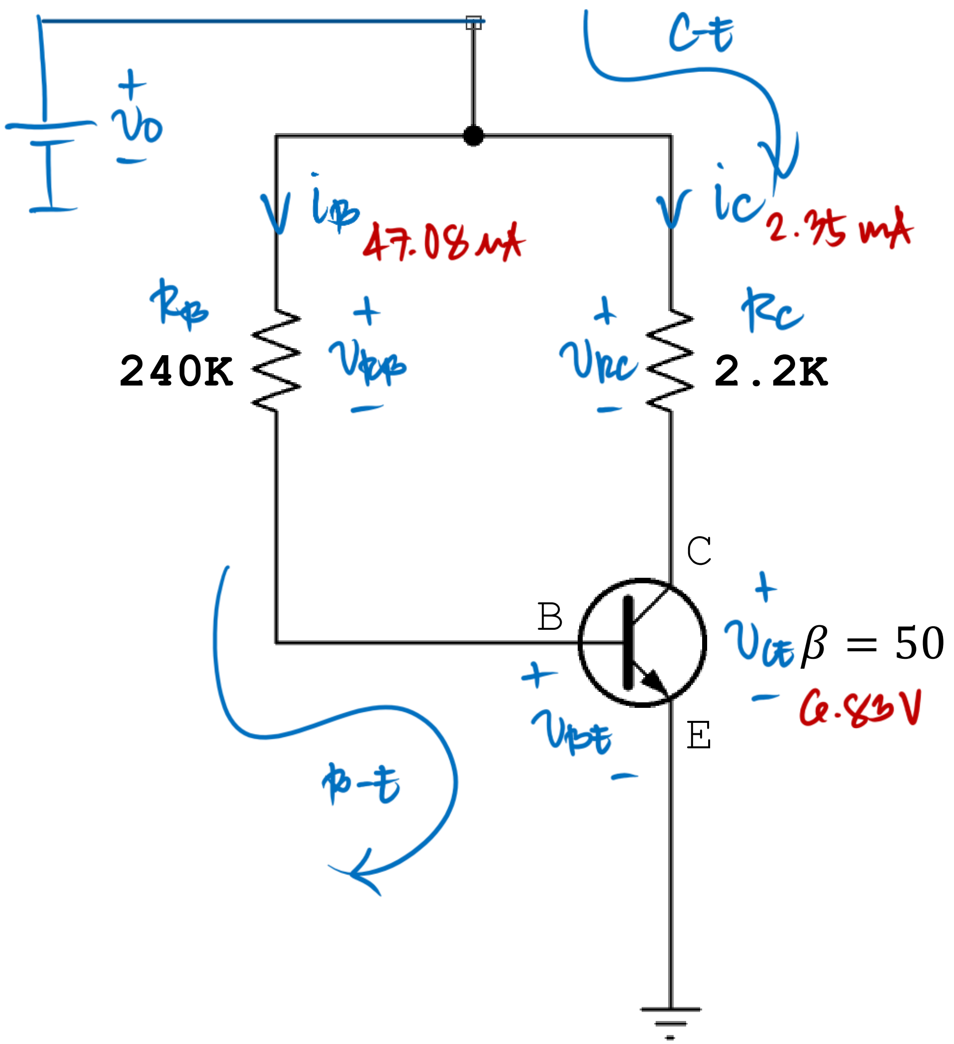
$$i_C = \beta i_B$$

$$i_C = 50\,(47.08\,\mu)$$

$$\boxed{i_C = 2.35\ \text{mA}}$$

ans

EXERCISE



Solution

KVL @ C-E

$$-\cancel{V_o}^{\,V_{cc}} + V_{RC} + V_{CE} = 0$$

$$V_{CE} = V_{cc} - V_{RC}$$

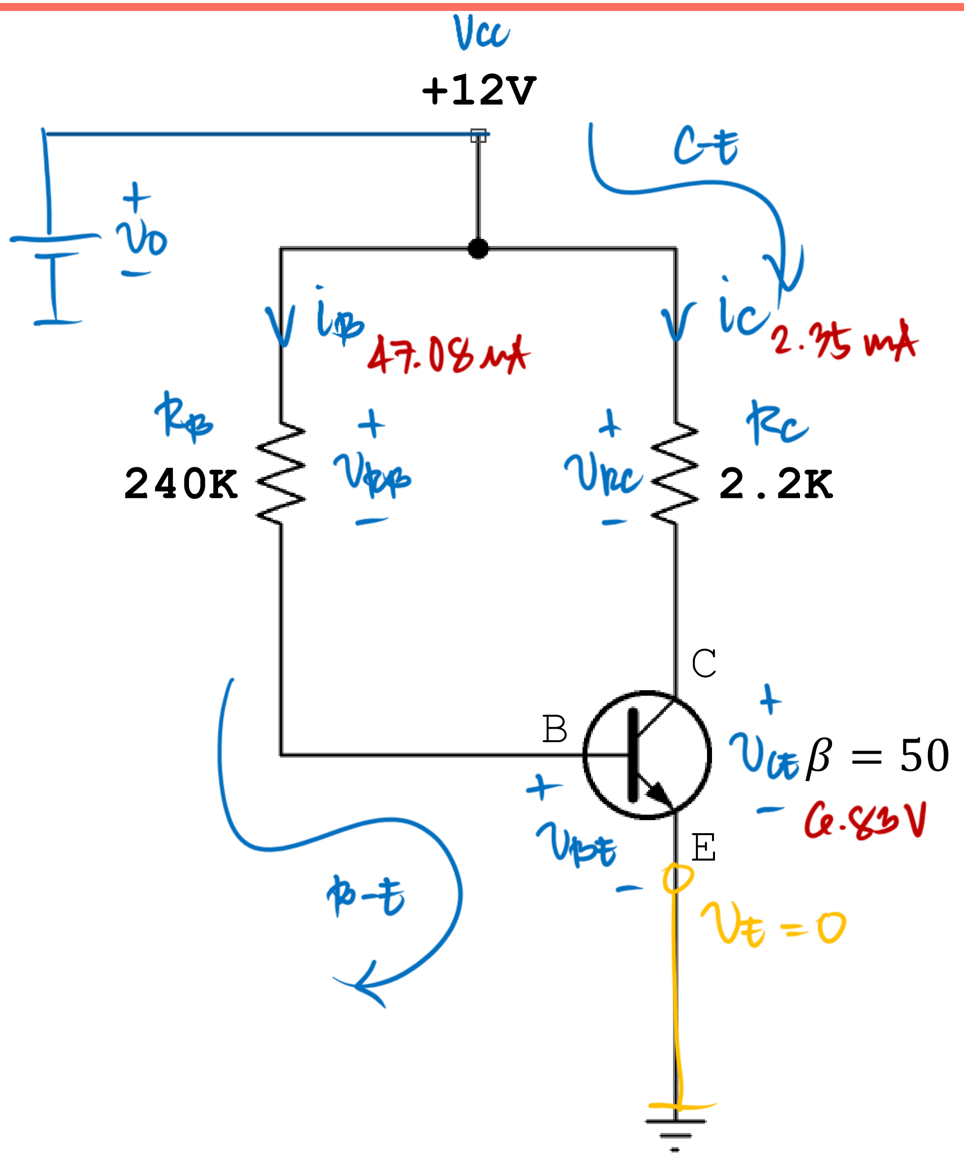
$$V_{CE} = V_{cc} - i_C R_C$$

$$V_{CE} = 12 - 2.35m(2.2k)$$

$$\boxed{V_{CE} = 6.83\,V}$$

ans

EXERCISE



Solution

Node Analysis

$$V_{BE} = V_B - \cancel{V_E}^{\,0}$$

$$\boxed{V_B = 0.7V}$$

ans

$$V_{CE} = V_C - \cancel{V_E}^{\,0}$$

$$\underline{V_C = 6.83V}$$

$$V_{BC} = V_B - V_C$$

$$V_{BC} = 0.7 - 6.83$$

$$\boxed{V_{BC} = -6.13V}$$

ans

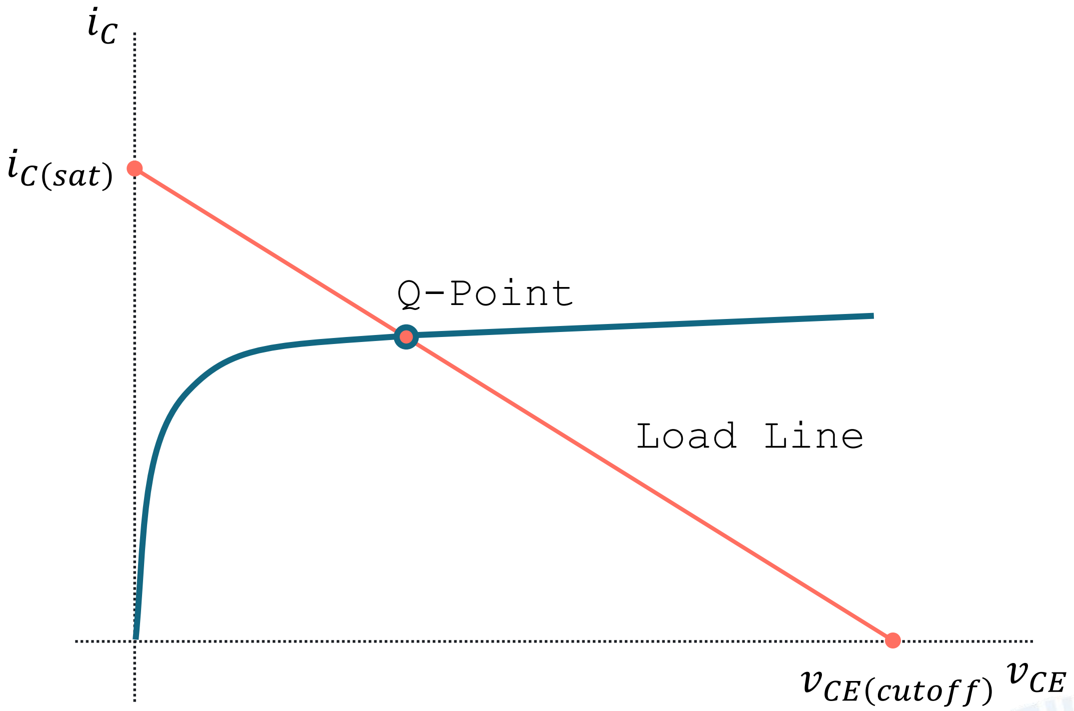
LOAD LINE ANALYSIS

SATURATION POINT

The **saturation point** is the operating state where BJT conducts the **maximum collector current** ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

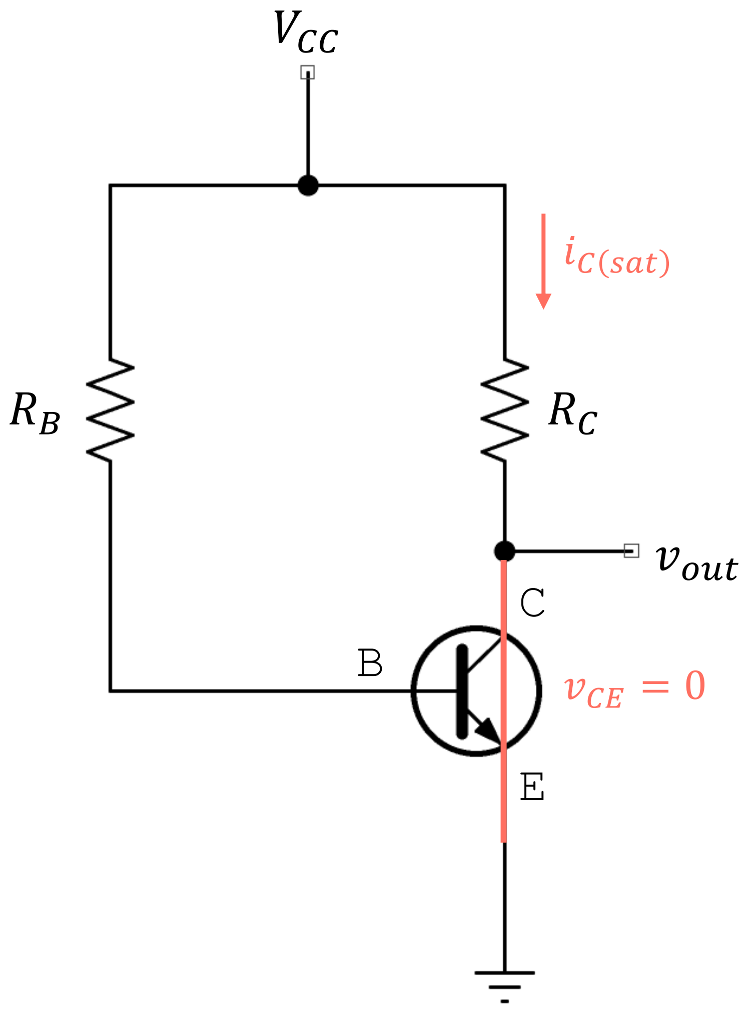
In this region the transistor acts like a **closed switch** (zero resistance between collector-emitter).

Collector Characteristic Curve

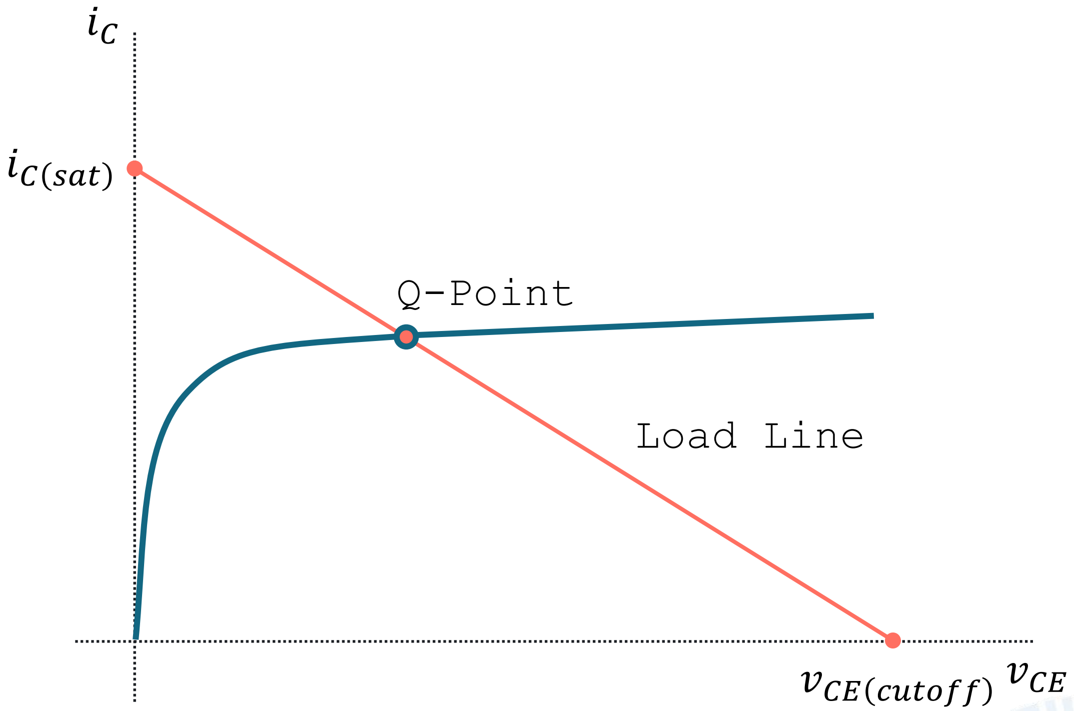


SATURATION POINT

Mentally Short



Collector Characteristic Curve

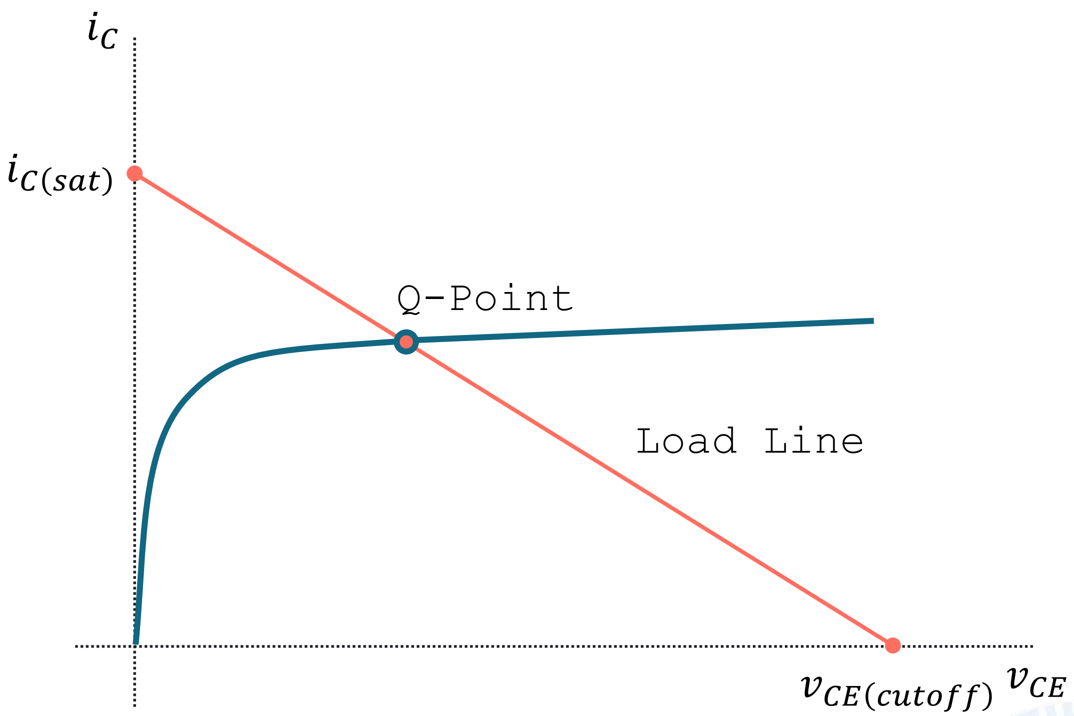


CUTOFF POINT

The **cutoff point** is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

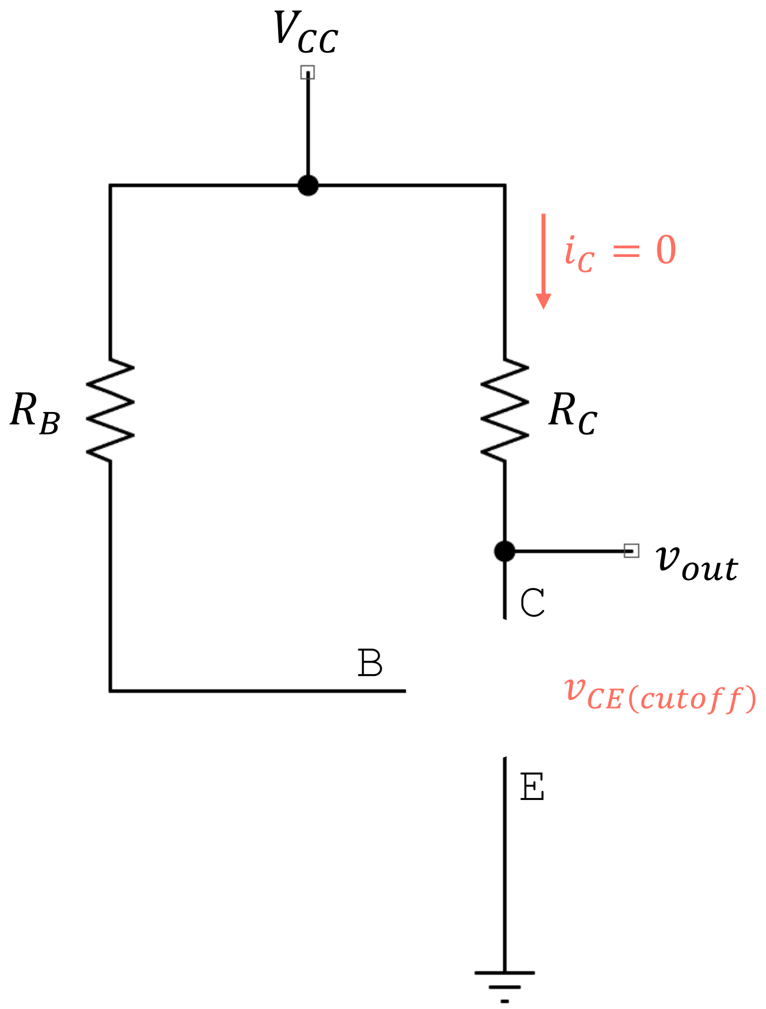
In this region the transistor acts like an **open switch** (infinite resistance between collector-emitter).

Collector Characteristic Curve

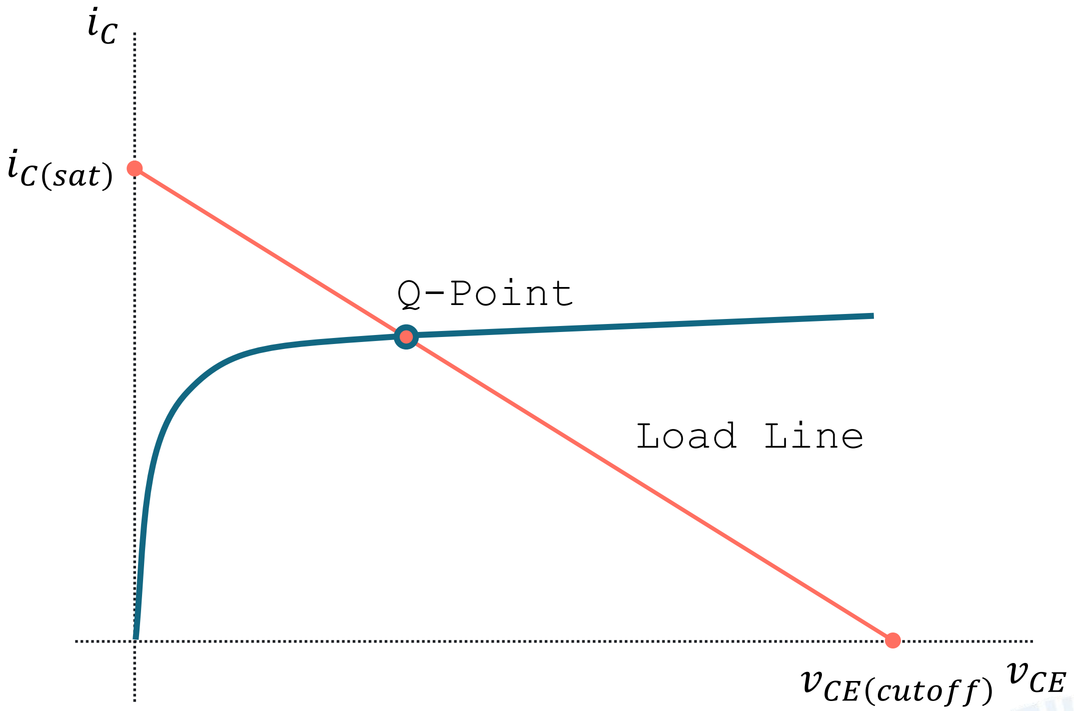


CUTOFF POINT

Mentally Open



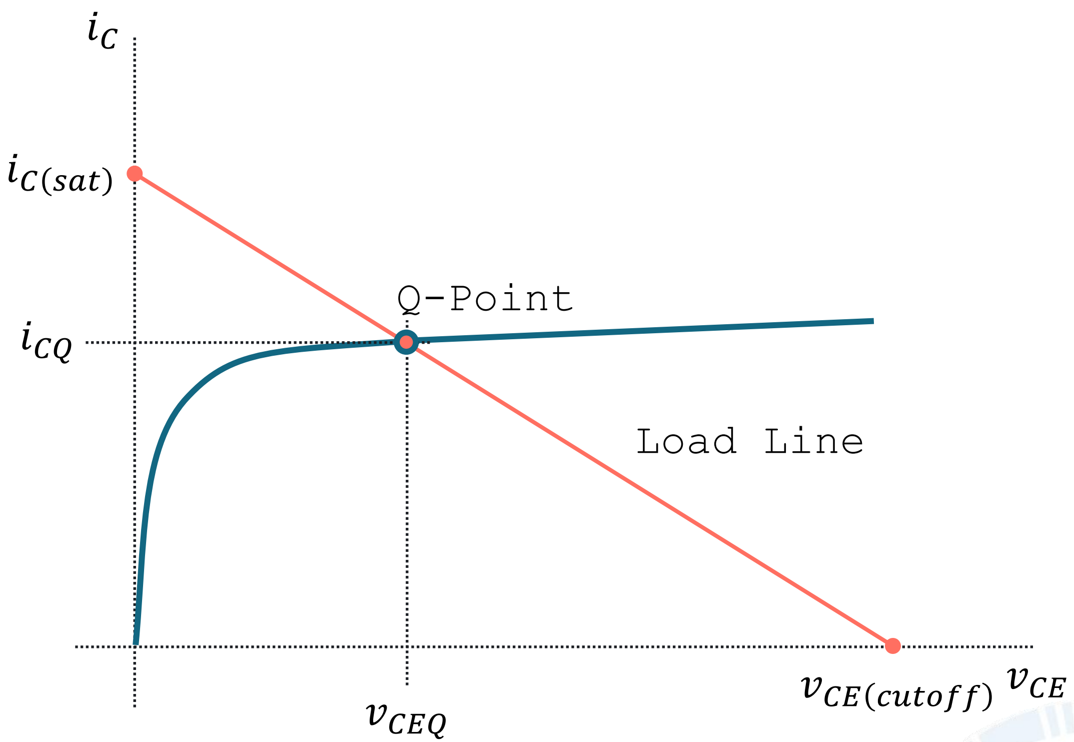
Collector Characteristic Curve



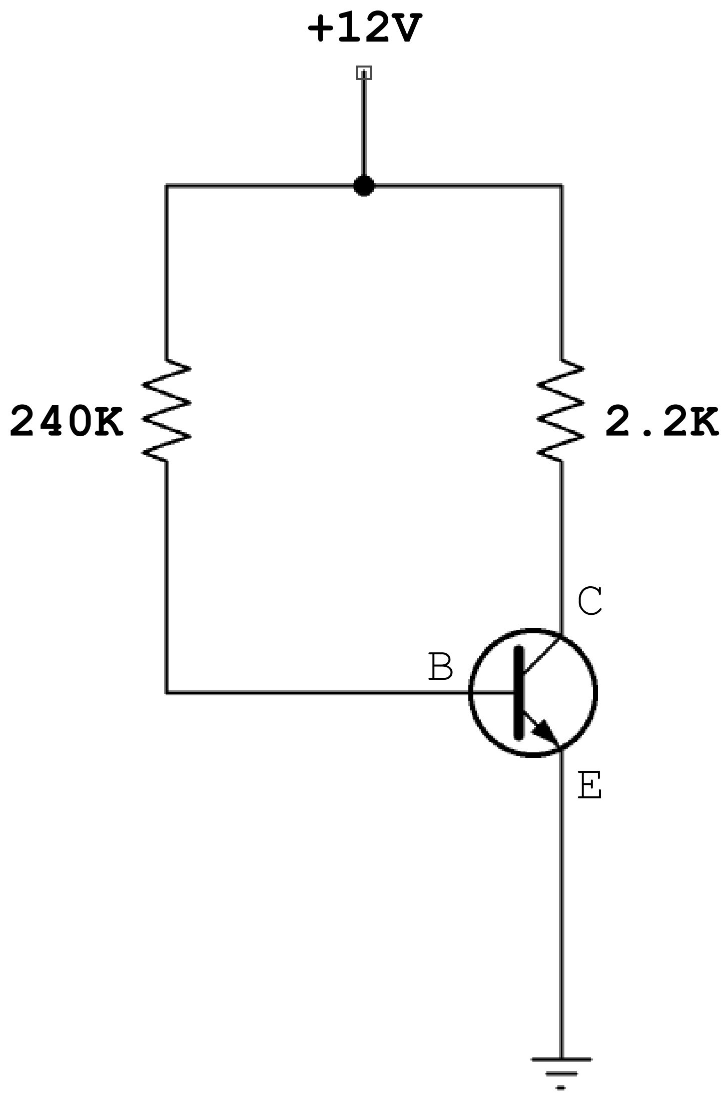
QUIESCENT POINT

The **Q-point** is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}).

Collector Characteristic Curve



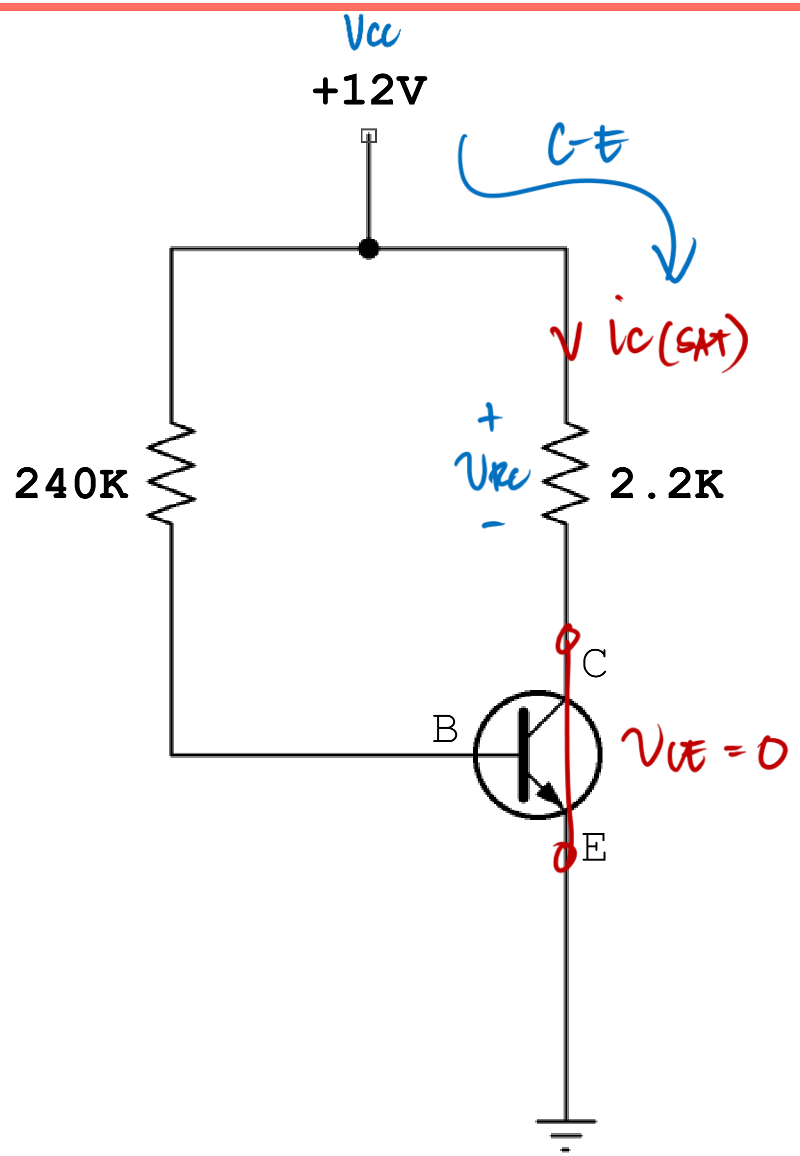
EXERCISE



Plot the DC load line for the fixed-bias circuit and clearly indicate the following points on the graph.

- Saturation current ($i_{C(sat)}$)
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

EXERCISE



Solution

Saturation Point

KVL @ C-E

$$-\cancel{V_o}^{\,V_{CC}} + V_{RC} + \cancel{V_{CE}}^{\,0} = 0$$

$$V_{RC} = V_{CC}$$

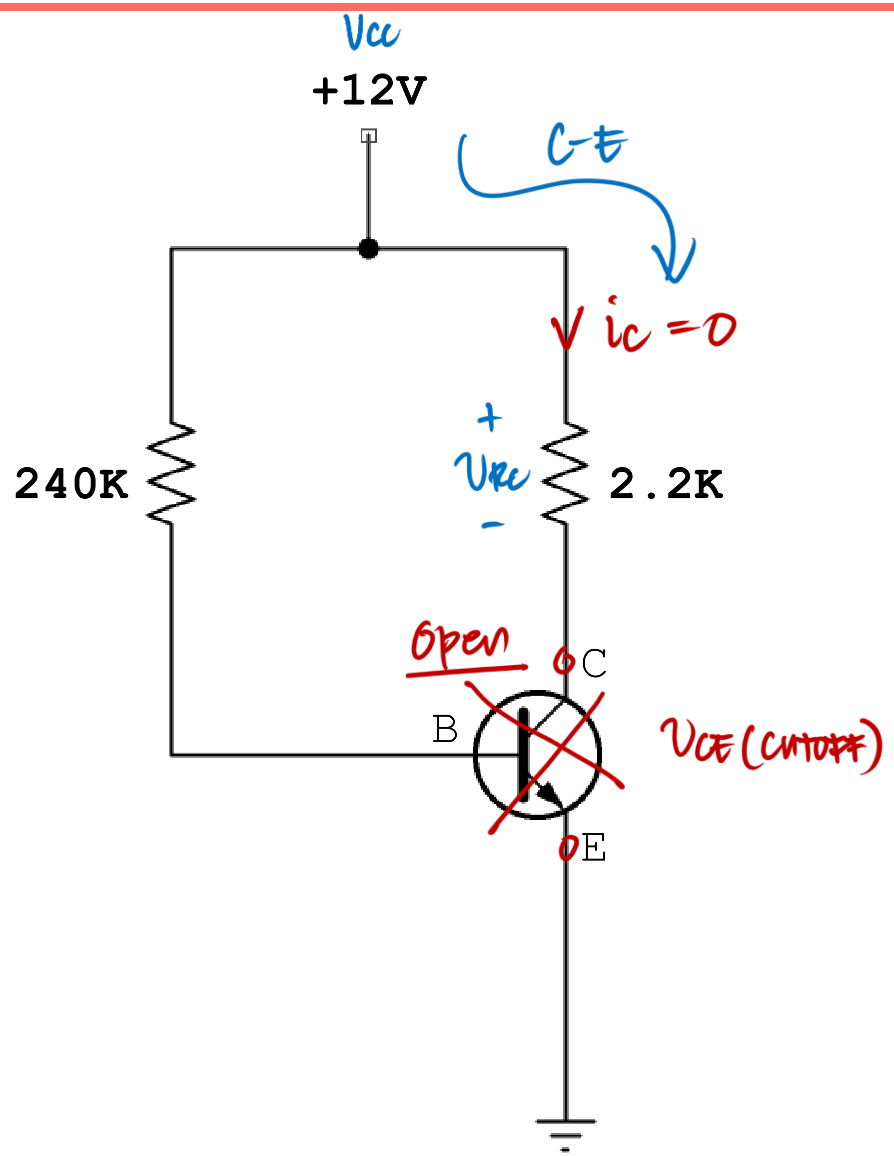
$$\frac{i_C \cancel{R_C}}{\cancel{R_C}} = \frac{V_{CC}}{R_C}$$

$$i_{C(SAT)} = \frac{12}{2.2K}$$

$$\boxed{i_{C(SAT)} = 5.45\ mA}$$

ans

EXERCISE



Solution

Cutoff Point

KVL @ C-E

$$-\overset{V_{CC}}{\cancel{V_0}} + \overset{0}{\cancel{V_{RC}}} + V_{CE} = 0$$

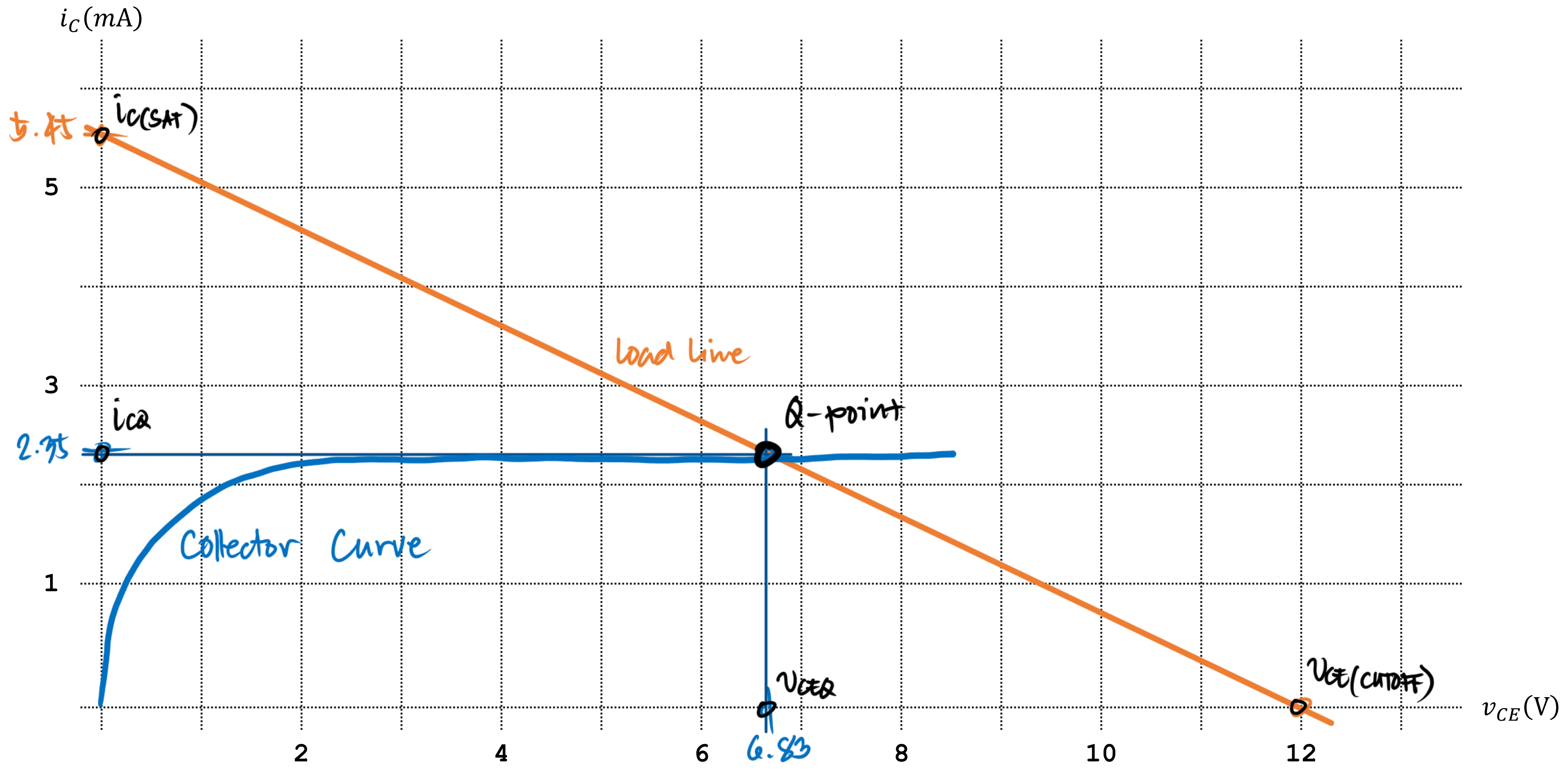
$$V_{CE(cutoff)} = V_{CC}$$

$$\boxed{V_{CE(cutoff)} = 12\,V}$$

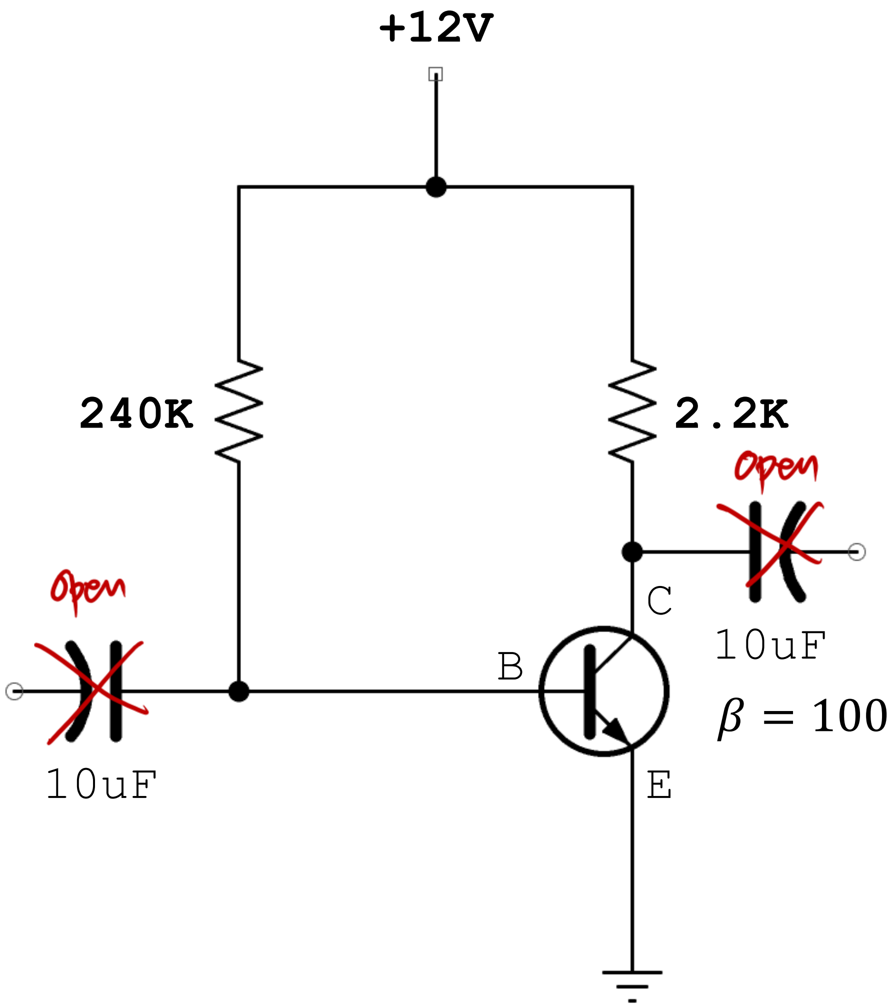
ans

EXERCISE

Load Line Analysis



EXERCISE



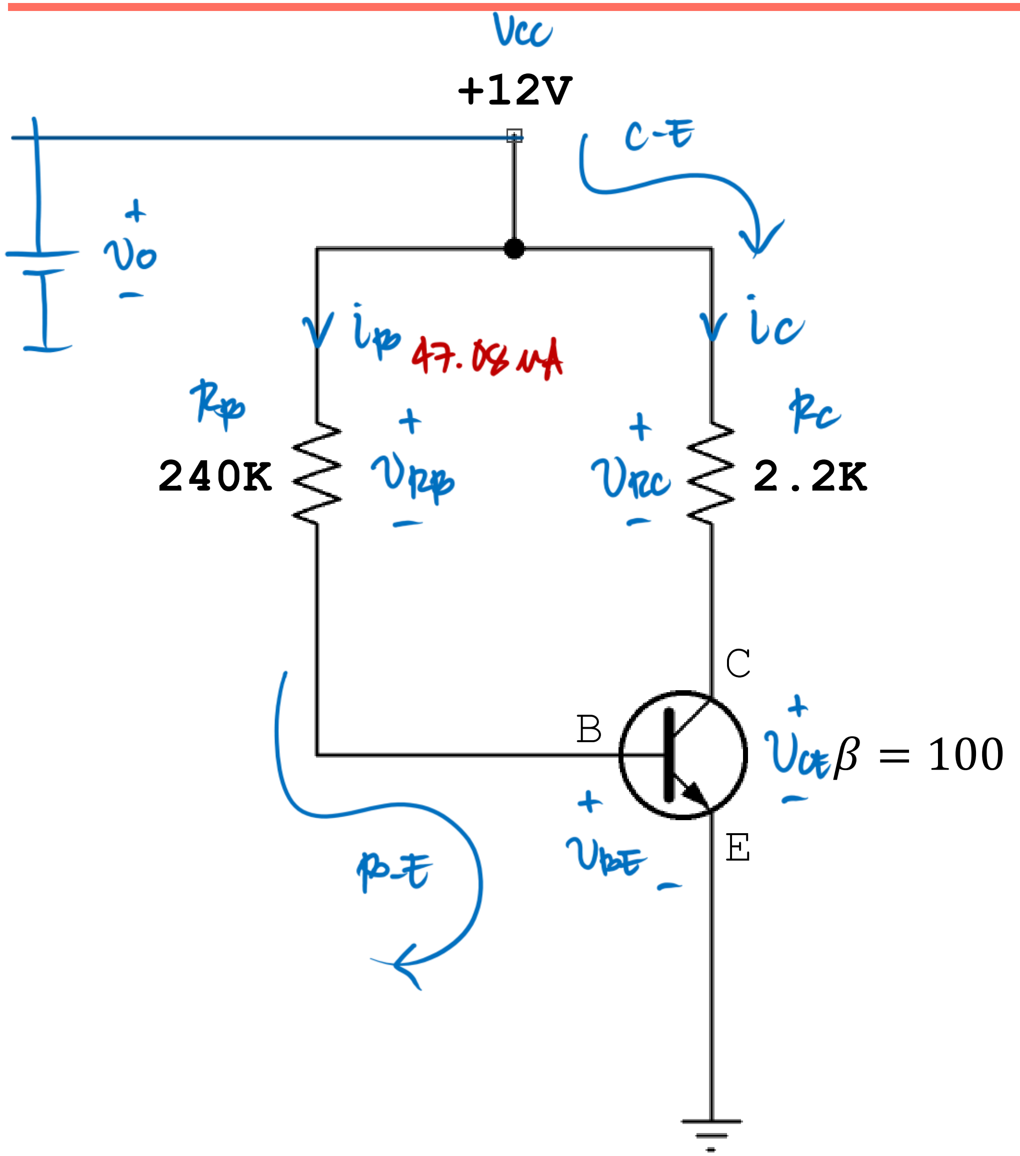
Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})

and clearly indicate the following points on the load line analysis graph.

- Saturation current $(i_{C(sat)})$
- Cutoff voltage $(v_{CE(cutoff)})$
- Operating Point (Q-Point)

EXERCISE



Solution

KVL @ B-E

$$-\cancel{V_o}^{\,V_{cc}} + V_{RB} + V_{BE} = 0$$

$$V_{RB} = V_{cc} - V_{BE}$$

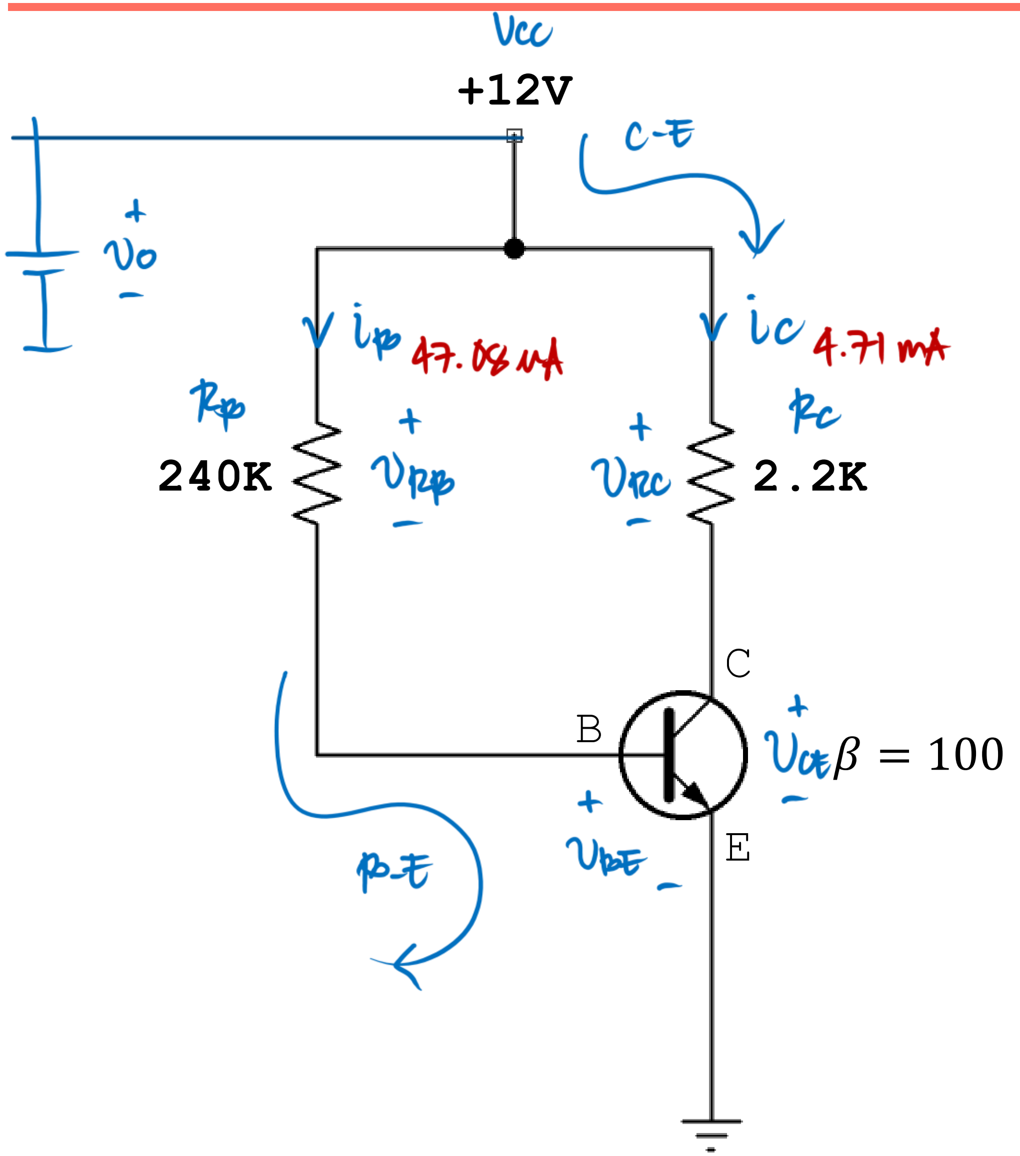
$$\frac{i_B \cancel{R_B}}{\cancel{R_B}} = \frac{V_{cc} - V_{BE}}{R_B}$$

$$i_B = \frac{12 - 0.7}{240K}$$

$$\boxed{i_{BQ} = 47.08\ \mu A}$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_c}{i_b}$$

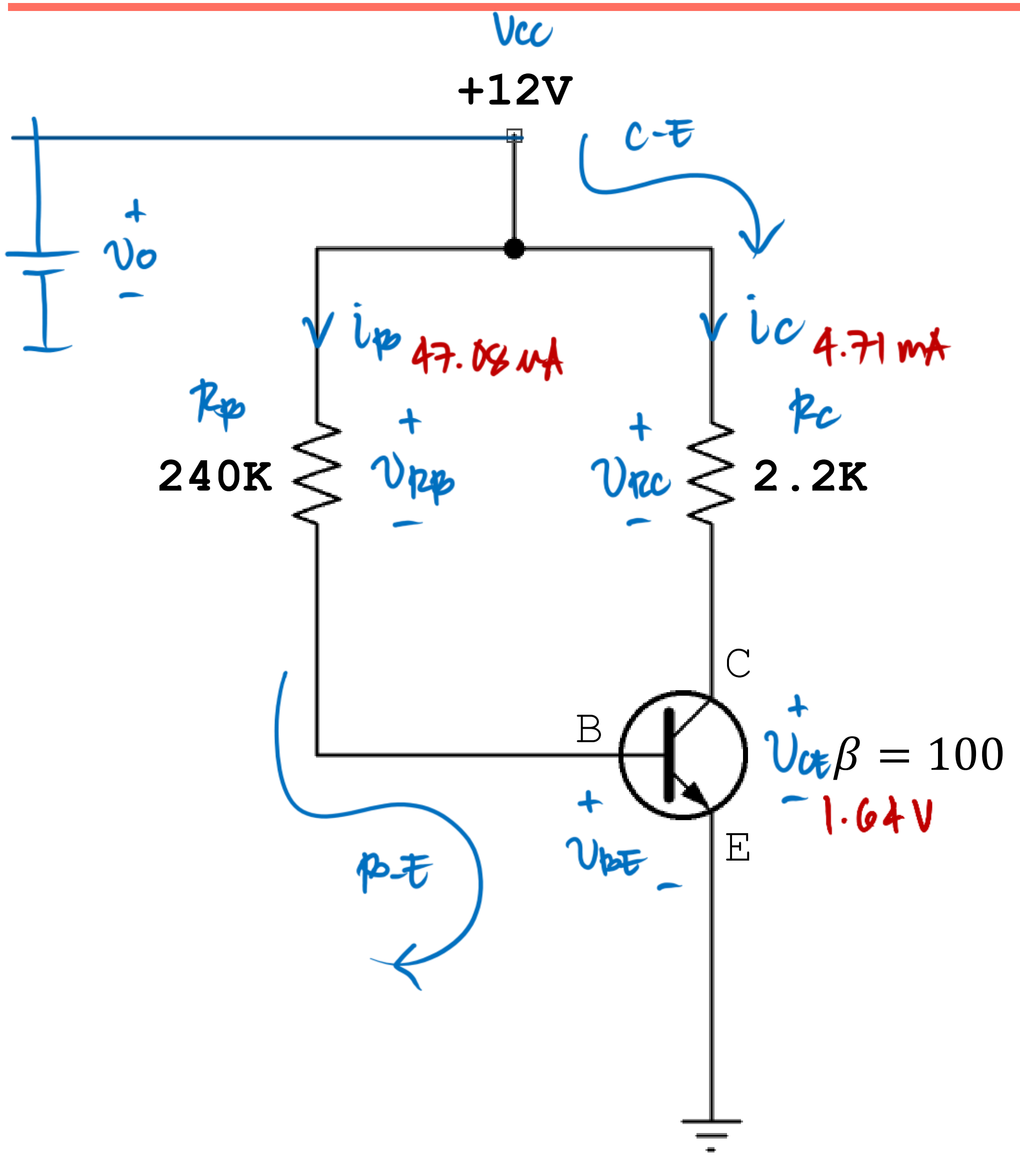
$$i_c = \beta i_b$$

$$i_c = 100(47.08\mu)$$

$$\boxed{i_{cQ} = 4.71\ mA}$$

ans

EXERCISE



Solution

KVL@ C-E

$$-\cancel{V_0}^{V_{cc}} + V_{RC} + \underline{V_{CE}} = 0$$

$$V_{CE} = V_{cc} - V_{RC}$$

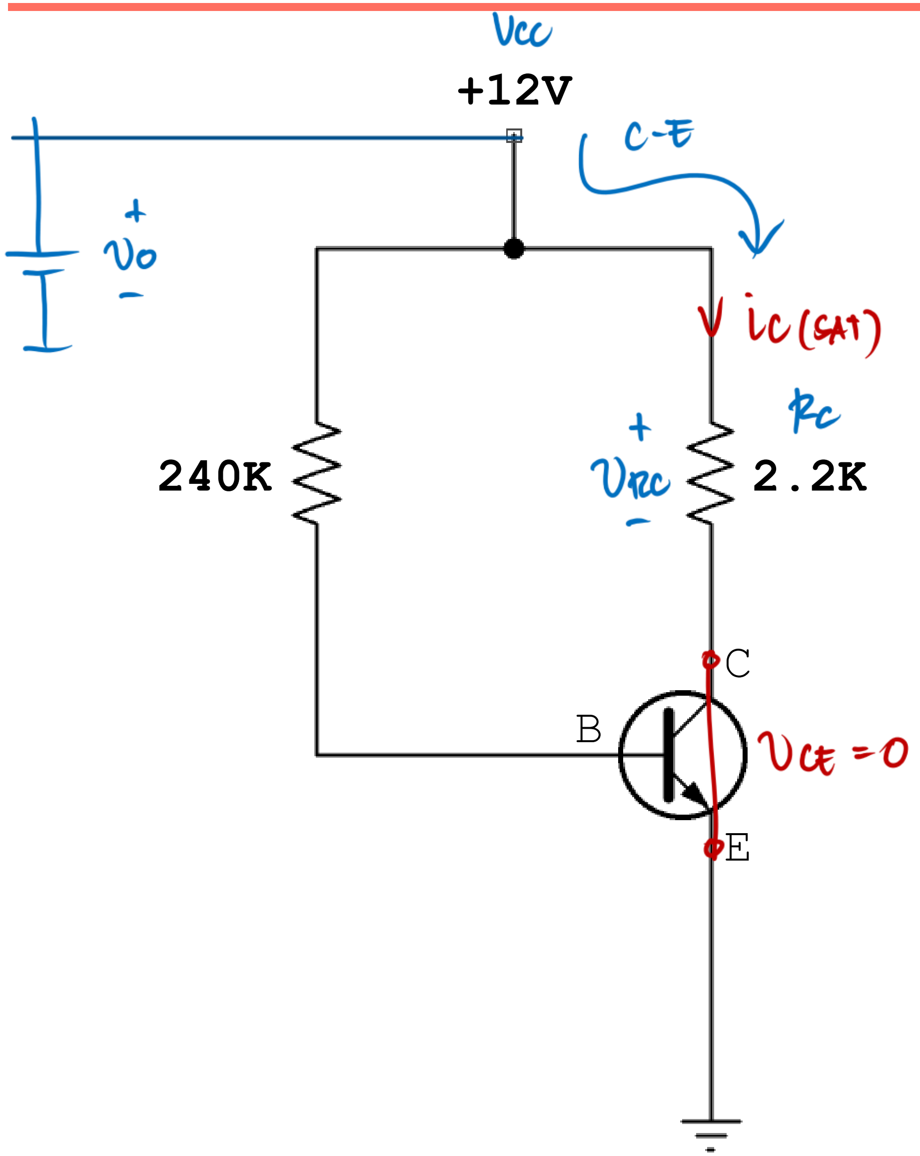
$$V_{CE} = V_{cc} - i_C R_C$$

$$V_{CE} = 12 - 4.71m(2.2k)$$

$$\boxed{V_{CEQ} = 1.64\ V}$$

ans

EXERCISE



Solution

KVL @ C-E

$$-\cancel{V_o}^{\;V_{CC}} + V_{RC} + \cancel{V_{CE}}^{\;0} = 0$$

$$V_{RC} = V_{CC}$$

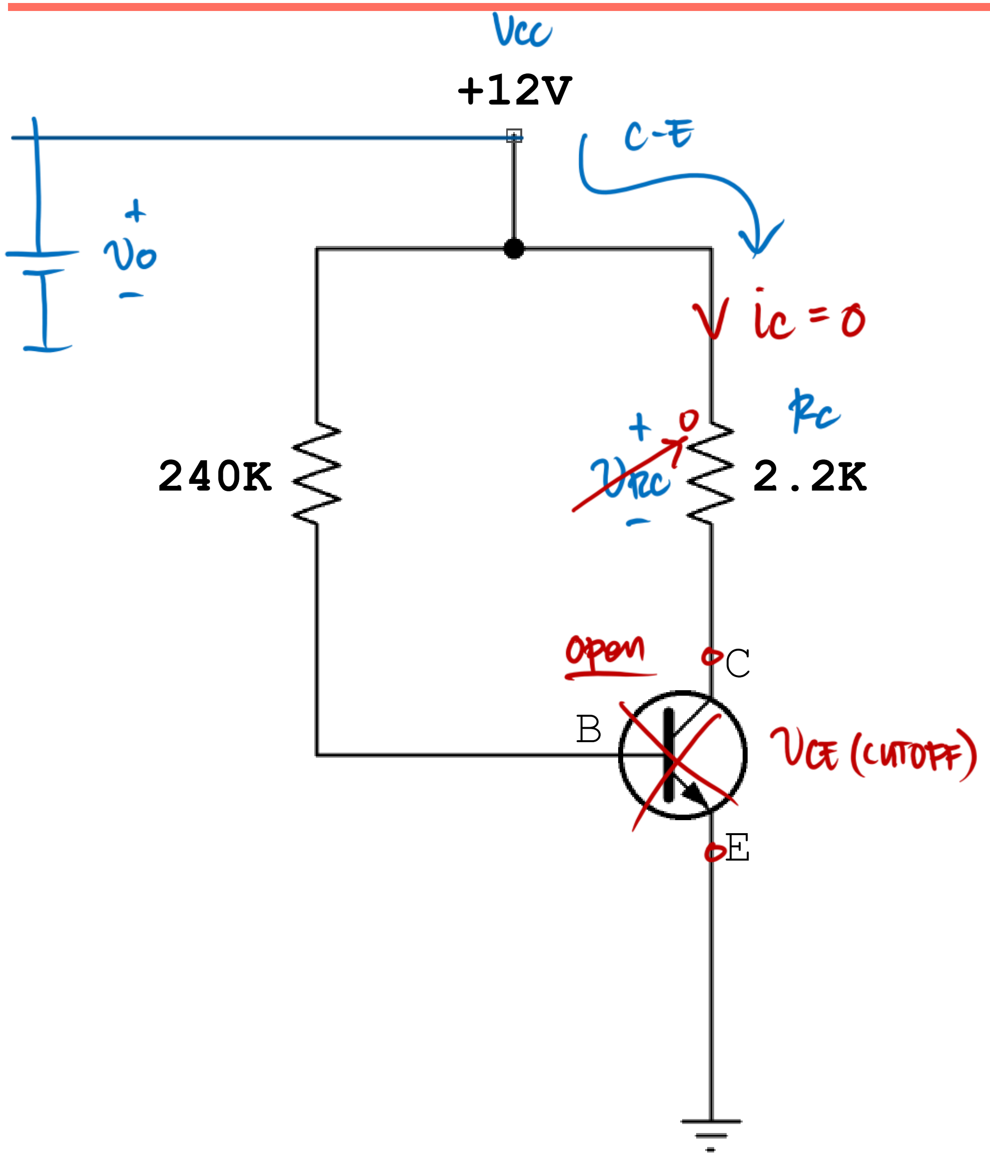
$$\frac{i_C \cancel{R_C}}{\cancel{R_C}} = \frac{V_{CC}}{R_C}$$

$$i_{C(SAT)} = \frac{12}{2.2K}$$

$$\boxed{i_{C(SAT)} = 5.45\,mA}$$

ans

EXERCISE



Solution

KVL @ C-E

$$-\cancel{V_o}^{\,V_{cc}} + \cancel{V_{RC}}^{\,0} + V_{CE} = 0$$

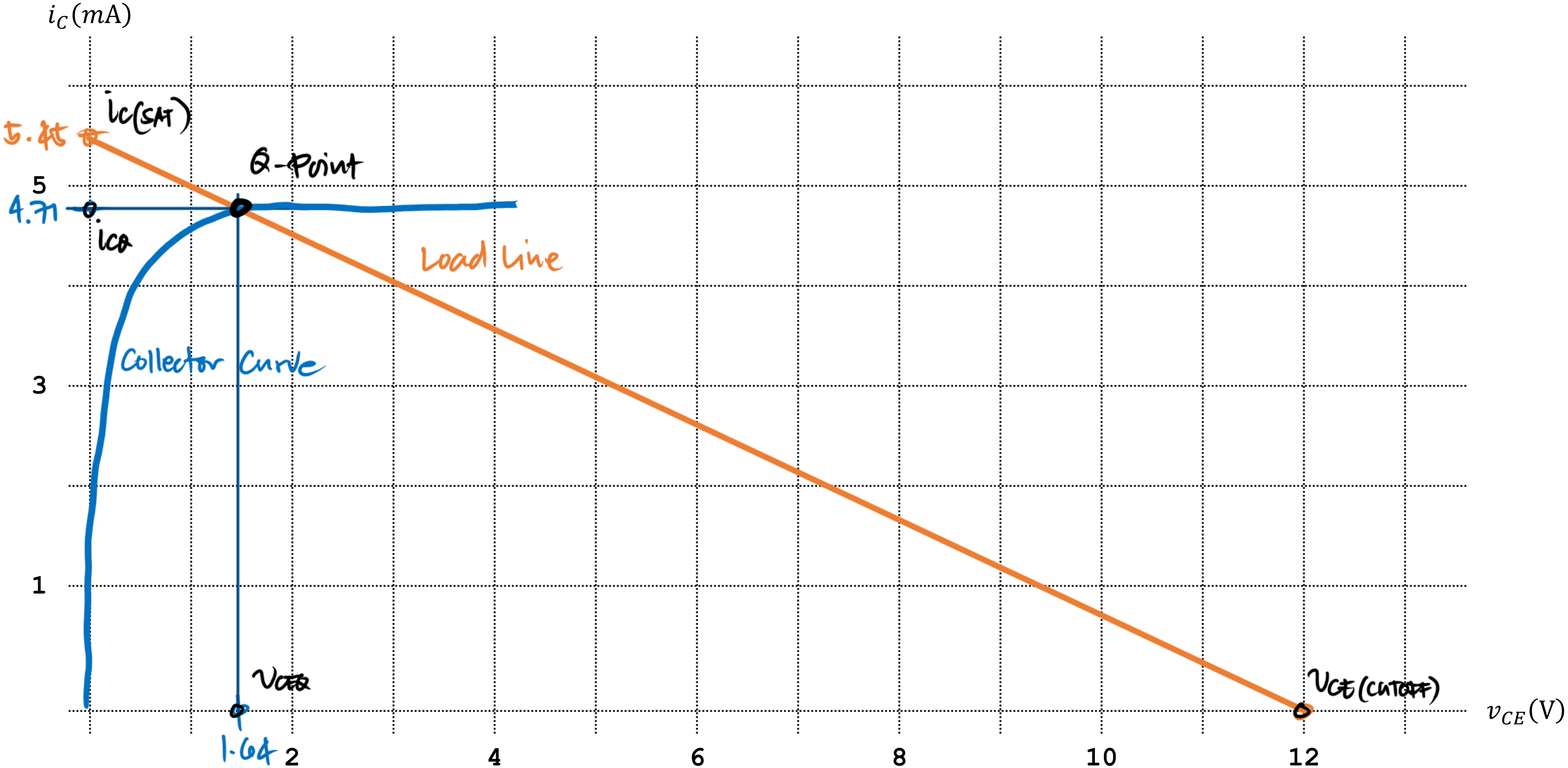
$$V_{CE} = V_{CC}$$

$$\boxed{V_{CE(CUTOFF)} = 12V}$$

ans

EXERCISE

Load Line Analysis



UNSTABLE Q-POINT

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{CE}$
Fixed-Bias	50	47.08	2.35	6.83	−76%
	100	47.08	4.71	1.64	
Emitter-Stabilized					
Voltage-Divider Bias					

LABORATORY