



MULTIPLEXER

COMBINATIONAL LOGIC CIRCUITS

prepared by:

Gyro A. Madrona
Electronics Engineer

TOPIC OUTLINE

Synthesis of Logic Functions

Shannon's Expansion Theorem



SYNTHESIS OF LOGIC FUNCTIONS

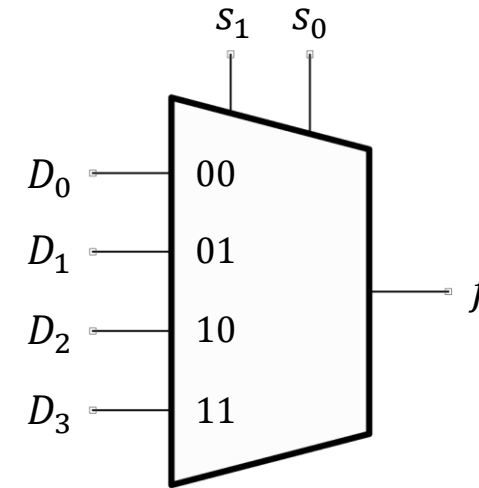


MULTIPLEXER

4-to-1 Multiplexer

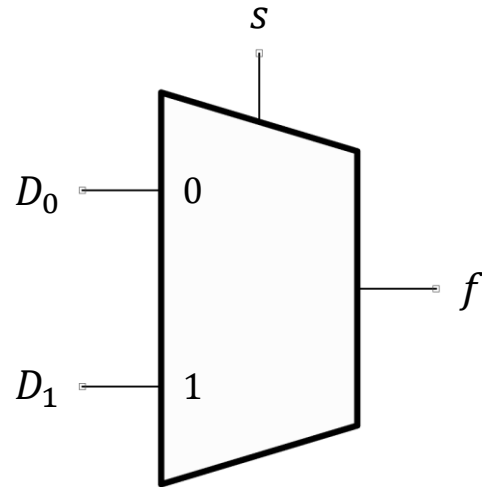
A multiplexer circuit has several data inputs, one or more select inputs, and **one output**. It passes the signal value on one of the data inputs to the output.

A multiplexer that has n data inputs (D_0, D_1, \dots, D_{n-1}), requires $\lceil \log_2 n \rceil$ select inputs.



2-TO-1 MUX

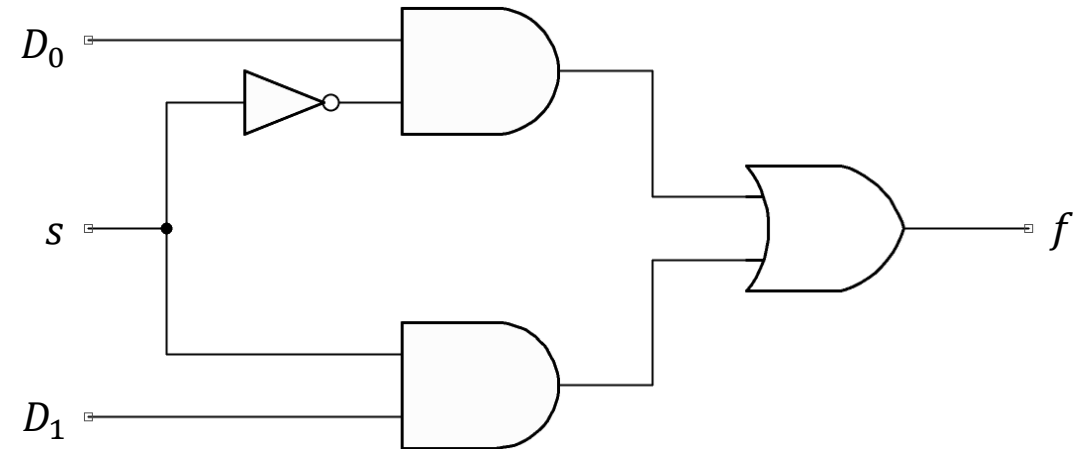
Graphical Symbol



Truth Table

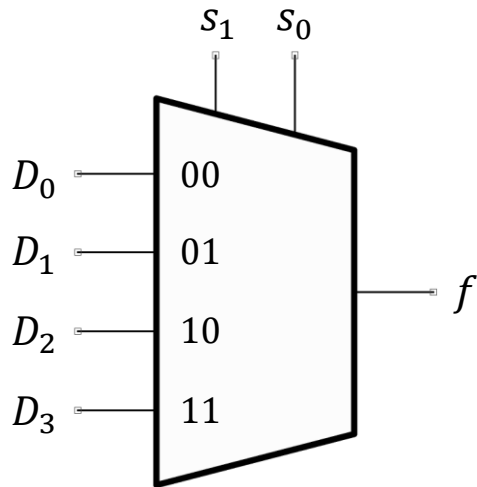
s	f
0	D_0
1	D_1

Sum-of-Products Implementation



4-TO-1 MUX

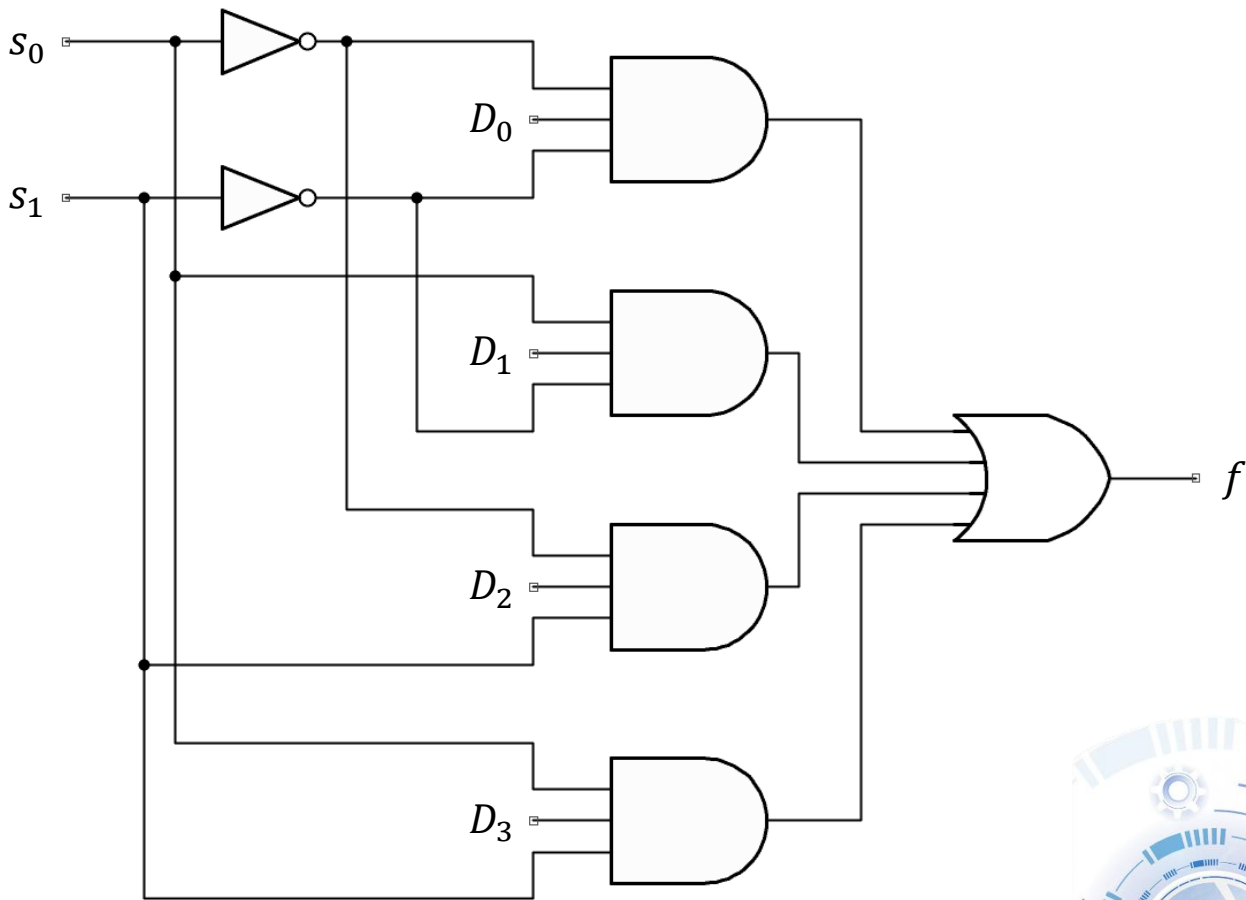
Graphical Symbol



Truth Table

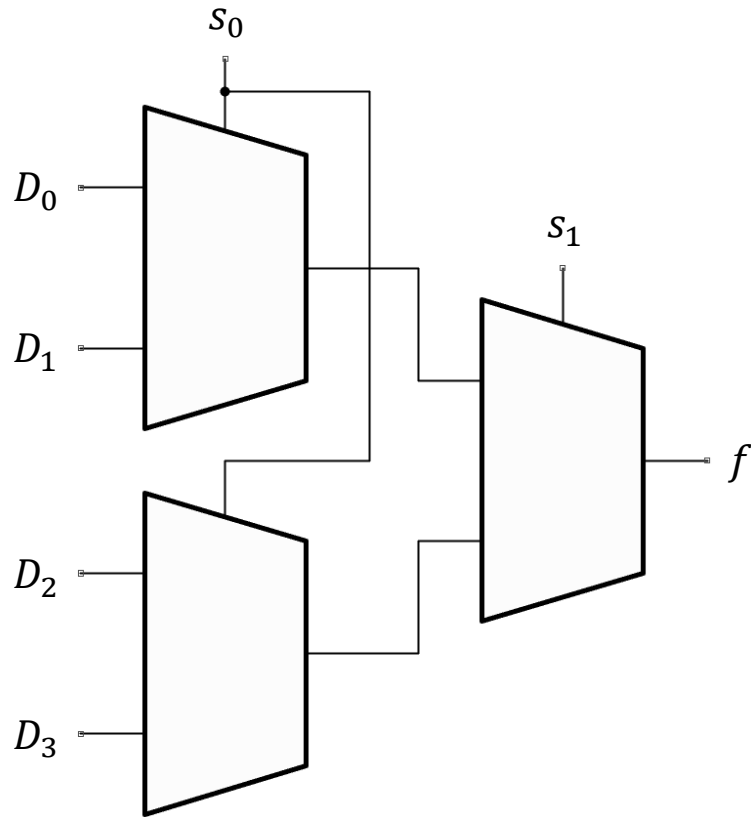
s_1	s_0	f
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Sum-of-Products Implementation

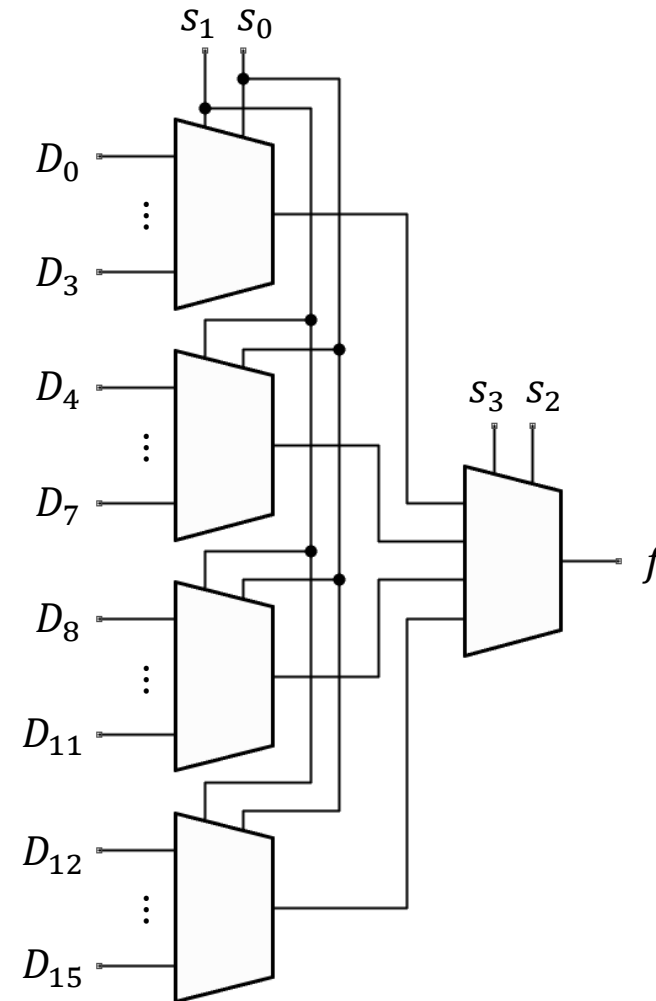


USING 2-TO-1 MUX

Using 2-to-1 MUX to build a 4-to-1 MUX



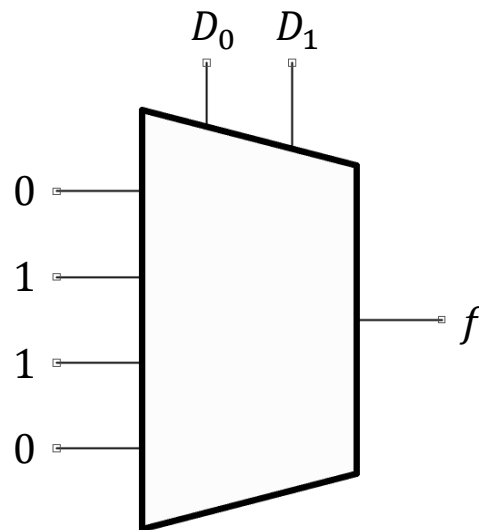
Using 2-to-1 MUX to build a 16-to-1 MUX



XOR LOGIC GATE

Implementation using 4-to-1 MUX

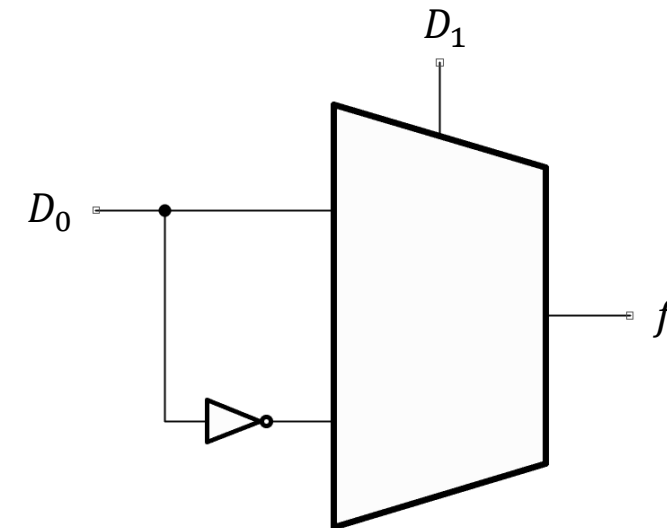
D_1	D_0	f	Minterm
0	0	0	
0	1	1	$\bar{D}_1 D_0$
1	0	1	$D_1 \bar{D}_0$
1	1	0	



Implementation using 2-to-1 MUX

D_1	f
0	D_0
1	\bar{D}_0

Modified Truth Table



EXERCISE

Implement the logic function described by the truth table using a 4-to-1 multiplexer configuration.

Solution

D_2	D_1	D_0	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



EXERCISE

Implement the logic function described by the truth table using a 2-to-1 multiplexer configuration.

Solution



EXERCISE

Implement the three-input XOR described by the truth table using a 4-to-1 multiplexer configuration.

Solution

D_2	D_1	D_0	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



EXERCISE

Implement the three-input XOR described by the truth table using a 2-to-1 multiplexer configuration.

Solution



SHANNON'S EXPANSION THEOREM



SHANNON'S EXPANSION THEOREM

Shannon's expansion theorem states that any Boolean function $f(x_0, x_1, \dots, x_{n-1})$ can be written in the form:

$$f(x_0, x_1, \dots, x_{n-1}) = \bar{x}_1 f_{\bar{x}_1} + x_1 f_{x_1}$$

where

$$\begin{aligned} f_{\bar{x}_1} &= \text{the cofactor of } f \text{ with respect to } \bar{x}_1 \\ &= (x_0, \mathbf{0}, \dots, x_{n-1}) \end{aligned}$$

$$\begin{aligned} f_{x_1} &= \text{the cofactor of } f \text{ with respect to } x_1 \\ &= (x_0, \mathbf{1}, \dots, x_{n-1}) \end{aligned}$$

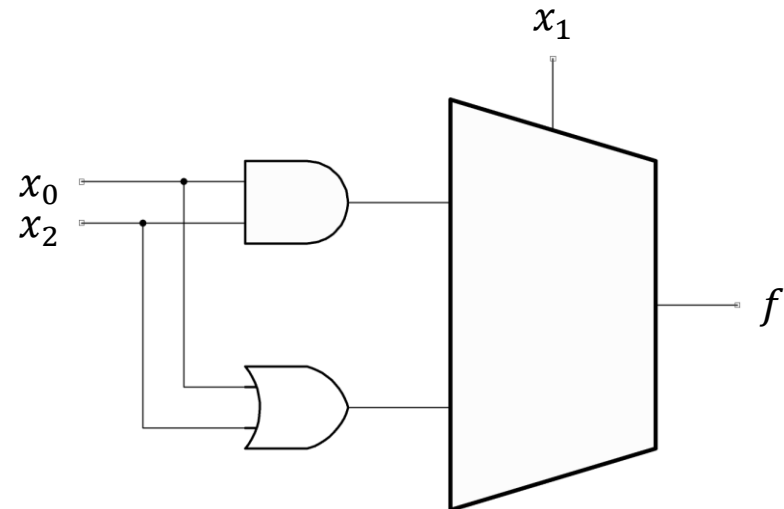
Expanding the given function with respect to x_1

$$f(x_0, x_1, x_2) = x_0 \mathbf{x_1} + x_0 x_2 + \mathbf{x_1} x_2$$

$$\begin{aligned} f(x_0, x_1, x_2) &= \bar{x}_1(x_0 \cdot \mathbf{0} + x_0 x_2 + \mathbf{0} \cdot x_2) \\ &\quad + x_1(x_0 \cdot \mathbf{1} + x_0 x_2 + \mathbf{1} \cdot x_2) \end{aligned}$$

$$f(x_0, x_1, x_2) = \bar{x}_1(x_0 x_2) + x_1(x_0 + x_0 x_2 + x_2)$$

$$f(x_0, x_1, x_2) = \bar{x}_1(x_0 x_2) + x_1(x_0 + x_2)$$



EXERCISE

Implement the logic function described by the truth table using Shannon's decomposition method.

Solution

D_2	D_1	D_0	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



EXERCISE

Implement the three-input XOR described by the truth table using a Shannon's decomposition method.

Solution

D_2	D_1	D_0	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



EXERCISE

Design a full-adder circuit using Shannon's decomposition method and simulate it in Multisim using the 74151 multiplexer.

Solution

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



LABORATORY

