

STRUCTURAL MODELING

VERILOG DESIGN STYLE

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TOPIC OUTLINE

Structural Modeling

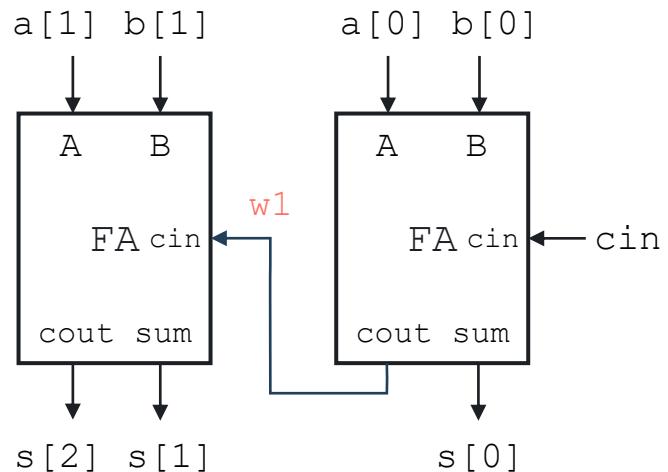
- 2-bit and 4-bit Full-Adder
- 4-bit Subtractor



STRUCTURAL MODELING

2-BIT FULL-ADDER

Block level representation



Key features of structural modeling

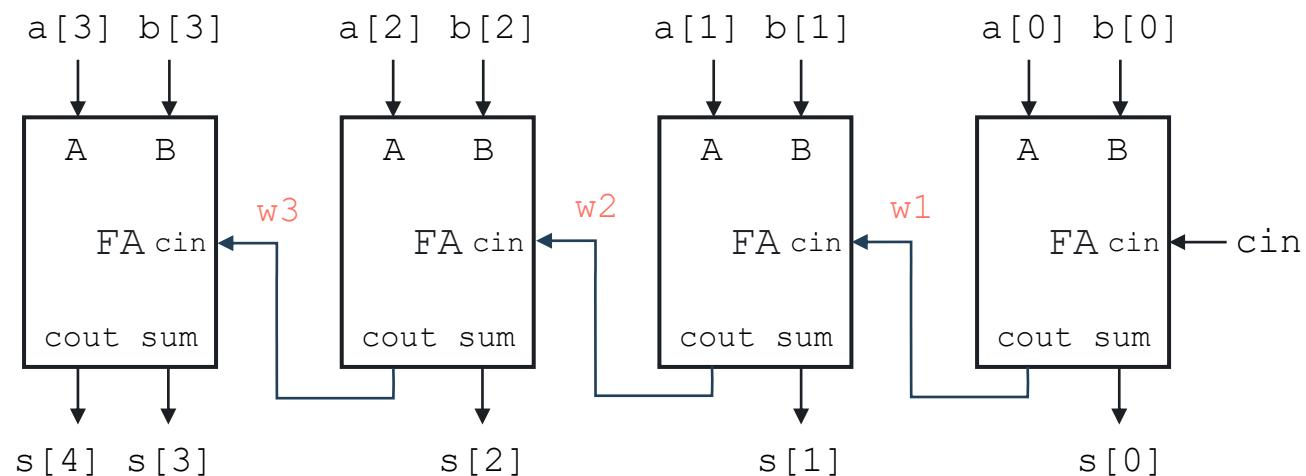
- Represents the hierarchy of the design.
- Uses **module instantiation** to build complex systems from smaller blocks.
- Emphasizes connectivity rather than functionality.

```
module 2b_adder(s,cout,a,b,cin);  
  input [1:0] a,b;  
  input cin;  
  output [2:0]s;  
  wire w1;  
  
  full_adder fa1(s[0],w1,a[0],b[0],cin);  
  full_adder fa2(s[1],s[2],a[1],b[1],w1);  
endmodule
```



4-BIT FULL-ADDER

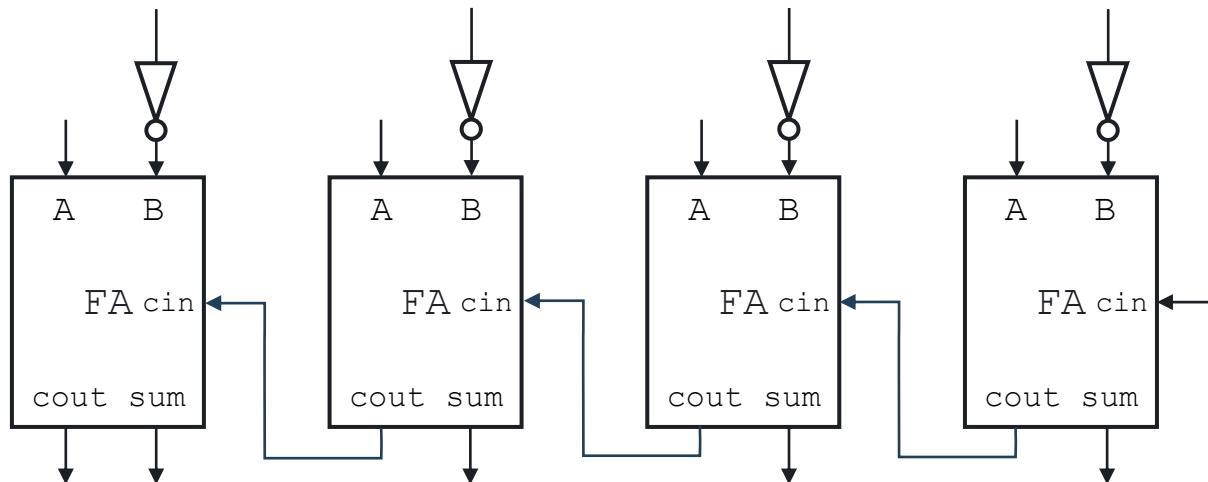
Block level representation



```
module 4b_adder(s,cout,a,b,cin);  
input [3:0] a,b;  
input cin;  
output [4:0]s;  
wire w1,w2,w3;  
  
full_adder fa1(s[0],w1,a[0],b[0],cin);  
full_adder fa2(s[1],w2,a[1],b[1],w1);  
full_adder fa3(s[2],w3,a[2],b[2],w2);  
full_adder fa4(s[3],s[4],a[3],b[3],w3);  
endmodule
```

4-BIT SUBTRACTOR

Block level representation



```
module 4b_subtractor();  
    // ports and nets  
  
    // subtractor blocks  
  
endmodule
```

LABORATORY