DECODERS

COMBINATIONAL LOGIC CIRCUITS

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TOPIC OUTLINE

Binary Decoder

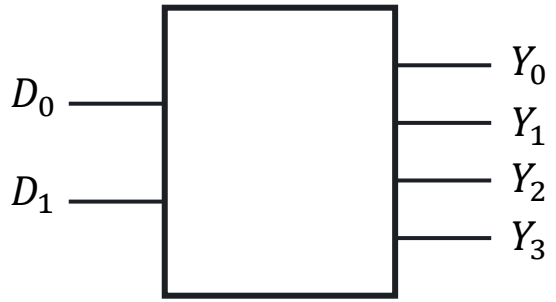
BCD-to-7-Segment Decoder

BINARY DECODER

BINARY DECODER

A **binary decoder** takes $\boldsymbol{n}$ input bits and activates one of $\boldsymbol{2^n}$ output lines.

Graphical Symbol



Truth Table

D_1	D_0	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

EXERCISE

Given the truth table, synthesize a 2-to-4 binary decoder with an enable input.

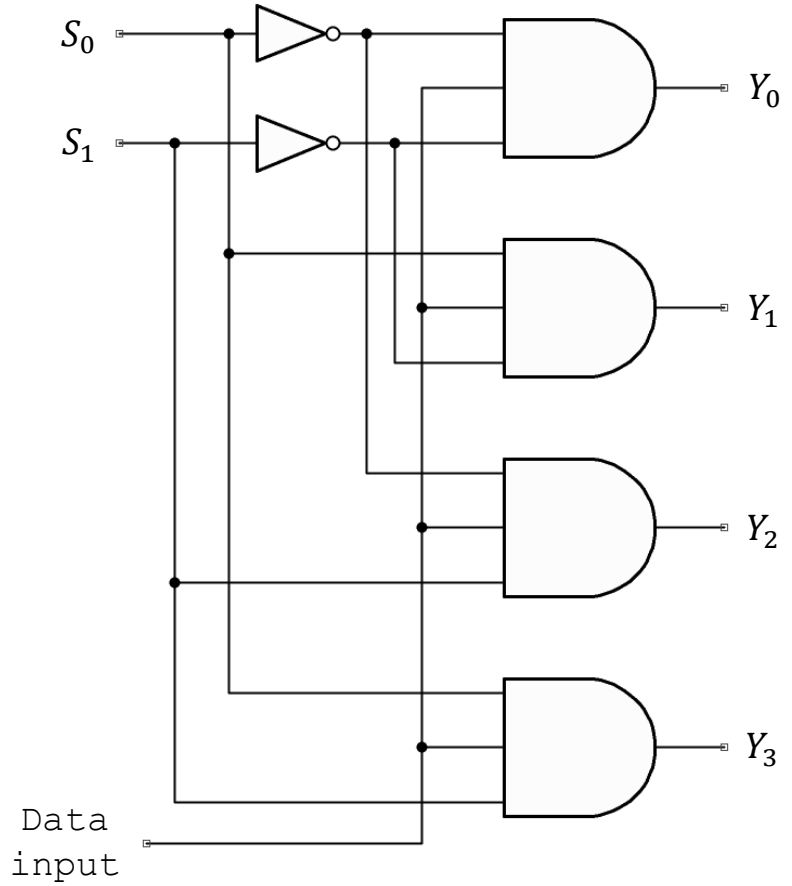
En	D_1	D_0	Y_0	Y_1	Y_2	Y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

Solution

DEMULTIPLEXER

A **demultiplexer** is a digital circuit that routes a **single data input** to one of **several outputs** based on select input lines, performing the inverse function of a multiplexer.

A 1-line-to-4-line Demultiplexer

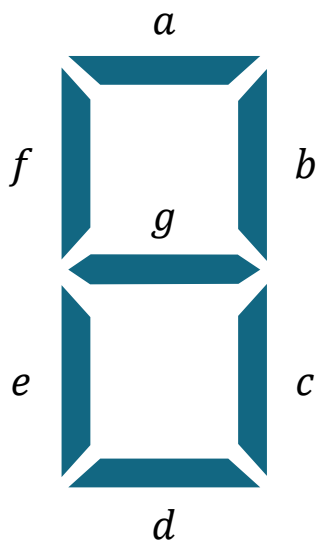


BCD-TO-7-SEGMENT DECODER

THE 7-SEGMENT DISPLAY

A standard **7-segment display** consists of **seven LEDs** (segments) arranged in a rectangular layout to form the number 8. Each segment is labeled from a to g, and an optional eighth segment (DP) is used for the decimal point.

Segment Arrangement



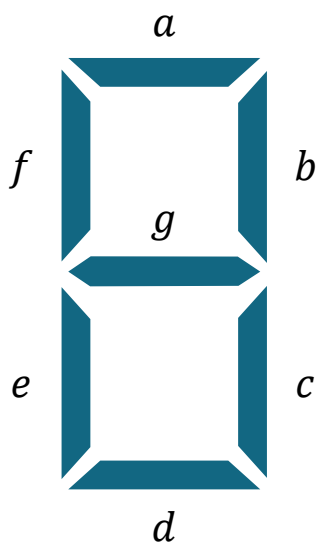
EXPRESSION FOR SEGMENT A

Truth Table

N	$DCBA$	f_a
0		
1		
2		
3		
4		
5		
6		
7		
8		

N	$DCBA$	f_a
9		
10		
11		
12		
13		
14		
15		

Segment Arrangement



EXPRESSION FOR SEGMENT A

Truth Table

N	$DCBA$	f_a
0		
1		
2		
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4		
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8		

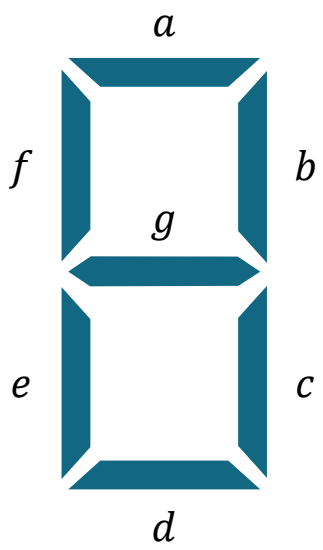
N	$DCBA$	f_a
9		
10		
11		
12		
13		
14		
15		

K-Map

EXERCISE

Synthesize and implement a combinational logic circuit that functions as a decoder for a 7-segment display.

Segment Arrangement



LABORATORY