LOGIC GATES

INTRODUCTION

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TOPIC OUTLINE

Logic Gates

- **Logic Symbol**

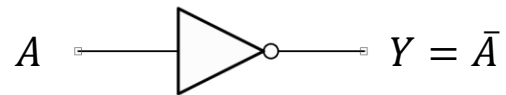- **Truth Table**

- **Timing Diagram**

LOGIC GATES

INVERTER

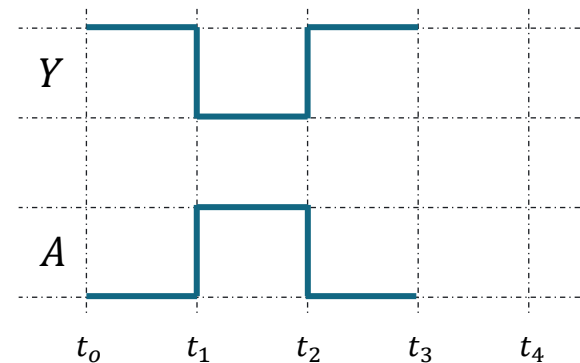The **inverter** (NOT gate) performs the operation called inversion or **complementation**.

Truth Table

A	Y
0	1
1	0

Logic Symbol

$A \quad \longrightarrow \quad Y = \bar{A}$

Timing Diagram

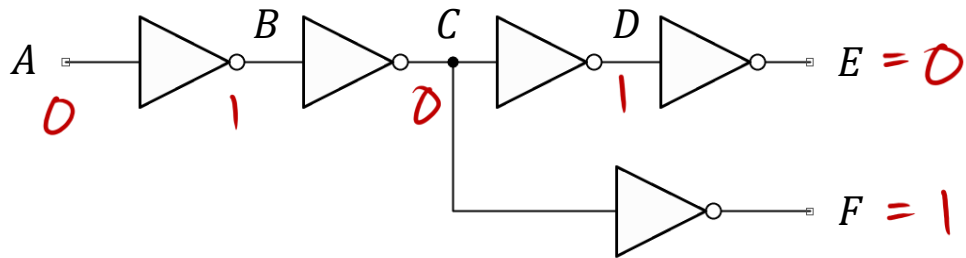
Y

A

$t_o \qquad t_1 \qquad t_2 \qquad t_3 \qquad t_4$

EXERCISE

Given the inverter network, determine the logic levels at points E and F when a <u>LOW</u> signal is applied at point A.
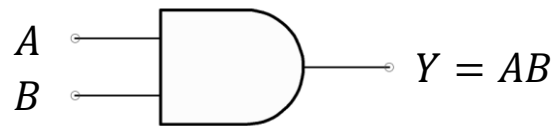
Solution

A — 0 → B = 1 → C = 0 → D = 1 → E = 0

F = 1

AND GATE

The **AND** gate is one of the basic gates that can be combined to form any logic function. It performs logical **multiplication**.
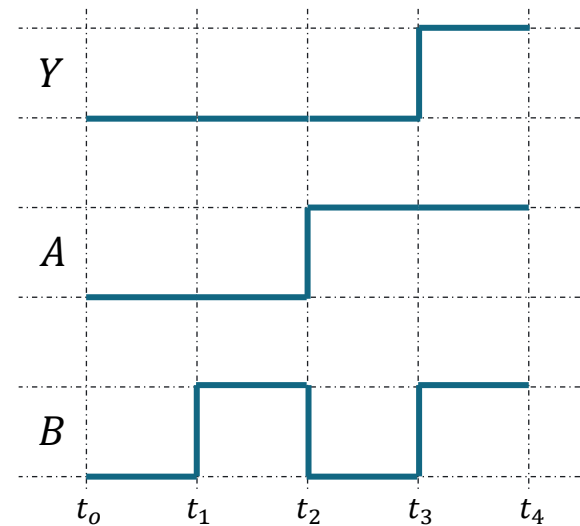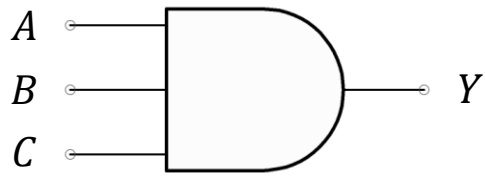
Truth Table

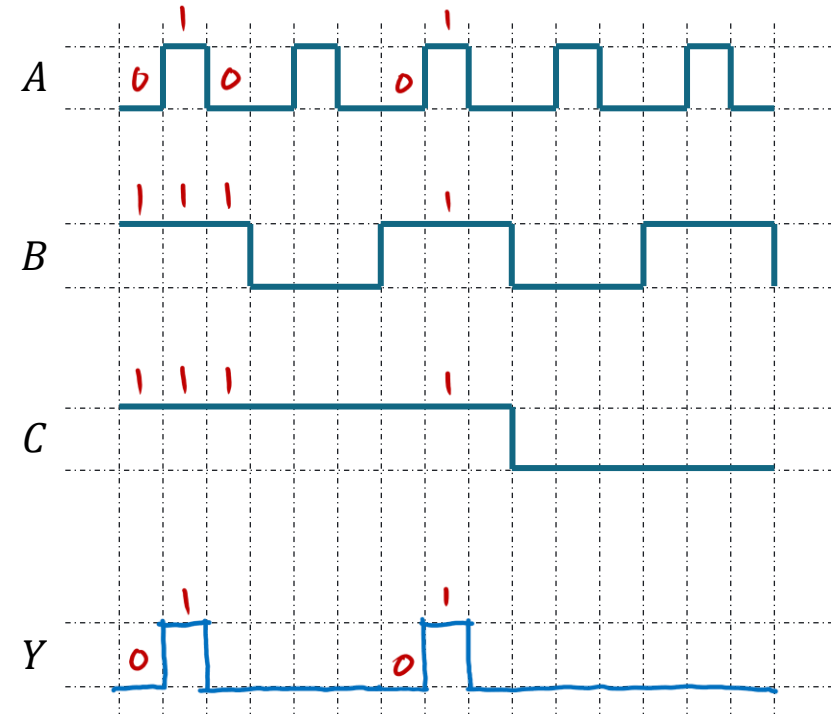| A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Logic Symbol

$Y = AB$

Timing Diagram

EXERCISE

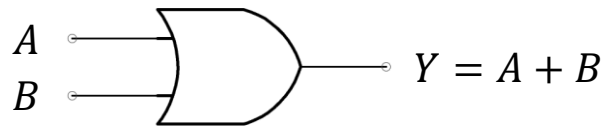For the 3-input AND gate, determine the output waveform in relation to the inputs.

OR GATE

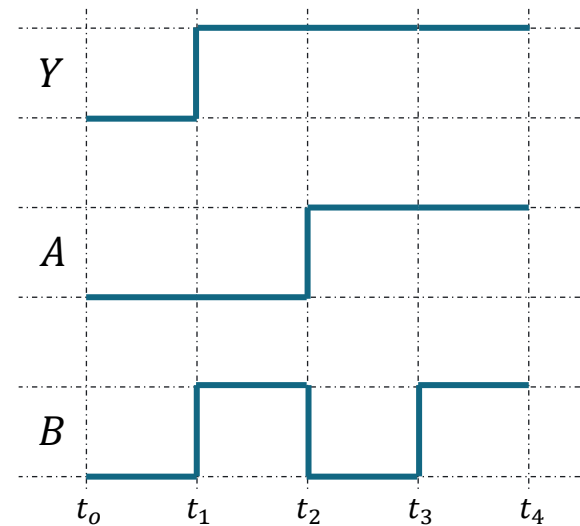The **OR** gate is another basic gates from which all logic functions are constructed. It performs logical **addition**.
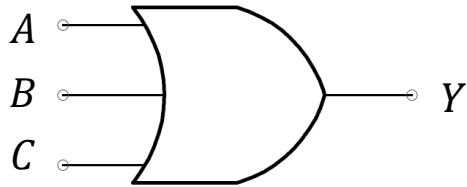
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Logic Symbol
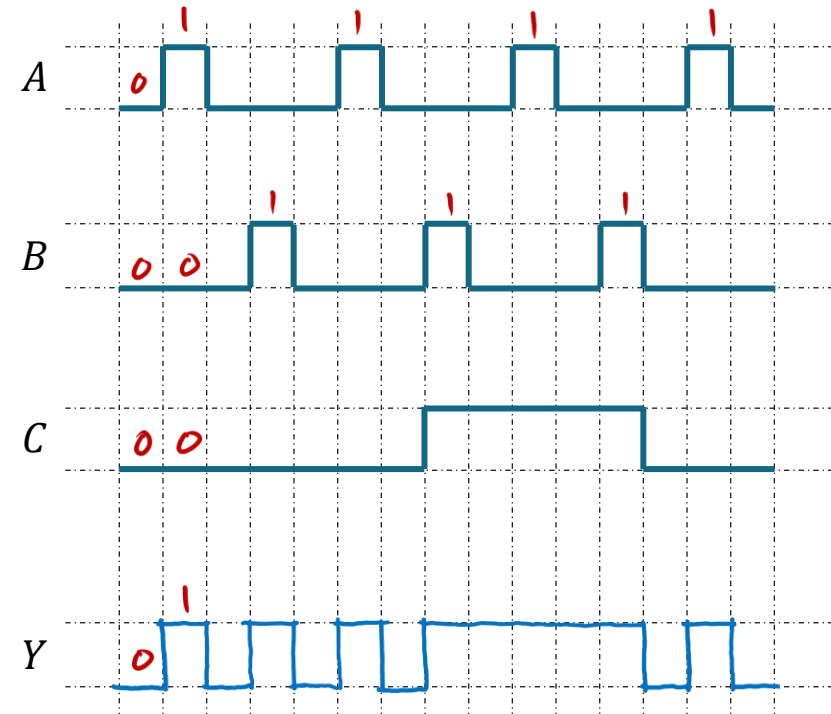

$$Y = A + B$$

Timing Diagram

EXERCISE

For the 3-input OR gate, determine the output waveform in relation to the inputs.
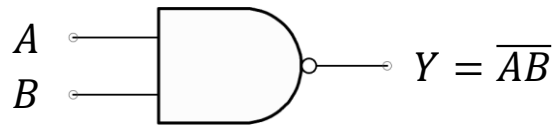
Solution

NAND GATE

The **NAND** gate is a logical complement of the AND gate. It is considered a universal gate, meaning it can be used in combination to perform AND, OR, and inverter operations.
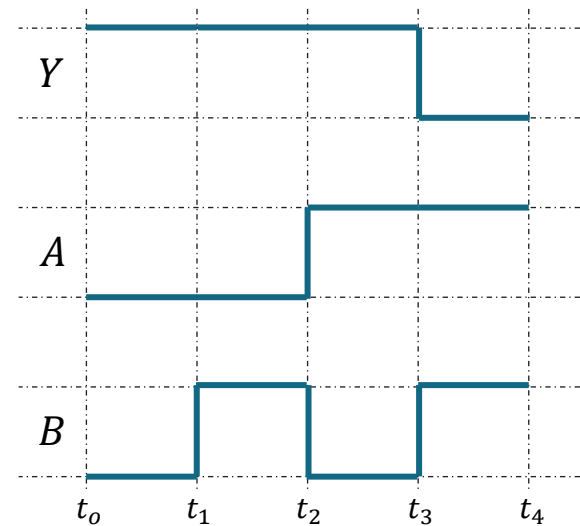
Truth Table

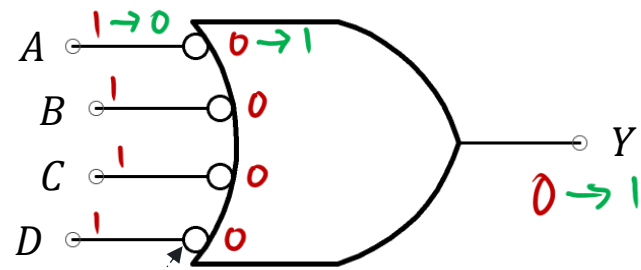| A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Logic Symbol

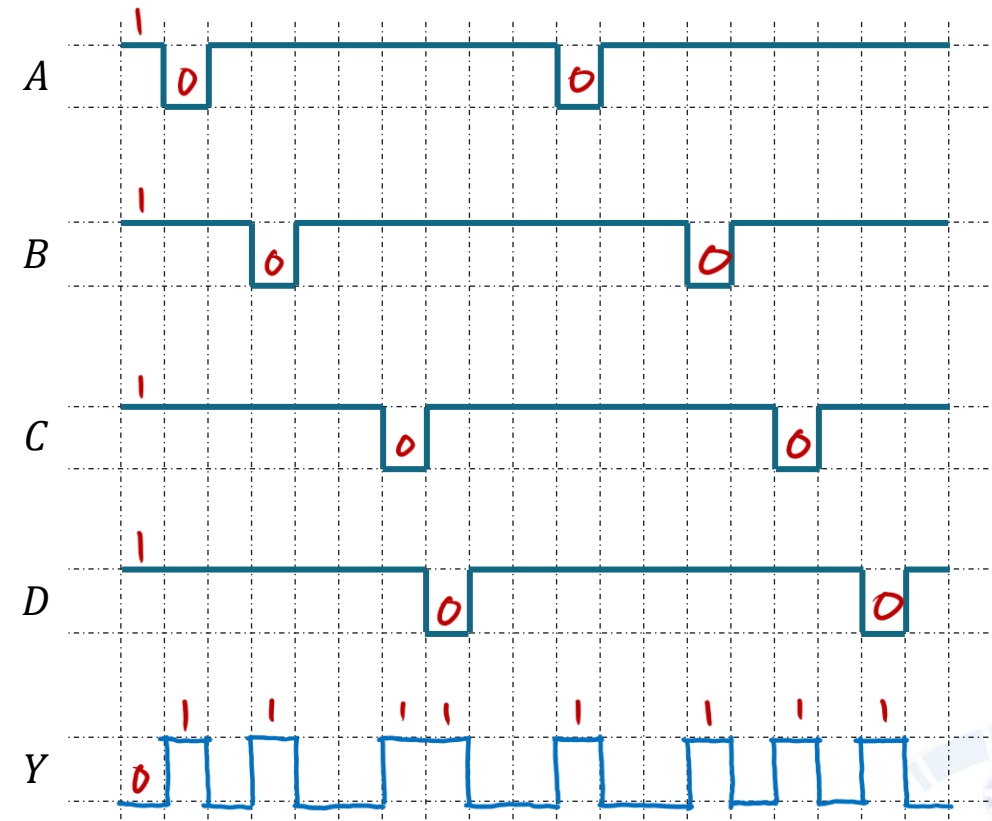$$Y = \overline{AB}$$

Timing Diagram

EXERCISE

For the 4-input NAND gate, operating as negative-OR gate, determine the output with respect to the inputs.
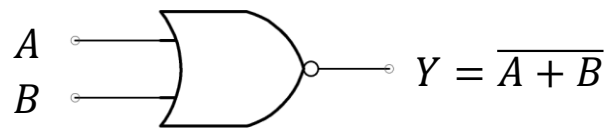

Bubble indicates active-LOW input

Solution

NOR GATE

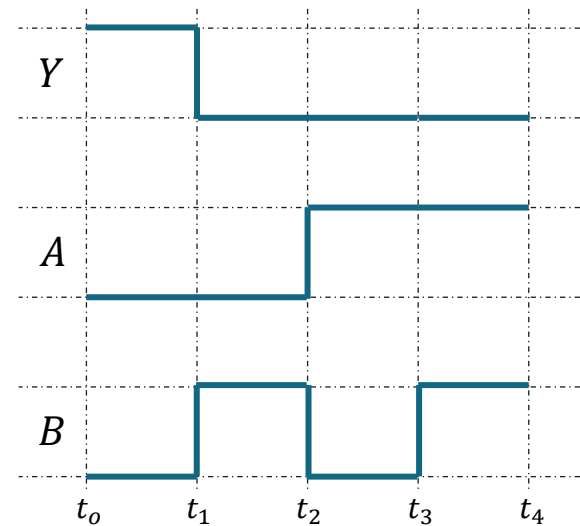NOR gate is also a universal gate, and it is the logical complement of the OR gate.

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic Symbol

$$Y = \overline{A + B}$$

A
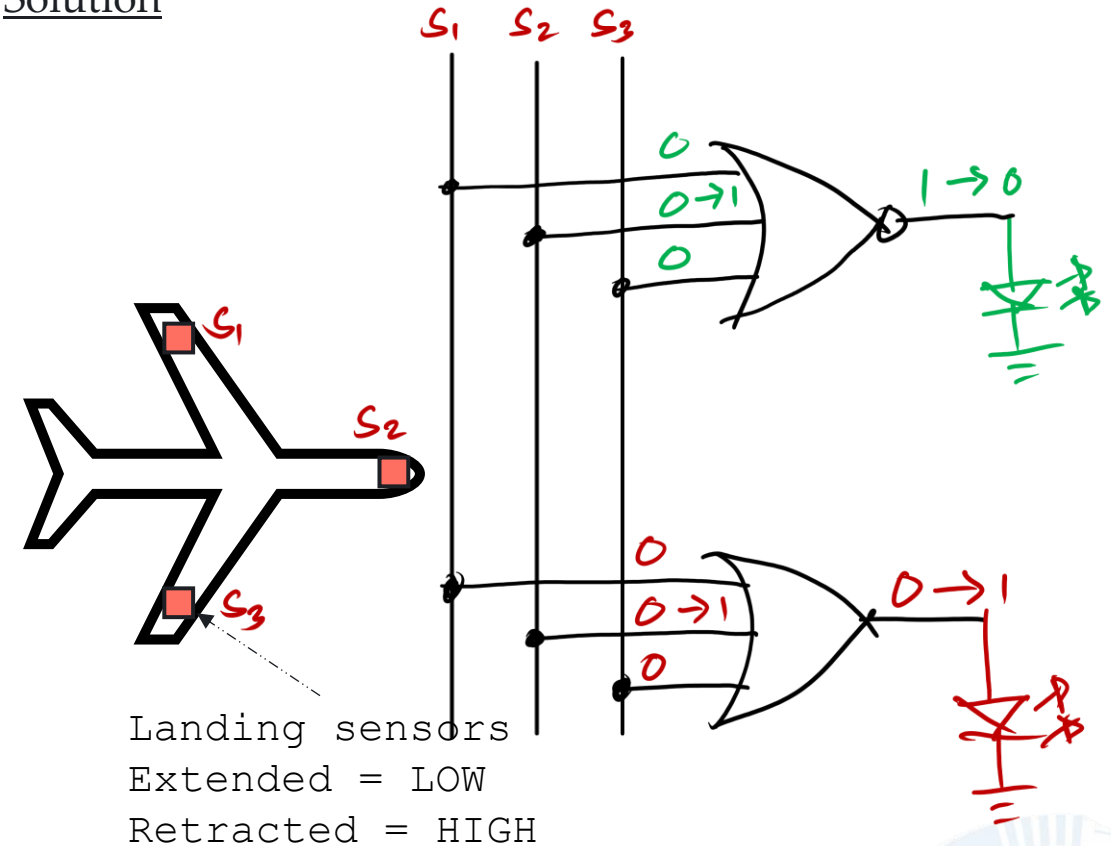B

Timing Diagram

Y

A

B

t_o t_1 t_2 t_3 t_4

EXERCISE

As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. A green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. A red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.
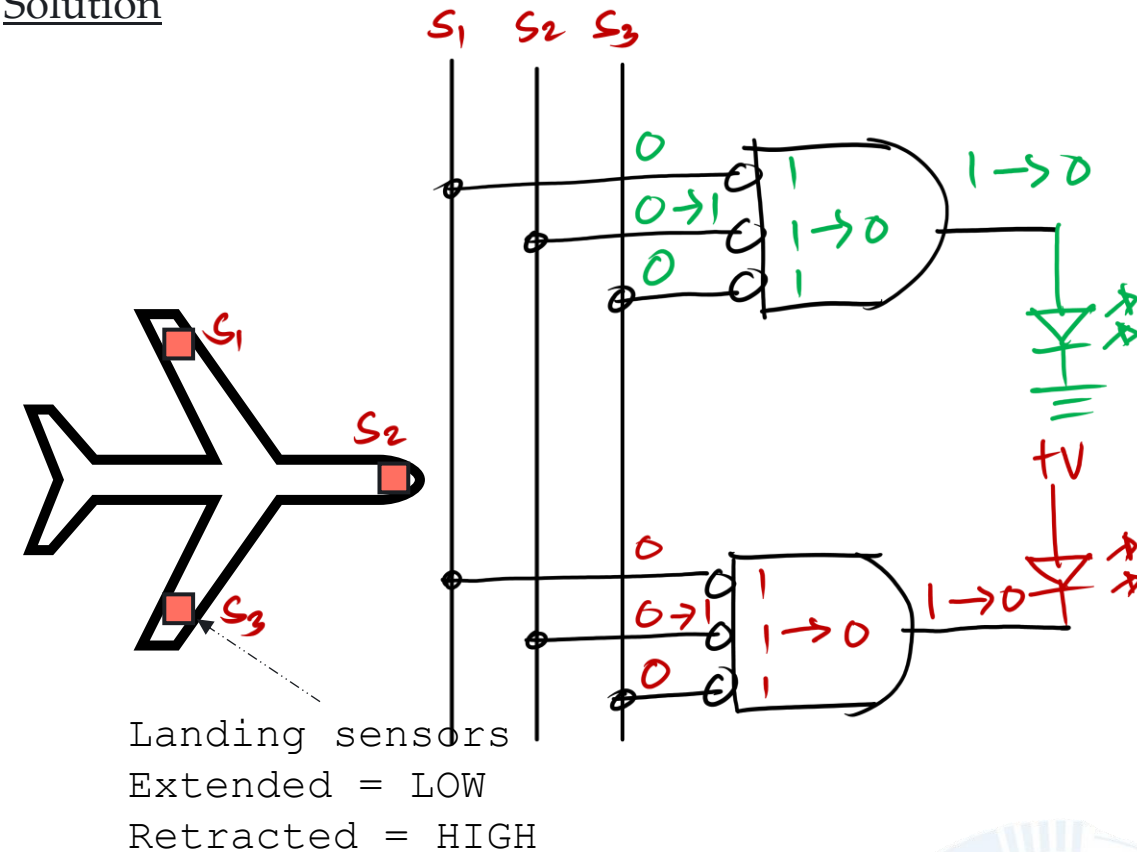
$S_1 = 0 \quad S_2 = 0 \quad S_3 = 0$

Solution

Landing sensors
Extended = LOW
Retracted = HIGH

EXERCISE

As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. A green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. A red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.
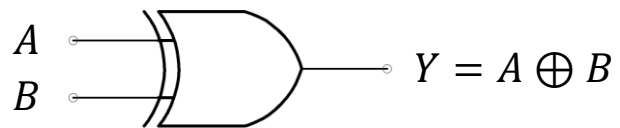
$S_1 = 0 \quad S_2 = 0 \quad S_3 = 0$

Solution

Landing sensors
Extended = LOW
Retracted = HIGH

EXCLUSIVE-OR GATE

The exclusive-OR (**XOR**) gate performs **modulo-2 addition**.

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Logic Symbol

$$Y = A \oplus B$$
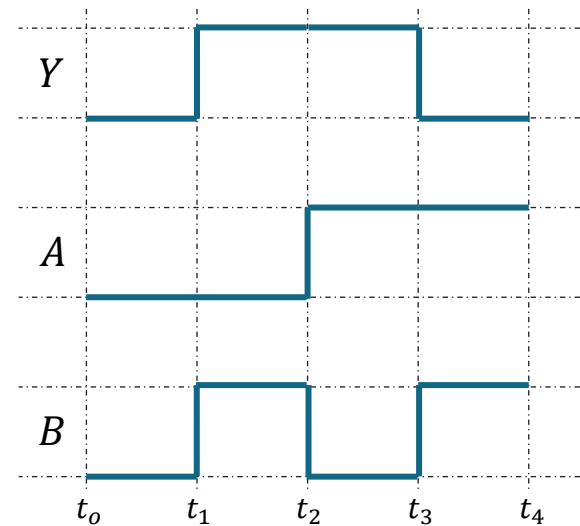
Timing Diagram

EXCLUSIVE-NOR GATE

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

The exclusive-NOR (**XNOR**) gate is the logical complement of the XOR gate.

Logic Symbol

$$Y = \overline{A \oplus B}$$

A
B

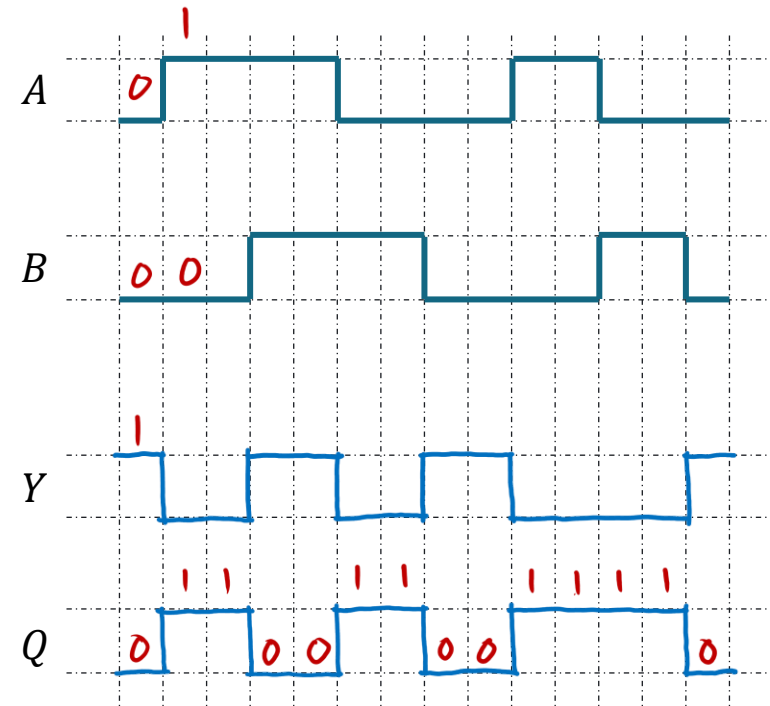Timing Diagram

Y

A

B

t_o t_1 t_2 t_3 t_4
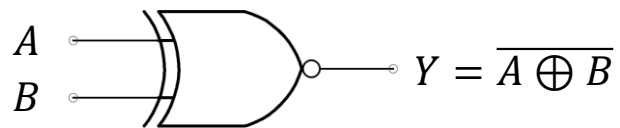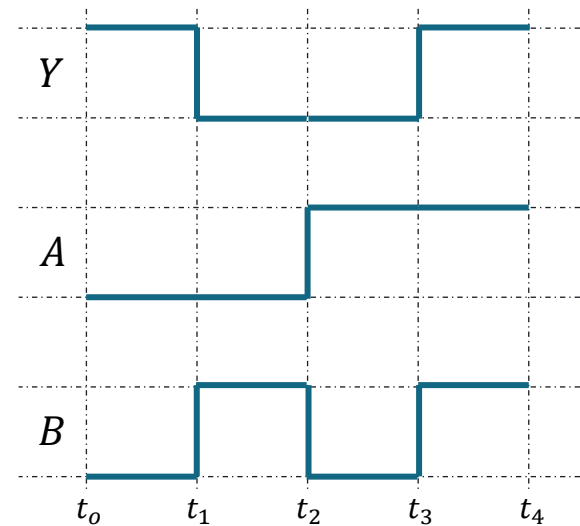
EXERCISE

Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B.
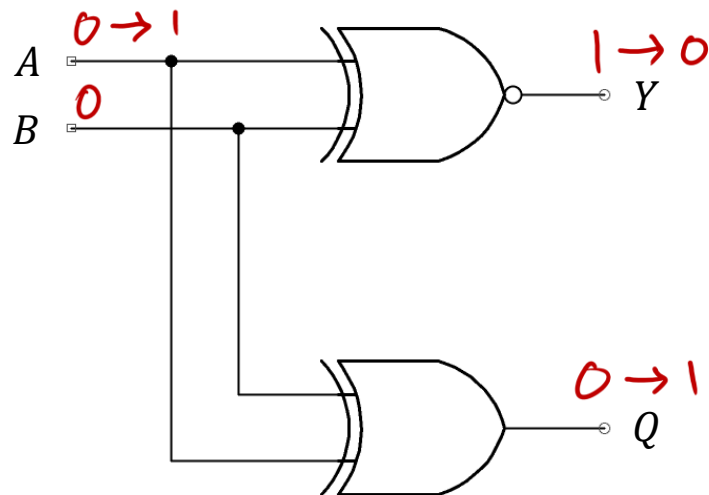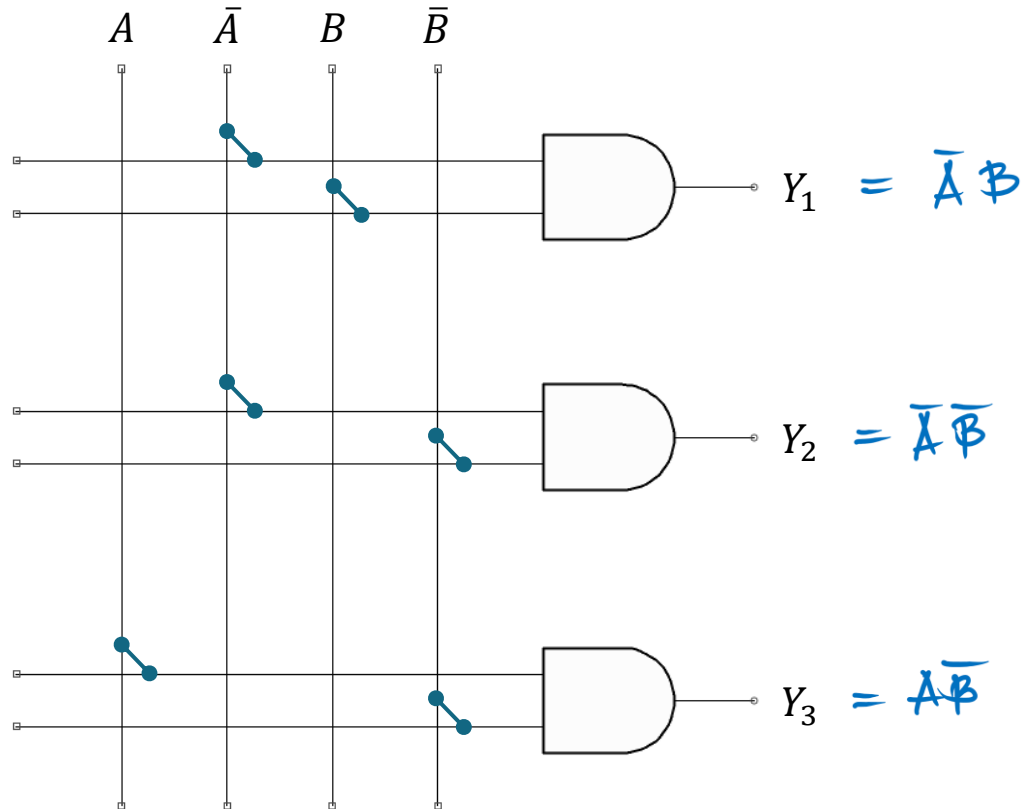
EXERCISE

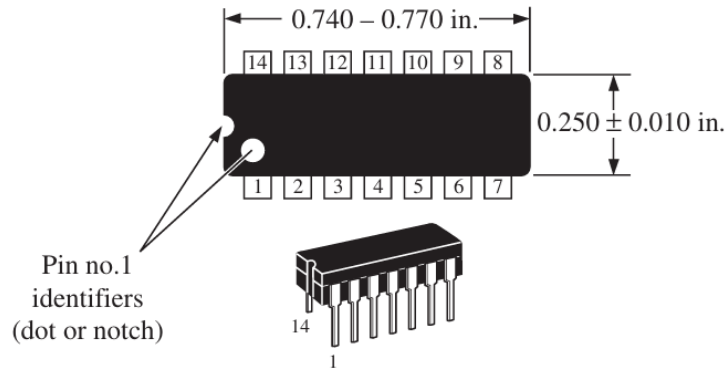In the simple programmed AND array with programmable links, determine the Boolean output expressions.
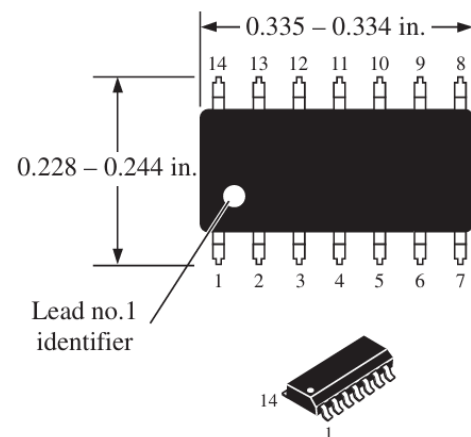
Solution

$$Y_1 = \bar{A}B$$

$$Y_2 = \bar{A}\bar{B}$$

$$Y_3 = A\bar{B}$$

IC PACKAGES

DIP (Dual In-line Package)

0.740 – 0.770 in.

14 13 12 11 10 9 8

0.250 ± 0.010 in.

1 2 3 4 5 6 7

Pin no.1 identifiers (dot or notch)

14

1

SOIC (Small-Outline IC)

0.335 – 0.334 in.

14 13 12 11 10 9 8

0.228 – 0.244 in.

1 2 3 4 5 6 7

Lead no.1 identifier

14

1

Datasheet links

7404-Inverter Gate datasheet

7408-AND Gate datasheet

7432-OR Gate datasheet
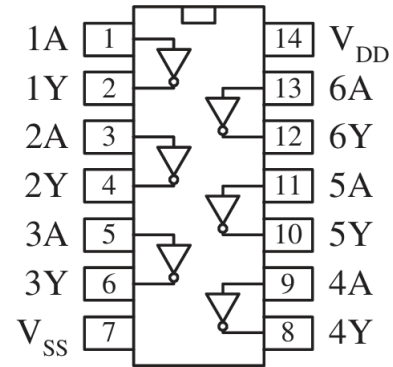
7403-NAND Gate datasheet

7402-NOR Gate datasheet
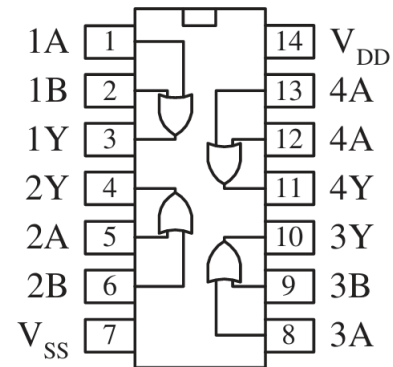
74136-XOR Gate datasheet

74266-XNOR Gate datasheet

PIN CONFIGURATION

Hex inverter
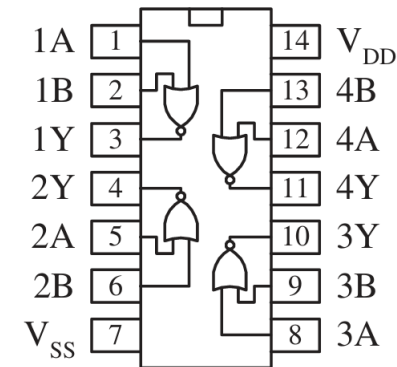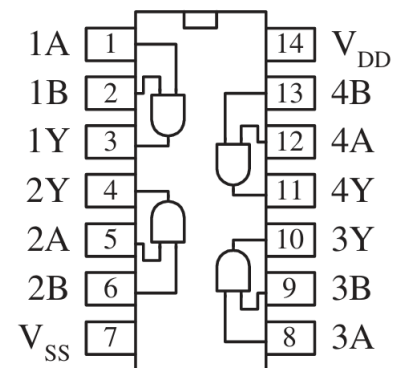

Quad 2-input OR

Quad 2-input NOR

Quad 2-input AND

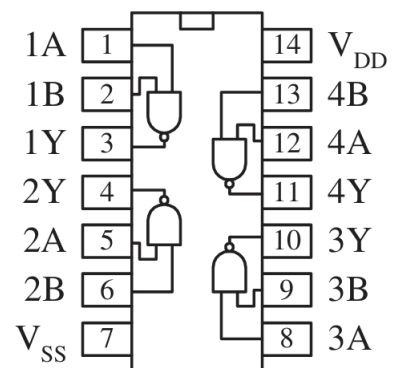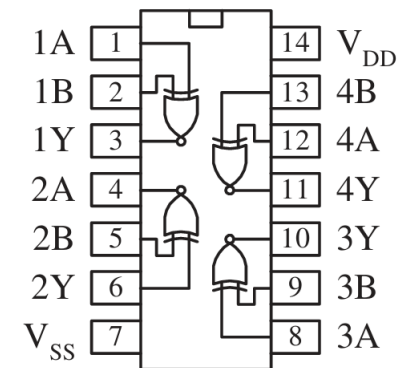### Quad 2-input NAND

Quad 2-input XNOR

Quad 2-input XOR

LABORATORY