VOLTAGE-DIVIDER BIAS

BJT DC BIASING

prepared by:

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TOPIC OUTLINE

Voltage-Divider Bias Circuit

- **Base-Emitter Loop**
- **Collector-Emitter Loop**
- **Load Line Analysis**

VOLTAGE-DIVIDER BIAS CIRCUIT

CURRENT GAIN

The current gain parameters **alpha** (α) and **beta** (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

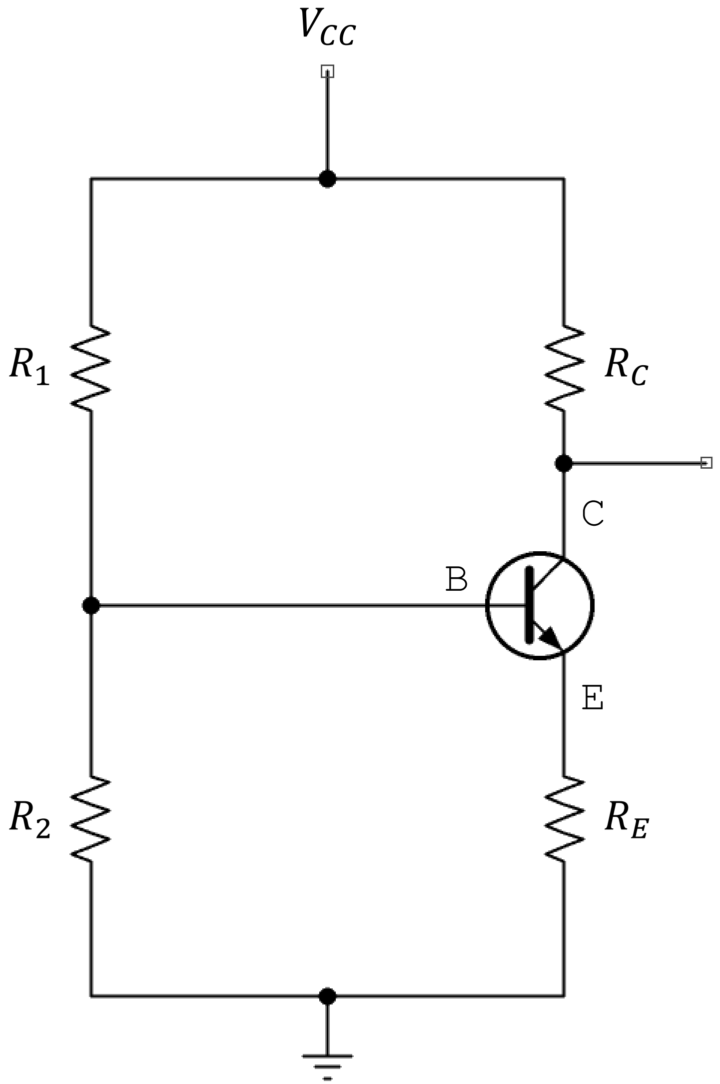
α is always less than 1 (typically 0.95 to 0.995)

Beta (β) is the ratio of the collector current to the base current.

Formula

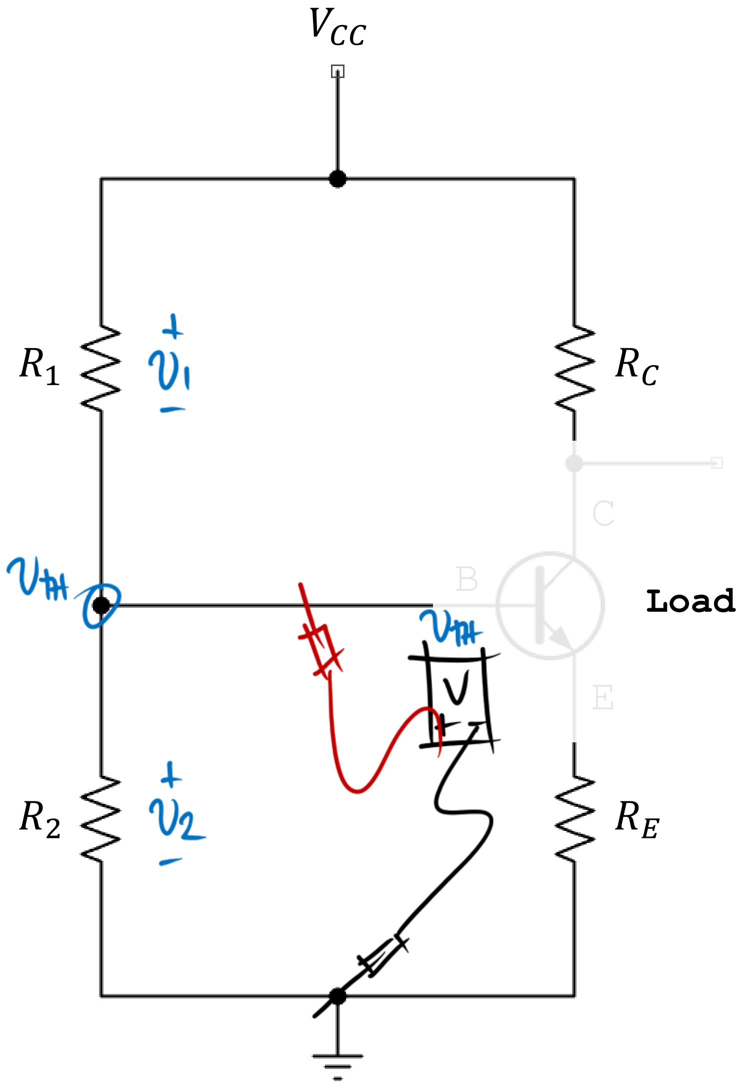
$$\beta = \frac{i_C}{i_B}$$

VOLTAGE-DIVIDER BIAS CIRCUIT



The **voltage-divider bias** uses a pair of resistors (R_1 and R_2) to form a voltage divider that sets the base voltage. This configuration is less sensitive to variations in transistor beta (β) and offers a more **stable operating point**.

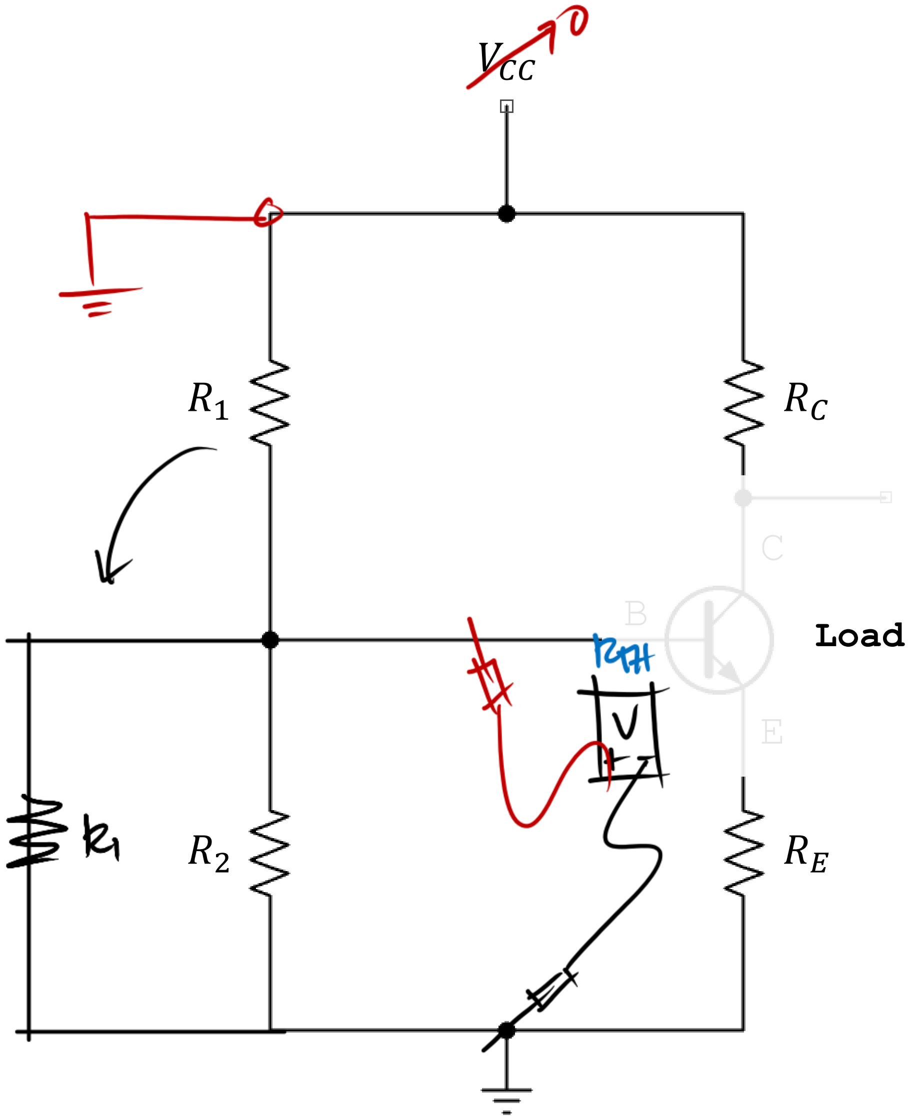
THEVENIN EQUIVALENT CIRCUIT



Thevenin Voltage

$$\boxed{v_{TH} = V_{CC} \frac{R_2}{R_1 + R_2}}$$

THEVENIN EQUIVALENT CIRCUIT



Thevenin Voltage

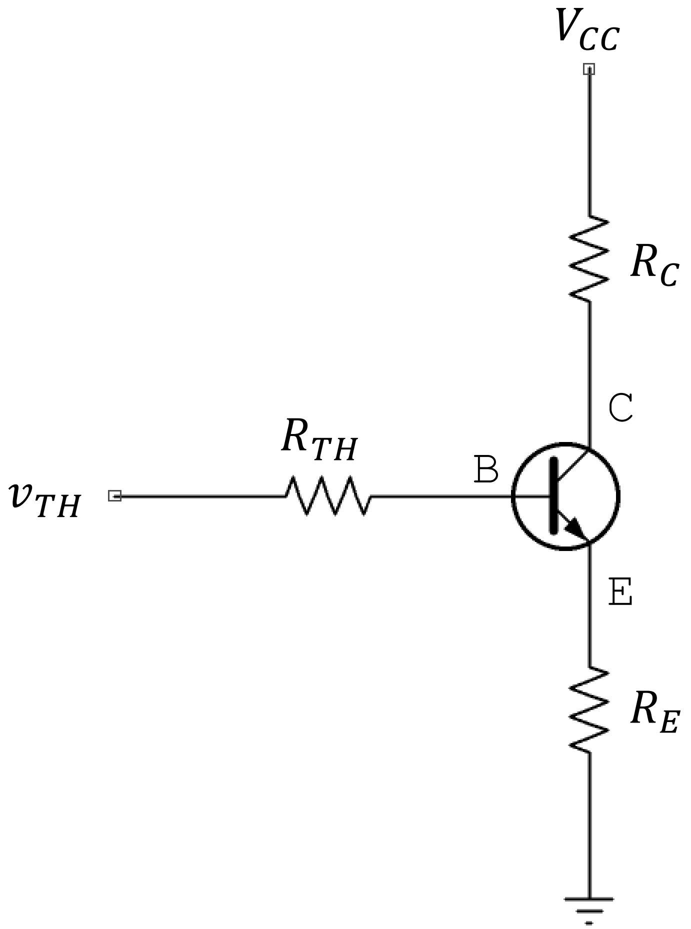
$$\boxed{v_{TH} = V_{cc}\frac{R_2}{R_1 + R_2}}$$

Thevenin Resistance

$$\frac{1}{R_{TH}} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$\boxed{R_{TH} = \left(1/R_1 + 1/R_2\right)^{-1}}$$

THEVENIN EQUIVALENT CIRCUIT



Thevenin Voltage

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$$\frac{1}{R_{TH}} = \frac{1}{R_1} + \frac{1}{R_2}$$

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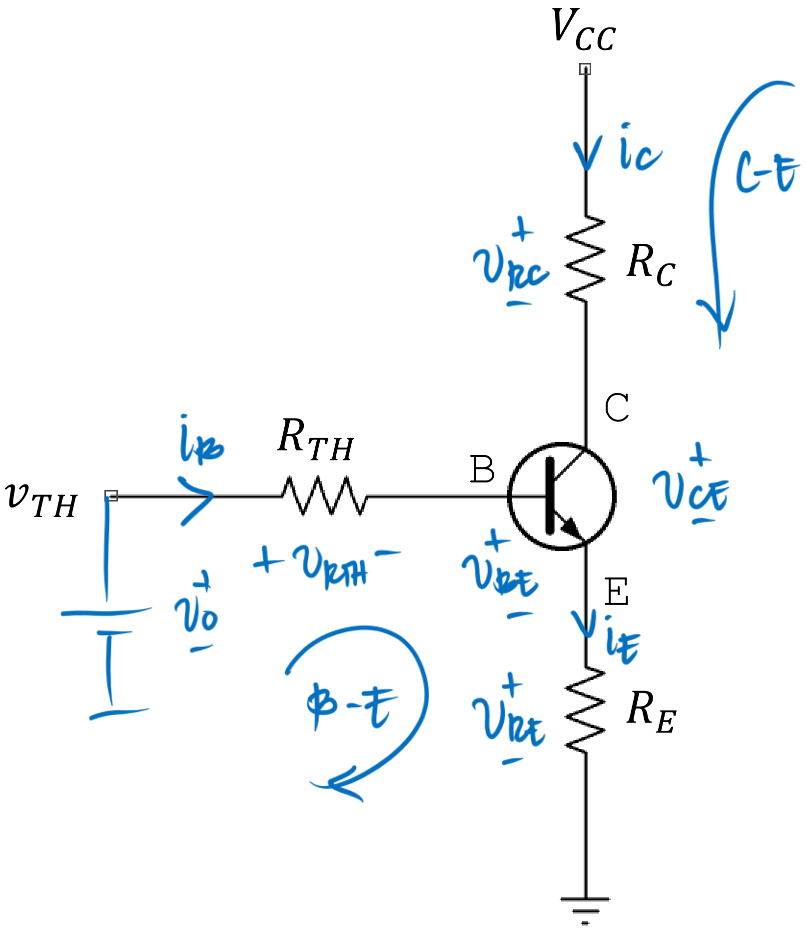
BASE-EMITTER LOOP



KVL @B-E

$$\overset{v_{TH}}{-\cancel{v_o}} + v_{RTH} + v_{BE} + v_{RE} = 0$$

$$v_{RTH} + v_{RE} = v_{TH} - v_{BE}$$

$$i_B R_{TH} + \underline{i_E} R_E = v_{TH} - v_{BE}$$

$$i_E = i_B + i_C \rightarrow \beta = \frac{i_C}{i_B}$$

$$i_E = \underline{i_B} + \beta \underline{i_B}$$

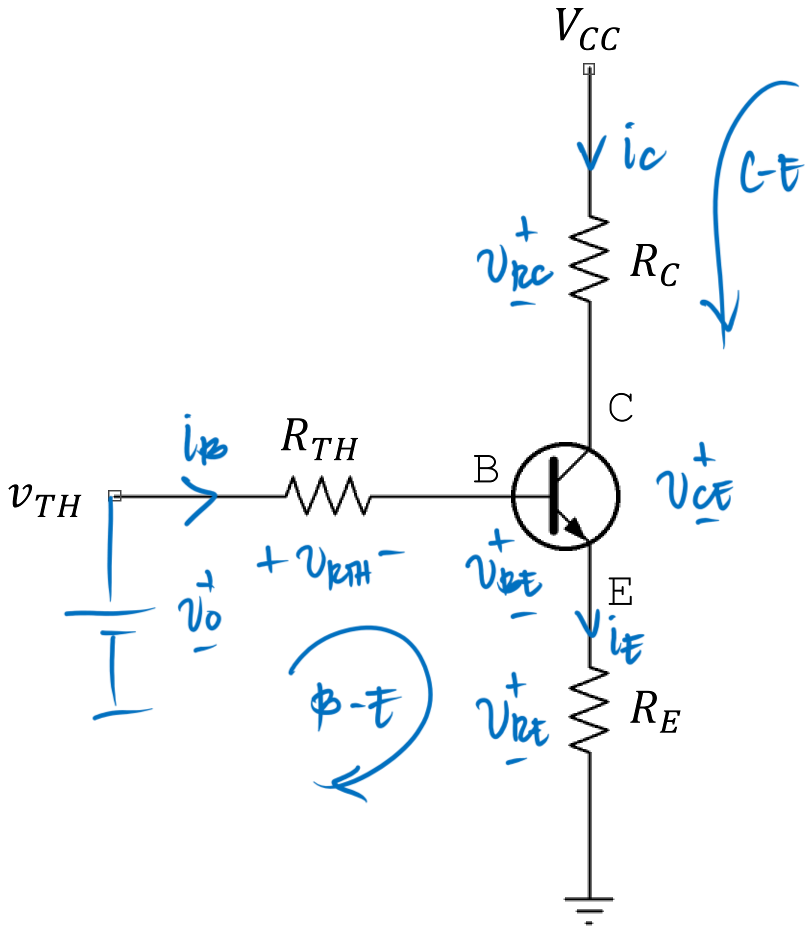
$$i_C = \beta i_B$$

$$\underline{i_E = i_B(\beta+1)}$$

$$i_B R_{TH} + i_B(\beta+1) R_E = v_{TH} - v_{BE}$$

$$i_B \underbrace{\left[R_{TH} + (\beta+1)R_E\right]}_{\cdots} = \underbrace{v_{TH} - v_{BE}}_{\cdots}$$

BASE-EMITTER LOOP

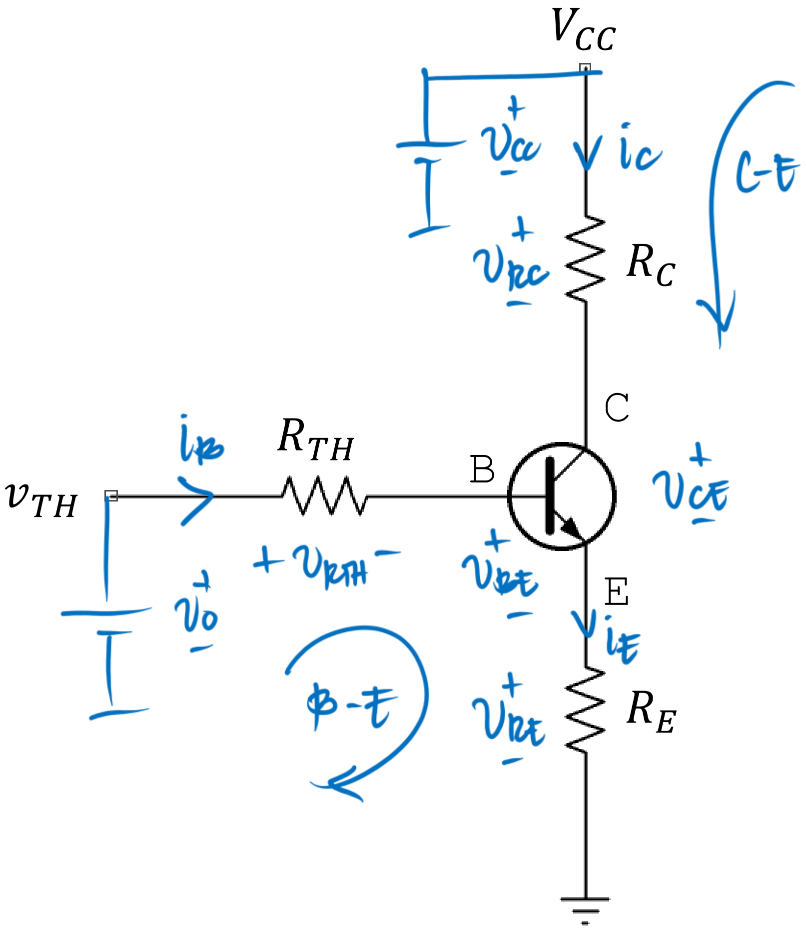


KVL @B-E

$$\underline{i_B\left[R_{TH} + (\beta+1)R_E\right]} = \underline{v_{TH} - v_{BE}}$$

$$\boxed{i_B = \frac{v_{TH} - v_{BE}}{R_{TH} + (\beta+1)R_E}}$$

COLLECTOR-EMITTER LOOP



KVL @C-E

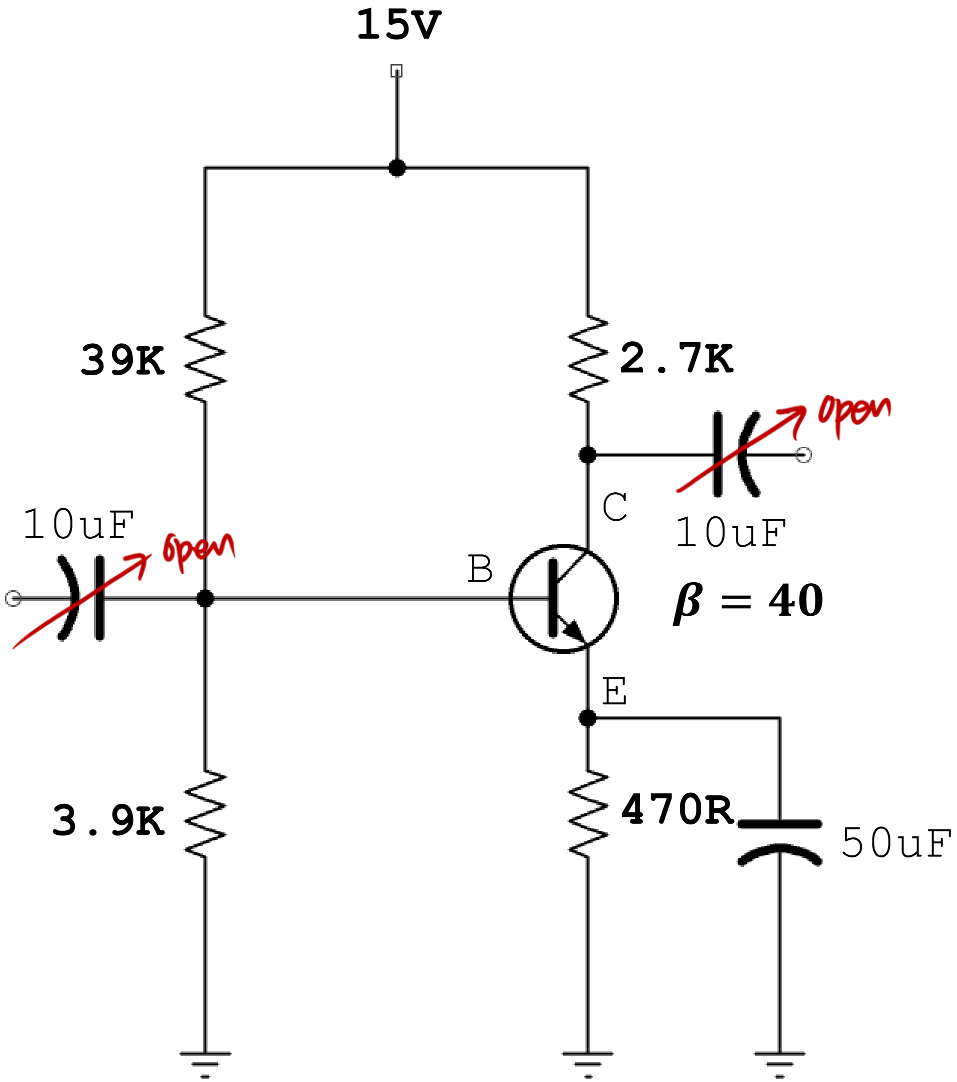
$$-V_{CC} + v_{RC} + \underline{v_{CE}} + v_{RE} = 0$$

$$v_{CE} = V_{CC} - v_{RC} - v_{RE}$$

$$v_{CE} = V_{CC} - i_C R_C - \overset{i_C}{\cancel{i_E}} R_E \rightarrow i_E \approx i_C$$

$$\boxed{v_{CE} = V_{CC} - i_C(R_C + R_E)}$$

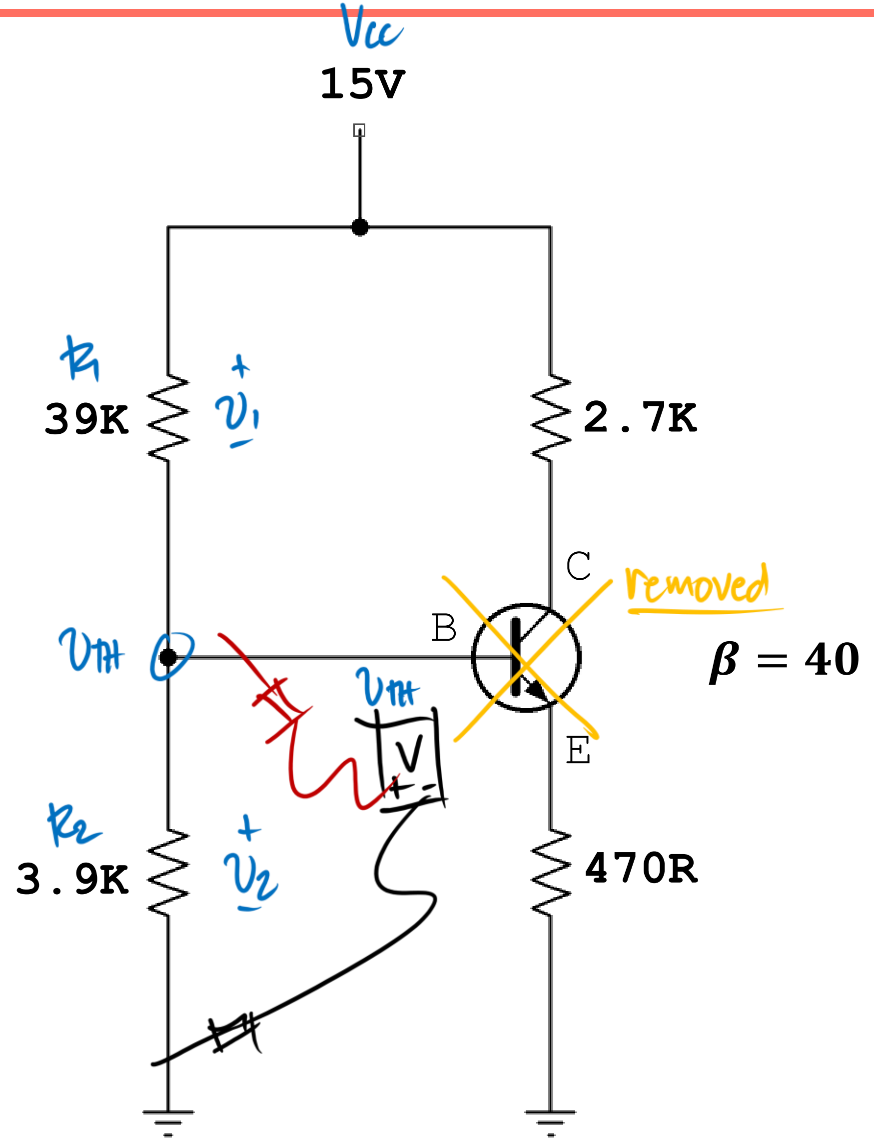
EXERCISE



For the given voltage-divider bias network, determine:

- Base current $\left(i_{BQ}\right)$
- Collector current $\left(i_{CQ}\right)$
- Collector-Emitter voltage $\left(v_{CEQ}\right)$
- Emitter voltage (v_E)
- Collector Voltage (v_C)

EXERCISE



Solution

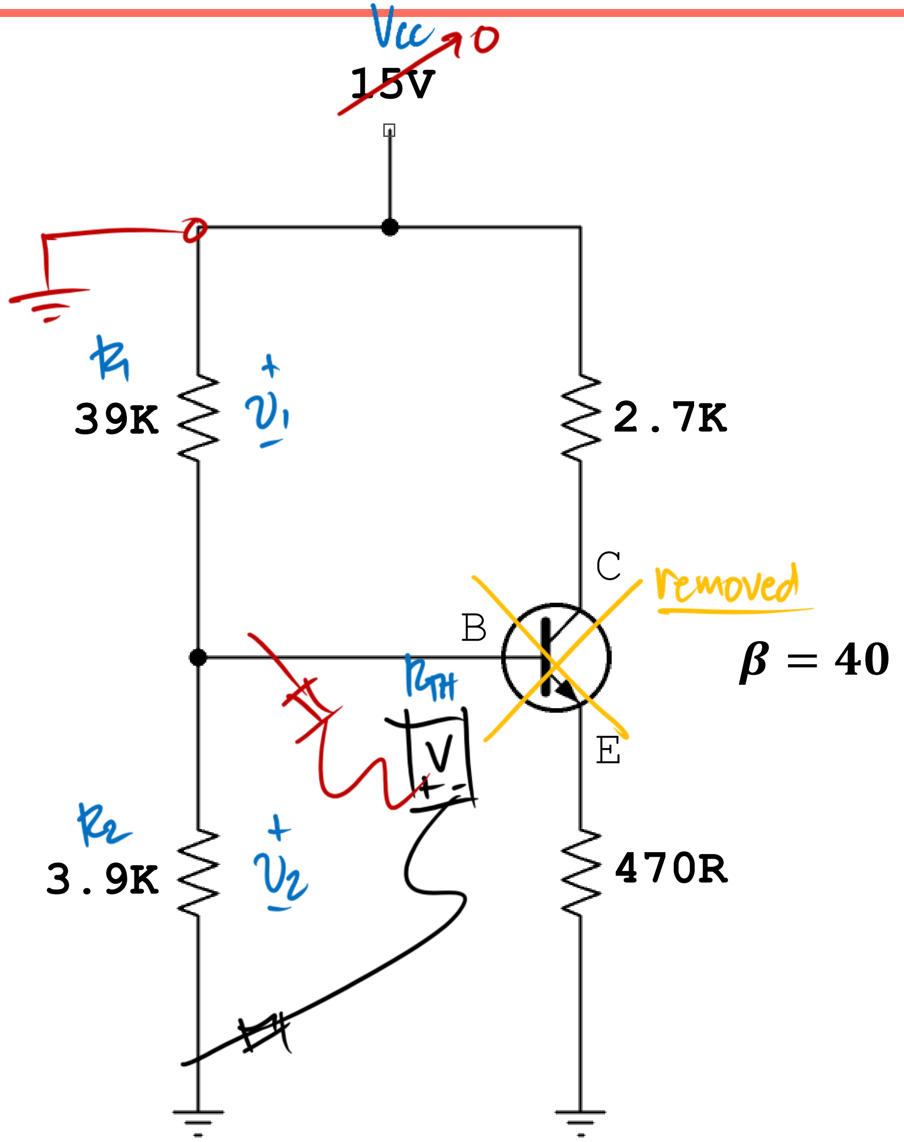
Thevenin Voltage

$$v_{TH} = V_{cc}\frac{R_2}{R_1+R_2}$$

$$v_{TH} = 15\frac{3.9K}{39K+3.9K}$$

$$v_{TH} = 1.36V$$

EXERCISE



Solution

Thevenin Resistance

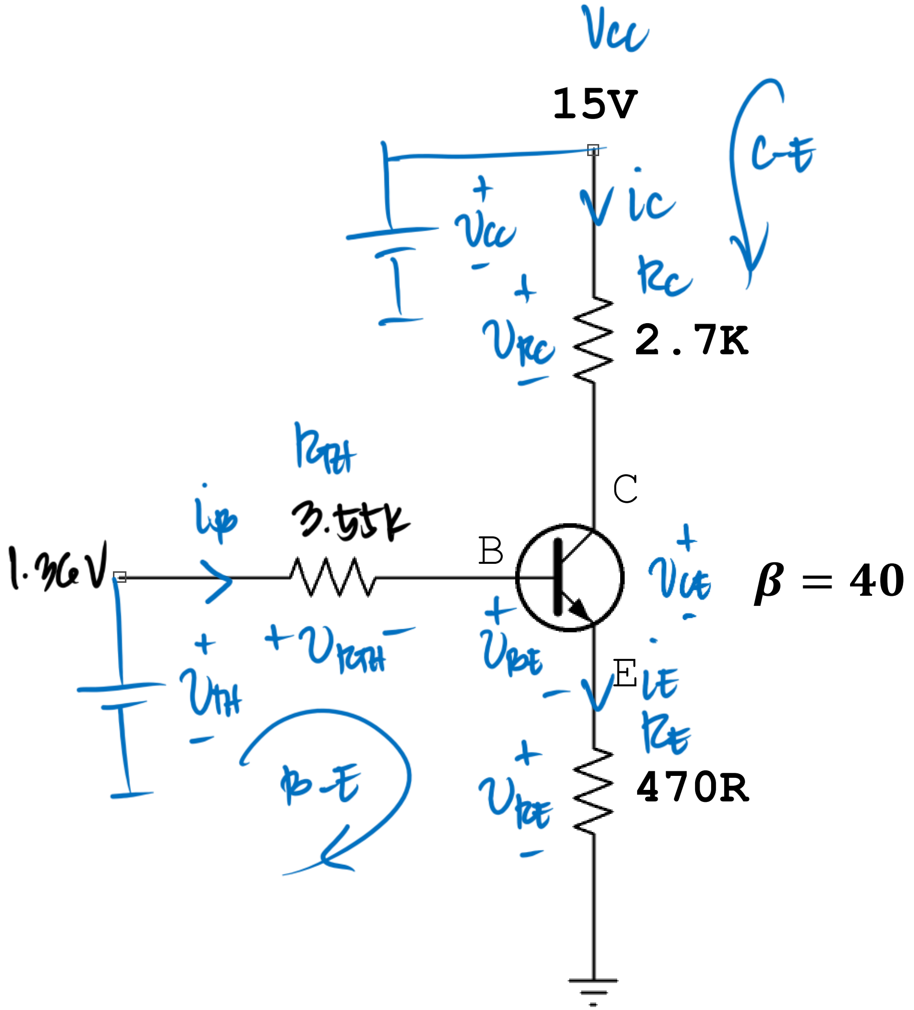
$$\frac{1}{R_{TH}} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$\frac{1}{R_{TH}} = \frac{1}{39k} + \frac{1}{3.9k}$$

$$\frac{1}{R_{TH}} = \frac{11}{39k}$$

$$R_{TH} = 3.55 k\Omega$$

EXERCISE



Solution

KVL @ B-E

$$-V_{TH} + \underline{V_{RTH}} + V_{BE} + \underline{V_{RE}} = 0$$

$$V_{RTH} + V_{RE} = V_{TH} - V_{BE}$$

$$i_B R_{TH} + \underline{i_E} R_E = V_{TH} - V_{BE}$$

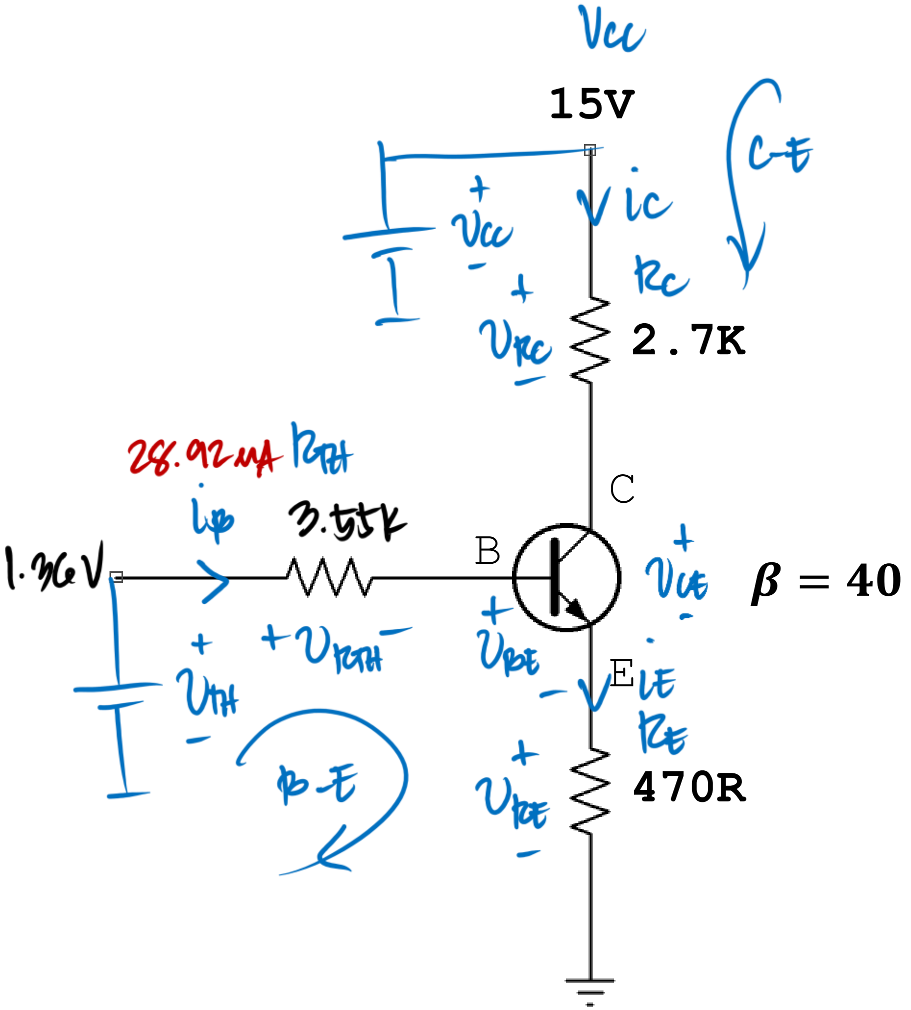
$$i_E = i_B + i_C \rightarrow \beta = \frac{i_C}{i_B}$$

$$i_E = i_B + \beta i_B \qquad i_C = \beta i_B$$

$$i_E = i_B(\beta+1)$$

$$\underline{i_B} R_{TH} + \underline{i_B}(\beta+1) R_E = V_{TH} - V_{BE}$$

EXERCISE



Solution

KVL @ B-E

$$i_B R_{TH} + i_B(\beta+1)R_E = V_{TH} - V_{BE}$$

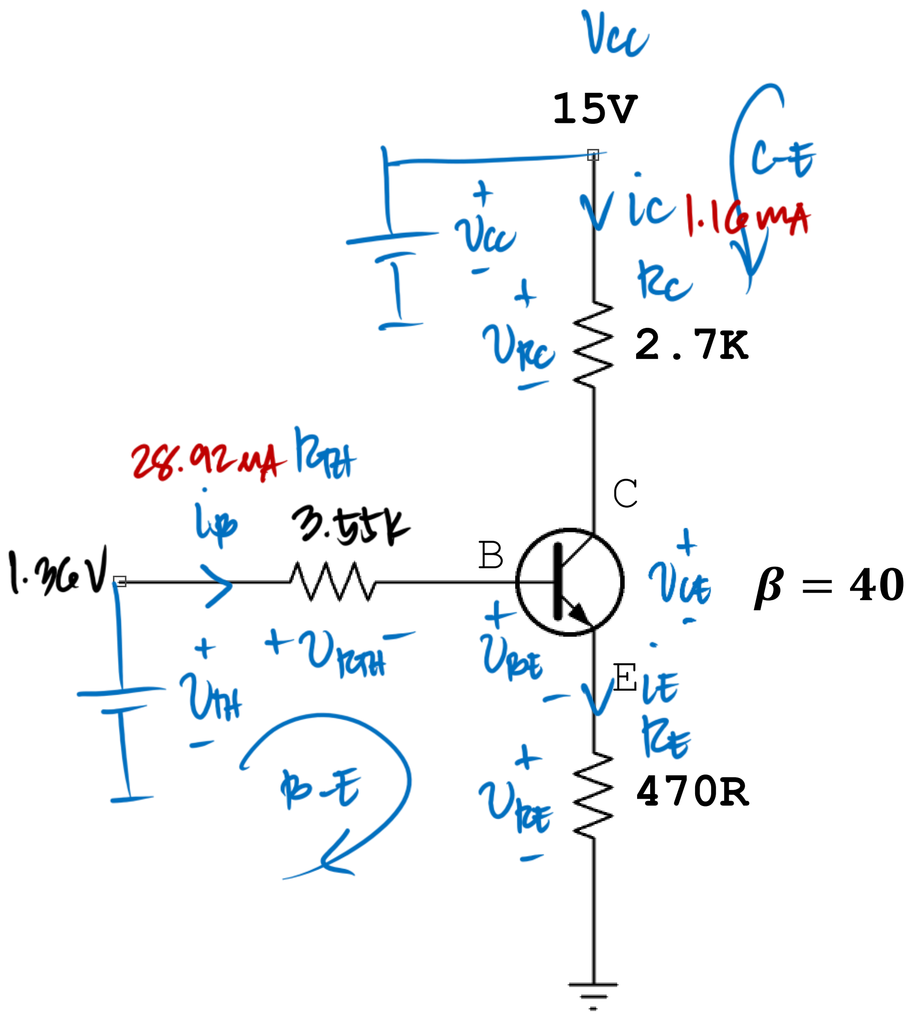
$$i_B\left[R_{TH} + (\beta+1)R_E\right] = V_{TH} - V_{BE}$$

$$i_B = \frac{1.36 - 0.7}{3.55K + (40+1)470}$$

$$\boxed{i_{BQ} = 28.92\mu A}$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_C}{i_B}$$

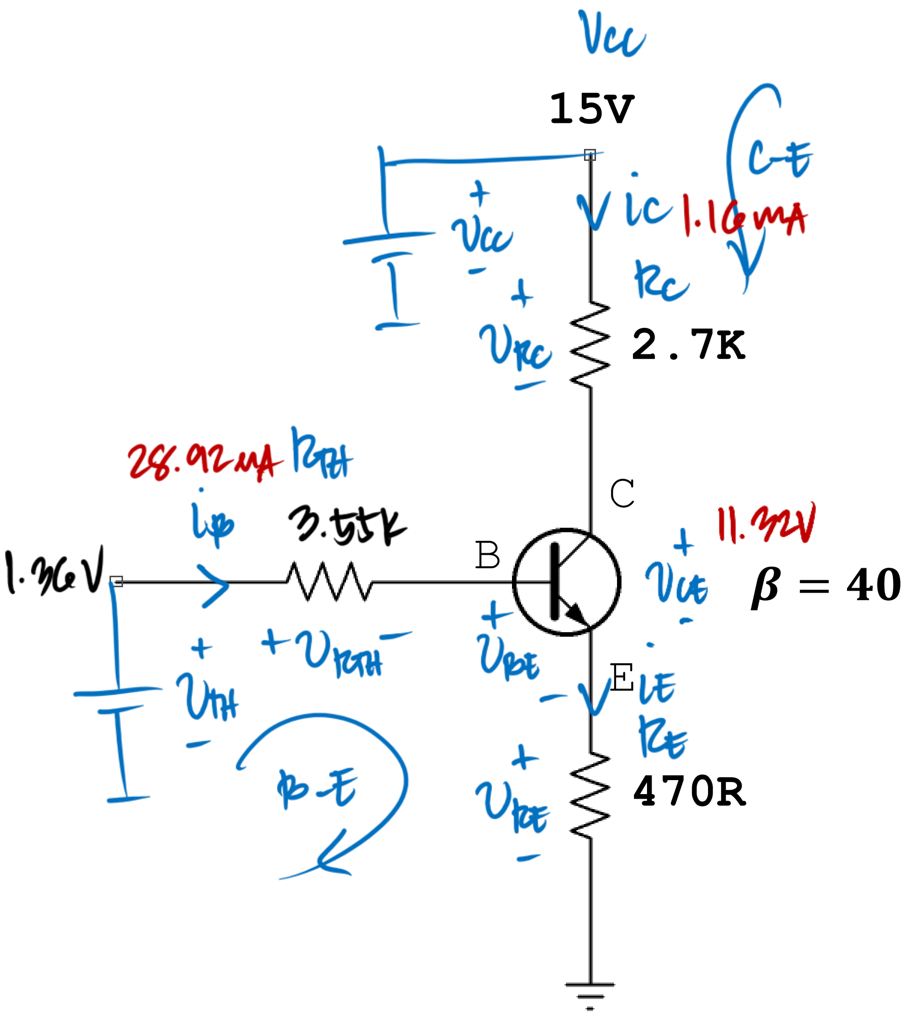
$$i_C = \beta i_B$$

$$i_C = 40(28.92\mu)$$

$$\boxed{i_{CQ} = 1.16 \text{ mA}}$$

ans

EXERCISE



Solution

KVL @ C-E

$$-V_{CC} + V_{RC} + \underline{V_{CE}} + V_{RE} = 0$$

$$V_{CE} = V_{CC} - V_{RC} - V_{RE}$$

$$V_{CE} = V_{CC} - i_C R_C - \overset{i_C}{\cancel{i_E}} R_E \rightarrow i_C \approx i_E$$

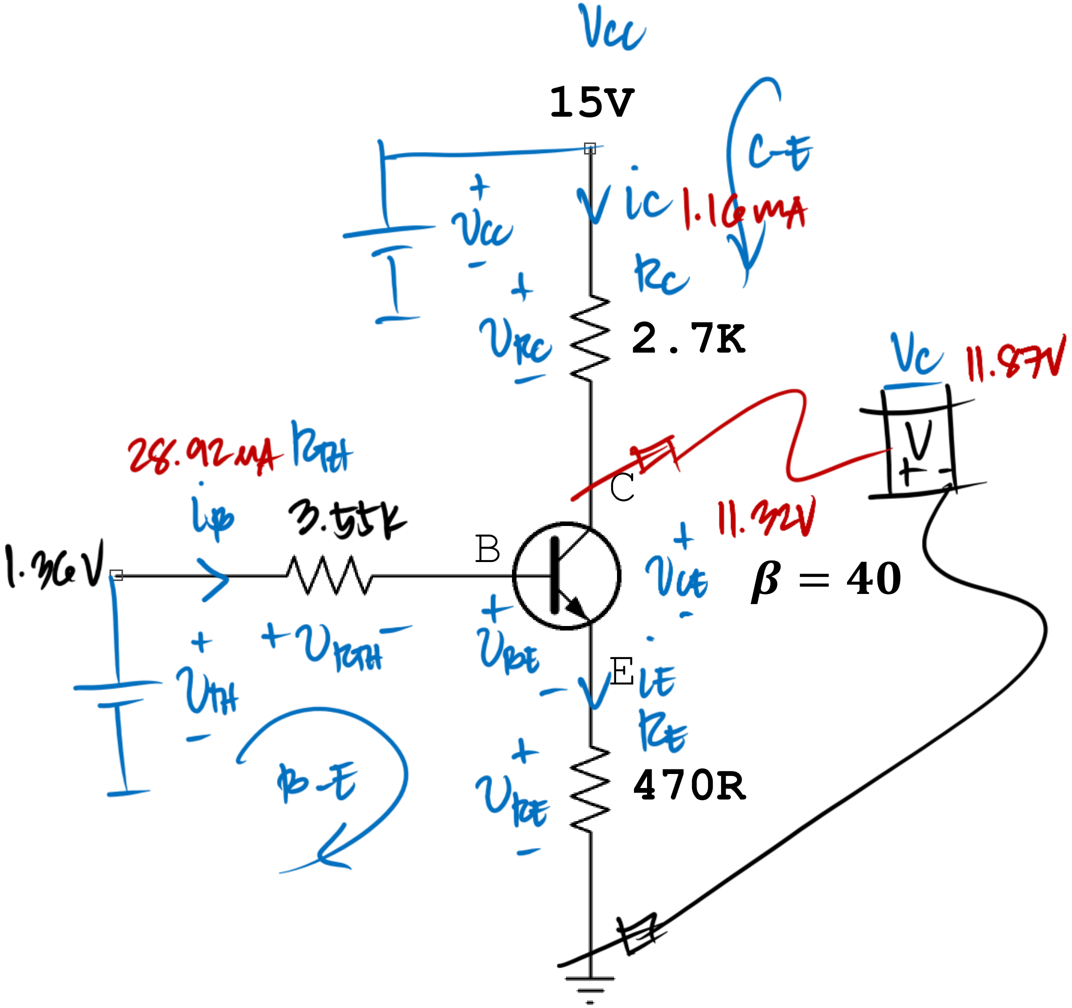
$$V_{CE} = V_{CC} - i_C (R_C + R_E)$$

$$V_{CE} = 15 - 1.16m(2.7K + 470)$$

$$\boxed{V_{CEQ} = 11.32V}$$

ans

EXERCISE



Solution

KVL@ C-E

$$-V_{cc} + V_{RC} + V_C = 0$$

$$V_C = V_{cc} - V_{RC}$$

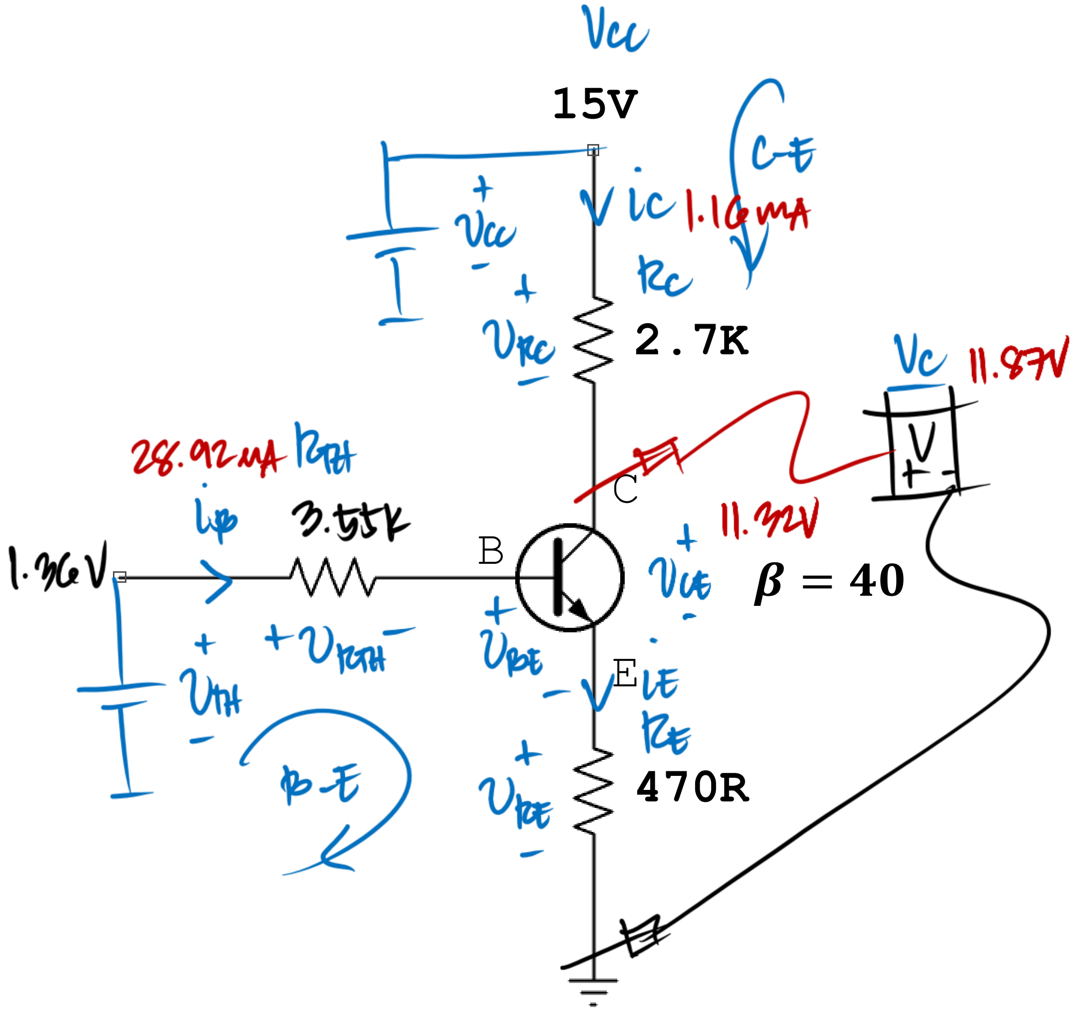
$$V_C = V_{cc} - i_C R_C$$

$$V_C = 15 - 1.16m(2.7K)$$

$$\boxed{V_C = 11.87V}$$

ans

EXERCISE



Solution

Node Analysis Method

$v_{CE} = v_C - v_E$

$v_E = v_C - v_{CE}$

$v_E = 11.87 - 11.32$

$$\boxed{v_E = 0.55V}$$

ans

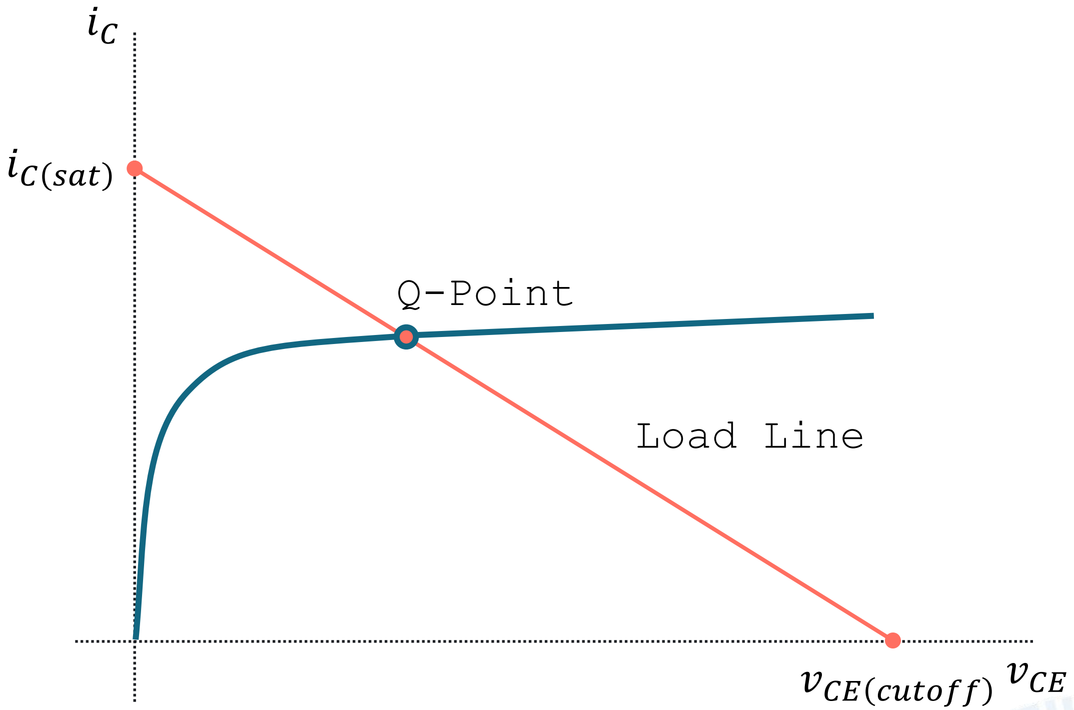
LOAD LINE ANALYSIS

SATURATION POINT

The **saturation point** is the operating state where BJT conducts the **maximum collector current** ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

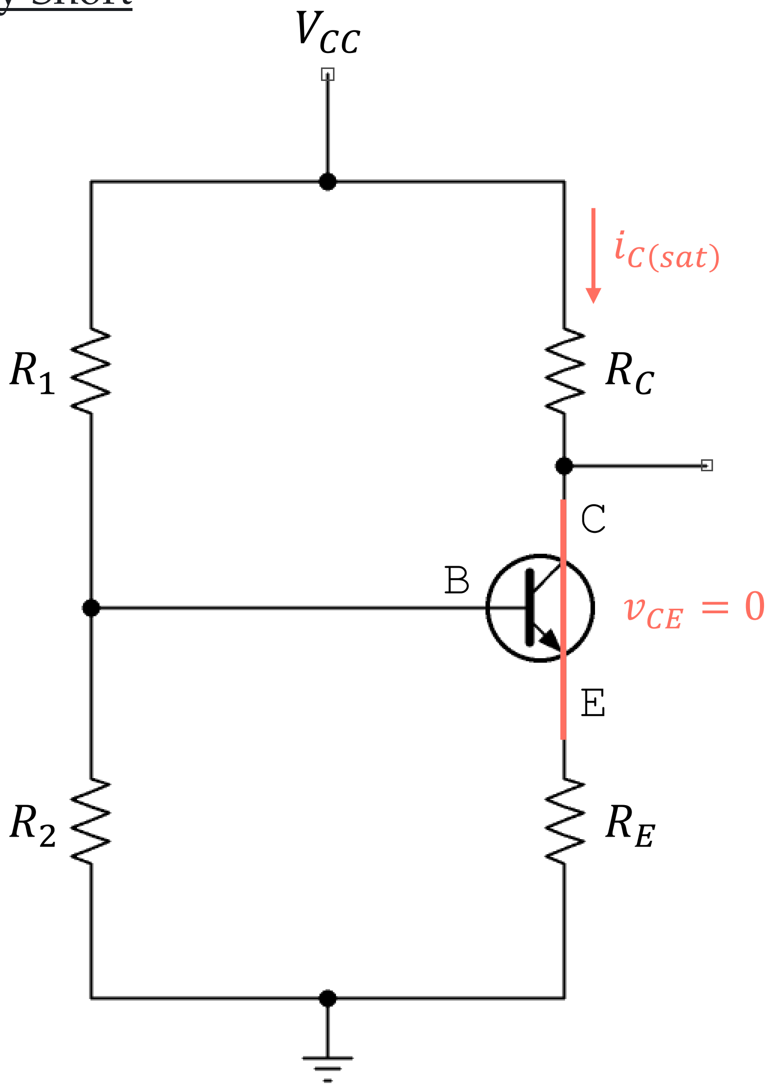
In this region the transistor acts like a **closed switch** (zero resistance between collector-emitter).

Collector Characteristic Curve

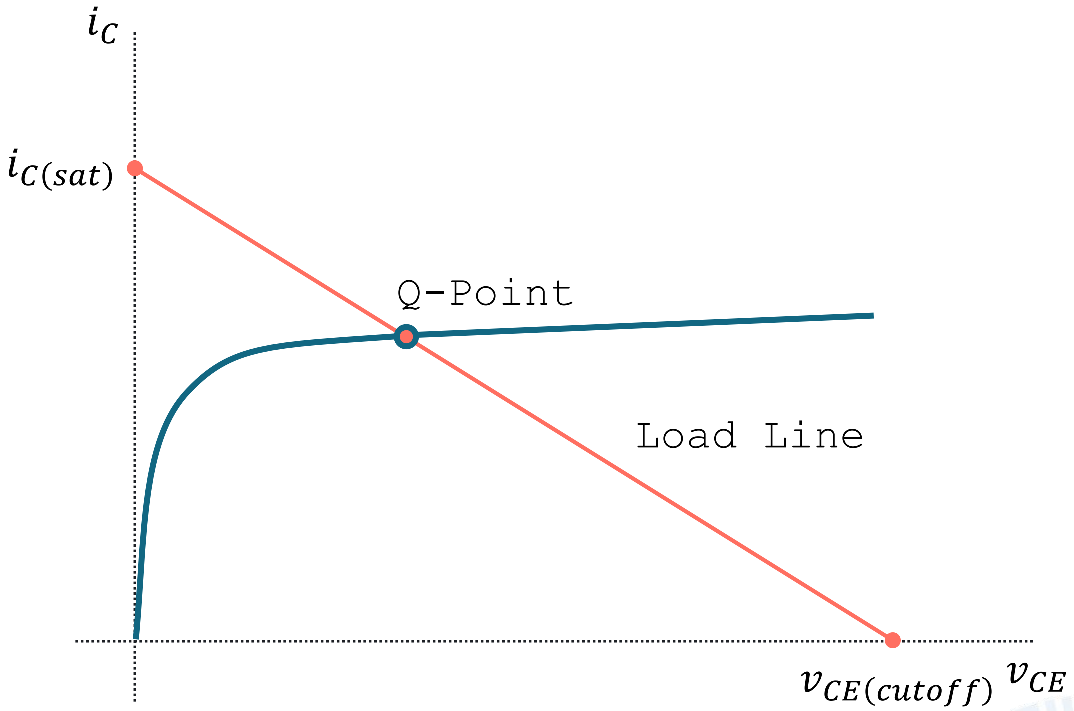


SATURATION POINT

Mentally Short



Collector Characteristic Curve

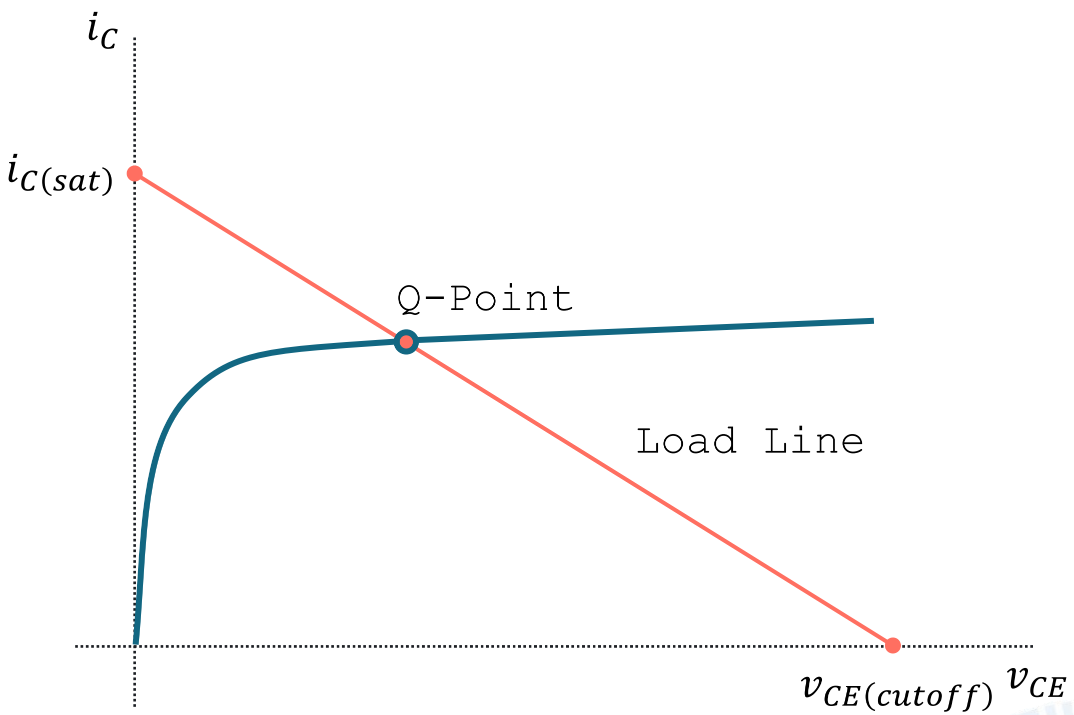


CUTOFF POINT

The **cutoff point** is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

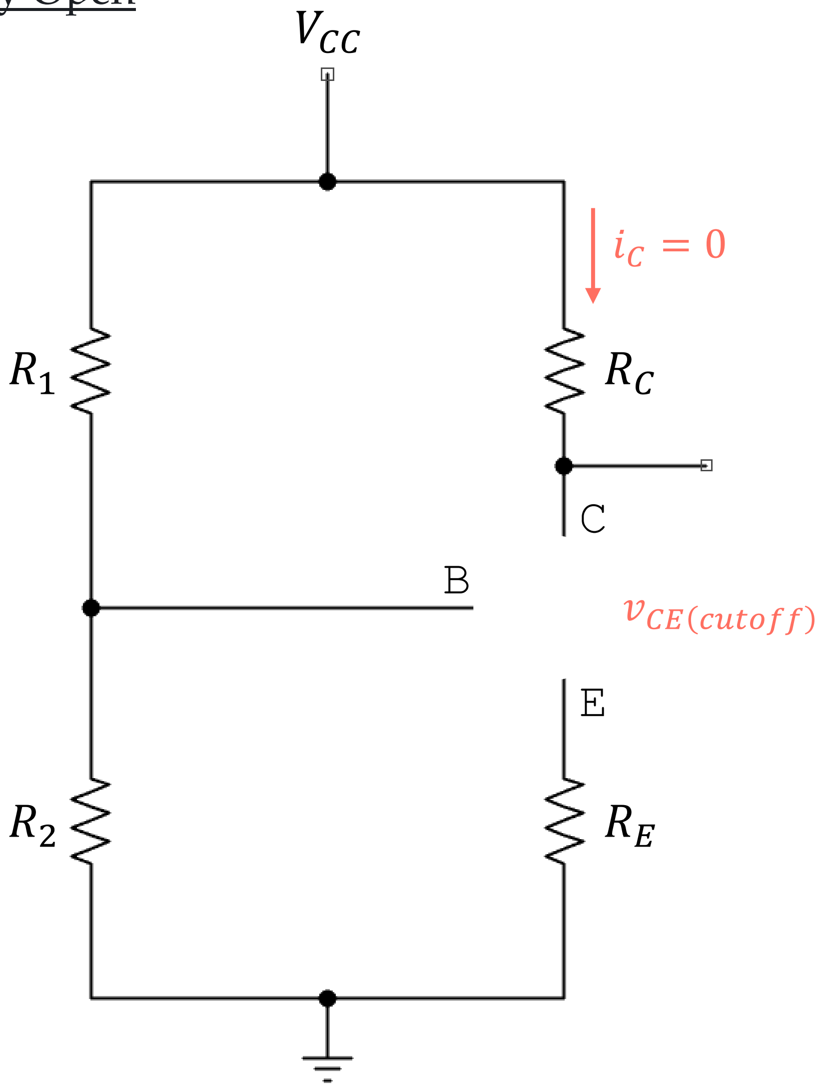
In this region the transistor acts like an **open switch** (infinite resistance between collector-emitter).

Collector Characteristic Curve

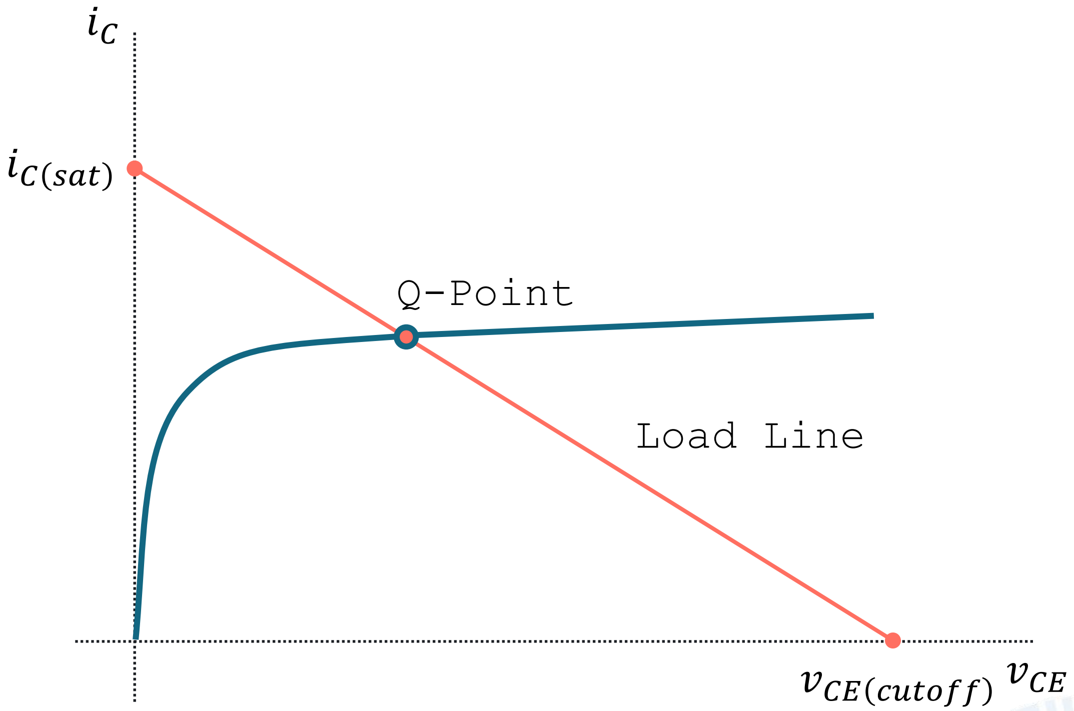


CUTOFF POINT

Mentally Open



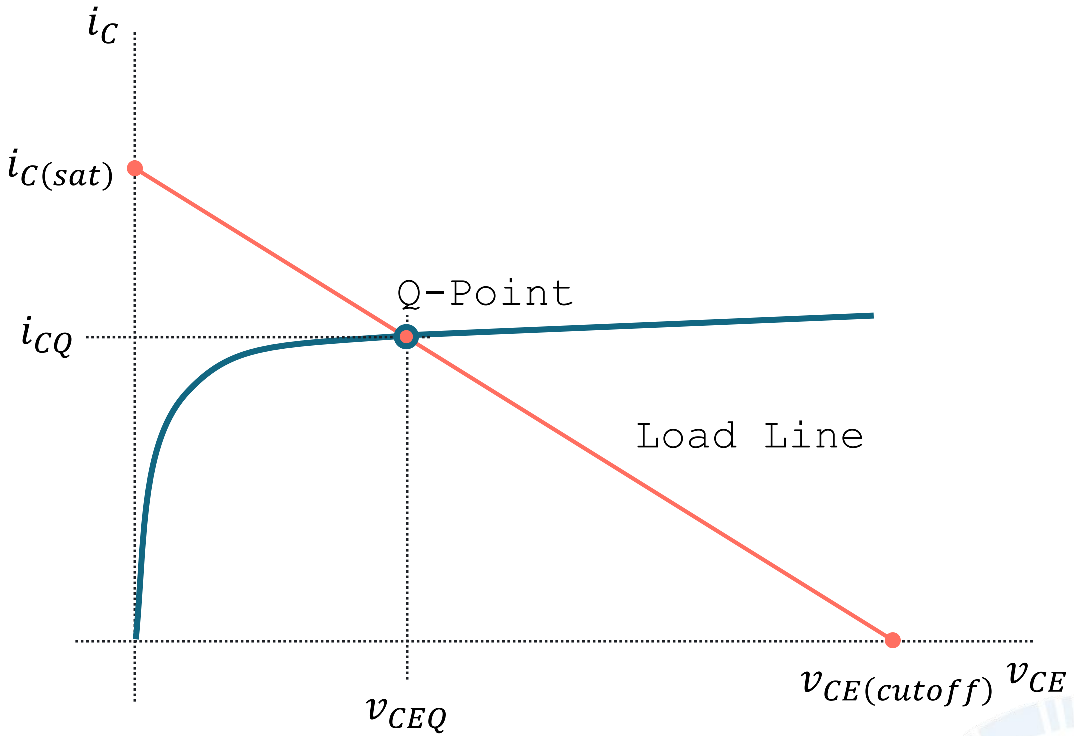
Collector Characteristic Curve



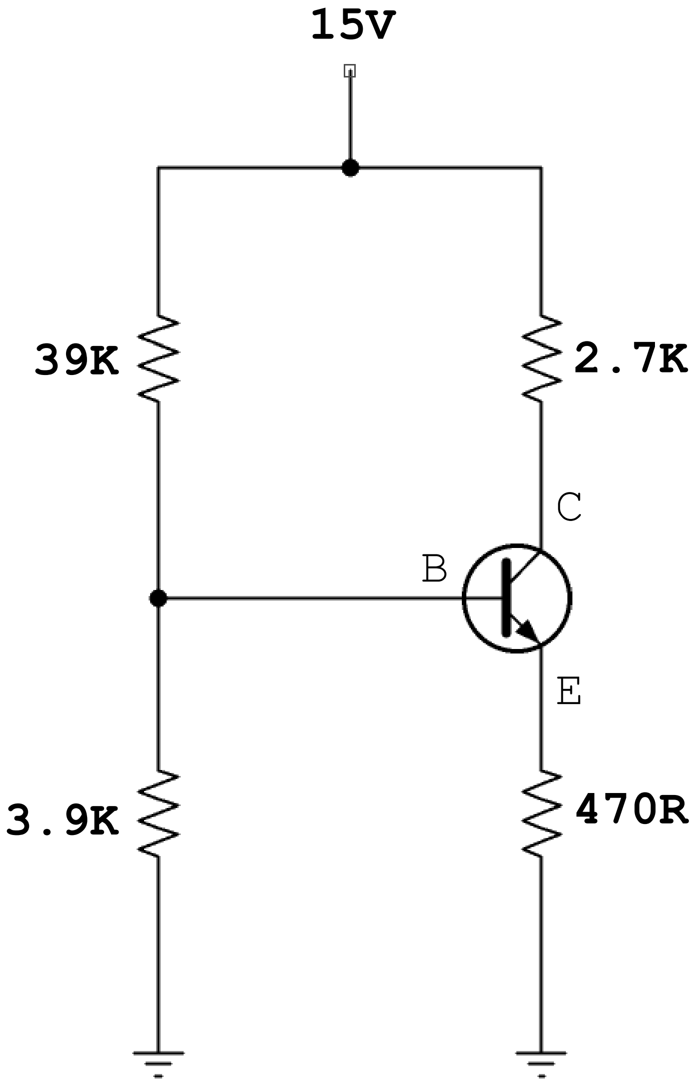
QUIESCENT POINT

The **Q-point** is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}).

Collector Characteristic Curve



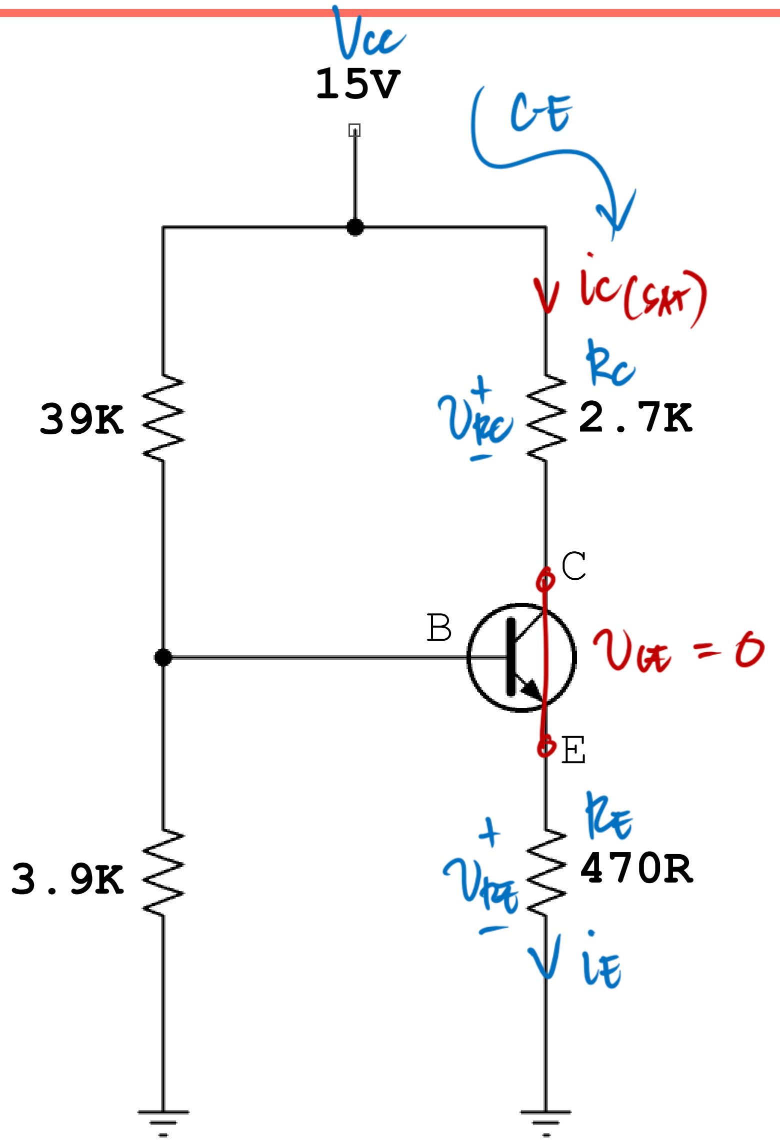
EXERCISE



Plot the DC load line analysis for the voltage-divider bias network, indicating:

- Saturation current ($i_{C(sat)}$)
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

EXERCISE



Solution

Saturation Point

KVL @ C-E

$$-V_{CC} + V_{RC} + \cancelto{0}{V_{CE}} + V_{RE} = 0$$

$$i_C R_C + \overset{i_C}{\cancel{i_E}} R_E = V_{CC} \rightarrow i_E \approx i_C$$

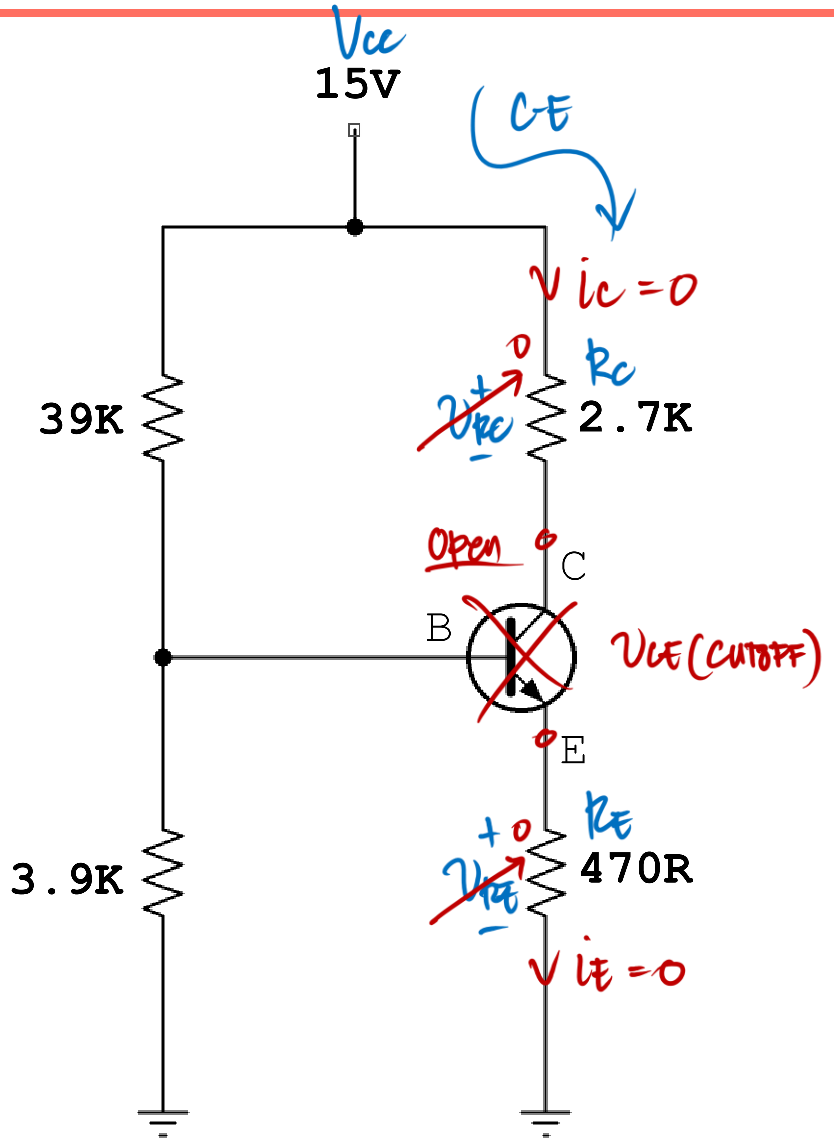
$$\cancelto{0}{\frac{i_C(R_C + R_E)}{R_C + R_E}} = \frac{V_{CC}}{R_C + R_E}$$

$$i_C = \frac{15}{2.7k + 470}$$

$$\boxed{i_{C(SAT)} = 4.73\,mA}$$

ans

EXERCISE



Solution

Cutoff Point

KVL @ C-E

$$-V_{CC} + \cancel{V_{RC}}^{0} + V_{CE} + \cancel{V_{RE}}^{0} = 0$$

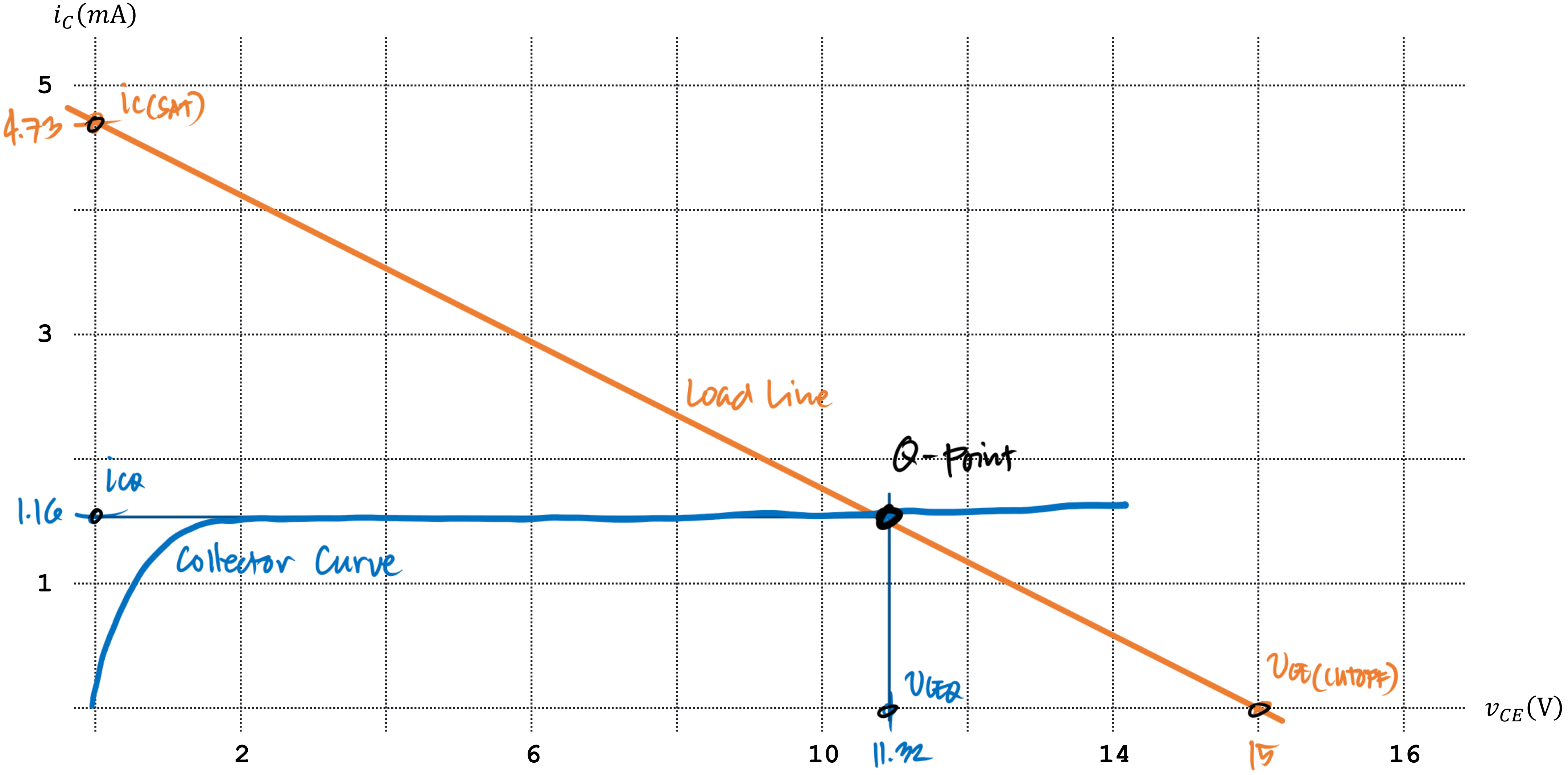
$$V_{CE} = V_{CC}$$

$$\boxed{V_{CE(CUTOFF)} = 15V}$$

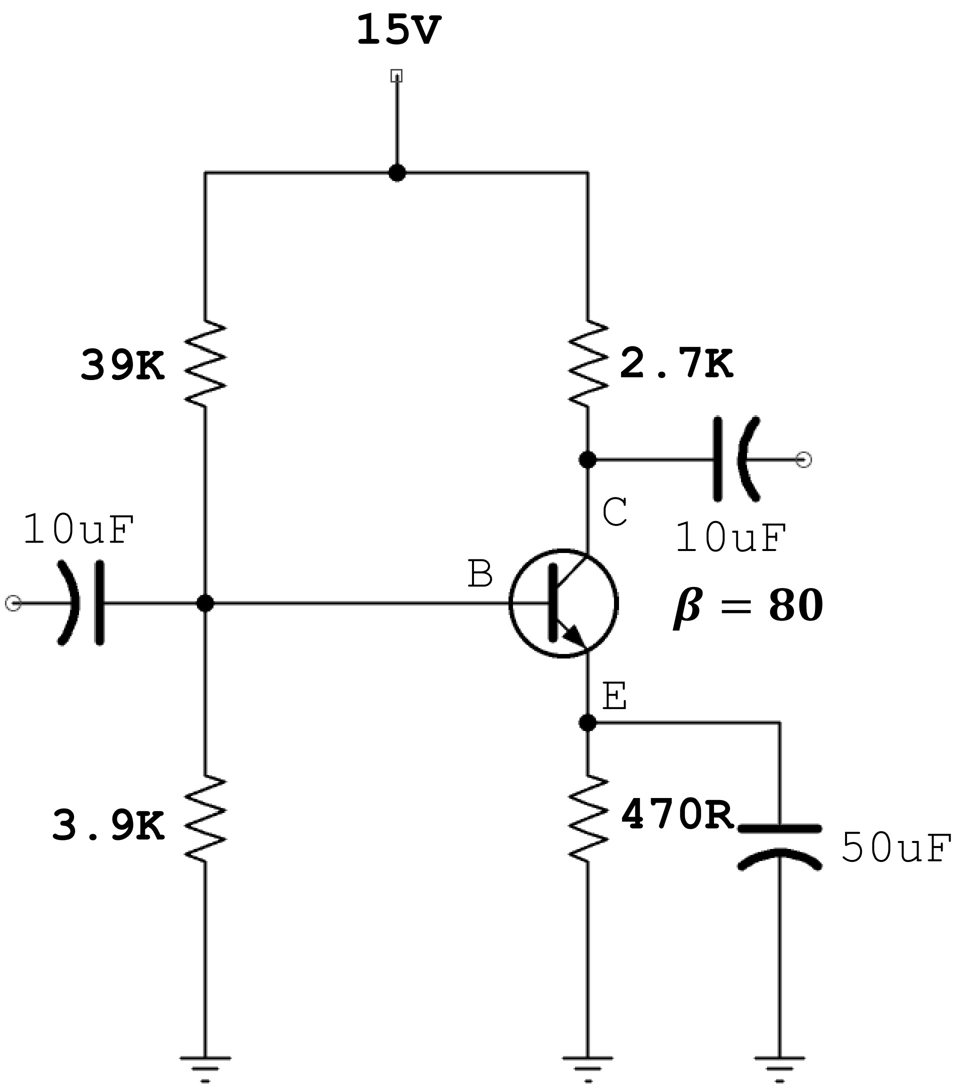
ans

EXERCISE

Load Line Analysis



EXERCISE



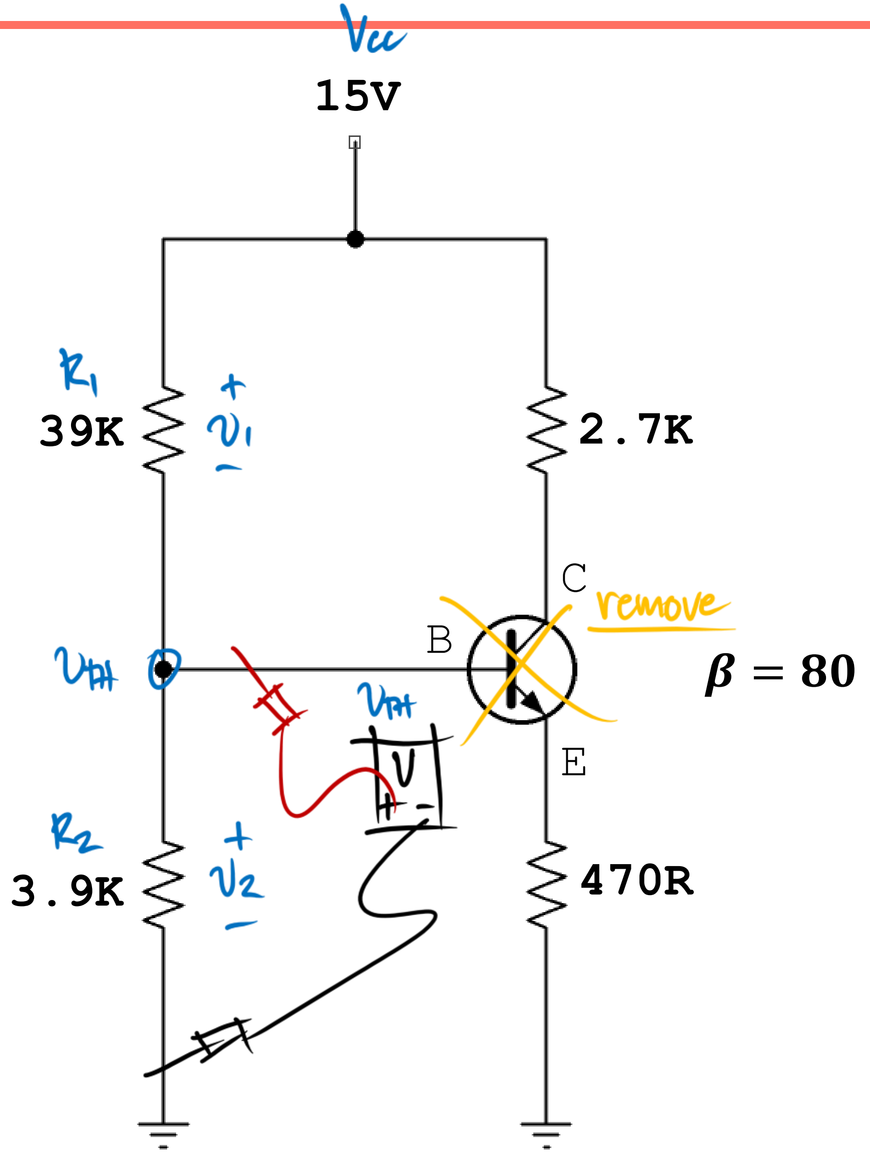
For the given voltage-divider bias network, determine:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})

And plot the DC load line analysis indicating:

- Saturation current $(i_{C(sat)})$
- Cutoff voltage $(v_{CE(cutoff)})$
- Operating Point (Q-Point)

EXERCISE



Solution

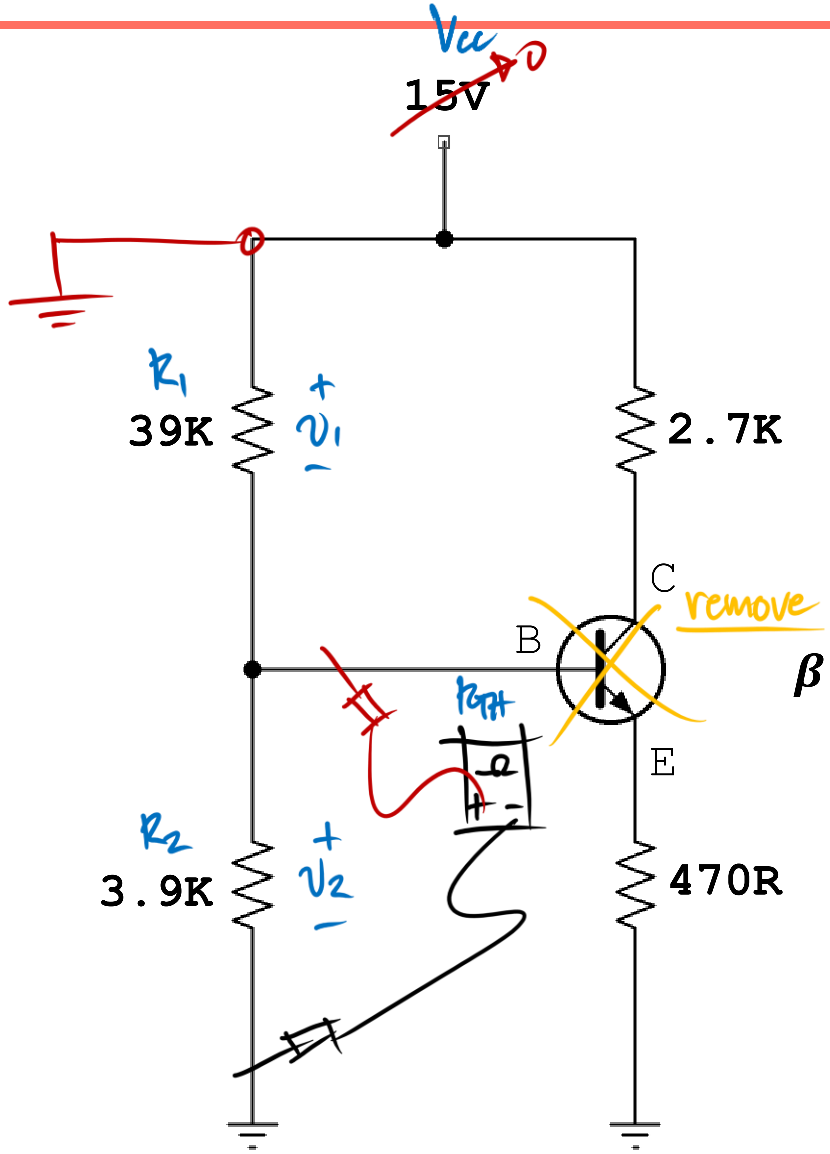
Thevenin Voltage

$$v_{TH} = V_{cc} \frac{R_1}{R_1 + R_2}$$

$$v_{TH} = 15 \frac{3.9K}{39K + 3.9K}$$

$$v_{TH} = 1.36V$$

EXERCISE



$\beta = 80$

Solution

Thevenin Resistance

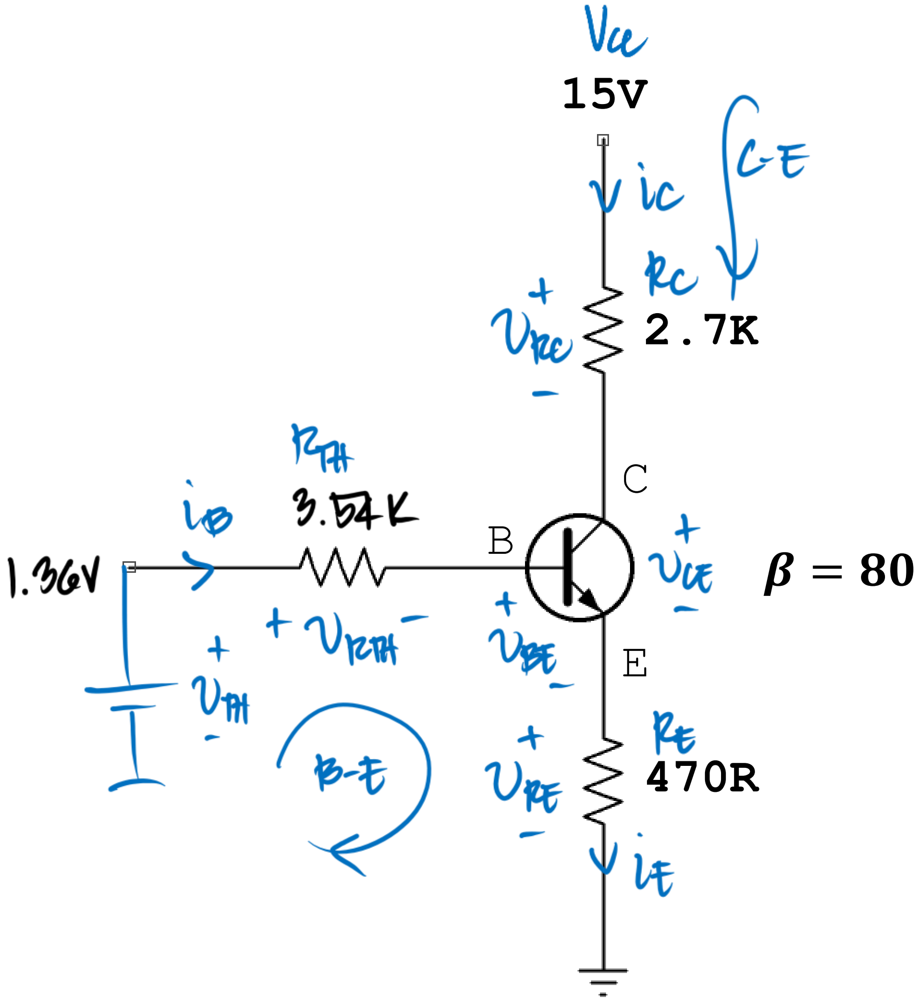
$$\frac{1}{R_{TH}} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$\frac{1}{R_{TH}} = \frac{1}{39K} + \frac{1}{3.9K}$$

$$\frac{1}{R_{TH}} = \frac{11}{39K}$$

$$R_{TH} = 3.54K$$

EXERCISE



Solution

KVL @ B-E

$$-v_{TH} + \underline{v_{RTH}} + v_{BE} + \underline{v_{RE}} = 0$$

$$v_{RTH} + v_{RE} = v_{TH} - v_{BE}$$

$$i_B R_{TH} + \underline{i_E} R_E = v_{TH} - v_{BE}$$

$$i_E = i_B + i_C \rightarrow \beta = \frac{i_C}{i_B}$$

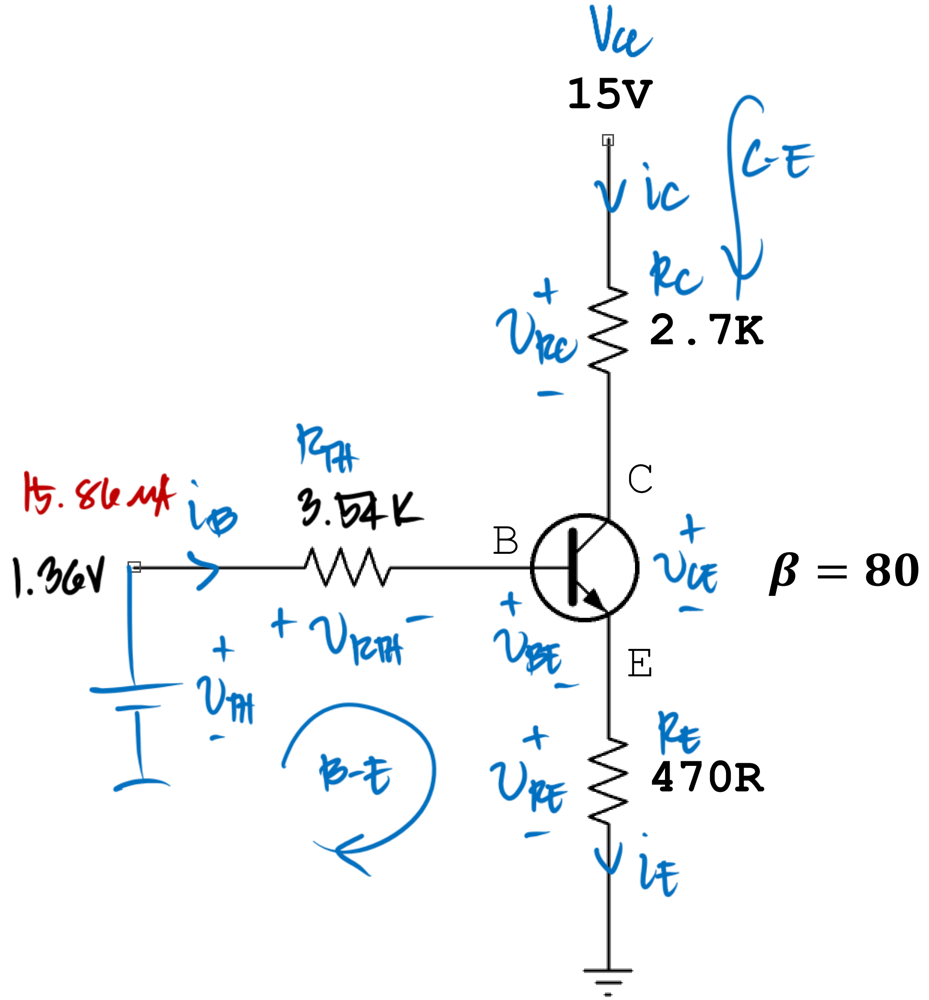
$$i_E = \underline{i_B} + \beta \underline{i_B}$$

$$i_C = \beta i_B$$

$$i_E = i_B(\beta+1)$$

$$\underline{i_B} R_{TH} + \underline{i_B}(\beta+1) R_E = v_{TH} - v_{BE}$$

EXERCISE



Solution

KVL @ B-E

$$i_B R_{TH} + i_B(\beta+1)R_E = v_{TH} - v_{BE}$$

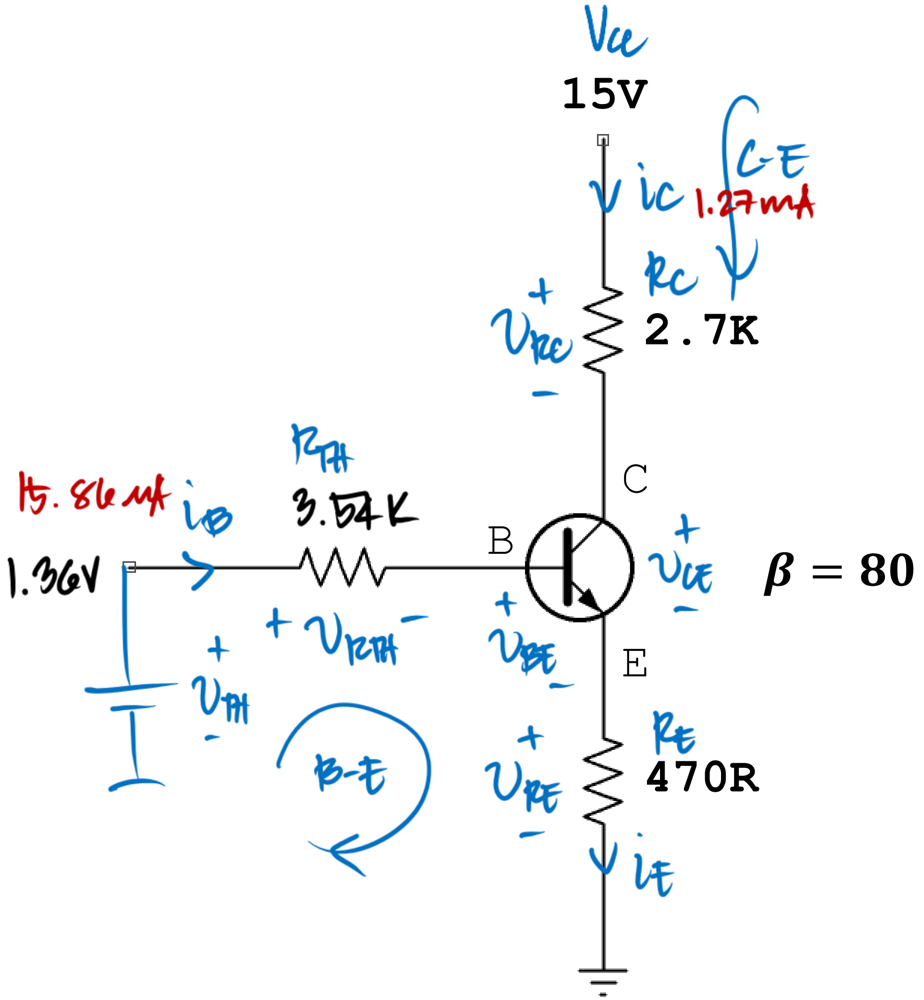
$$i_B\left[R_{TH} + (\beta+1)R_E\right] = v_{TH} - v_{BE}$$

$$i_B = \frac{1.36 - 0.7}{3.54K + (80+1)470}$$

$$\boxed{i_B = 15.86\,\mu A}$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_C}{i_B}$$

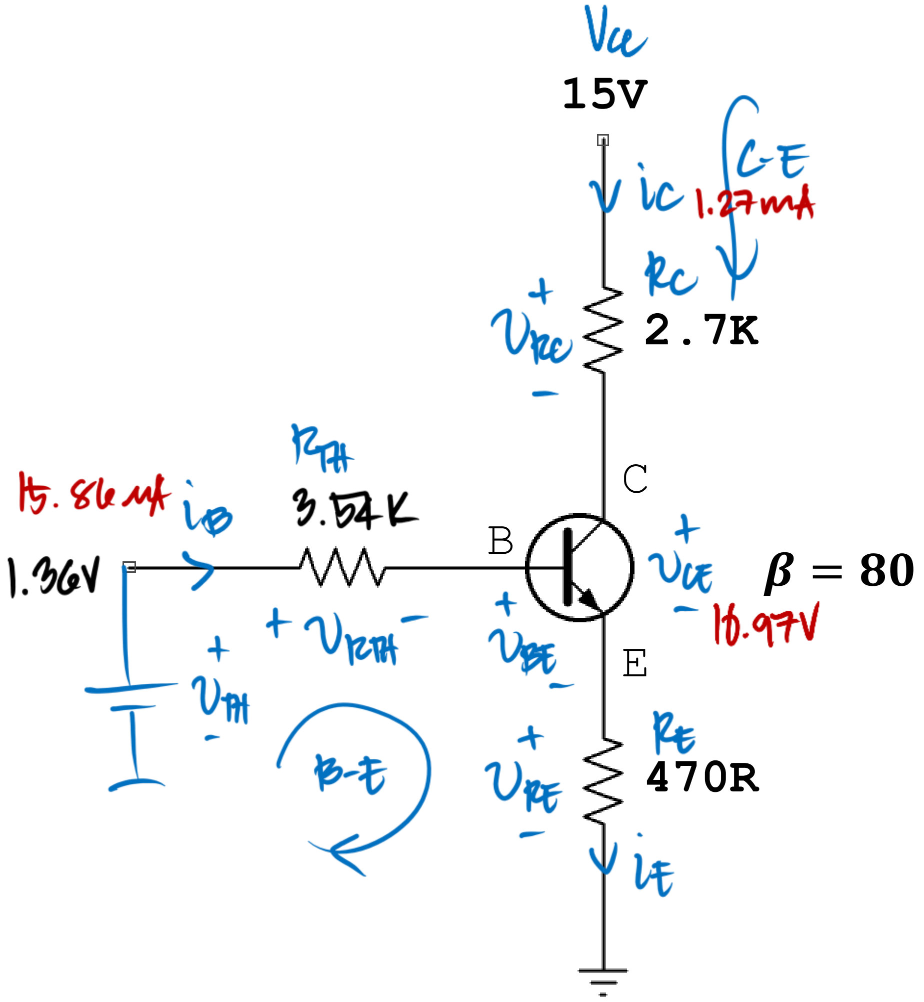
$$i_C = \beta i_B$$

$$i_C = 80(15.86\mu)$$

$$\boxed{i_{CQ} = 1.27\ \text{mA}}$$

ans

EXERCISE



Solution

KVL @ C-E

$$-V_{CC} + V_{RC} + \underline{V_{CE}} + V_{RE} = 0$$

$$V_{CE} = V_{CC} - V_{RC} - V_{RE}$$

$$V_{CE} = V_{CC} - i_C R_C - \overset{i_C}{\cancel{i_E}} R_E \rightarrow i_C \approx i_E$$

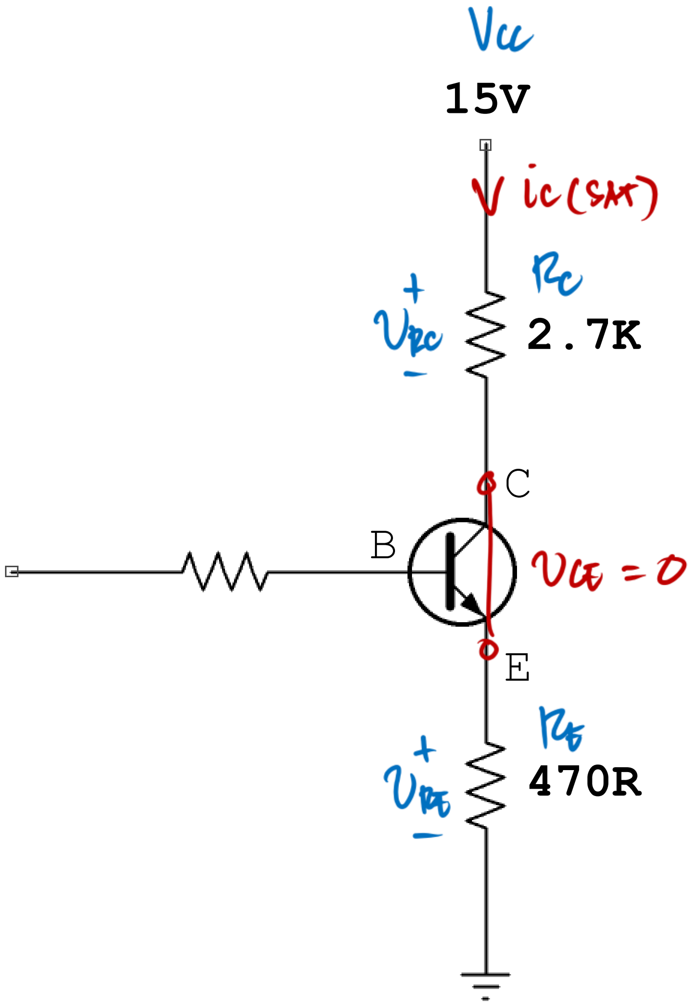
$$V_{CE} = V_{CC} - i_C(R_C + R_E)$$

$$V_{CE} = 15 - 1.27m(2.7K + 470)$$

$$\boxed{V_{CEQ} = 10.97V}$$

ans

EXERCISE



Solution

Saturation Point

KVL @ CE

$$-V_{cc} + V_{RC} + \overset{0}{\cancel{V_{CE}}} + V_{RE} = 0$$

$$V_{RC} + V_{RE} = V_{cc}$$

$$i_C R_C + \overset{i_C}{\cancel{i_E}} R_E = V_{cc} \rightarrow i_C \approx i_E$$

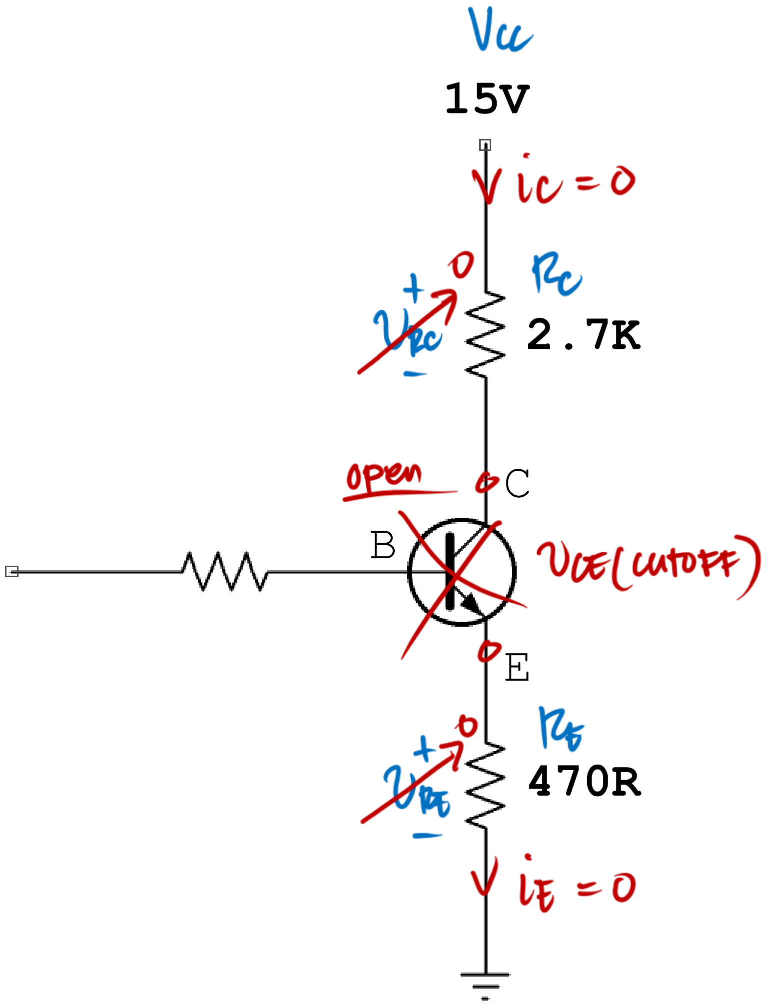
$$\frac{i_C \overset{1}{\cancel{(R_C + R_E)}}}{\cancel{R_C + R_E}} = \frac{V_{cc}}{R_C + R_E}$$

$$i_C = \frac{15}{2.7k + 470}$$

$$\boxed{i_{CQ} = 4.73\ mA}$$

ans

EXERCISE



Solution

Cutoff Point

KVL@ CE

$$-V_{CC} + \cancel{V_{RC}}^{\,0} + V_{CE} + \cancel{V_{RE}}^{\,0} = 0$$

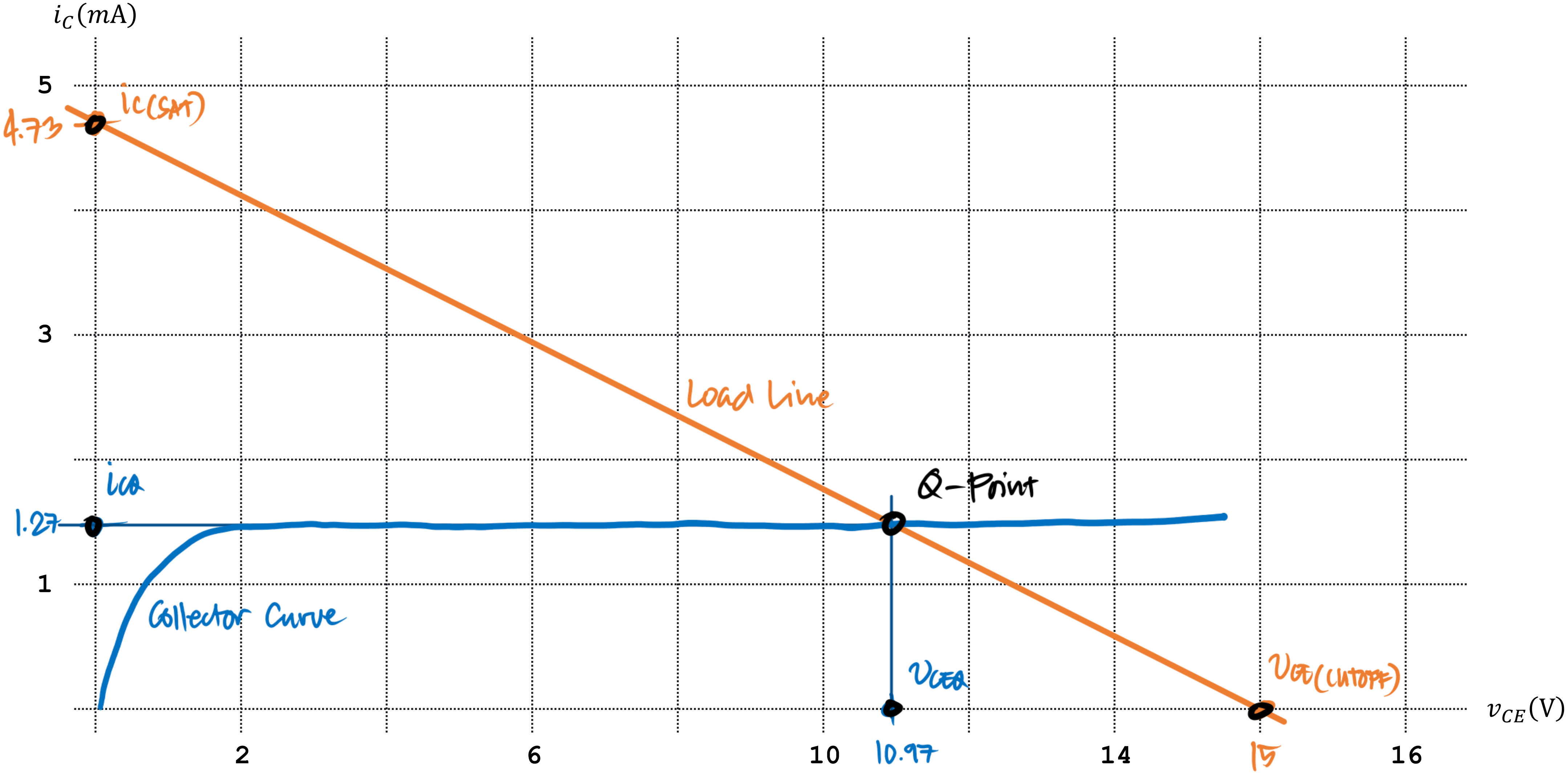
$$V_{CE} = V_{CC}$$

$$\boxed{V_{CE(CUTOFF)} = 15V}$$

ans

EXERCISE

Load Line Analysis



INDEPENDENT OF THE TRANSISTOR BETA

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{CE}$
Fixed-Bias	50	47.08	2.35	6.83	-76%
	100	47.08	4.71	1.64	
Emitter-Stabilized	45	23.74	1.07	14.54	-31%
	90	37.04	3.33	10.01	
Voltage-Divider Bias	45	28.92	1.16	11.32	-3%
	80	15.86	1.27	10.97	

LABORATORY