HALF AND FULL ADDERS

COMBINATIONAL LOGIC CIRCUITS

prepared by:

Gyro A. Madrona
Electronics Engineer

TOPIC OUTLINE

Half-Adder

Full-Adder

HALF-ADDER

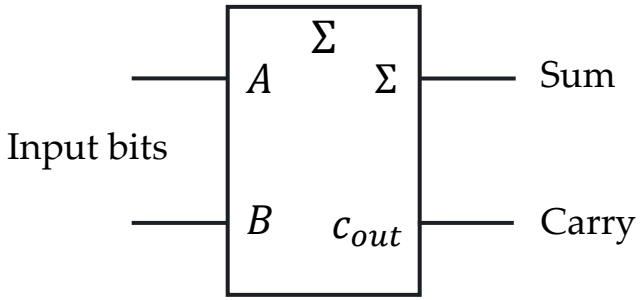
HALF-ADDER

The **half-adder** accepts two binary digits on its inputs and produces two binary digits on its outputs – a **sum bit** and a **carry bit**.

Truth Table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Logic Symbol



EXERCISE

Using the truth table of a half-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

Truth Table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Minterm

$\bar{A}B$

$A\bar{B}$

AB

Solution

$Cout = AB$

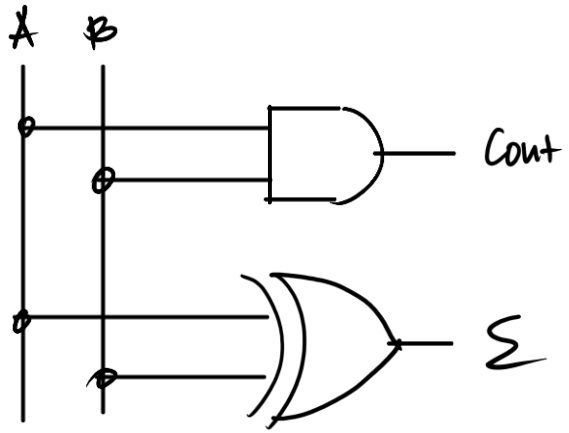
ans

$\Sigma = \bar{A}B + A\bar{B}$

XOR

$\Sigma = A \oplus B$

ans

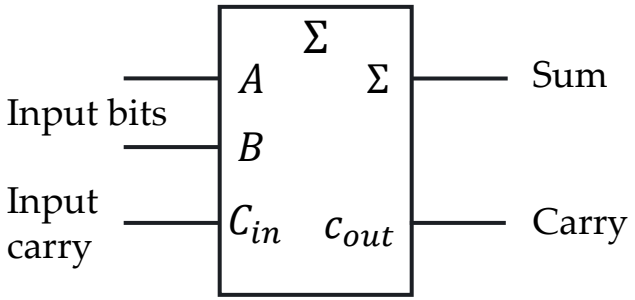


FULL-ADDER

FULL-ADDER

The **full-adder** accepts two input bits and an **input carry** and generates a sum output and an output carry.

Logic Symbol



Truth Table

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

EXERCISE

Using the truth table of a full-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Minterm

$\bar{A}B\,Cin$

$A\bar{B}\,Cin$

$AB\,\bar{Cin}$

$AB\,Cin$

Solution

$$Cout = \bar{A}B\,Cin + A\bar{B}\,Cin + AB\,\bar{Cin} + AB\,Cin$$

$$Cout = Cin(\bar{A}B + A\bar{B}) + AB(\bar{Cin} + Cin)$$

XOR

$$Cout = Cin(A \oplus B) + AB$$

any

EXERCISE

Using the truth table of a full-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

A	B	C_{in}	C_{out}	Σ	Minterm
0	0	0	0	0	
0	0	1	0	1	$\bar{A}\bar{B}C_{in}$
0	1	0	0	1	$\bar{A}B\bar{C}_{in}$
0	1	1	1	0	
1	0	0	0	1	$A\bar{B}\bar{C}_{in}$
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	1	ABC_{in}

Solution

$$\Sigma = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

$$\Sigma = C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

XNOR XOR

$$\Sigma = C_{in}(\overline{A \oplus B}) + \bar{C}_{in}(A \oplus B)$$

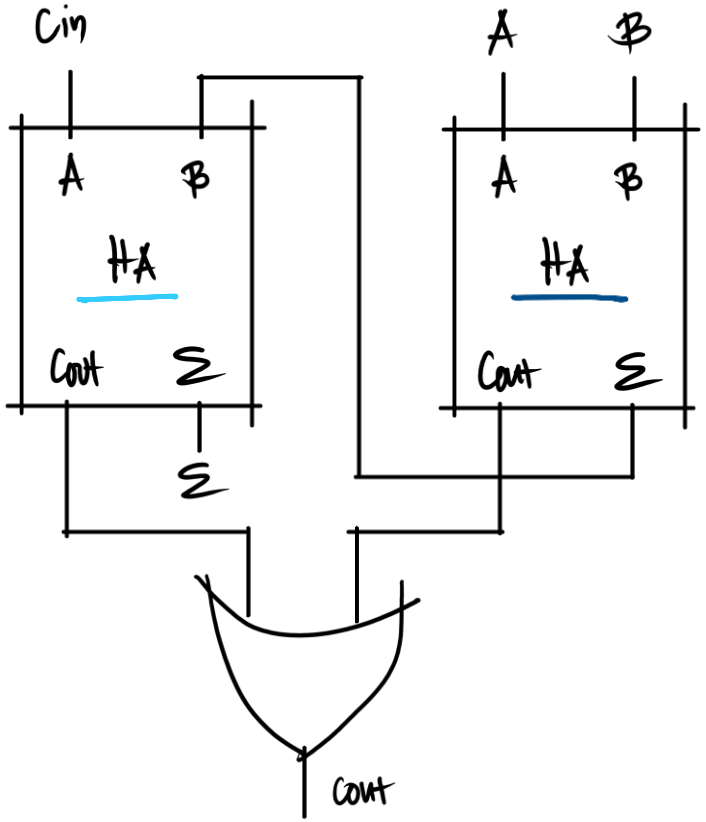
$x \quad \bar{y} \quad + \quad \bar{x} \quad y \leftarrow$ XOR

$$\Sigma = C_{in} \oplus A \oplus B$$

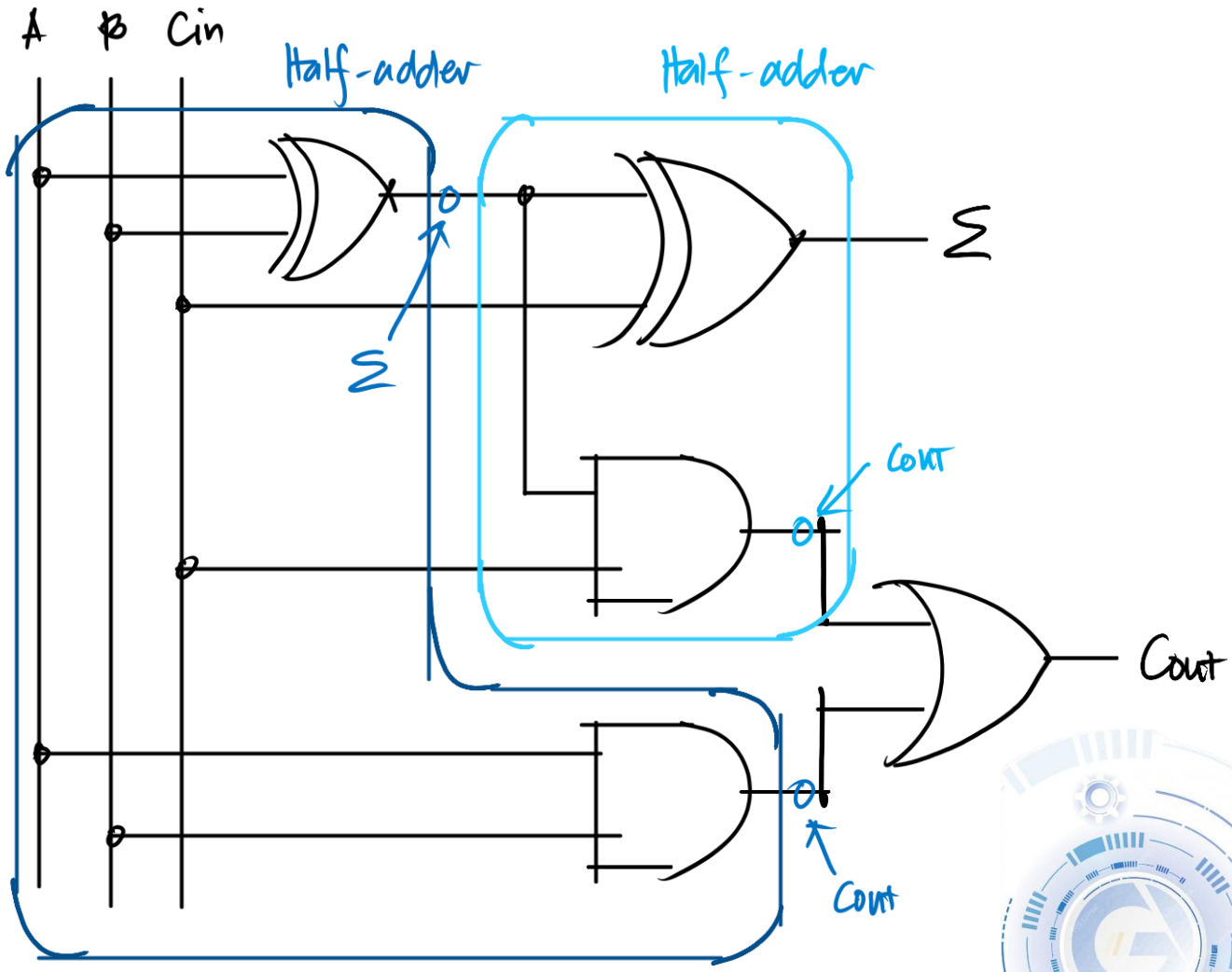
ans

EXERCISE

Using the truth table of a full-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

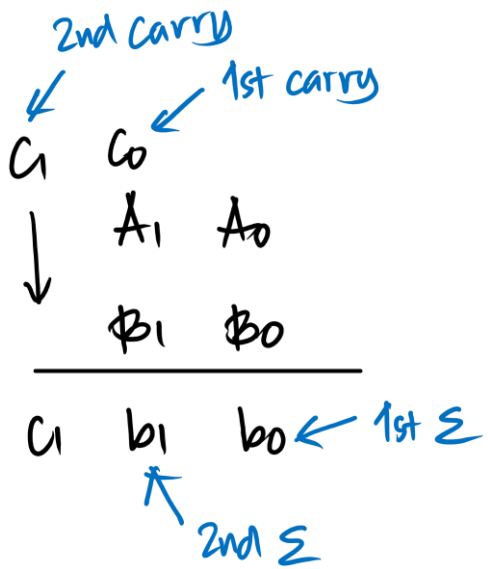


Solution

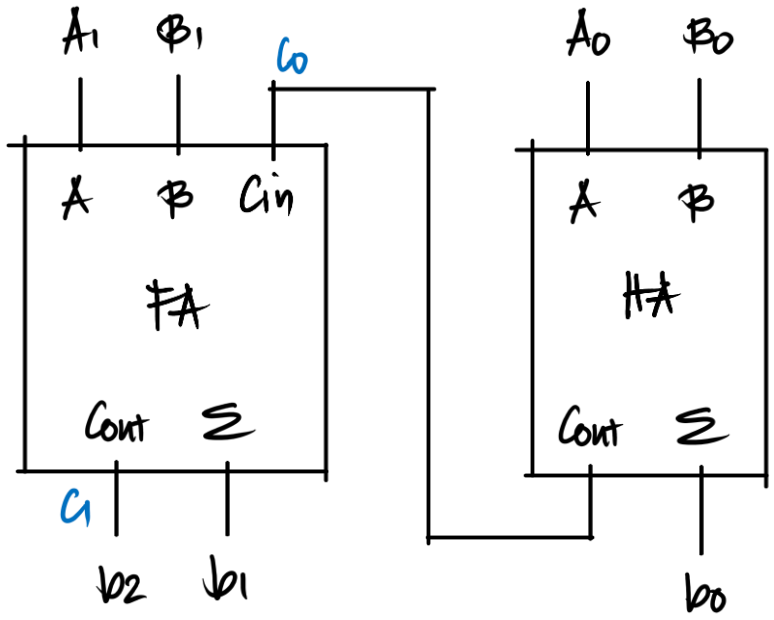


EXERCISE

Create a block-level representation of a 2-bit binary adder using full-adder modules.



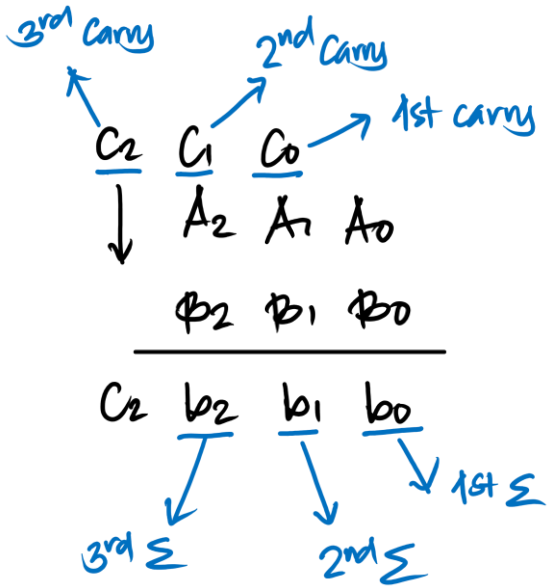
Solution

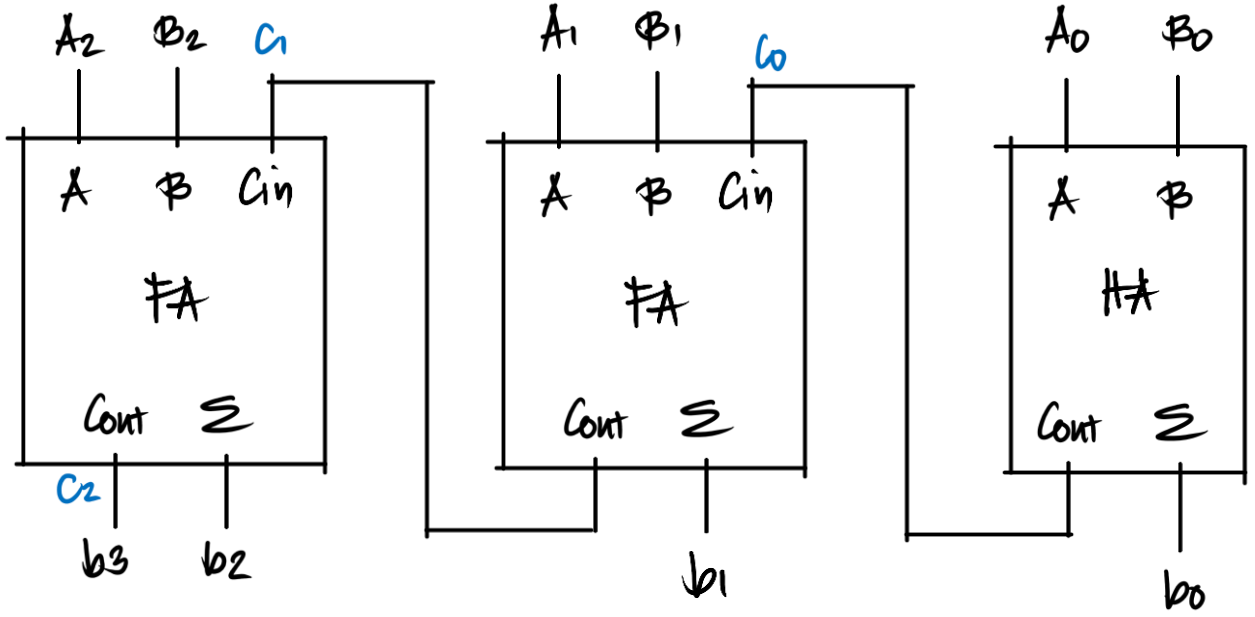


EXERCISE

Create a block-level representation of a 3-bit binary adder using full-adder modules.

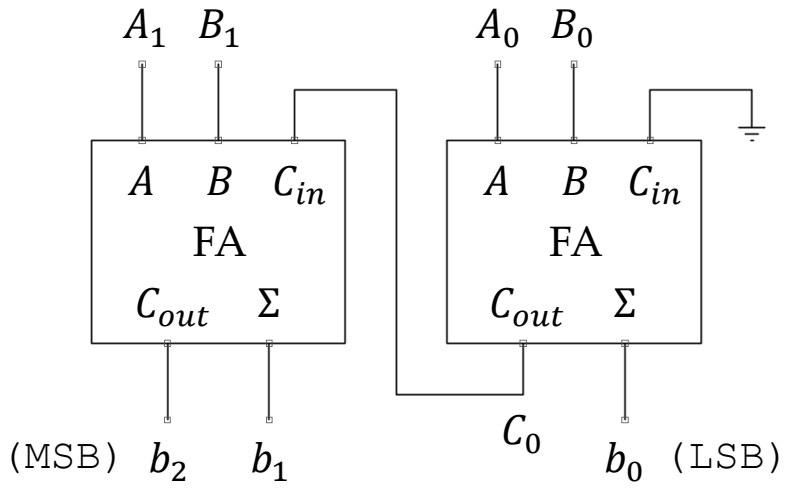
Solution





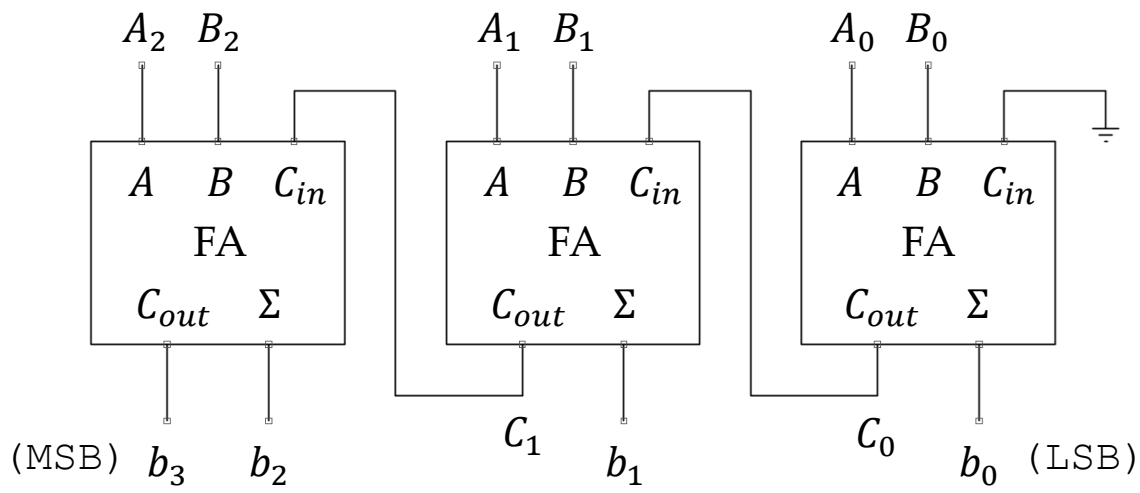
PARALLEL BINARY ADDERS

2-bit Parallel Adder



$$\begin{array}{r} \quad C_1 \; C_0 \\ \quad A_1 \; A_0 \\ + \quad B_1 \; B_0 \\ \hline b_2 \; b_1 \; b_0 \end{array}$$

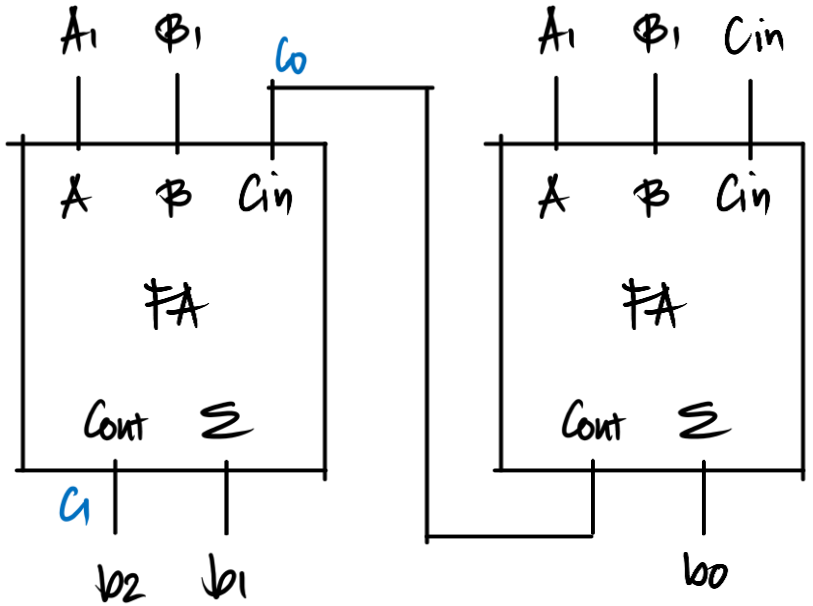
3-bit Parallel Adder



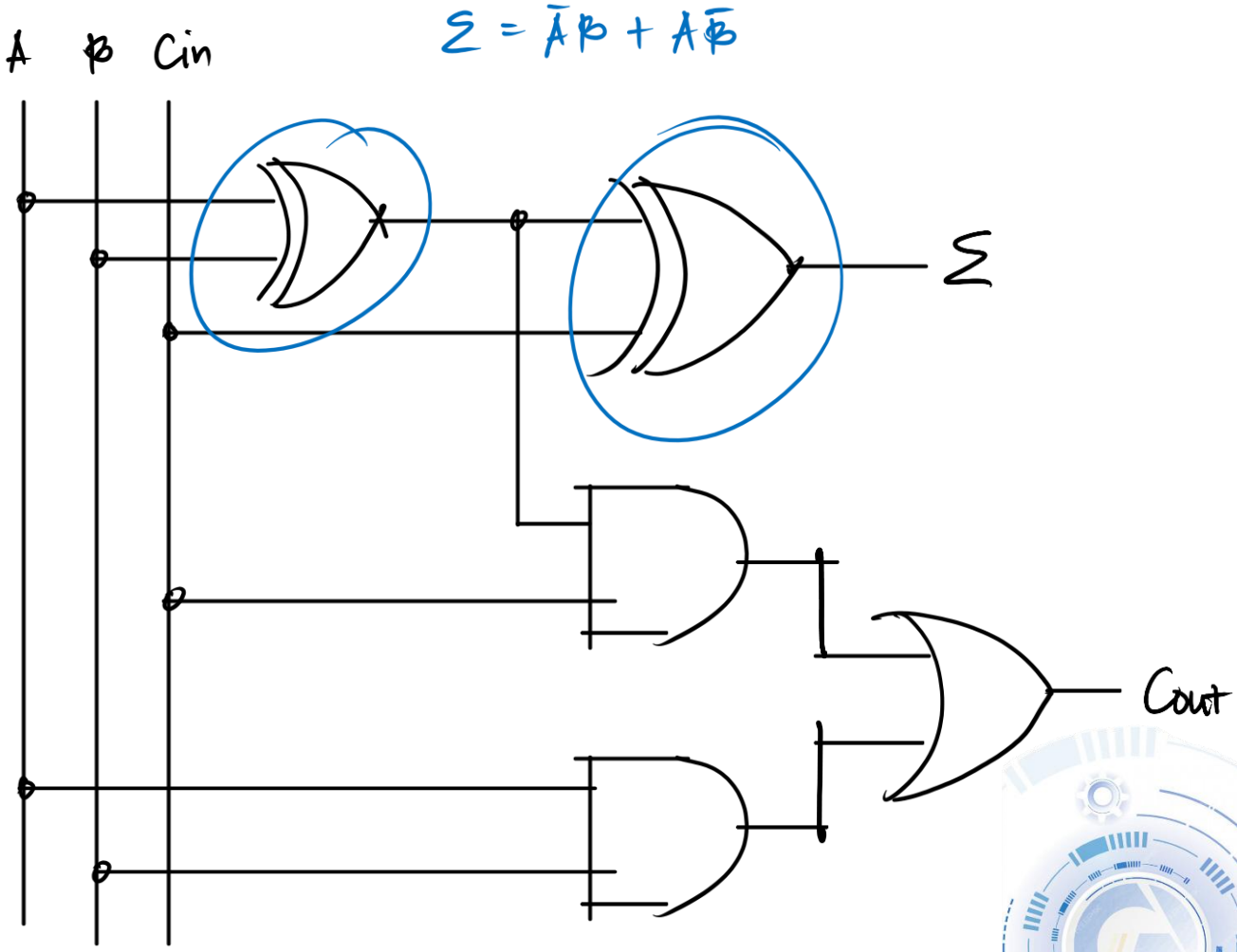
$$\begin{array}{r} \quad C_2 \; C_1 \; C_0 \\ \quad A_2 \; A_1 \; A_0 \\ + \quad B_2 \; B_1 \; B_0 \\ \hline b_3 \; b_2 \; b_1 \; b_0 \end{array}$$

EXERCISE

Synthesize and implement a 2-bit parallel binary adder without utilizing XOR or XNOR gates.



Solution



LABORATORY