LOGIC GATES

INTRODUCTION

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TOPIC OUTLINE

Logic Gates

- Logic Symbol
- Truth Table
- Timing Diagram

LOGIC GATES

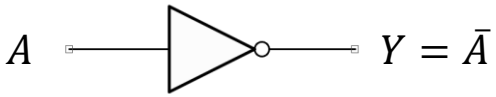
INVERTER

The **inverter** (NOT gate) performs the operation called inversion or **complementation**.

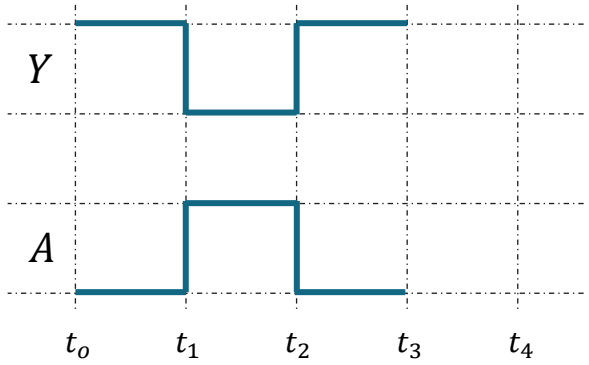
Truth Table

A	Y
0	1
1	0

Logic Symbol

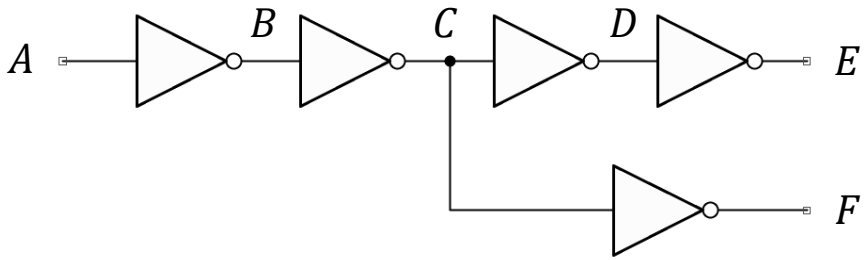


Timing Diagram



EXERCISE

Given the inverter network, determine the logic levels at points E and F when a LOW signal is applied at point A.



Solution

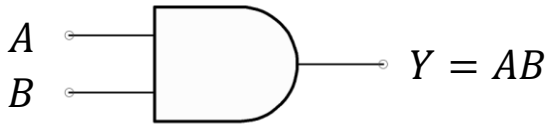
AND GATE

The **AND** gate is one of the basic gates that can be combined to form any logic function. It performs logical **multiplication**.

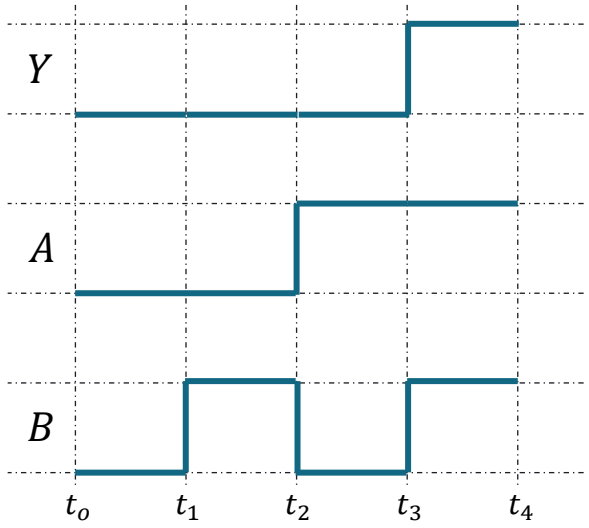
Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Logic Symbol

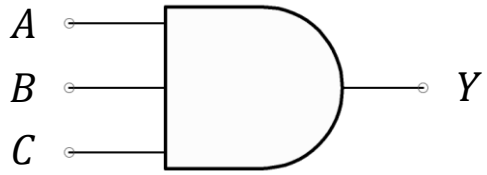


Timing Diagram

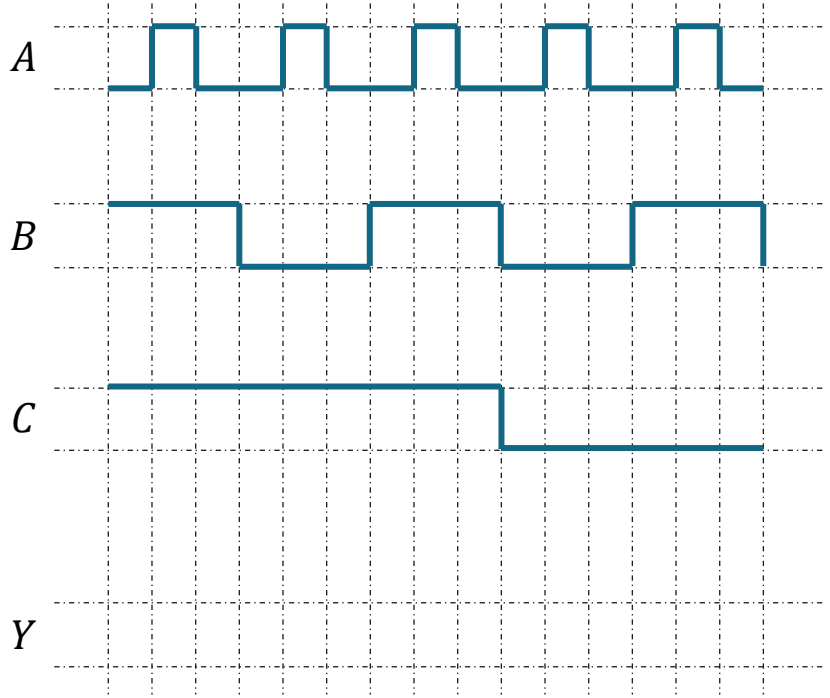


EXERCISE

For the 3-input AND gate, determine the output waveform in relation to the inputs.



Solution



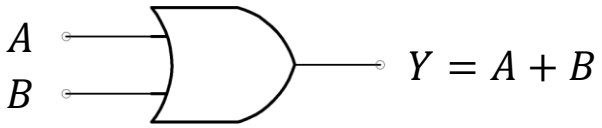
OR GATE

The OR gate is another basic gates from which all logic functions are constructed. It performs logical **addition**.

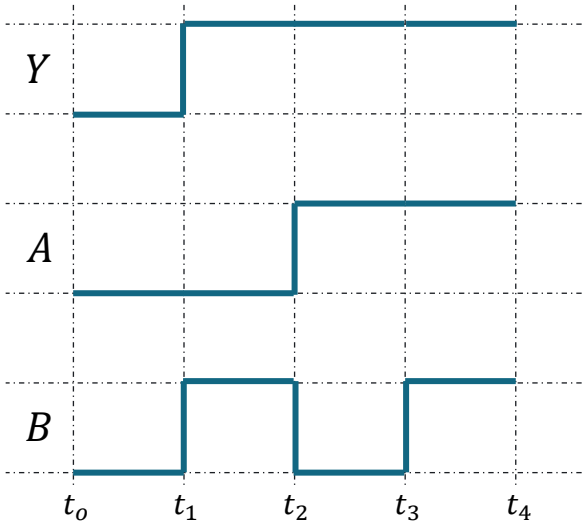
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Logic Symbol

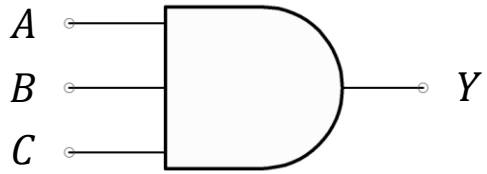


Timing Diagram

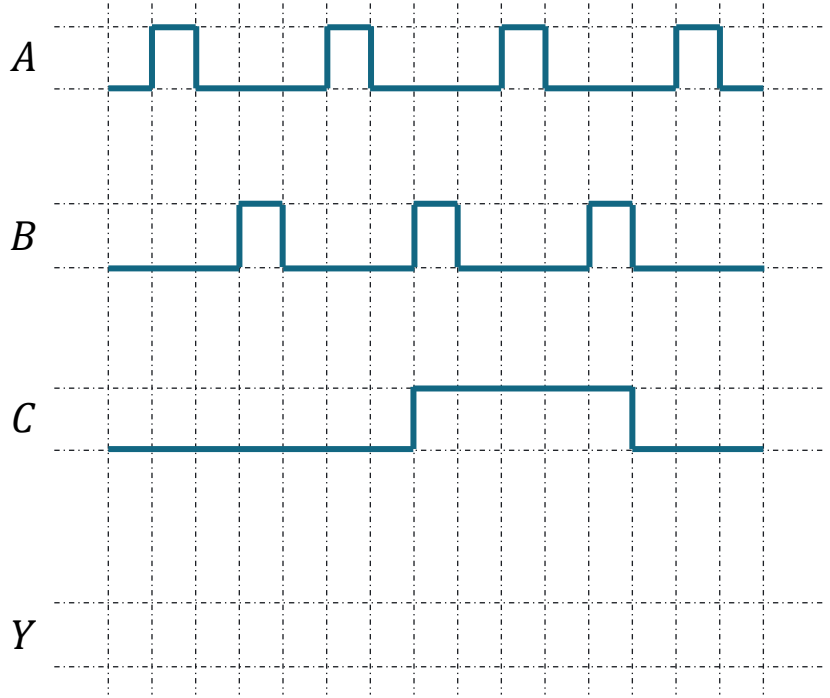


EXERCISE

For the 3-input OR gate, determine the output waveform in relation to the inputs.



Solution



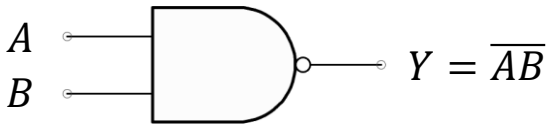
NAND GATE

The **NAND** gate is a logical complement of the AND gate. It is considered a universal gate, meaning it can be used in combination to perform AND, OR, and inverter operations.

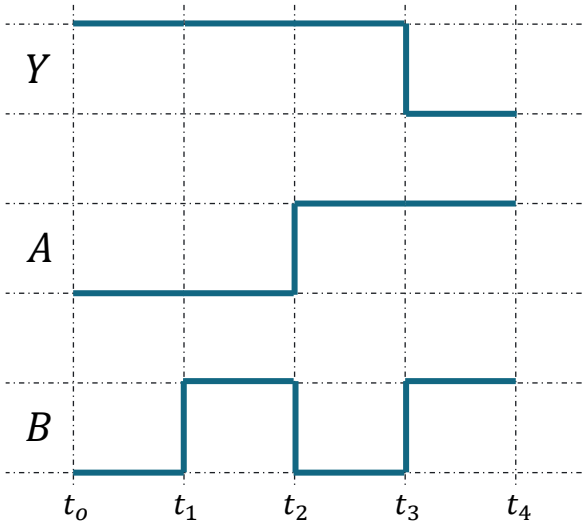
Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Logic Symbol

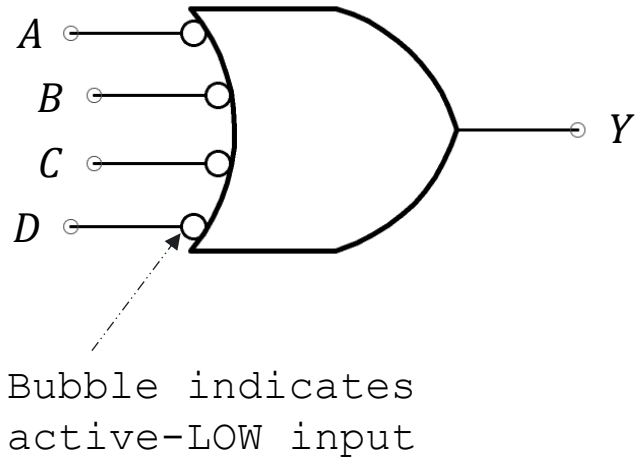


Timing Diagram

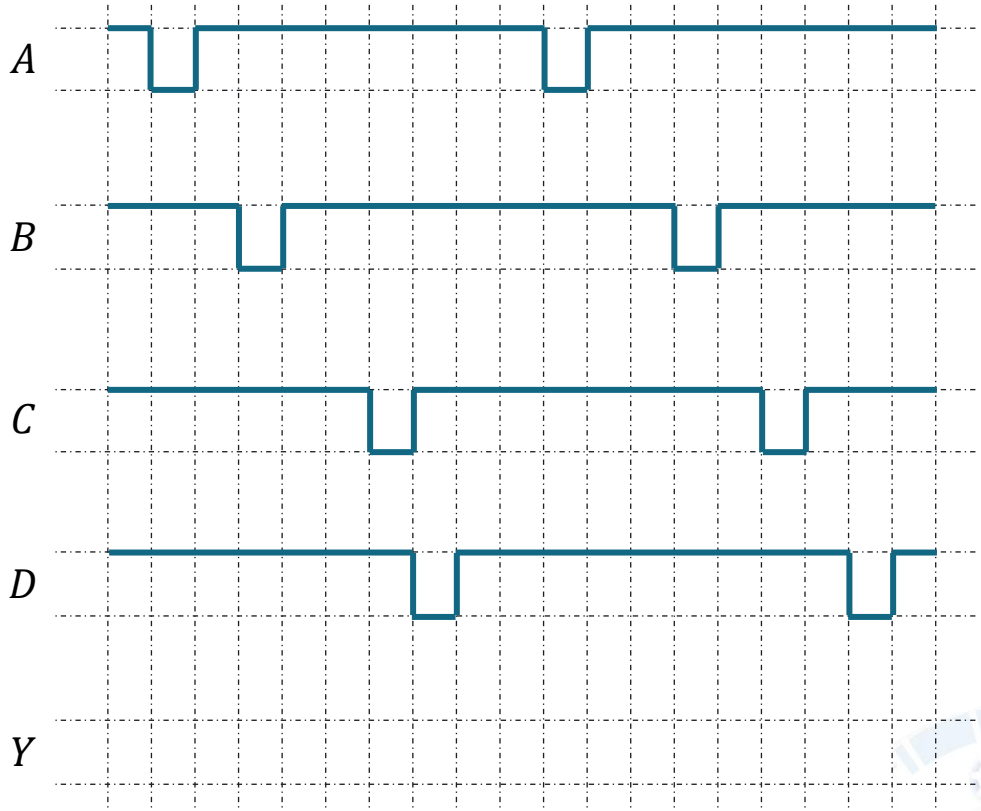


EXERCISE

For the 4-input NAND gate, operating as negative-OR gate, determine the output with respect to the inputs.



Solution



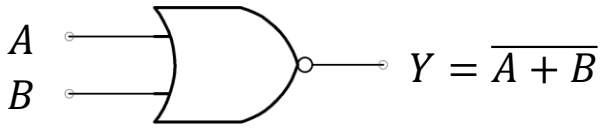
NOR GATE

NOR gate is also a universal gate, and it is the logical complement of the OR gate.

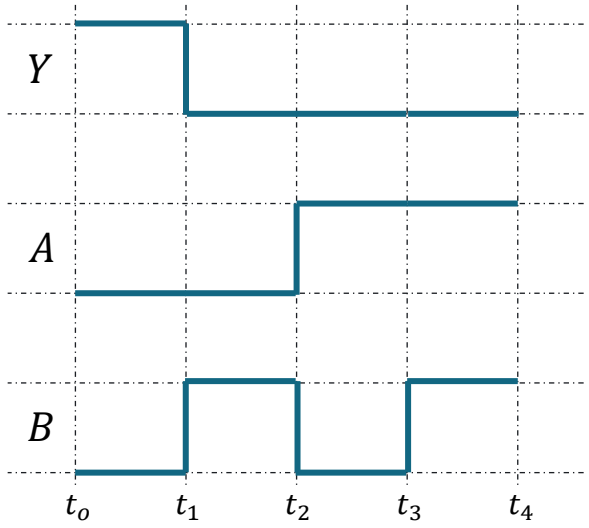
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic Symbol



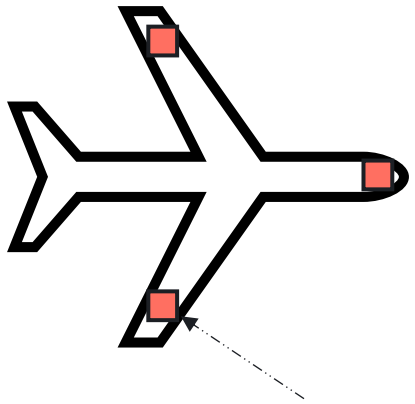
Timing Diagram



EXERCISE

As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. A green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. A red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.

Solution



Landing sensors
Extended = LOW
Retracted = HIGH

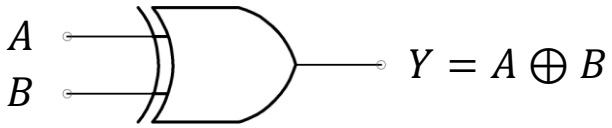
EXCLUSIVE-OR GATE

The exclusive-OR (**XOR**) gate performs **modulo-2 addition**.

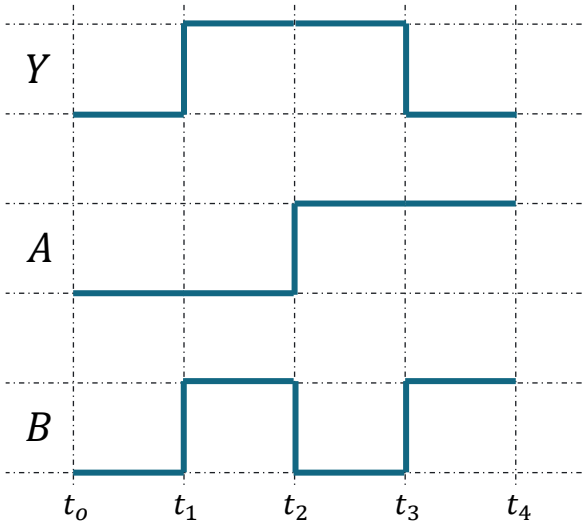
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Logic Symbol



Timing Diagram



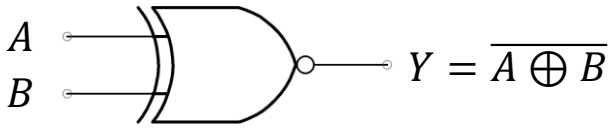
EXCLUSIVE-NOR GATE

The exclusive-NOR (**XNOR**) gate is the logical complement of the XOR gate.

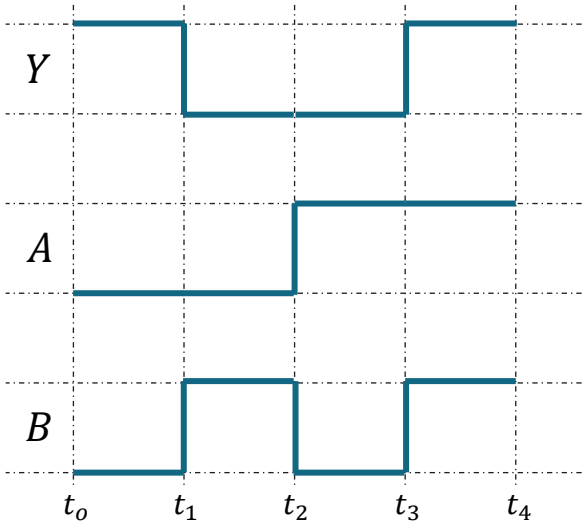
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Logic Symbol

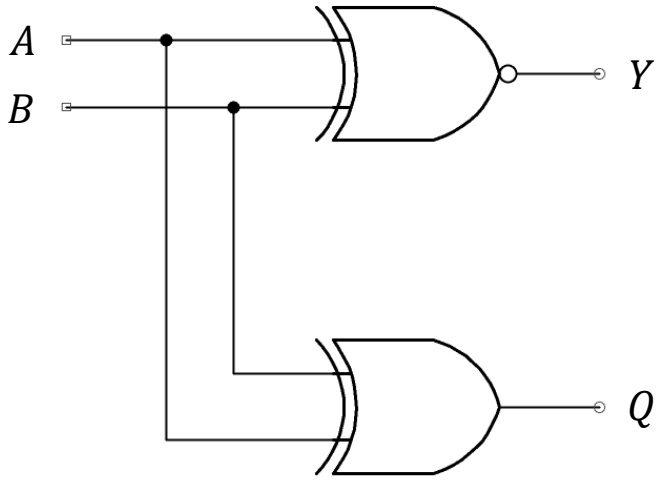


Timing Diagram

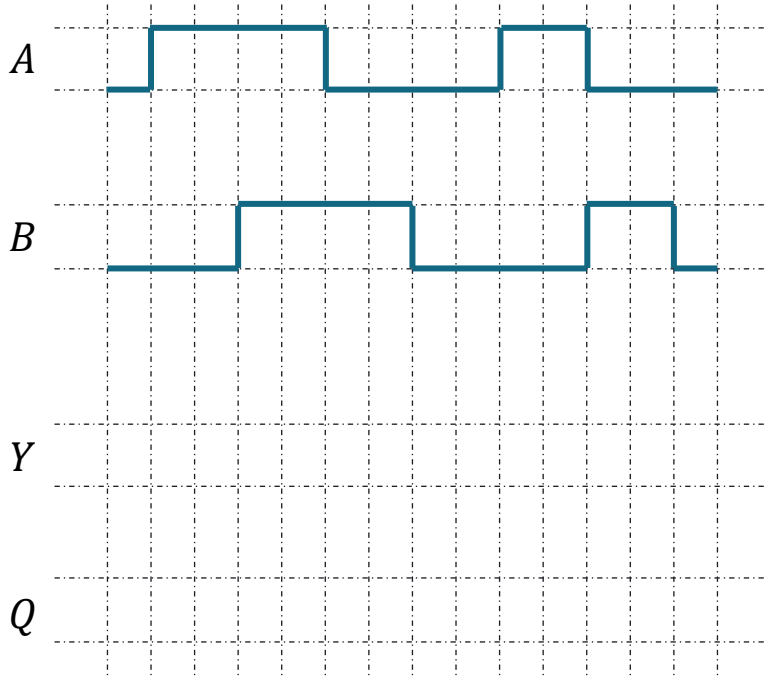


EXERCISE

Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B.

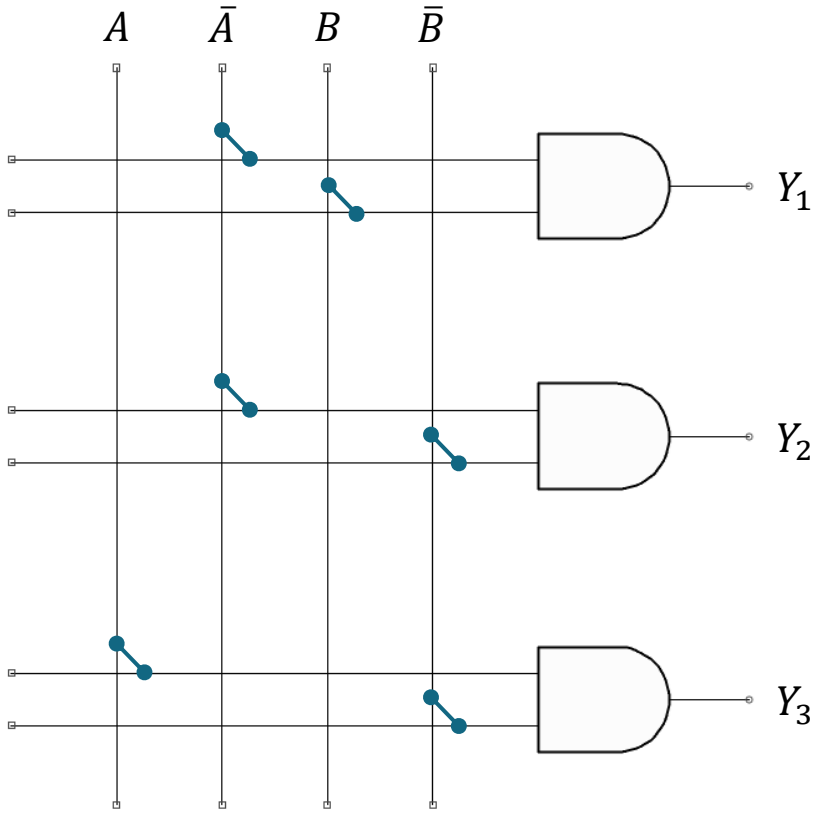


Solution



EXERCISE

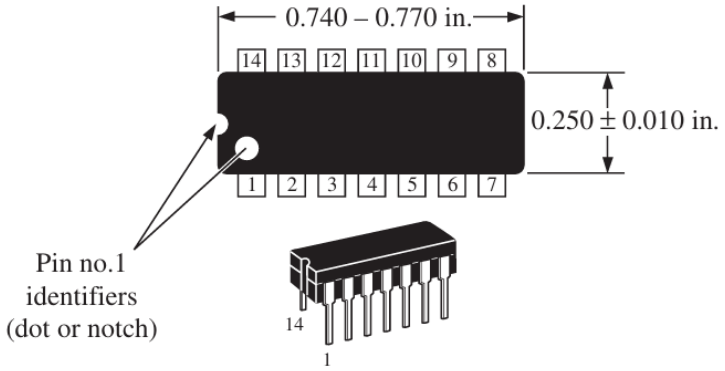
In the simple programmed AND array with programmable links, determine the Boolean output expressions.



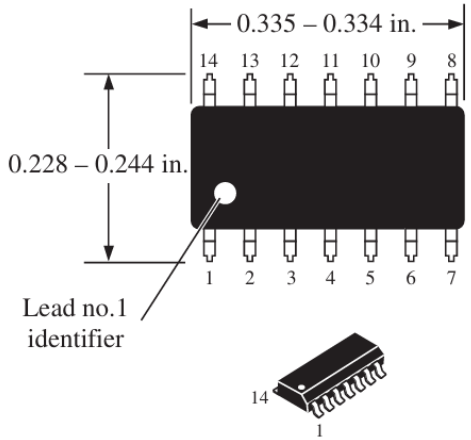
Solution

IC PACKAGES

DIP (Dual In-line Package)



SOIC (Small-Outline IC)



Datasheet links

7404-Inverter Gate datasheet

7408-AND Gate datasheet

7432-OR Gate datasheet

7403-NAND Gate datasheet

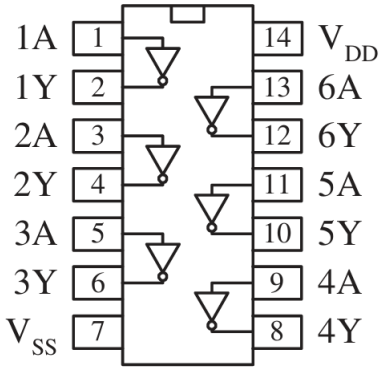
7402-NOR Gate datasheet

74136-XOR Gate datasheet

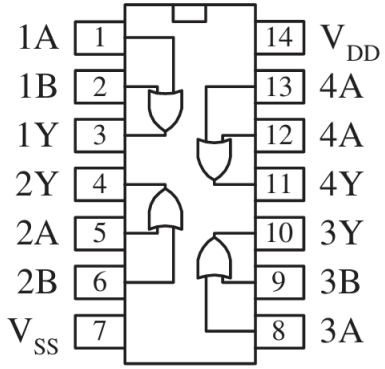
74266-XNOR Gate datasheet

PIN CONFIGURATION

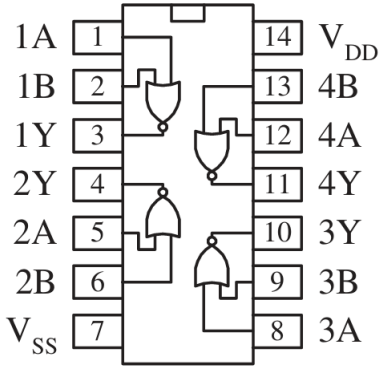
Hex inverter



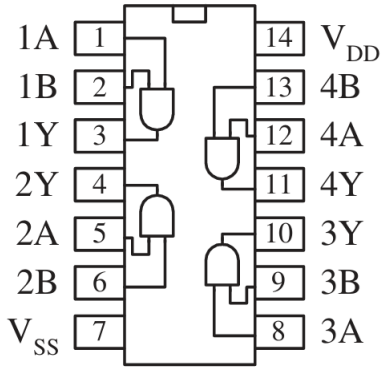
Quad 2-input OR



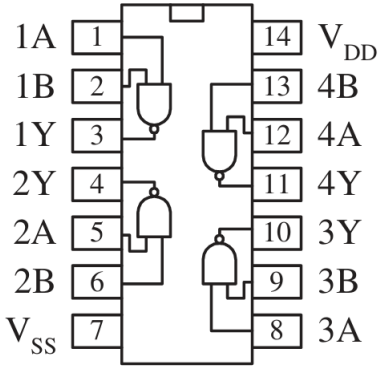
Quad 2-input NOR



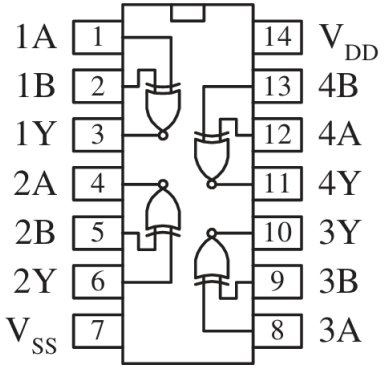
Quad 2-input AND



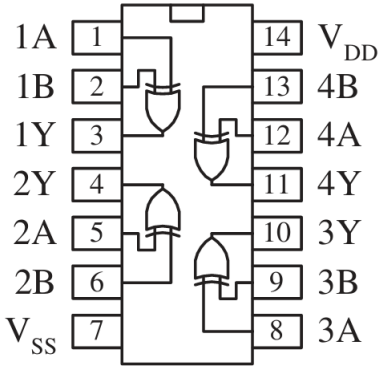
Quad 2-input NAND



Quad 2-input XNOR



Quad 2-input XOR



LABORATORY