

FIXED-BIAS CIRCUIT

BJT DC BIASING

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TOPIC OUTLINE

Fixed-Bias Circuit

- Base-Emitter Loop
- Collector-Emitter Loop
- Load Line Analysis



FIXED-BIAS CIRCUIT



CURRENT GAIN

The <u>current gain</u> parameters <u>alpha</u> (α) and <u>beta</u> (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

 α is always less than 1 (typically 0.95 to 0.995)

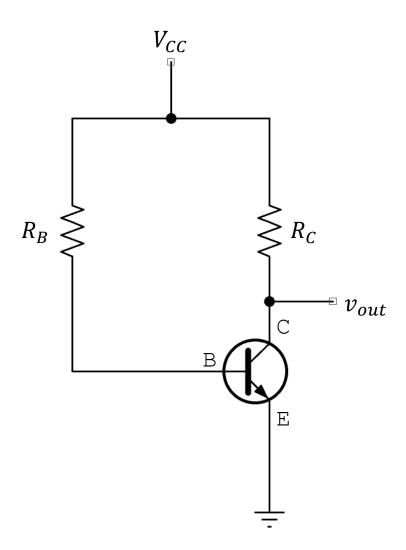
Beta (β) is the ratio of the collector current to the base current.

Formula

$$\beta = \frac{i_C}{i_B}$$



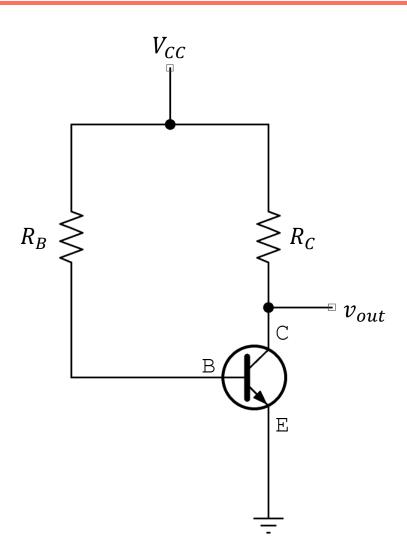
FIXED-BIAS CIRCUIT



Fixed-bias configuration is the simplest method – the biasing voltage applied to the base of the BJT is fixed by a single resistor (R_B) connected directly to the power supply (v_{CC}).



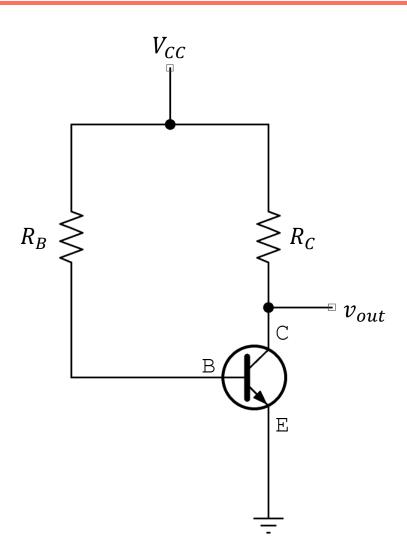
BASE-EMITTER LOOP



KVL @B-E

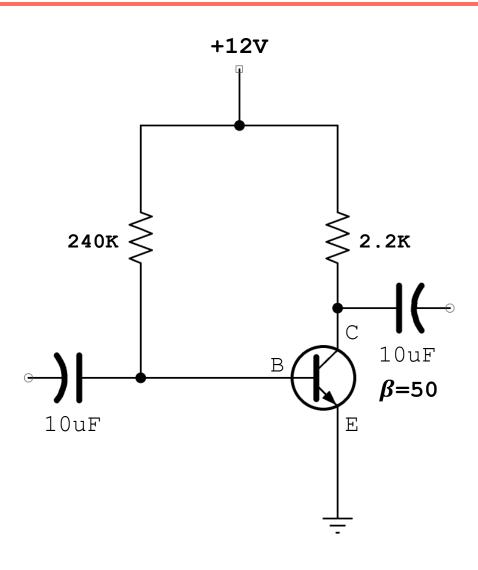


COLLECTOR-EMITTER LOOP



KVL @C-E

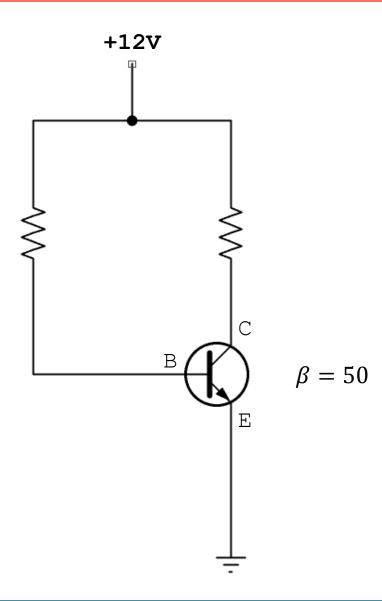




Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CO})
- Collector-Emitter voltage (v_{CEQ})
- Base voltage (v_B)
- Base-Collector voltage (v_{BC})





Solution



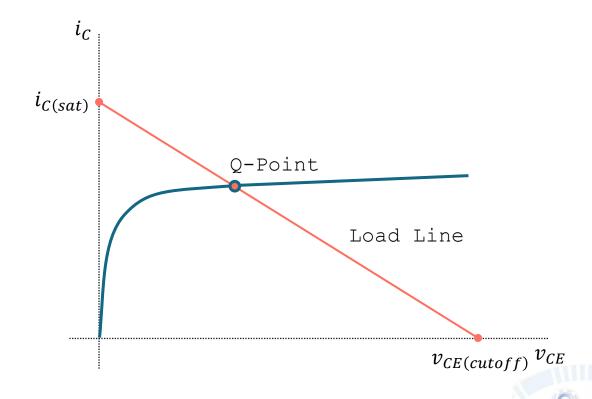
LOAD LINE ANALYSIS



SATURATION POINT

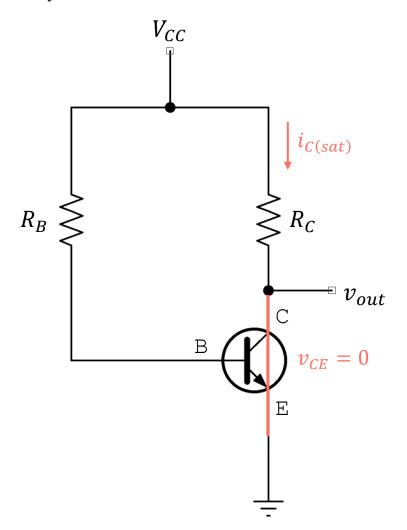
The <u>saturation point</u> is the operating state where BJT conducts the <u>maximum collector curren</u>t ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

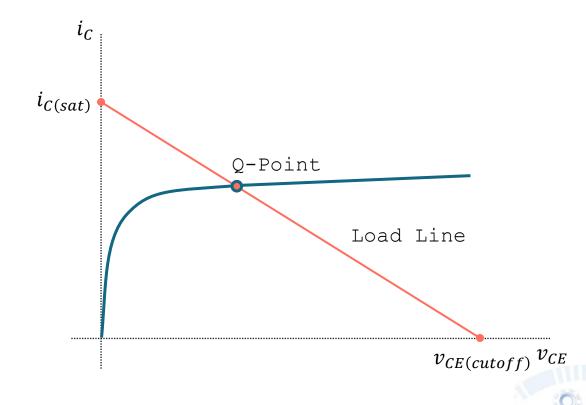
In this region the transistor acts like a <u>closed switch</u> (zero resistance between collector-emitter).



SATURATION POINT

Mentally Short

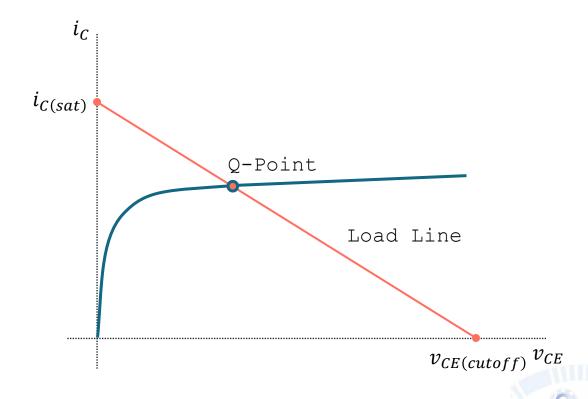




CUTOFF POINT

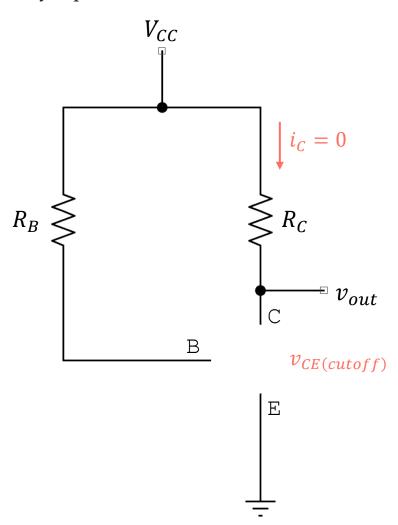
The <u>cutoff point</u> is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

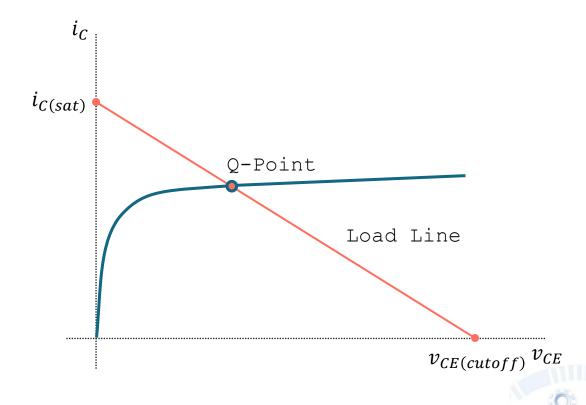
In this region the transistor acts like an <u>open switch</u> (infinite resistance between collector-emitter).



CUTOFF POINT

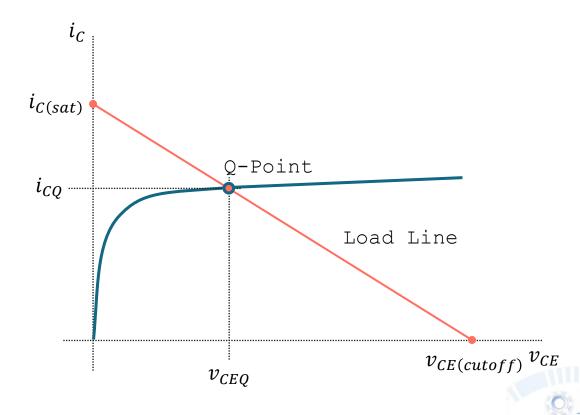
Mentally Open

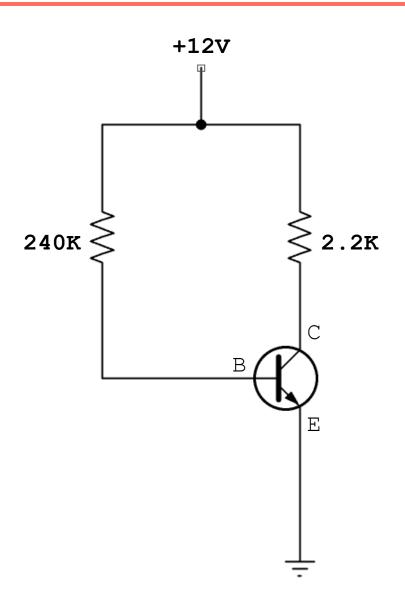




QUIESCENT POINT

The <u>Q-point</u> is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}) .

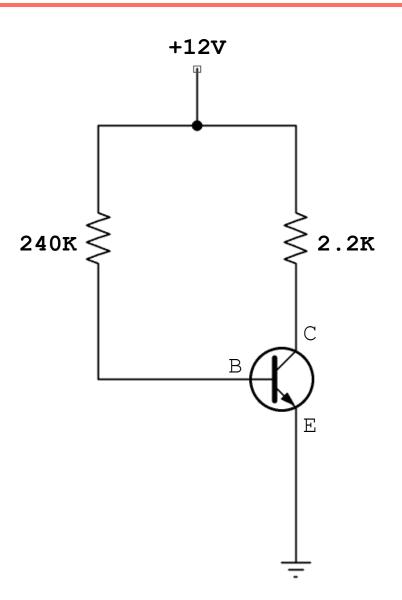




Plot the DC load line for the fixed-bias circuit and clearly indicate the following points on the graph.

- Saturation current $(i_{C(sat)})$
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

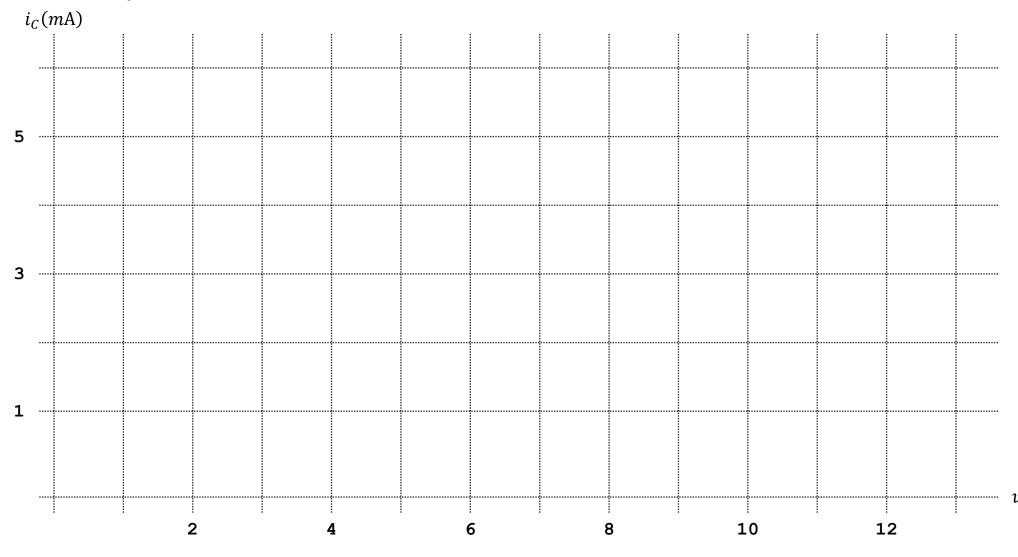


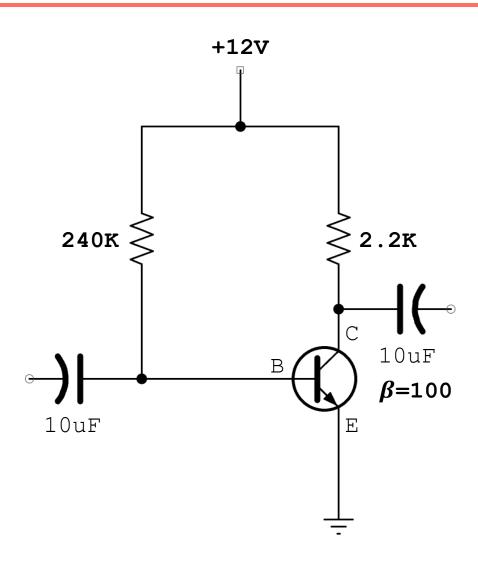


Solution



Load Line Analysis

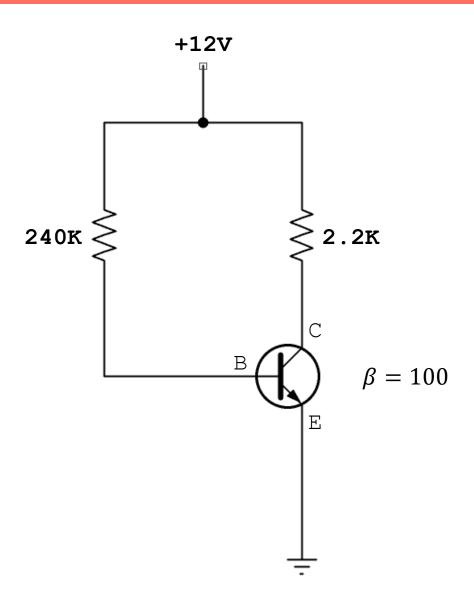




Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CO})
- Collector-Emitter voltage (v_{CEQ}) and clearly indicate the following points on the load line analysis graph.
- Saturation current $(i_{C(sat)})$
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

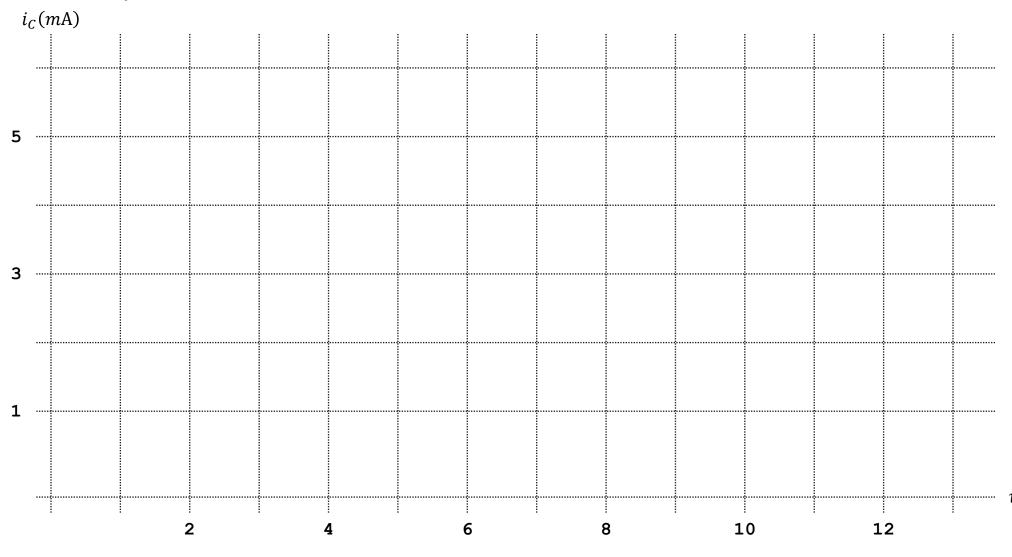




Solution



Load Line Analysis



UNSTABLE Q-POINT

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{\it CE}$
Fixed-Bias					
Emitter- Stabilized					
Voltage- Divider Bias					



LABORATORY

