LATCHES AND FLIP-FLOPS

SEQUENTIAL LOGIC CIRCUITS

prepared by:

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Electronics Engineer

TOPIC OUTLINE

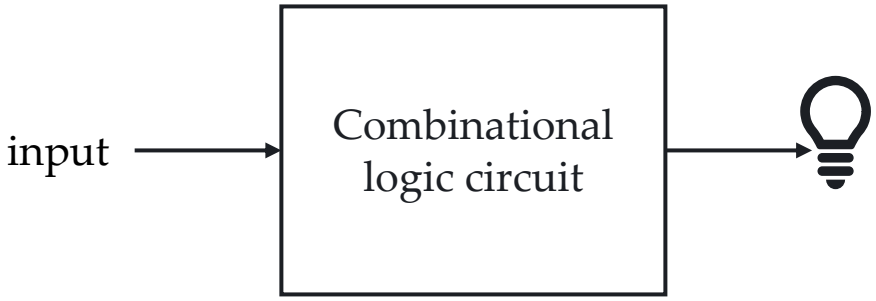
D Latch/Flip-Flop

SR Latch

JK Flip-Flop

D LATCH/FLIP-FLOP

SOMETHING WE CAN'T BUILD (YET)



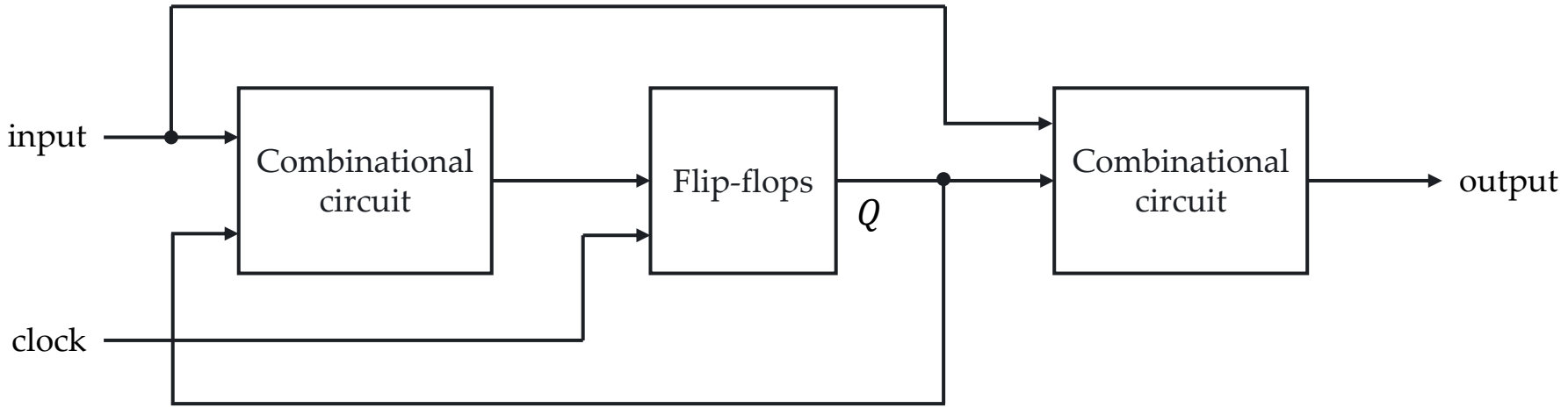
When the input = HIGH

- if the light is OFF, it turns ON 
- if the light is ON, it turns OFF 

The output of combinational logic circuit depends only on the present inputs. It **doesn't remember** whether the light was ON or OFF before.

SEQUENTIAL CIRCUITS

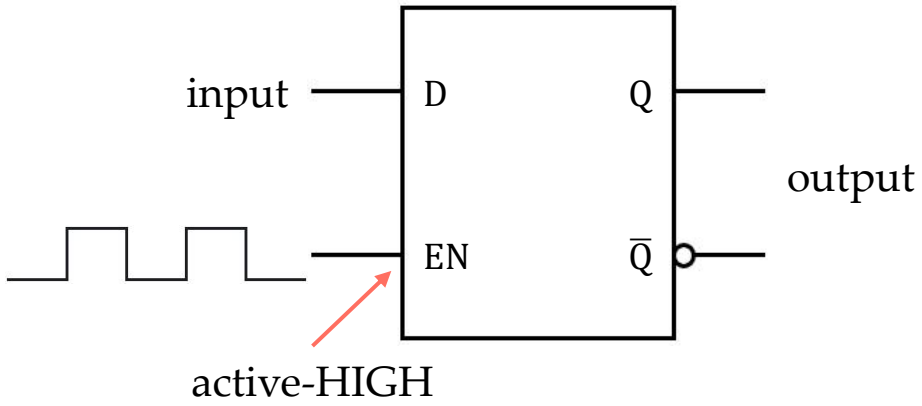
Sequential circuits are digital logic circuits whose outputs depend on the **past** behavior of the circuit, as well as on the **present** values of inputs.

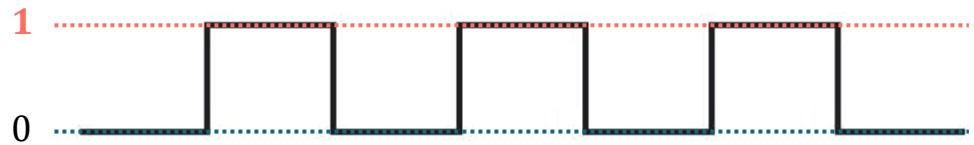


General form of a sequential circuit

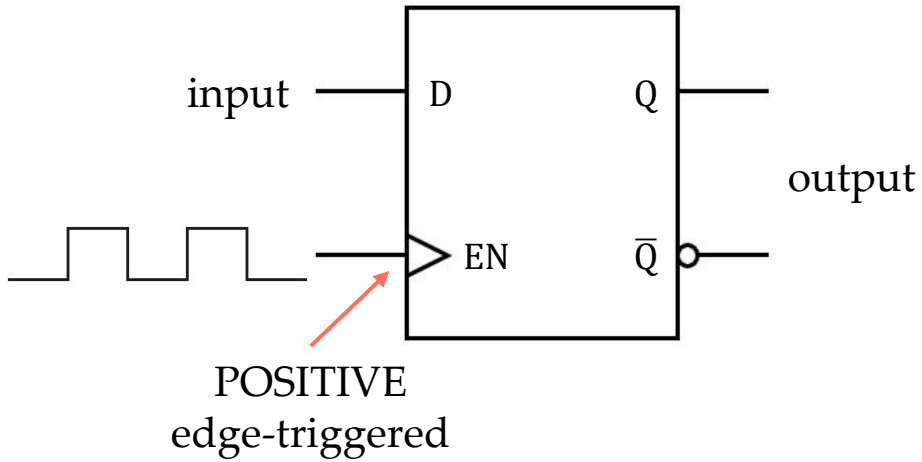
LATCH AND FLIP-FLOP

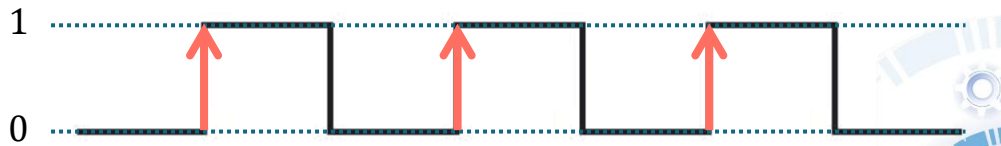
Latch is a **level** sensitive (HIGH or LOW) device.





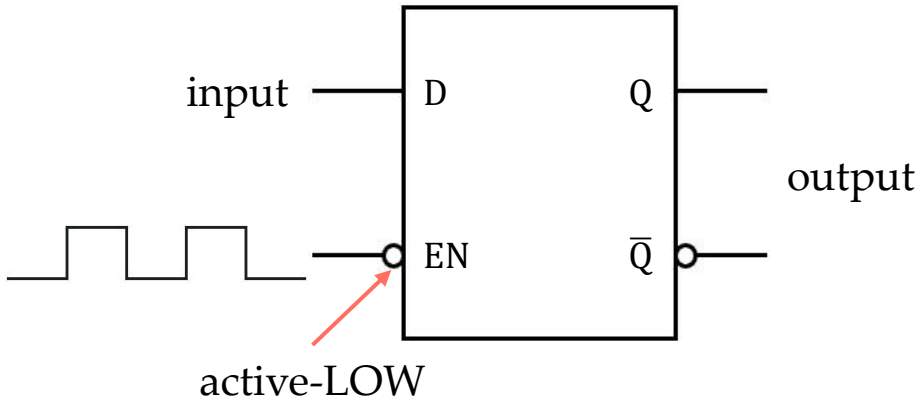
Flip-flop is an **edge**-triggered (rising or falling) device.



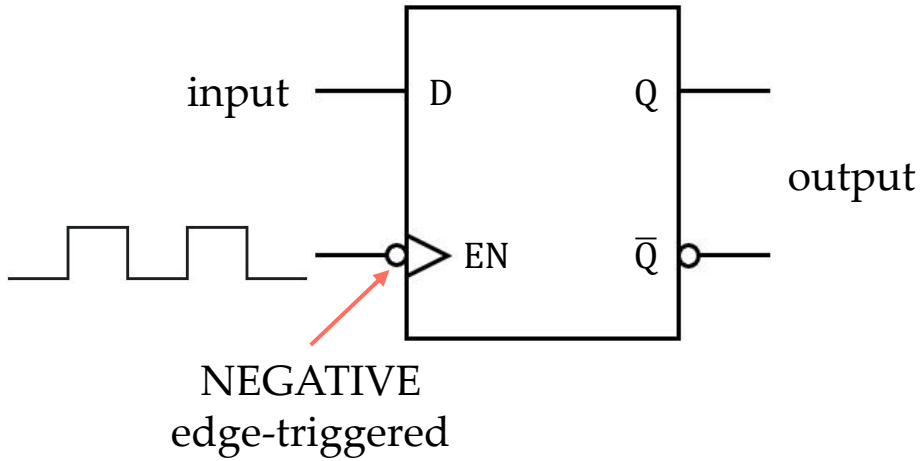


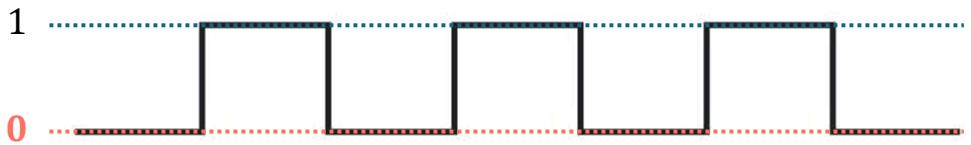
LATCH AND FLIP-FLOP

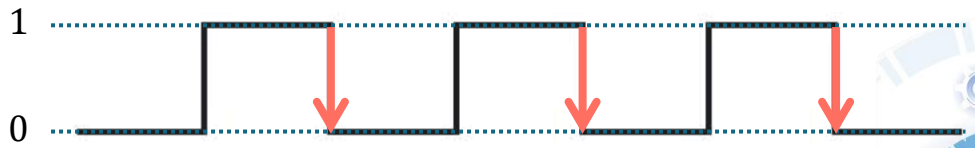
Latch is a **level** sensitive (HIGH or LOW) device.



Flip-flop is an **edge**-triggered (rising or falling) device.

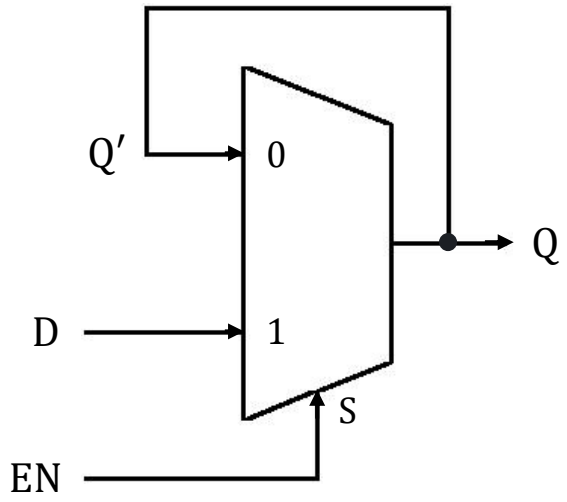






BASIC LATCH

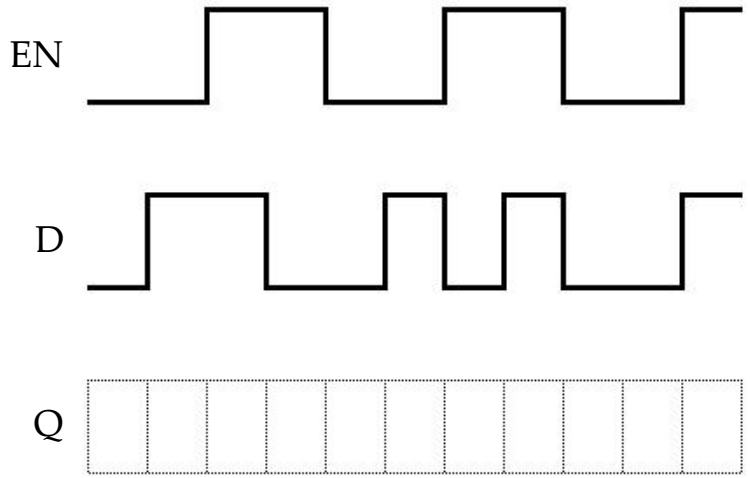
2-to-1 MUX as settable storage element



Characteristic Table

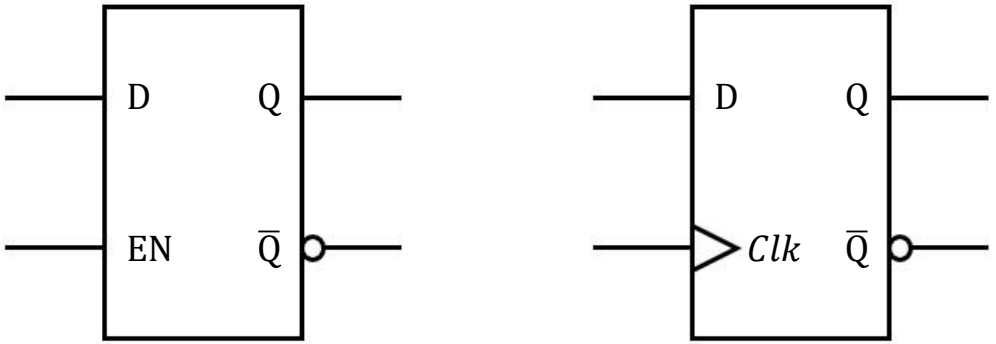
EN	D	Q
0	X	Q′
1	0	0
1	1	1

Timing Diagram

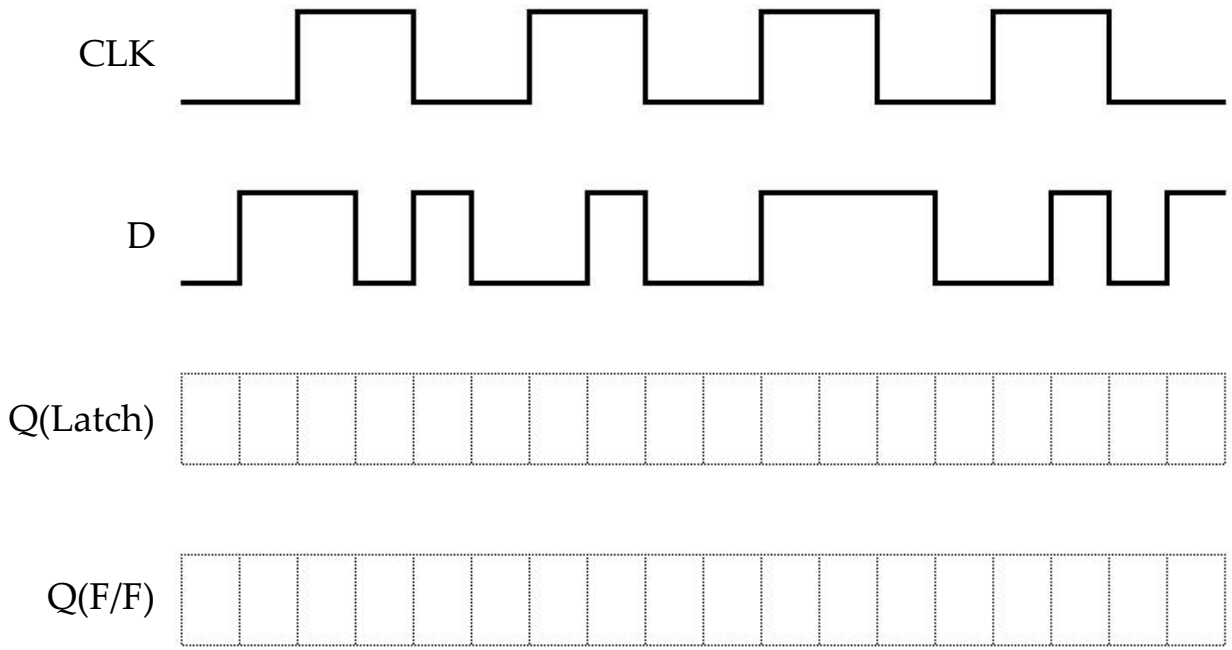


D LATCH/FLIP-FLOP

Graphical Symbol



Timing Diagram



Characteristic Table

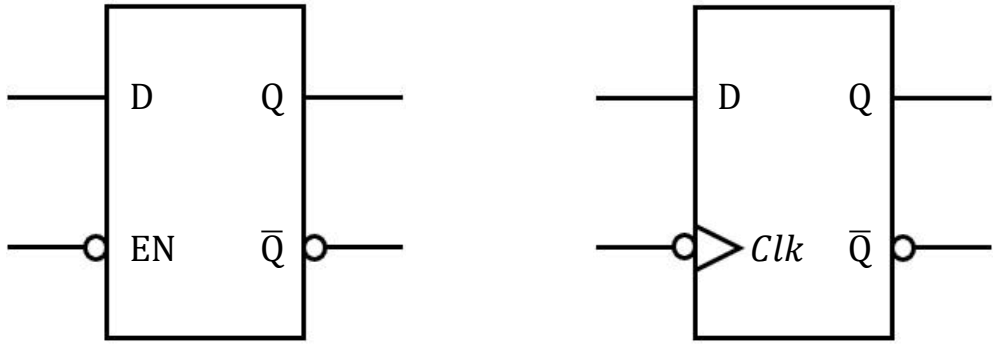
EN	D	Q
0	X	NC
1	0	0
1	1	1

Clk	D	Q(t+1)
0/1	X	Q(t)
↑	0	0
↑	1	1

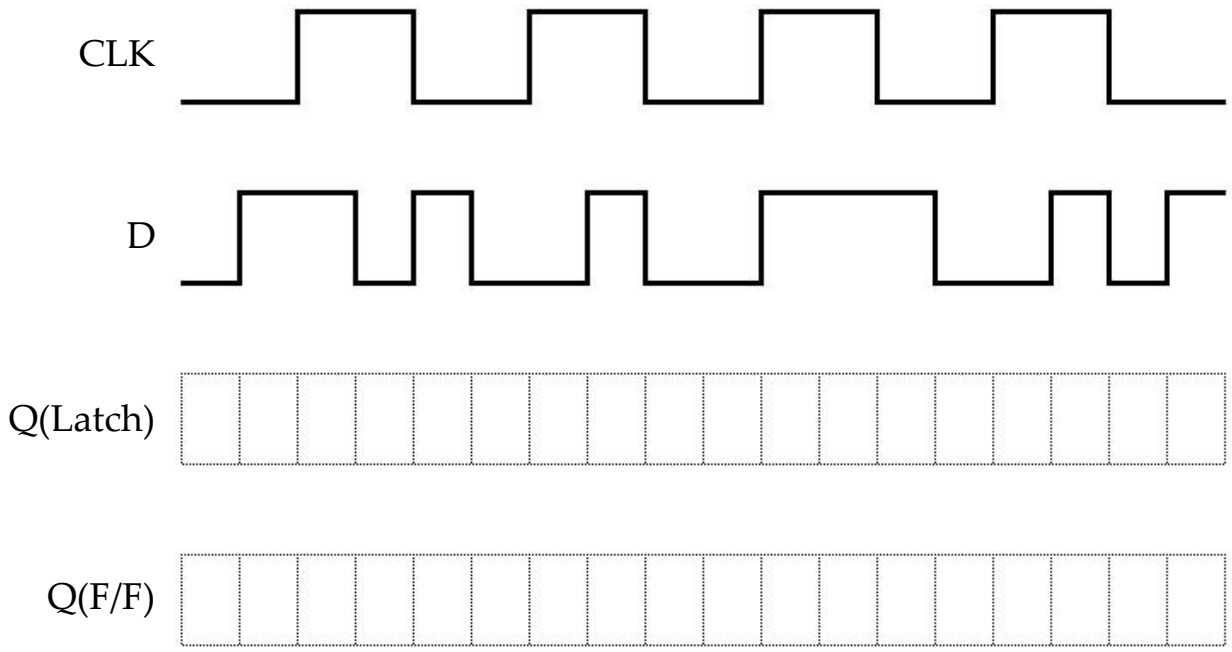
Q(t) – present state
Q(t+1) – next state

D LATCH/FLIP-FLOP

Graphical Symbol



Timing Diagram



Characteristic Table

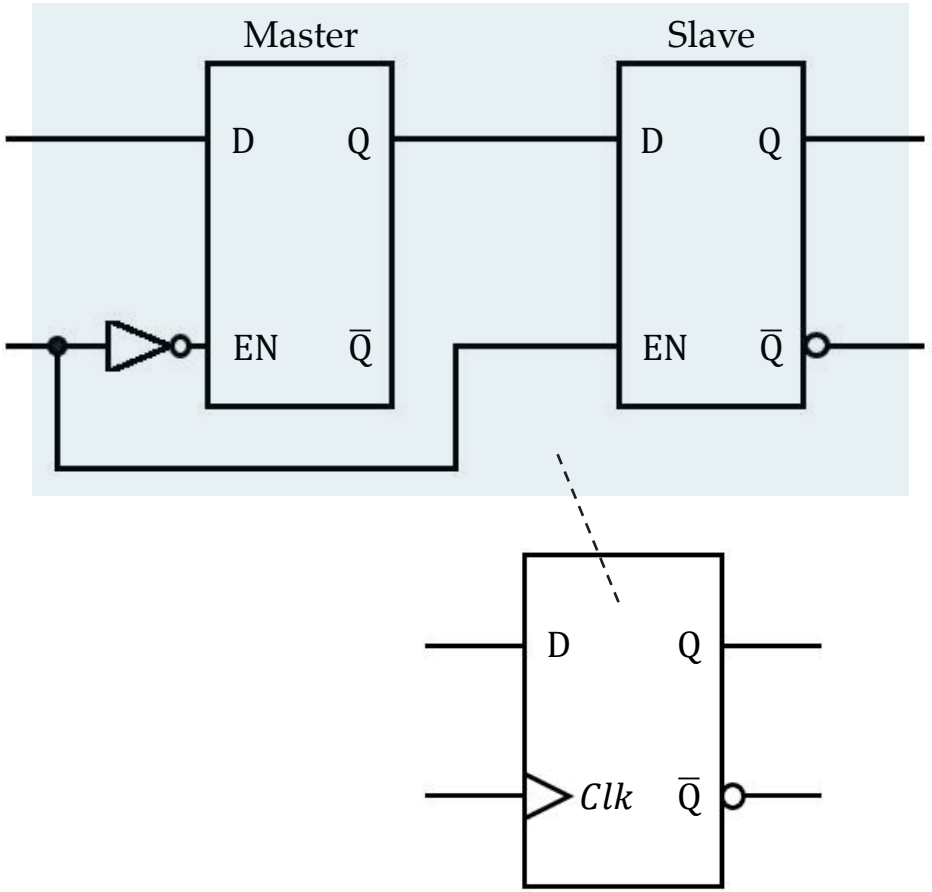
EN	D	Q
1	X	NC
0	0	0
0	1	1

Clk	D	Q(t+1)
0/1	X	Q(t)
↓	0	0
↓	1	1

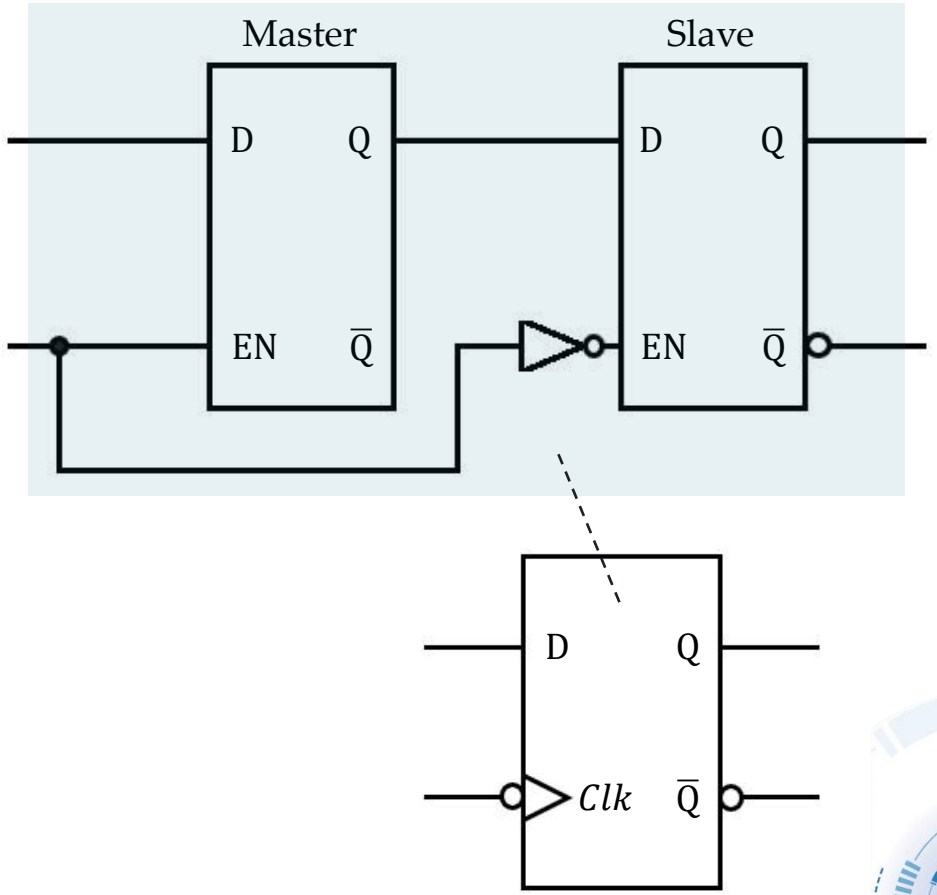
Q(t) – present state
Q(t+1) – next state

MASTER-SLAVE D FLIP-FLOP

Positive edge-triggered

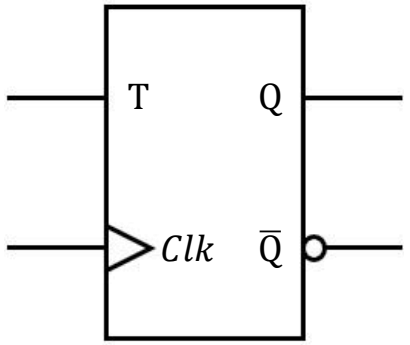


Negative edge-triggered

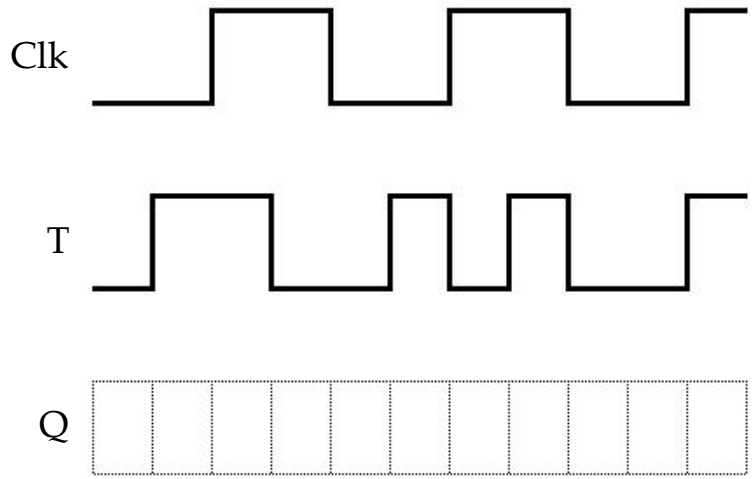


T FLIP-FLOP

Graphical Symbol



Timing Diagram

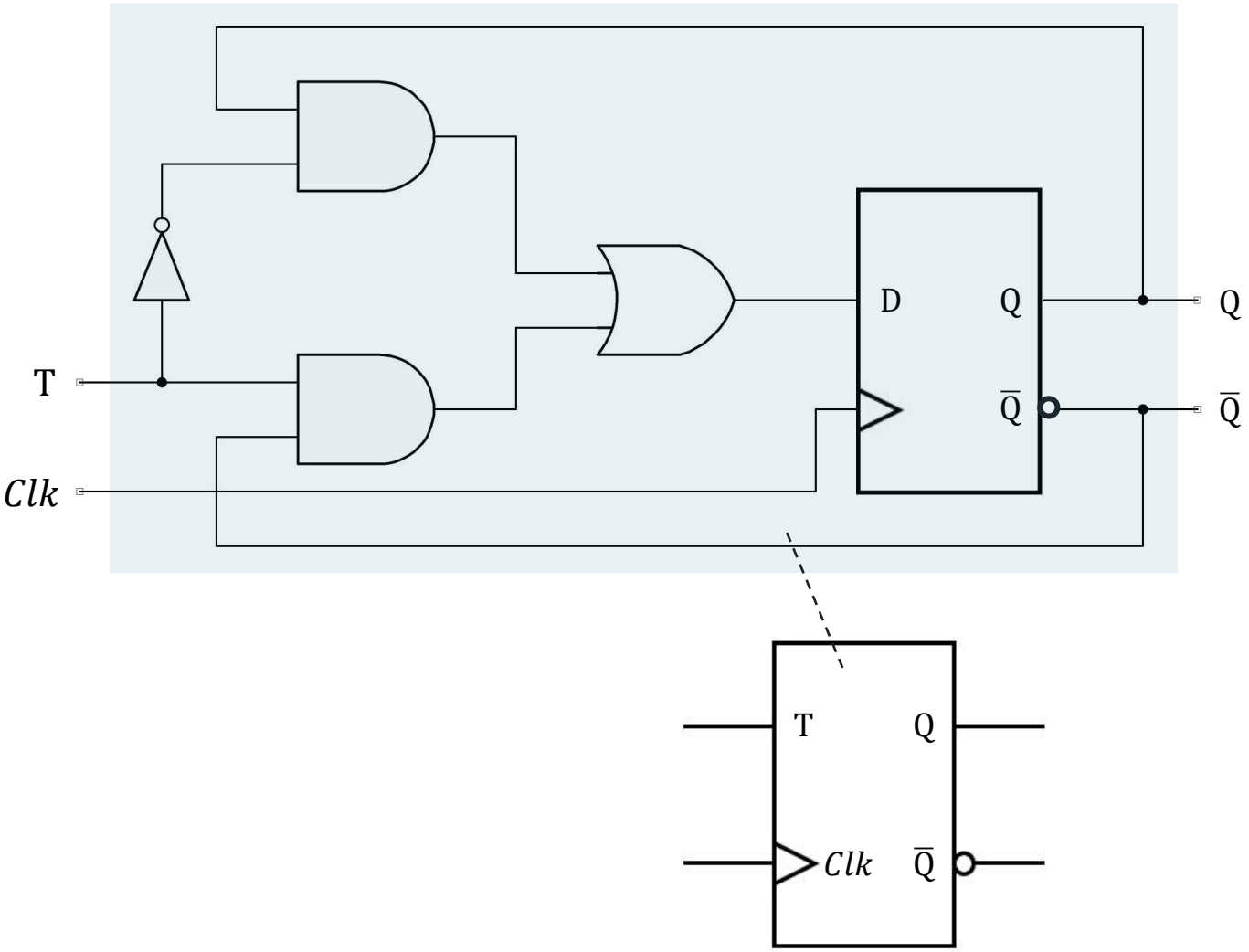


Characteristic Table

T	Q(t+1)
0	Q(t)
1	$\overline{Q}$(t)

T FLIP-FLOP

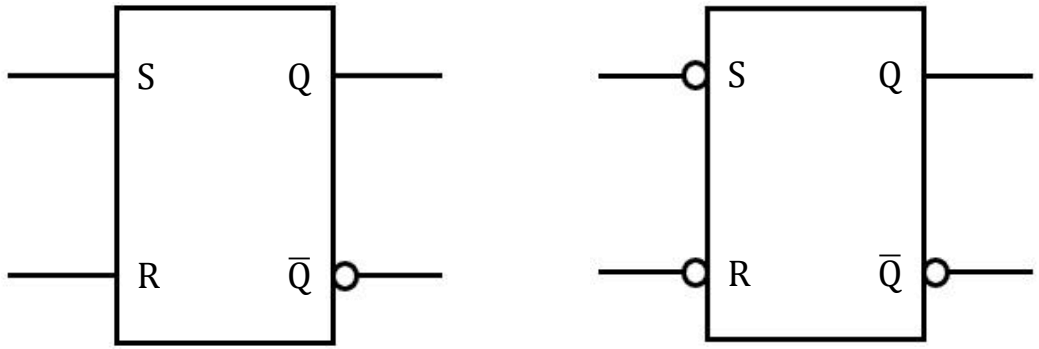
Implementation



SR LATCH

SR LATCH

Graphical Symbol



Characteristic Table

S	R	Q	$\overline{Q}$	Remark
0	0	1	1	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	NC	NC	Invalid

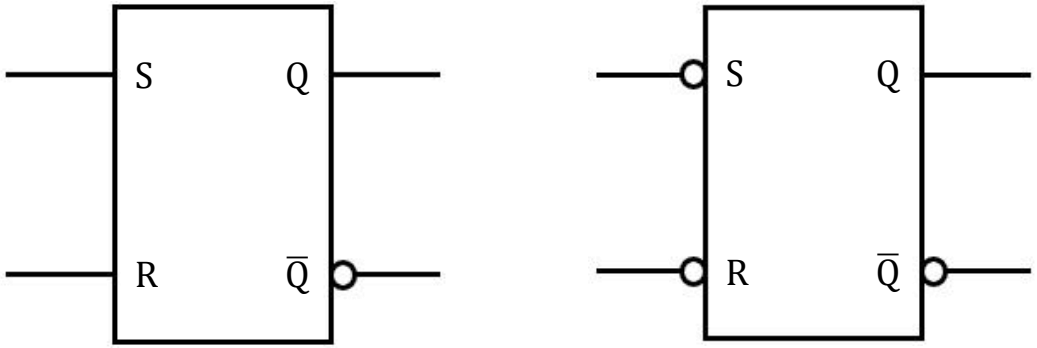
Active-HIGH

S	R	Q	$\overline{Q}$	Remark
0	0	NC	NC	Invalid
0	1	0	1	Set
1	0	1	0	Reset
1	1	1	1	No Change

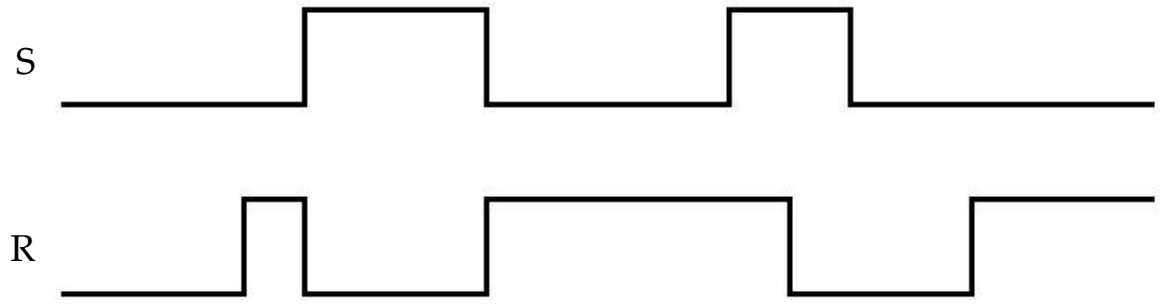
Active-LOW

SR LATCH

Graphical Symbol



Timing Diagram



Q(active-HIGH)

Q(active-LOW)

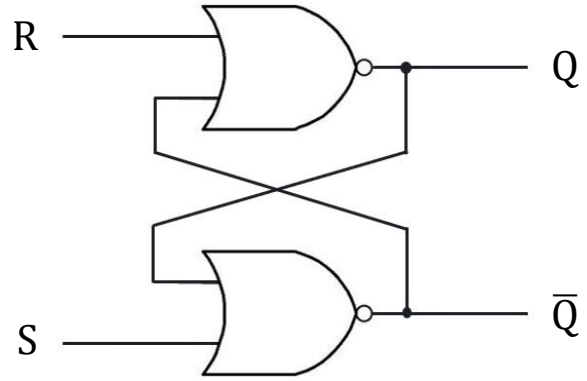
Characteristic Table

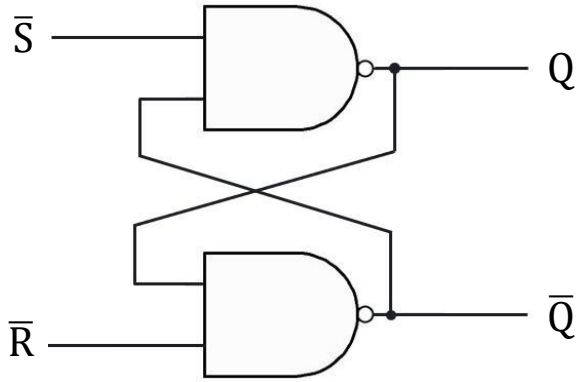
S	R	Q	$\overline{Q}$	Remark
0	0	1	1	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	NC	NC	Invalid

Active-HIGH

SR LATCH

Implementation





Characteristic Table

S	R	Q	$\overline{Q}$	Remark
0	0	1	1	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	NC	NC	Invalid

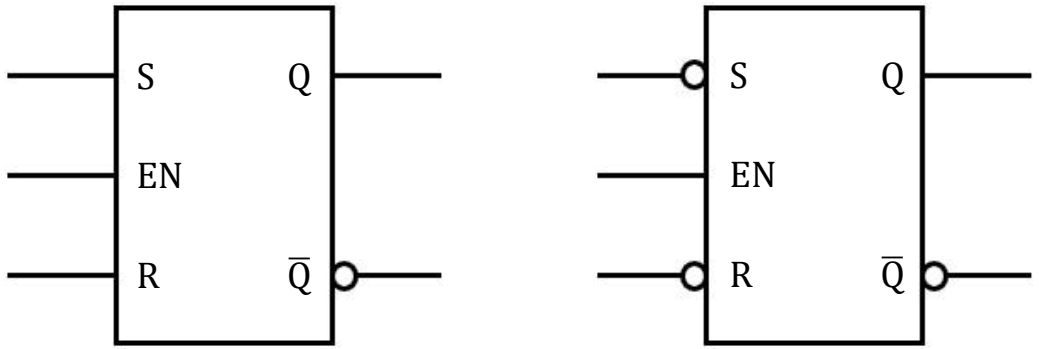
Active-HIGH

S	R	Q	$\overline{Q}$	Remark
0	0	NC	NC	Invalid
0	1	0	1	Set
1	0	1	0	Reset
1	1	1	1	No Change

Active-LOW

GATED SR LATCH

Graphical Symbol



Characteristic Table

EN	S	R	Q	$\overline{Q}$	Remark
0	X	X	Q	$\overline{Q}$	No Change
1	0	0	1	1	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	NC	NC	**Invalid**

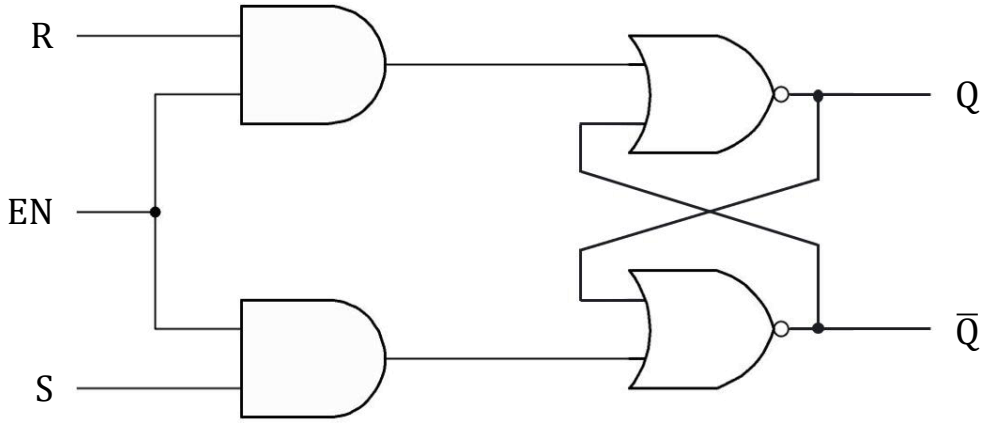
Active-HIGH

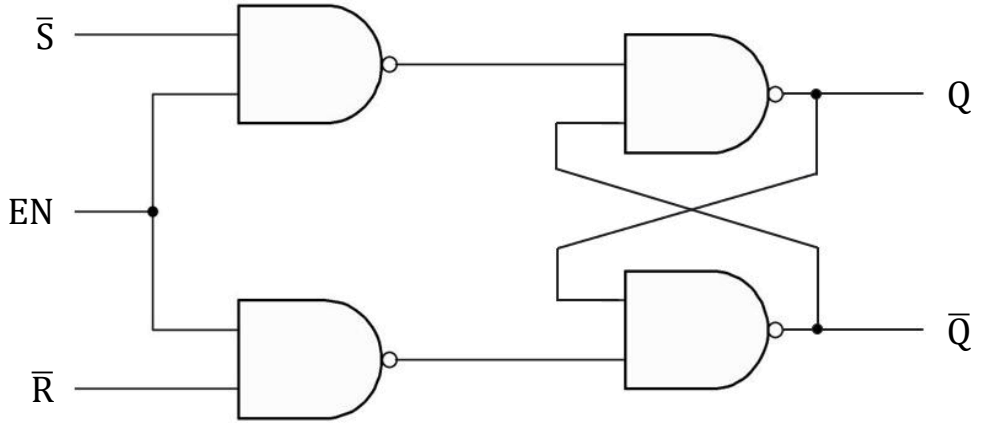
EN	S	R	Q	$\overline{Q}$	Remark
0	X	X	Q	$\overline{Q}$	No Change
1	0	0	NC	NC	**Invalid**
1	0	1	0	1	Set
1	1	0	1	0	Reset
1	1	1	1	1	No Change

Active-LOW

GATED SR LATCH

Implementation





Characteristic Table

EN	S	R	Q	$\bar{Q}$	Remark
0	X	X	Q	$\bar{Q}$	No Change
1	0	0	1	1	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	NC	NC	**Invalid**

Active-HIGH

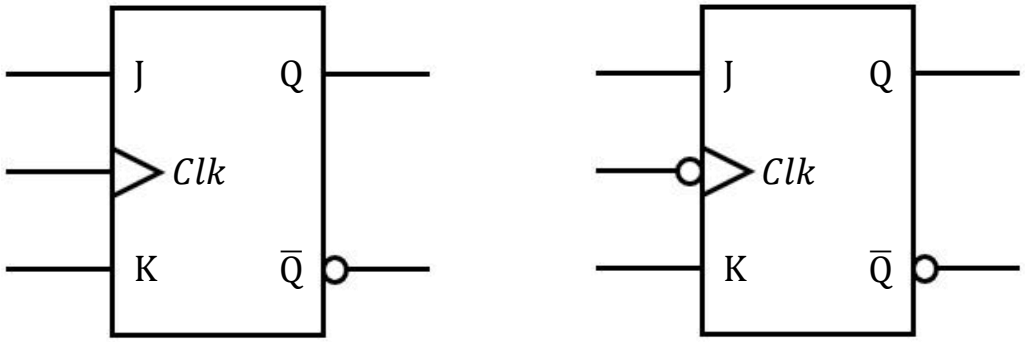
EN	S	R	Q	$\bar{Q}$	Remark
0	X	X	Q	$\bar{Q}$	No Change
1	0	0	NC	NC	**Invalid**
1	0	1	0	1	Set
1	1	0	1	0	Reset
1	1	1	1	1	No Change

Active-LOW

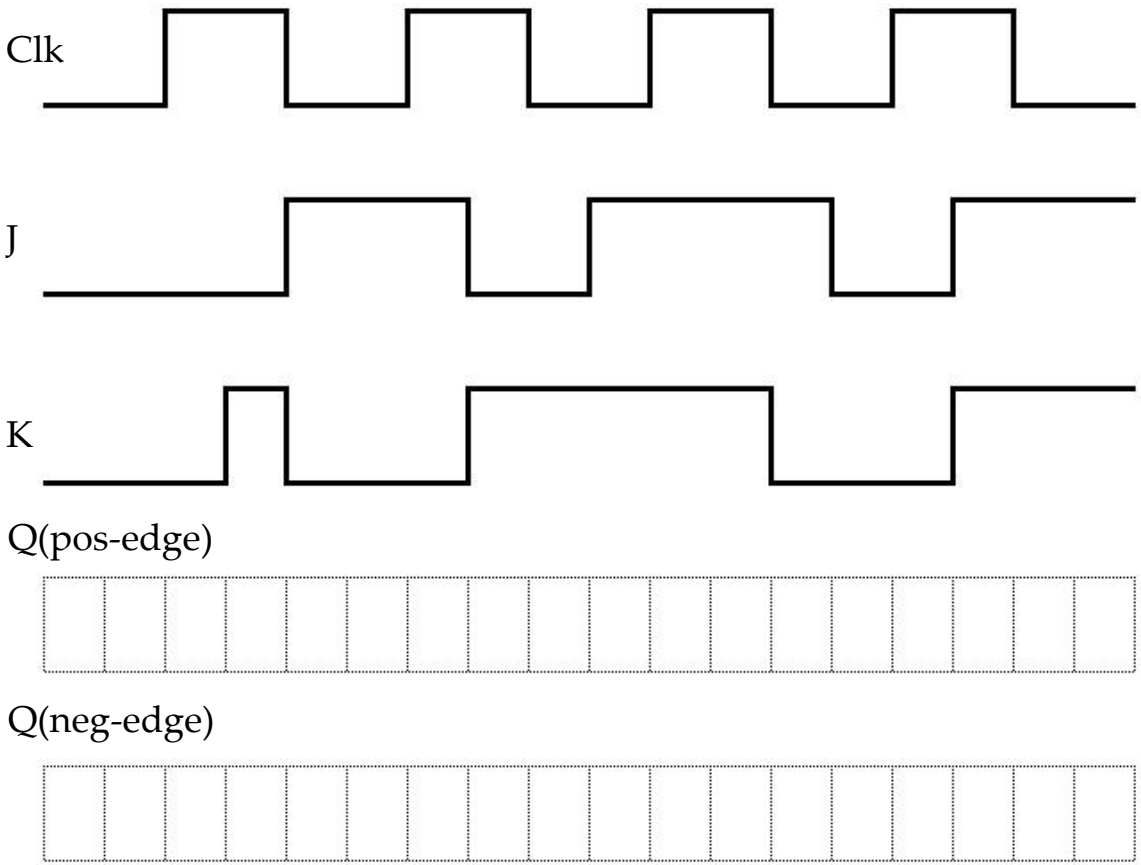
JK FLIP-FLOP

JK FLIP-FLOP

Graphical Symbol



Timing Diagram

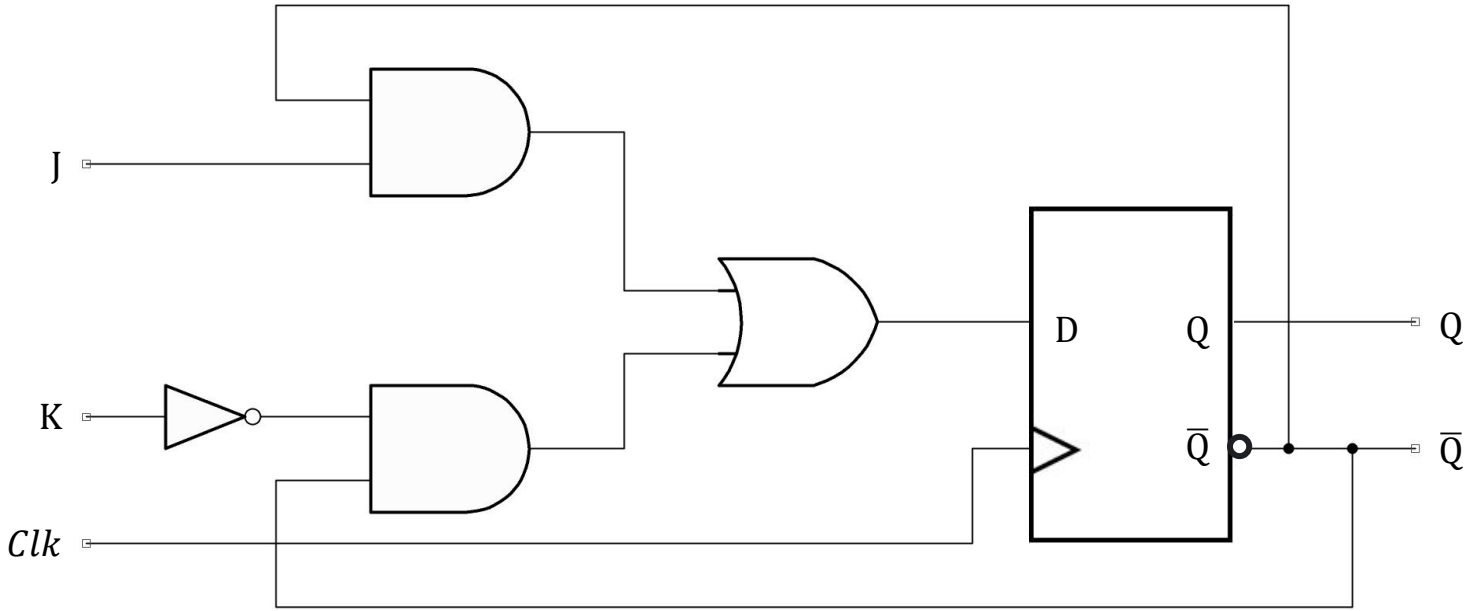


Characteristic Table

J	K	Q(t+1)	Remark
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}$(t)	Toggle

JK FLIP-FLOP

Implementation



LABORATORY