VERILOG HDL

INTRODUCTION

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TOPIC OUTLINE

Hardware Description Language

- Verilog and VHDL
- Verilog Code Structure
- Programmable Logic Device
- EDA Tool

HARDWARE DESCRIPTION LANGUAGE

HARDWARE DESCRIPTION LANGUAGE

Hardware Description Language (HDL) is a computer language used to describe the structure, design, and behavior of digital logic circuit.

Two most widely used HDL

Verilog

C-like syntax (similar programming languages like C)

VHDL

Ada-like syntax (more verbose and stricter)

HDL

Verilog

```
module half_adder(
     input A,
     input B,
     output cout,
     output sum
 );
     and(cout,A,B);
     xor(sum,A,B);
endmodule
```

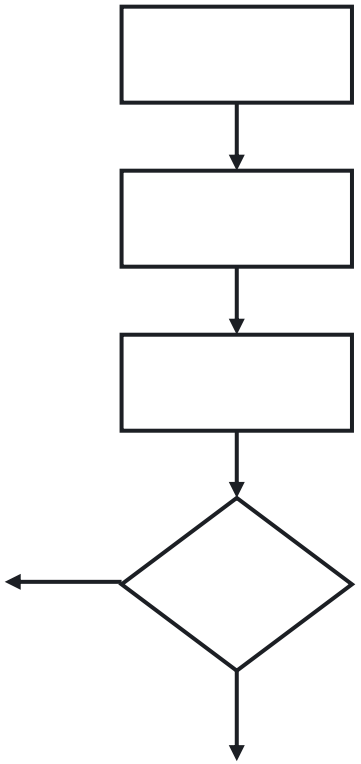
VHDL

```
entity half_adder is
    Port( A : in STD_LOGIC;
          B : in STD_LOGIC;
          cout : out STD_LOGIC;
          sum : out STD_LOGIC);
end half_adder;


architecture behavior of half_adder is
begin
     cout <= A and B;
     sum <= A xor B;
end behavior
```

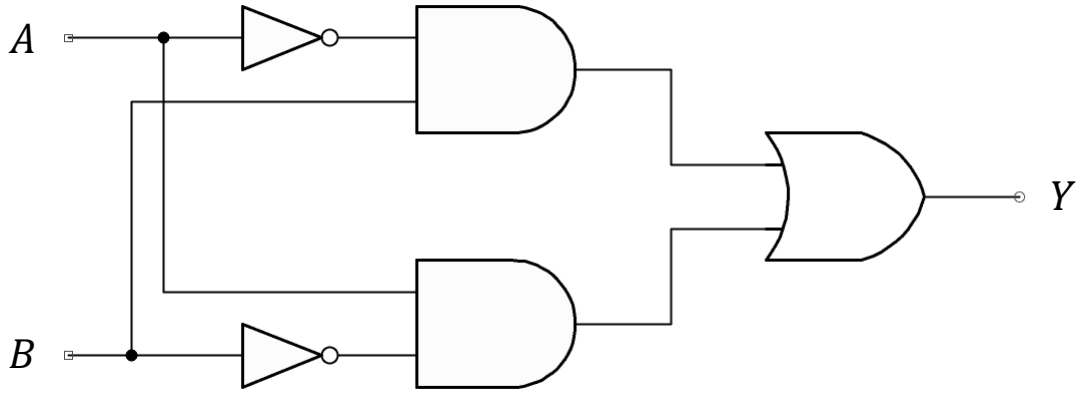
CONCURRENT DESIGN

Traditional Programming



Sequential execution

Hardware Description



Parallel execution

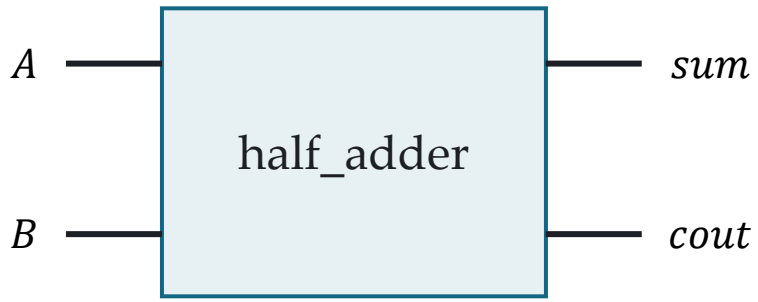
Take note that in HDL, you are describing the hardware, **not writing a program**.

VERILOG CODE STRUCTURE

Descriptive Module

- Describes the hardware

```
module half_adder(sum,cout,A,B);
    ------------------
    ------------------
    ------------------
endmodule
```



Testbench Module

- Simulation verification environment

```
module testbench();
    ------------------
    ------------------
    ------------------
endmodule
```

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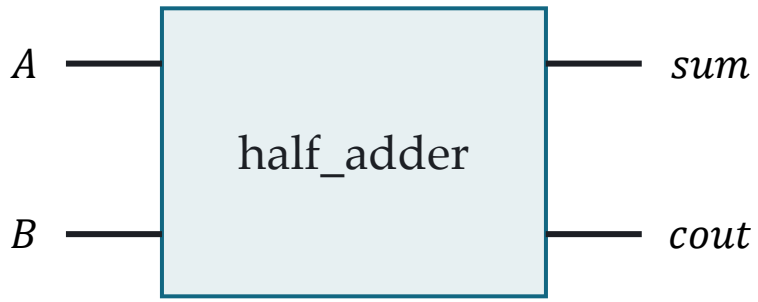
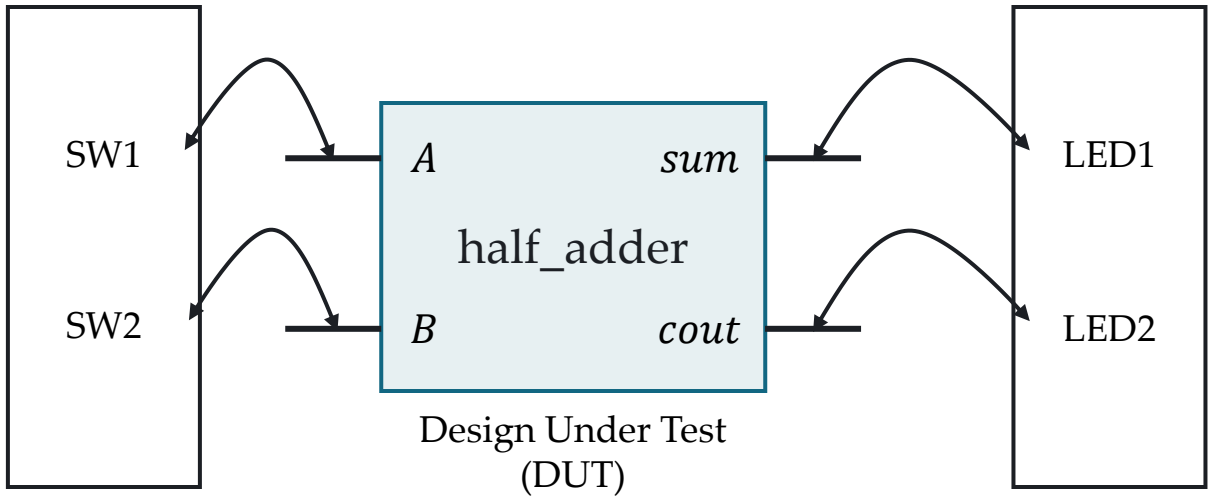


Testbench Module

- Simulation verification environment

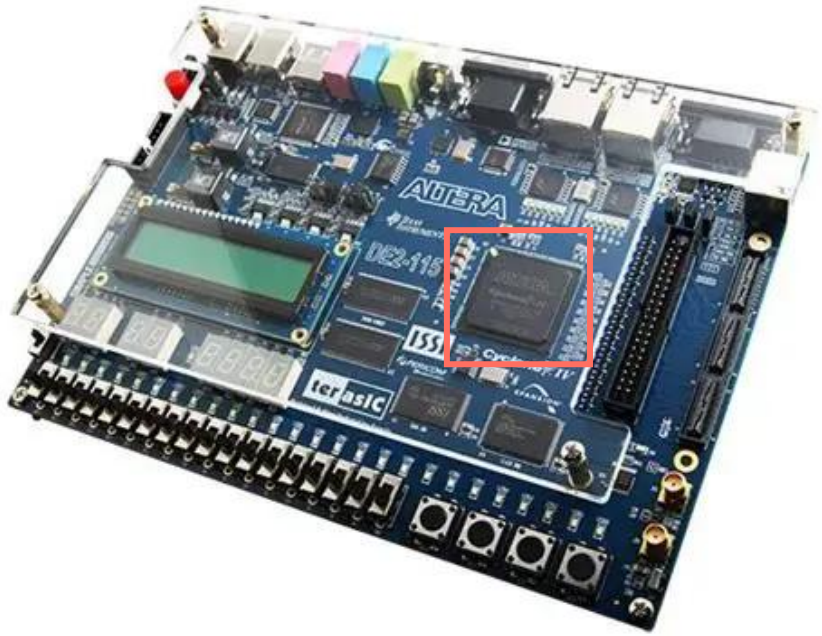


A **testbench** is used to verify and simulate the functionality of a design.

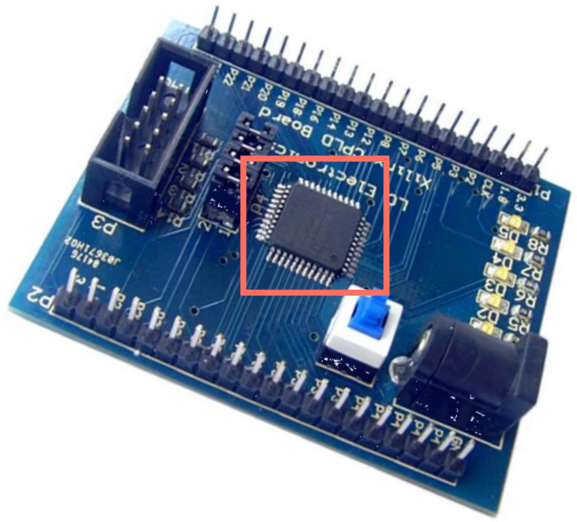
It does not represent actual hardware (non-synthesizable).

PROGRAMMABLE LOGIC DEVICE

FPGA (Field-Programmable Gate Array)



CPLD (Complex Programmable Logic Device)

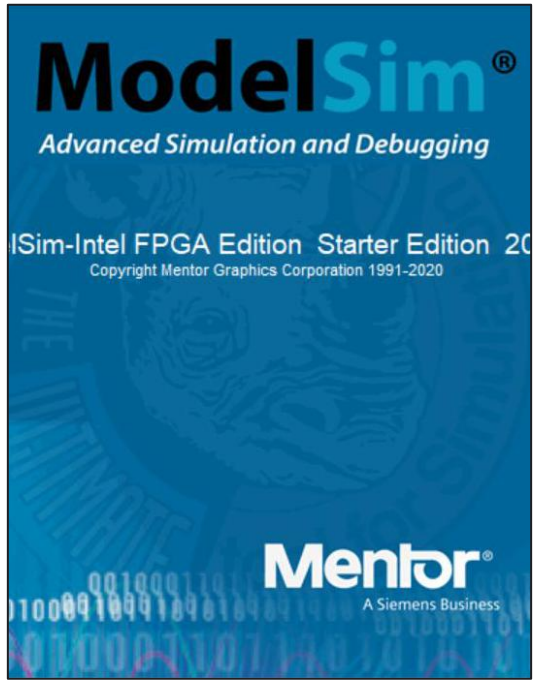


Development Board

EDA TOOLS

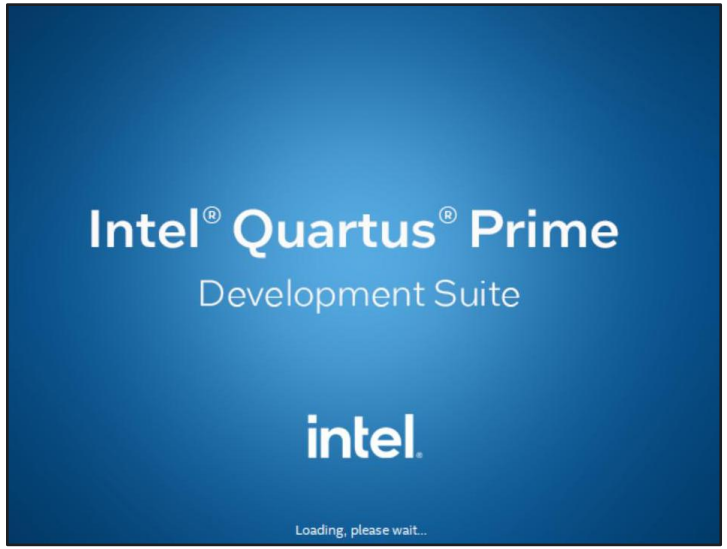
ModelSim

A simulation tool primarily used for functional verification of HDL designs (VHDL, Verilog, SystemVerilog)



Quartus Prime

An FPGA design suite from Intel for synthesis, implementation, and programming of FPGA (Field Programmable Gate Array) devices.



LABORATORY