DESIGN AND SYNTHESIS OF LOGIC CIRCUITS

COMBINATIONAL LOGIC CIRCUITS

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TOPIC OUTLINE

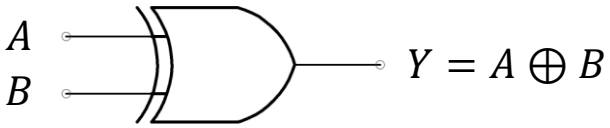
Synthesis of XOR/XNOR Gate

Synthesis of BCD-to-7-Segment Decoder

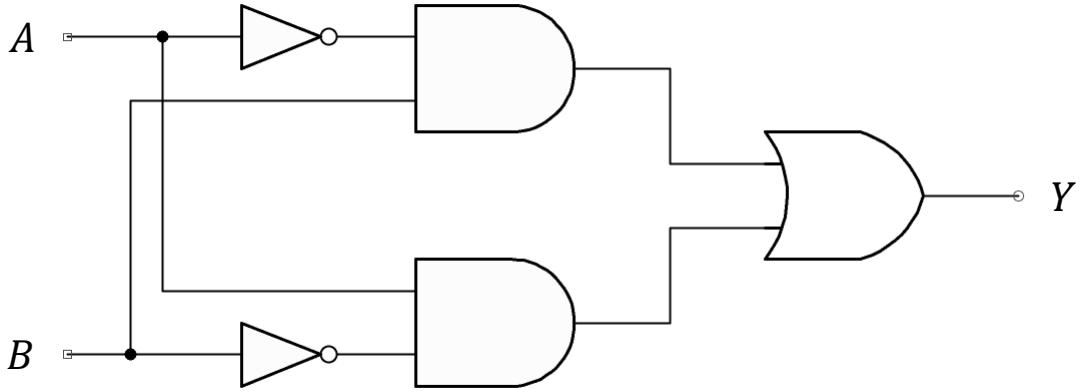
SYNTHESIS OF XOR/XNOR GATE

EXCLUSIVE-OR GATE

Logic Symbol



Equivalent Logic Circuit



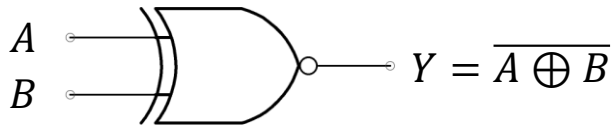
$$Y = \bar{A}B + A\bar{B}$$

Truth Table

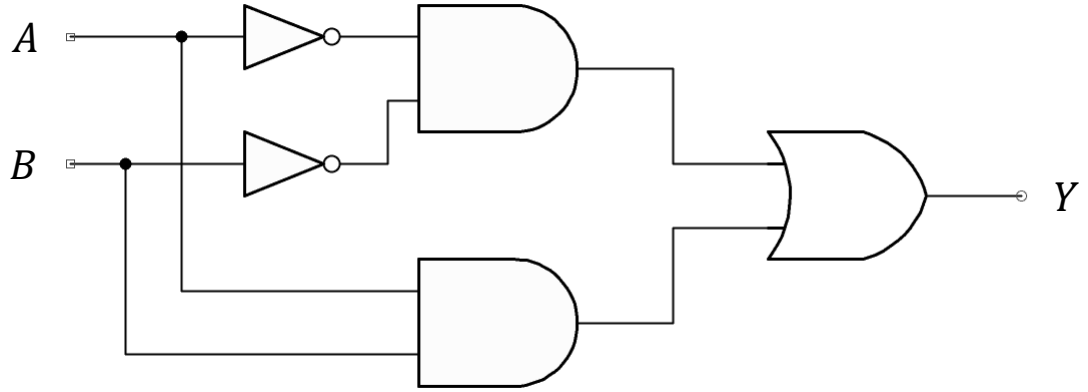
A	B	Y	Minterm
0	0	0	
0	1	1	$m_1 = \bar{A}B$
1	0	1	$m_2 = A\bar{B}$
1	1	0	

EXCLUSIVE-NOR GATE

Logic Symbol



Equivalent Logic Circuit



$$Y = \bar{A}\bar{B} + AB$$

Truth Table

A	B	Y	Minterm
0	0	1	$m_0 = \bar{A}\bar{B}$
0	1	0	
1	0	0	
1	1	1	$m_3 = AB$

EXERCISE

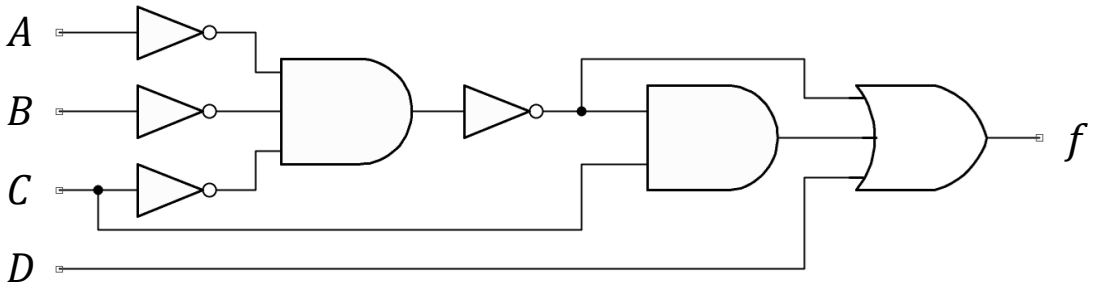
Develop a logic circuit with four input variables that will only produce a 1 output when exactly three input variables are 1s.

Solution

$ABCD$	Minterm

EXERCISE

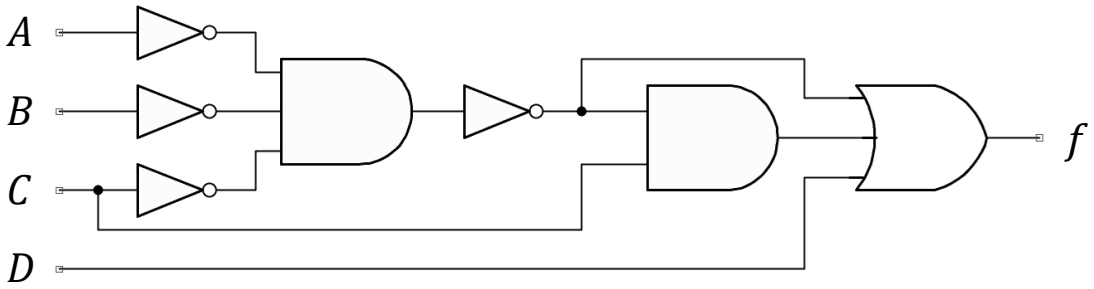
Reduce the combinational logic circuit to a minimum form.



Solution

EXERCISE

Reduce the combinational logic circuit to a minimum form.



Solution

N	$ABCD$	f
0	0000	
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	

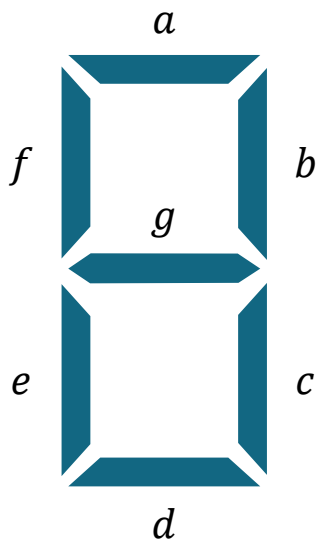
N	$ABCD$	f
9	1001	
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

SYNTHESIS OF BCD-TO-7-SEGMENT DECODER

THE 7-SEGMENT DISPLAY

A standard 7-segment display consists of **seven LEDs** (segments) arranged in a rectangular layout to form the number 8. Each segment is labeled from a to g, and an optional eighth segment (DP) is used for the decimal point.

Segment Arrangement



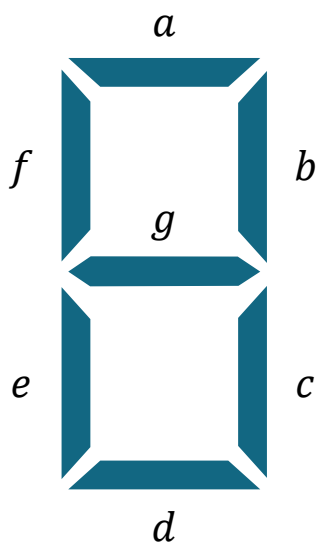
EXPRESSION FOR SEGMENT A

Truth Table

N	$DCBA$	f_a
0	0000	
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	

N	$DCBA$	f_a
9	1001	
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

Segment Arrangement



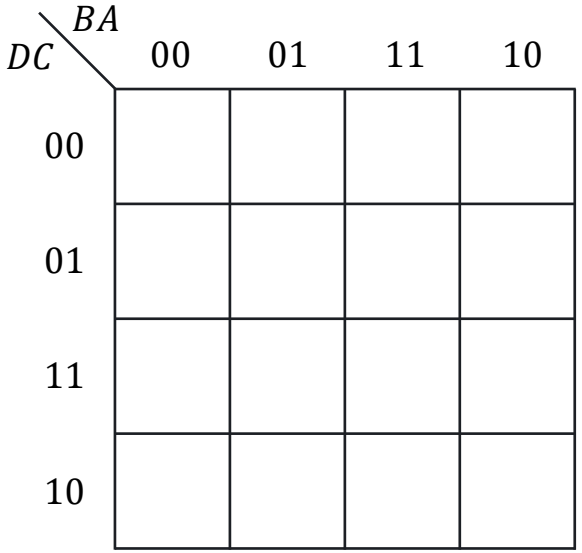
EXPRESSION FOR SEGMENT A

Truth Table

N	$DCBA$	f_a
0	0000	
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	

N	$DCBA$	f_a
9	1001	
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

K-Map



EXPRESSION FOR SEGMENT A

Truth Table

N	$DCBA$	f_a
0	0000	
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	

N	$DCBA$	f_a
9	1001	
10	1010	
11	1011	
12	1100	
13	1101	
14	1110	
15	1111	

QM Method

Group	$DCBA$	Minterm	1st Level

EXPRESSION FOR SEGMENT A

Prime Implicants Chart

Prime Implicants	m_0	m_2	m_3	m_5	m_7	m_8	m_9

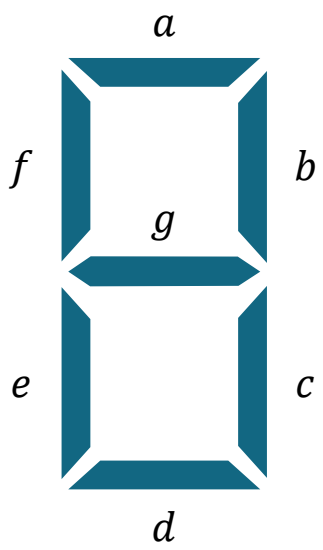
QM Method

Group	2nd Level	3rd Level

EXERCISE

Using Karnaugh Map and the Quine-McCluskey method, synthesize the minimized Boolean expressions for each segment (a–g) of a 7-segment display decoder.

Segment Arrangement



LABORATORY