FIXED-BIAS CIRCUIT

BJT DC BIASING

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TOPIC OUTLINE

Fixed-Bias Circuit

- Base-Emitter Loop
- Collector-Emitter Loop
- Load Line Analysis

FIXED-BIAS CIRCUIT

CURRENT GAIN

The current gain parameters **alpha** (α) and **beta** (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

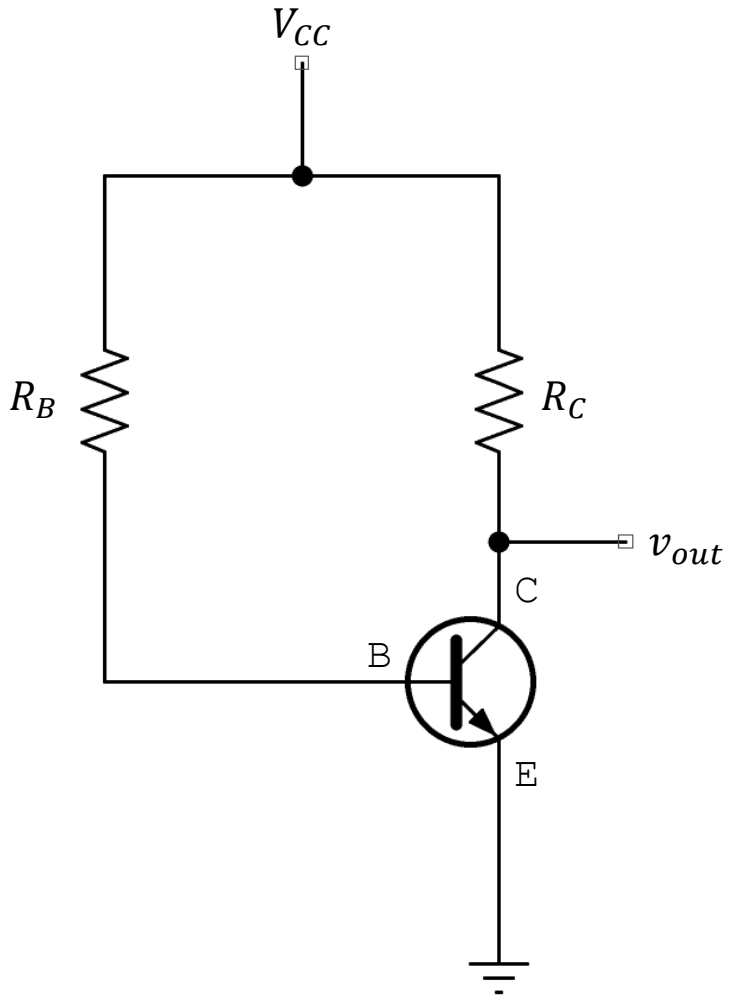
α is always less than 1 (typically 0.95 to 0.995)

Beta (β) is the ratio of the collector current to the base current.

Formula

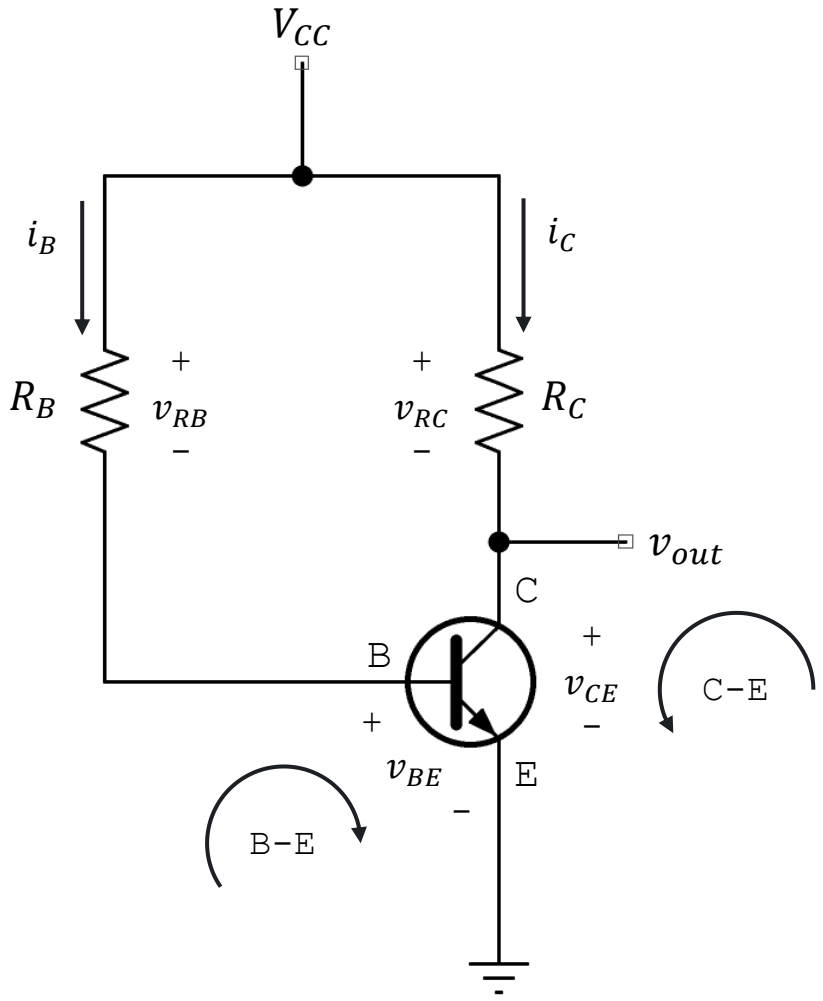
$$\beta = \frac{i_C}{i_B}$$

FIXED-BIAS CIRCUIT



Fixed-bias configuration is the simplest method – the biasing voltage applied to the base of the BJT is fixed by a single resistor (R_B) connected directly to the power supply (v_{CC}).

BASE-EMITTER LOOP



KVL @B-E

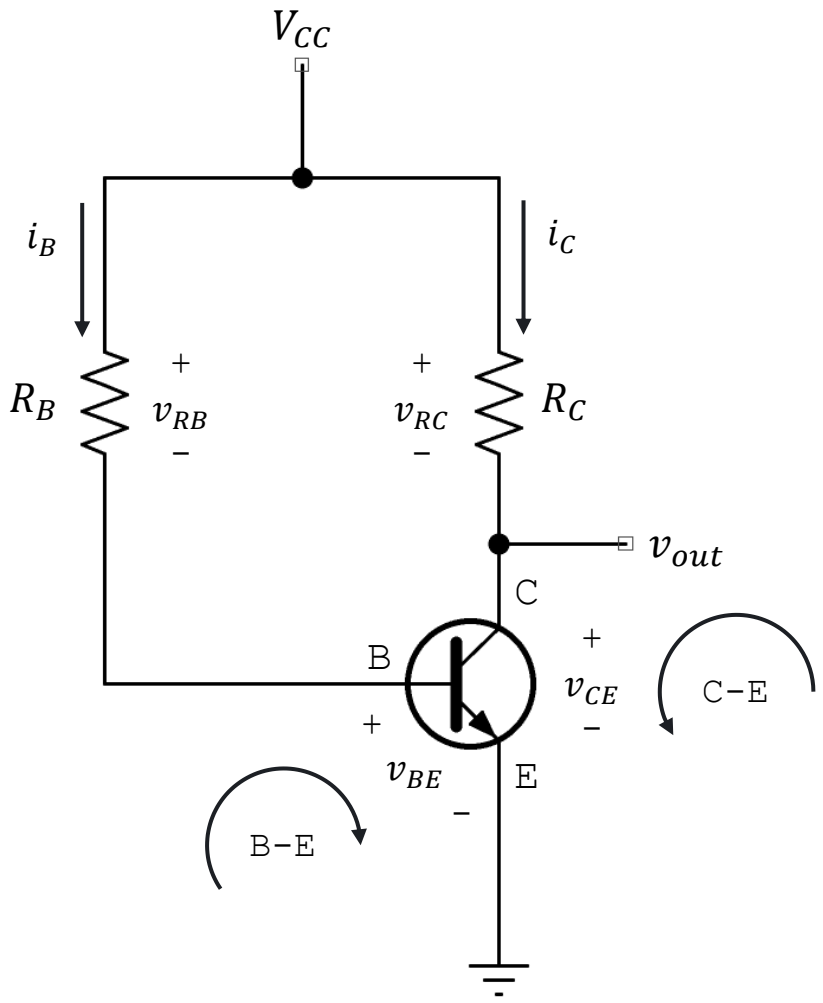
$$-v_{CC} + v_{RB} + v_{BE} = 0$$

$$v_{RB} = v_{CC} - v_{BE}$$

$$i_B R_B = v_{CC} - v_{BE}$$

$$i_B = \frac{v_{CC} - v_{BE}}{R_B}$$

COLLECTOR-EMITTER LOOP



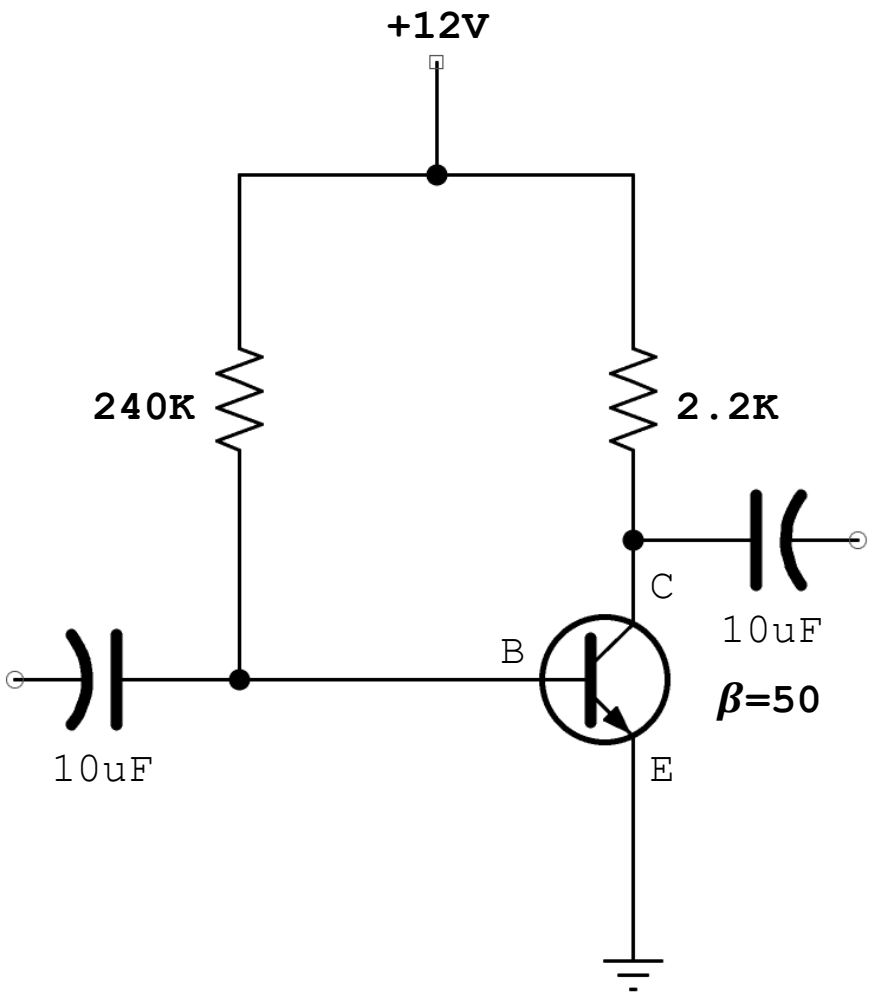
KVL @C-E

$$-v_{CC} + v_{RC} + v_{CE} = 0$$

$$v_{CE} = v_{CC} - v_{RC}$$

$$v_{CE} = v_{CC} - i_C R_C$$

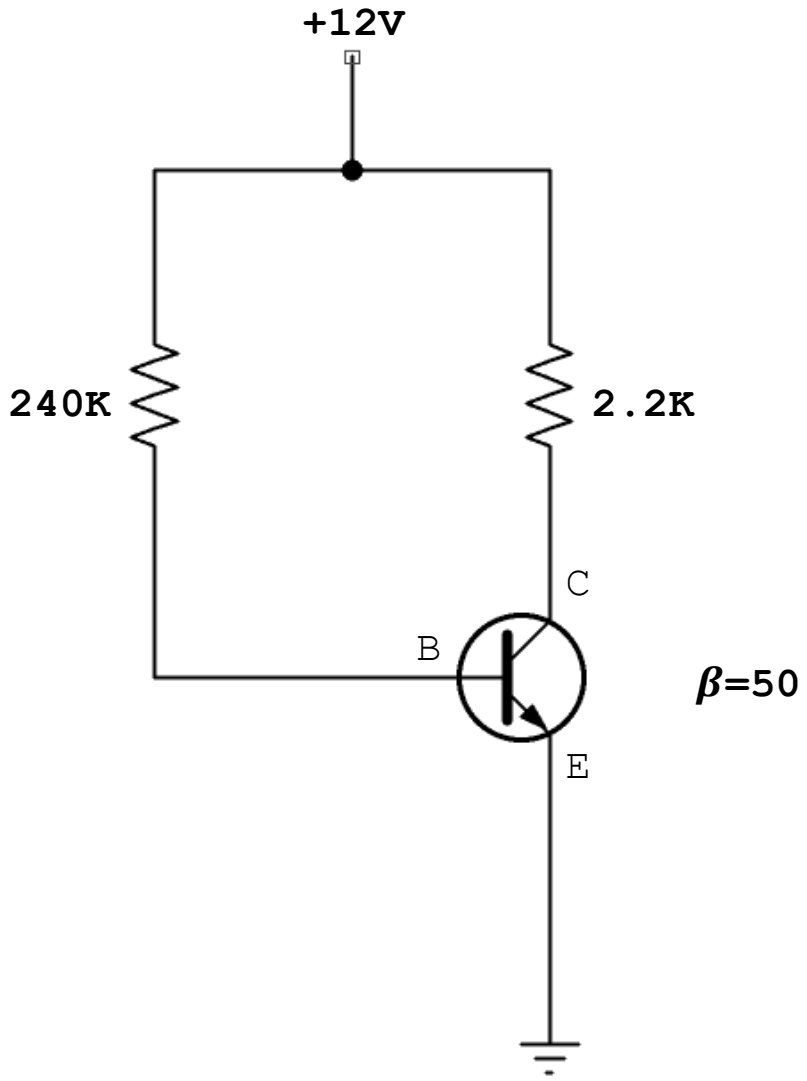
EXERCISE



Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})
- Base voltage (v_B)
- Base-Collector voltage (v_{BC})

EXERCISE



β=50

Solution

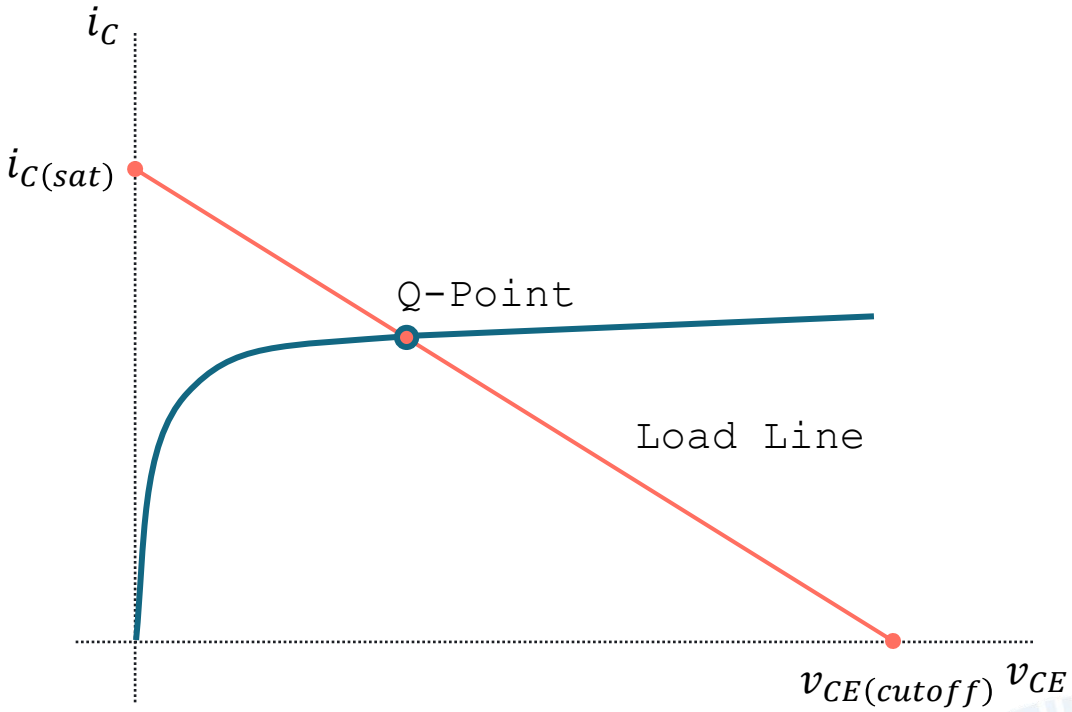
LOAD LINE ANALYSIS

SATURATION POINT

The **saturation point** is the operating state where BJT conducts the **maximum collector current** ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

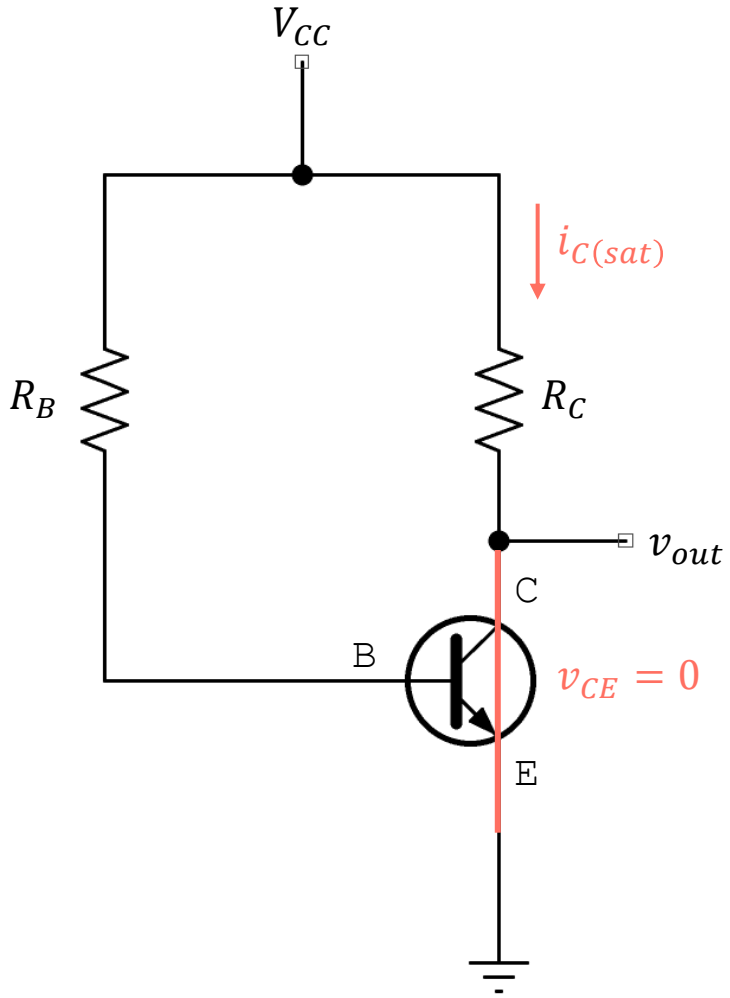
In this region the transistor acts like a **closed switch** (zero resistance between collector-emitter).

Collector Characteristic Curve

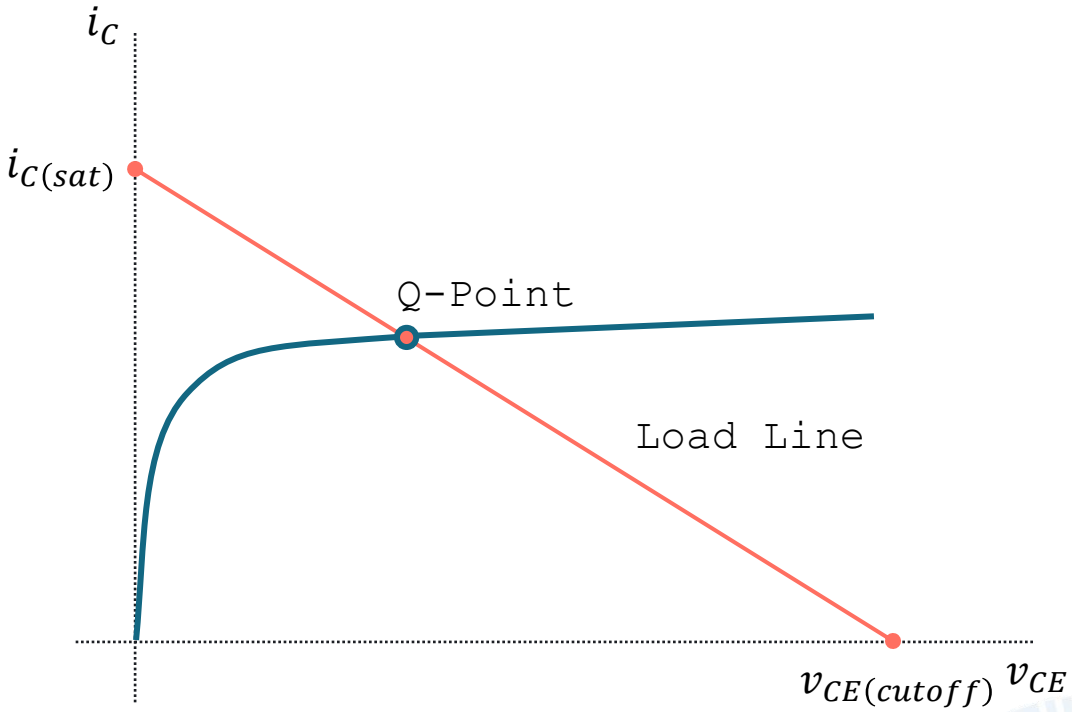


SATURATION POINT

Mentally Short



Collector Characteristic Curve

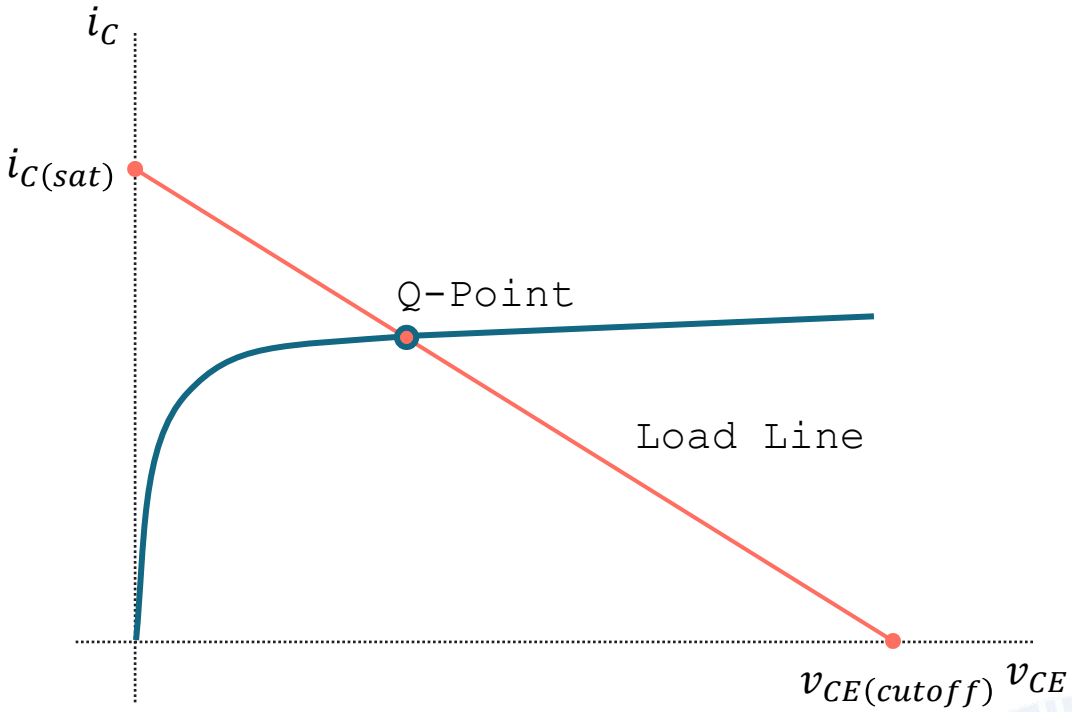


CUTOFF POINT

The **cutoff point** is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

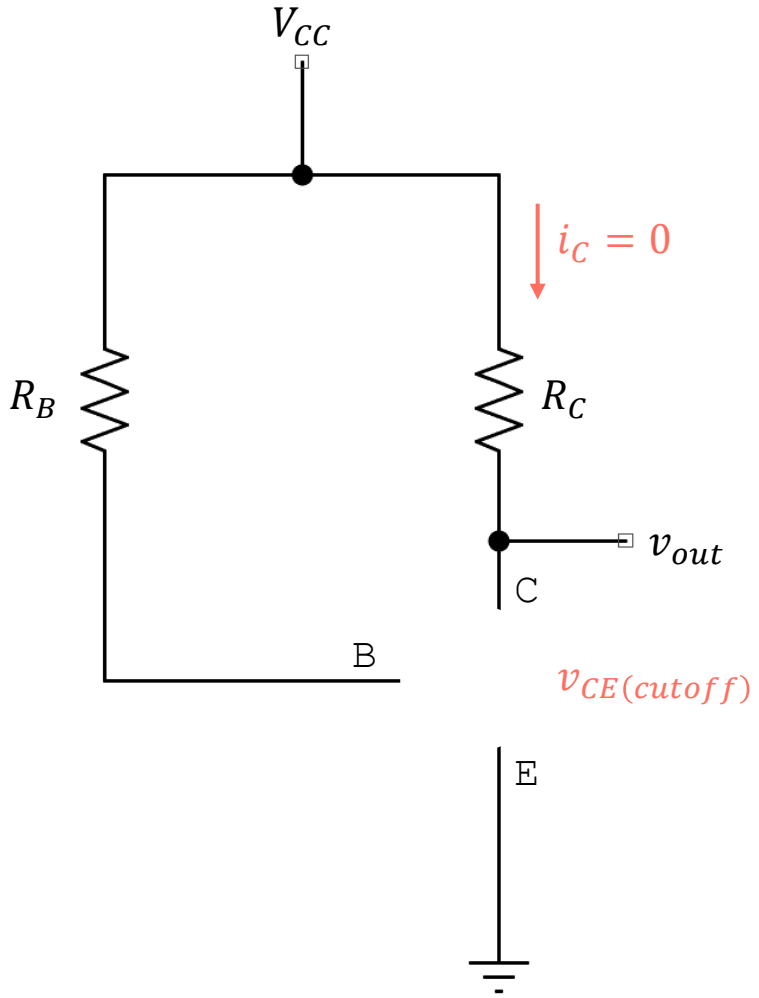
In this region the transistor acts like an **open switch** (infinite resistance between collector-emitter).

Collector Characteristic Curve

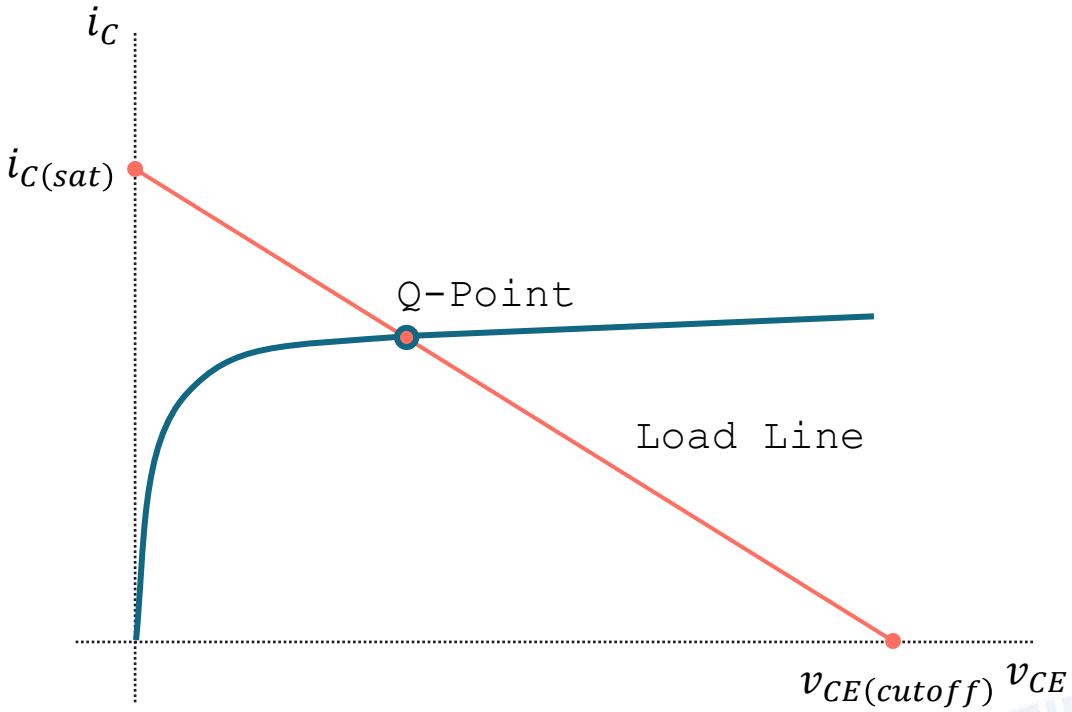


CUTOFF POINT

Mentally Open



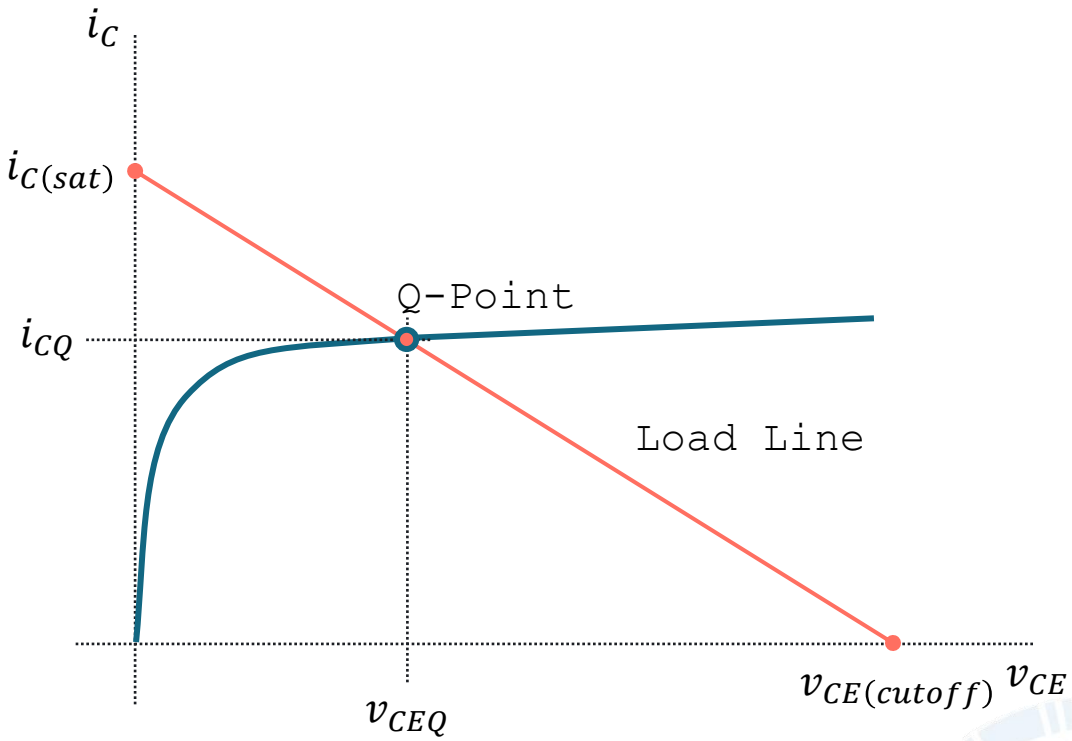
Collector Characteristic Curve



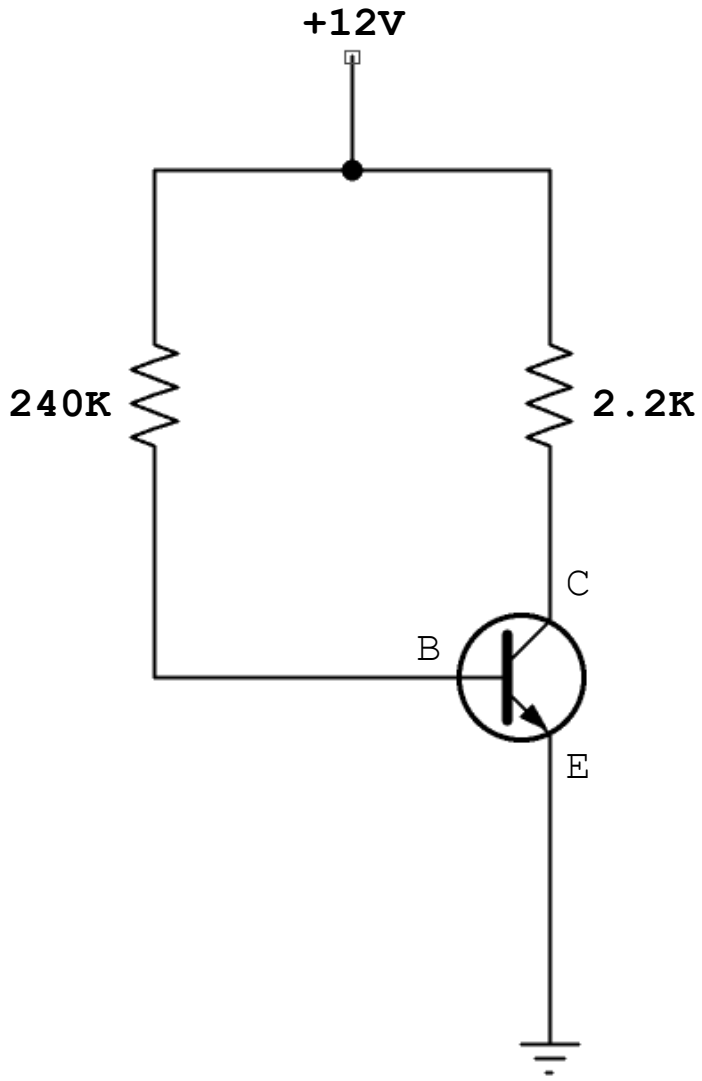
QUIESCENT POINT

The **Q-point** is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}).

Collector Characteristic Curve



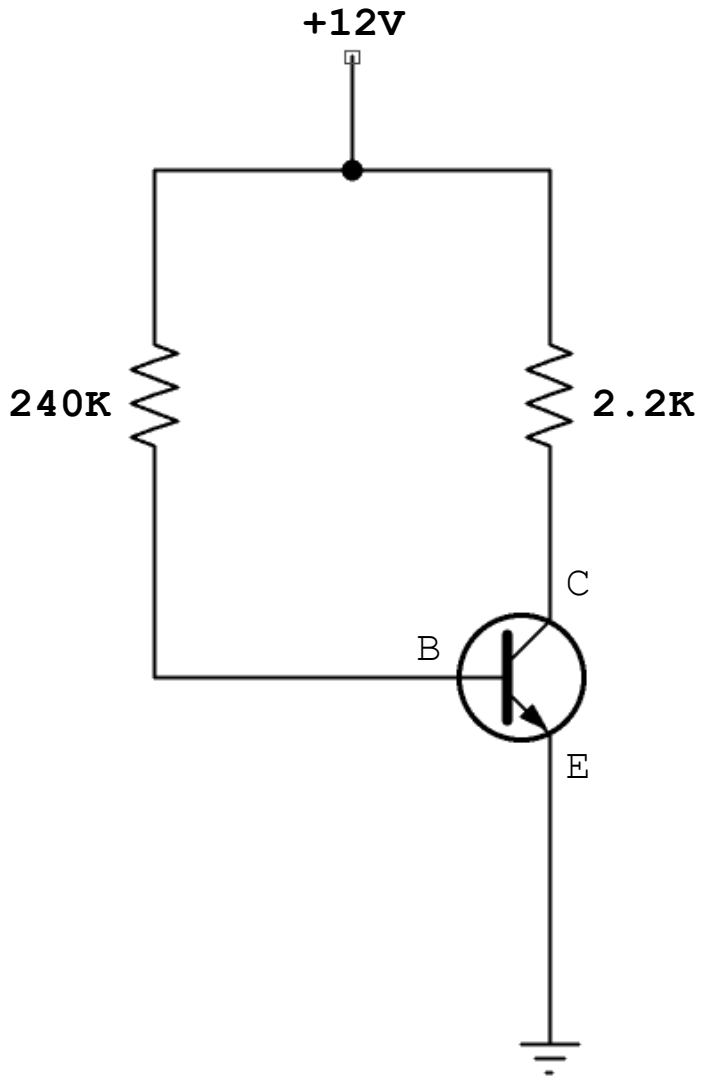
EXERCISE



Plot the DC load line for the fixed-bias circuit and clearly indicate the following points on the graph.

- Saturation current ($i_{C(sat)}$)
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

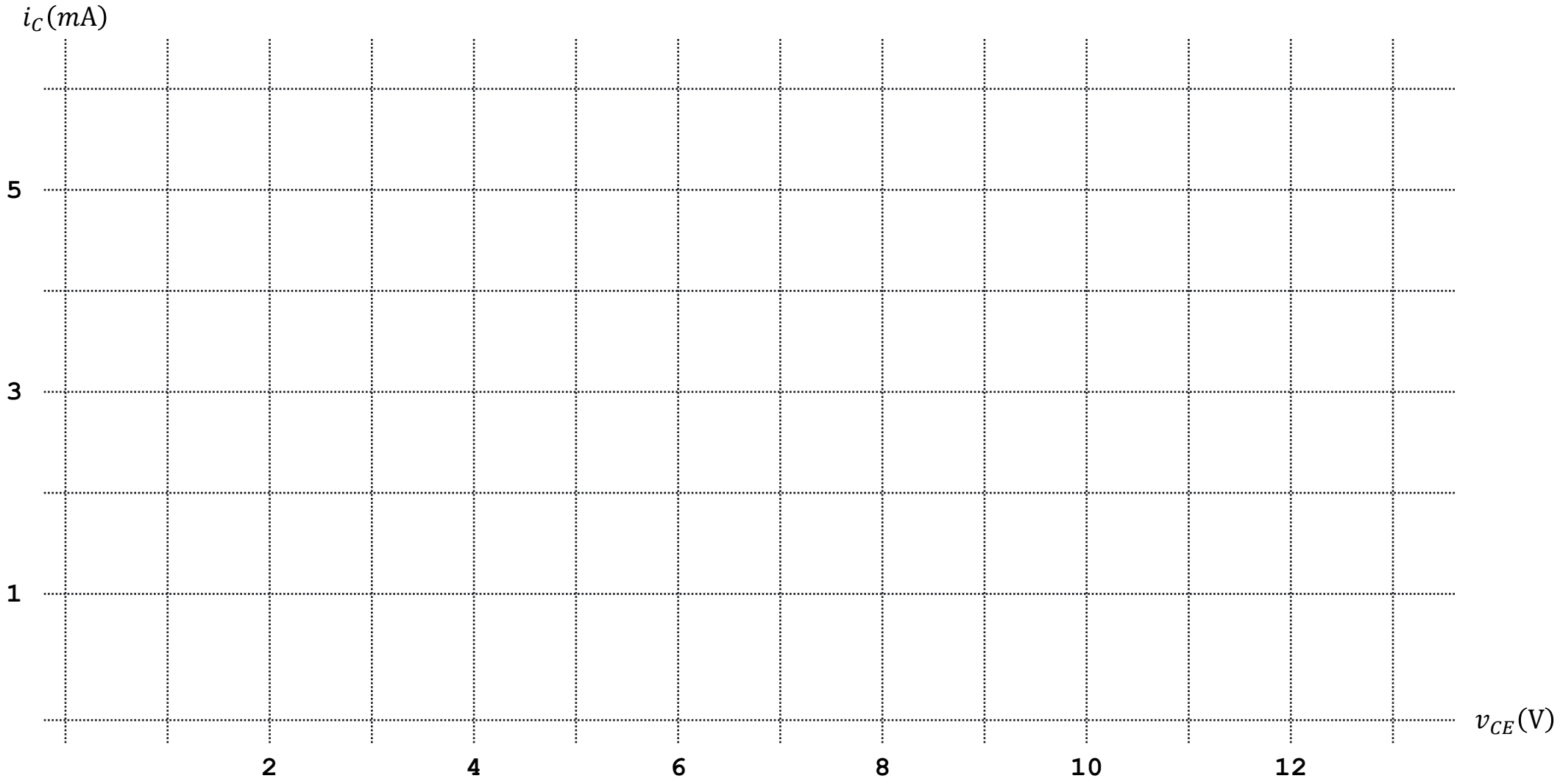
EXERCISE



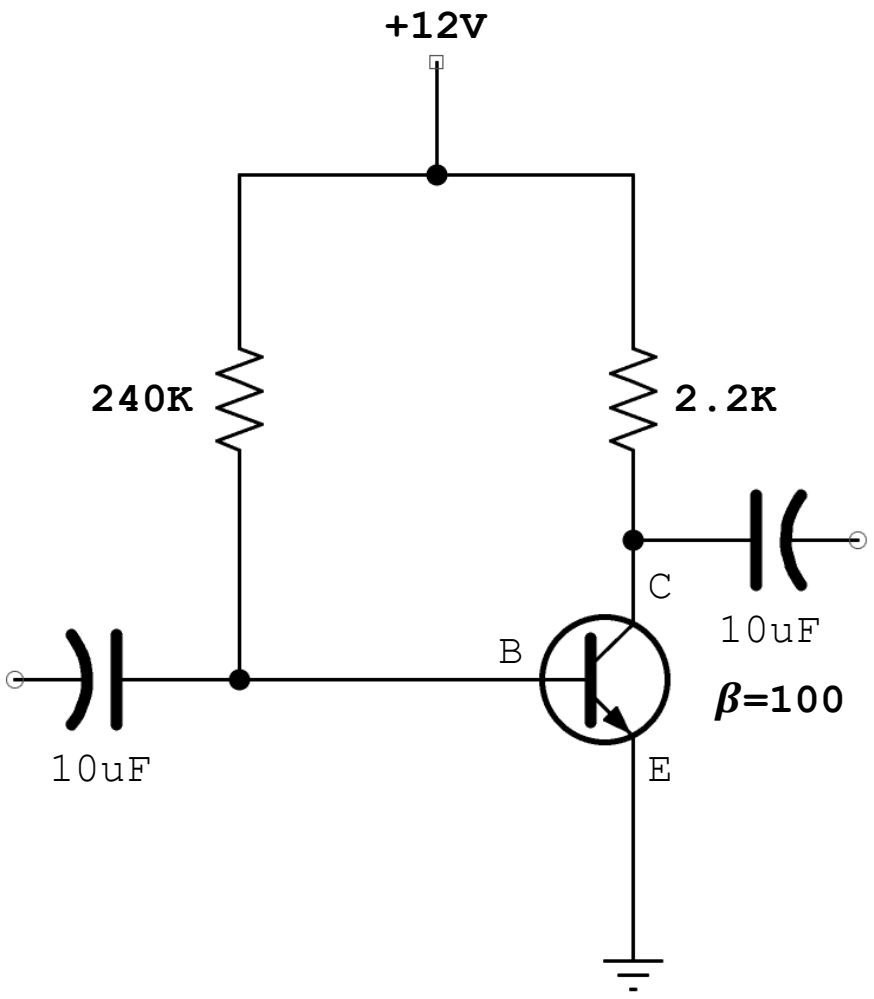
Solution

EXERCISE

Load Line Analysis



EXERCISE



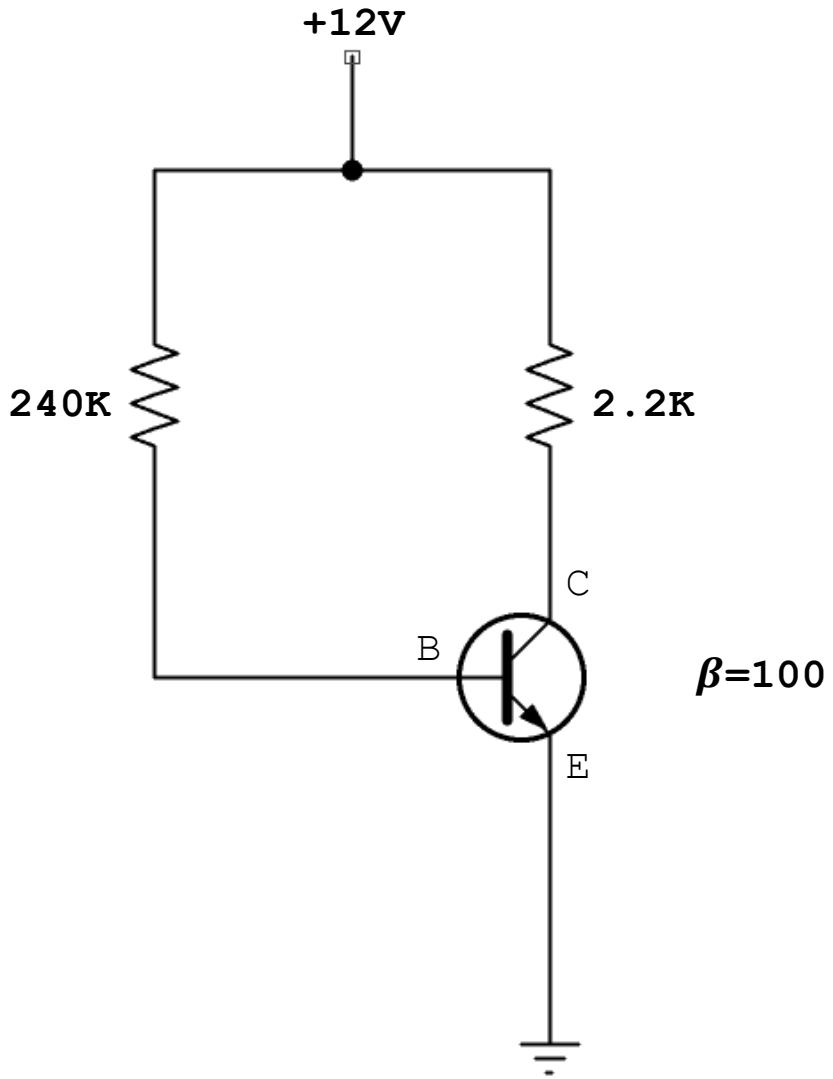
Determine the following parameters for the given fixed-bias circuit:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})

and clearly indicate the following points on the load line analysis graph.

- Saturation current $(i_{C(sat)})$
- Cutoff voltage $(v_{CE(cutoff)})$
- Operating Point (Q-Point)

EXERCISE

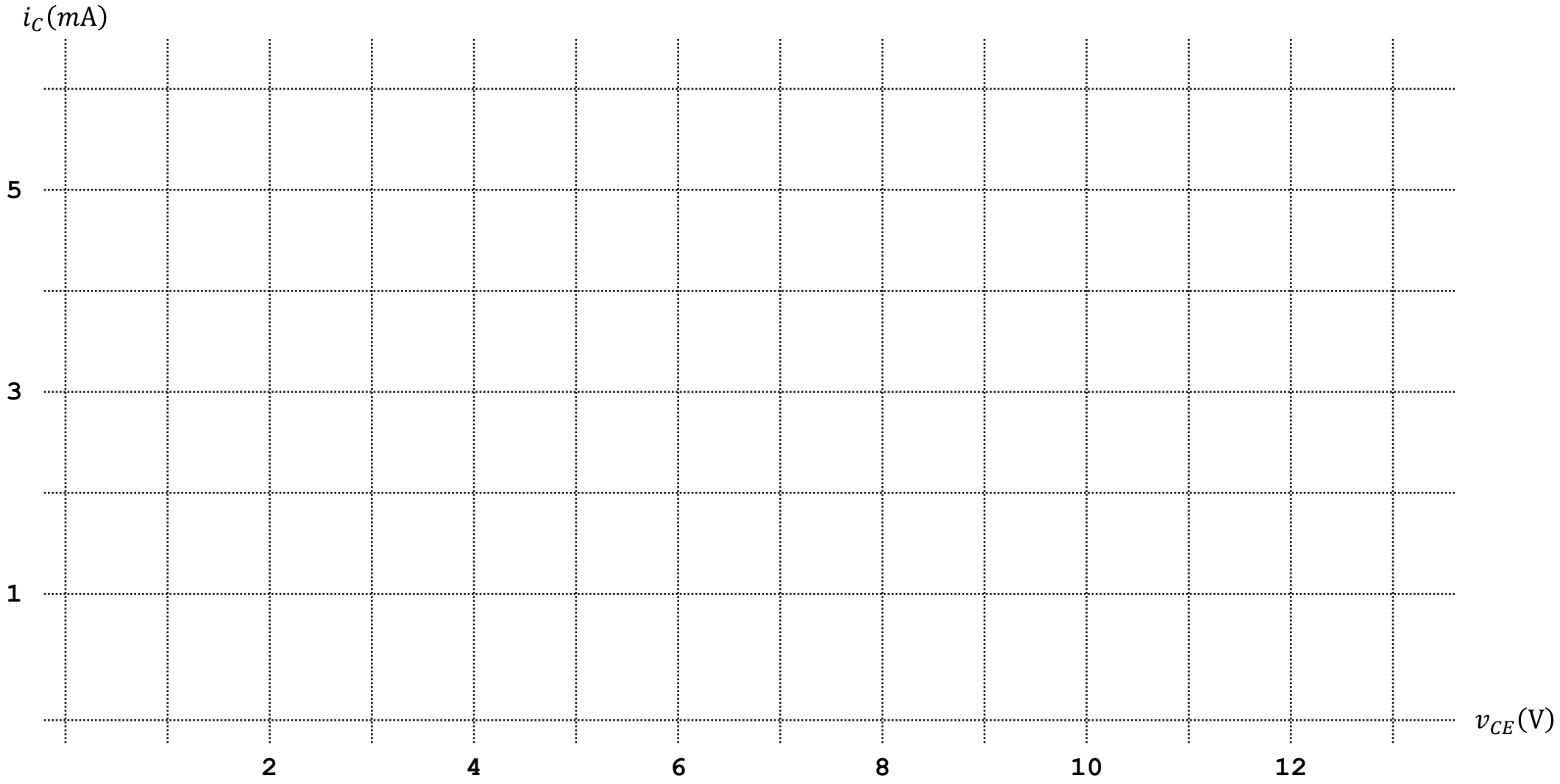


β=100

Solution

EXERCISE

Load Line Analysis



UNSTABLE Q-POINT

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{CE}$
Fixed-Bias					
Emitter-Stabilized					
Voltage-Divider Bias					

LABORATORY