HALF AND FULL ADDERS

COMBINATIONAL LOGIC CIRCUITS

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TOPIC OUTLINE

Half-Adder

Full-Adder

HALF-ADDER

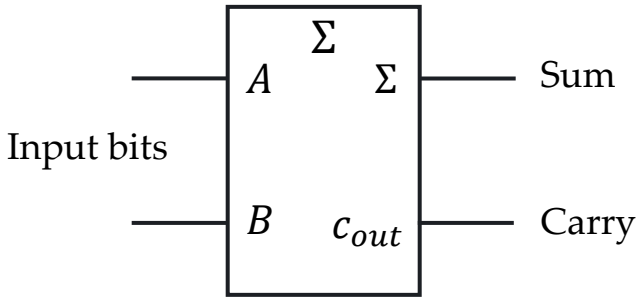
HALF-ADDER

The **half-adder** accepts two binary digits on its inputs and produces two binary digits on its outputs – a **sum bit** and a **carry bit**.

Truth Table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Logic Symbol



EXERCISE

Using the truth table of a half-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

Truth Table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

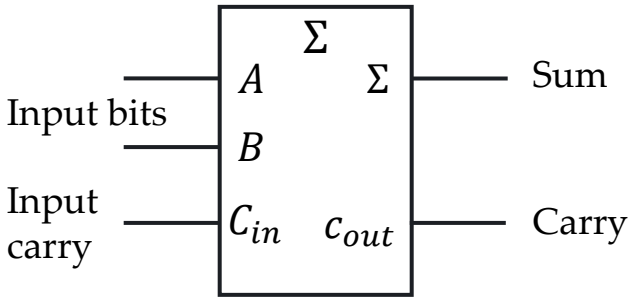
Solution

FULL-ADDER

FULL-ADDER

The **full-adder** accepts two input bits and an **input carry** and generates a sum output and an output carry.

Logic Symbol



Truth Table

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

EXERCISE

Using the truth table of a full-adder, derive and synthesize the minimized expressions for both the Sum and Carry outputs.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Solution

EXERCISE

Create a block-level representation of a 2-bit binary adder using full-adder modules.

Solution

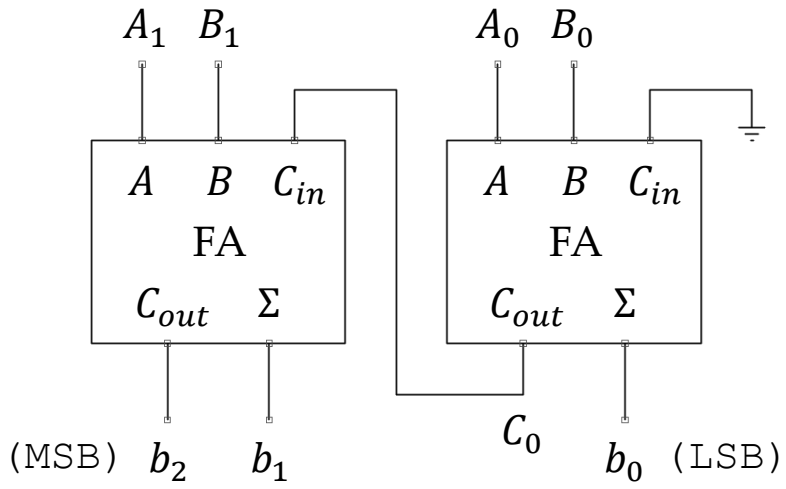
EXERCISE

Create a block-level representation of a 3-bit binary adder using full-adder modules.

Solution

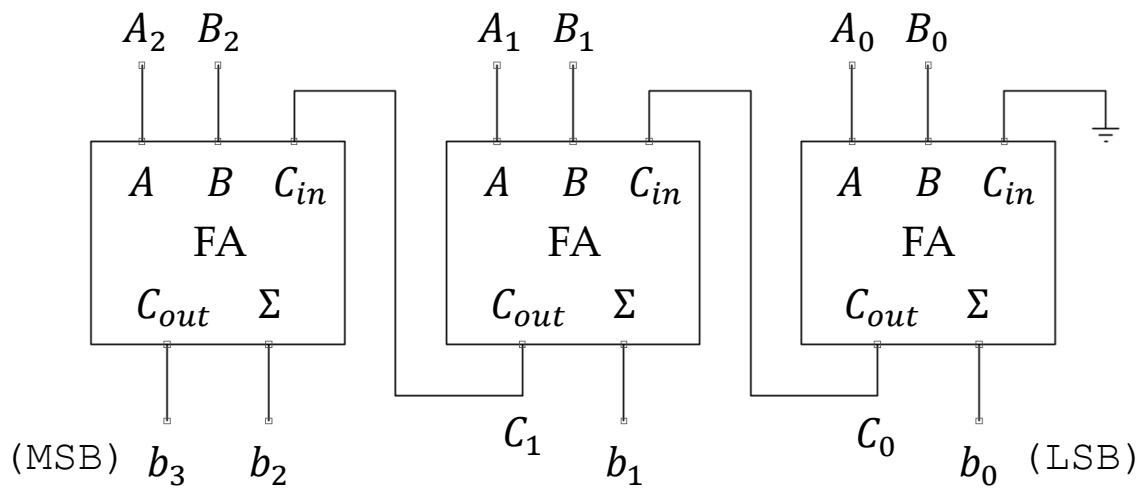
PARALLEL BINARY ADDERS

2-bit Parallel Adder



$$\begin{array}{r} C_1\ C_0 \\ A_1\ A_0 \\ B_1\ B_0 \\ \hline b_2\ b_1\ b_0 \end{array}$$

3-bit Parallel Adder



$$\begin{array}{r} C_2\ C_1\ C_0 \\ A_2\ A_1\ A_0 \\ B_2\ B_1\ B_0 \\ \hline b_3\ b_2\ b_1\ b_0 \end{array}$$

EXERCISE

Synthesize and implement a 2-bit parallel binary adder without utilizing XOR or XNOR gates.

Solution

LABORATORY