EMITTER-STABILIZED BIAS

BJT DC BIASING

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TOPIC OUTLINE

Emitter-Stabilized Bias Circuit

- **Base-Emitter Loop**
- **Collector-Emitter Loop**
- **Load Line Analysis**

EMITTER-STABILIZED BIAS CIRCUIT

CURRENT GAIN

The **current gain** parameters **alpha** (α) and **beta** (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

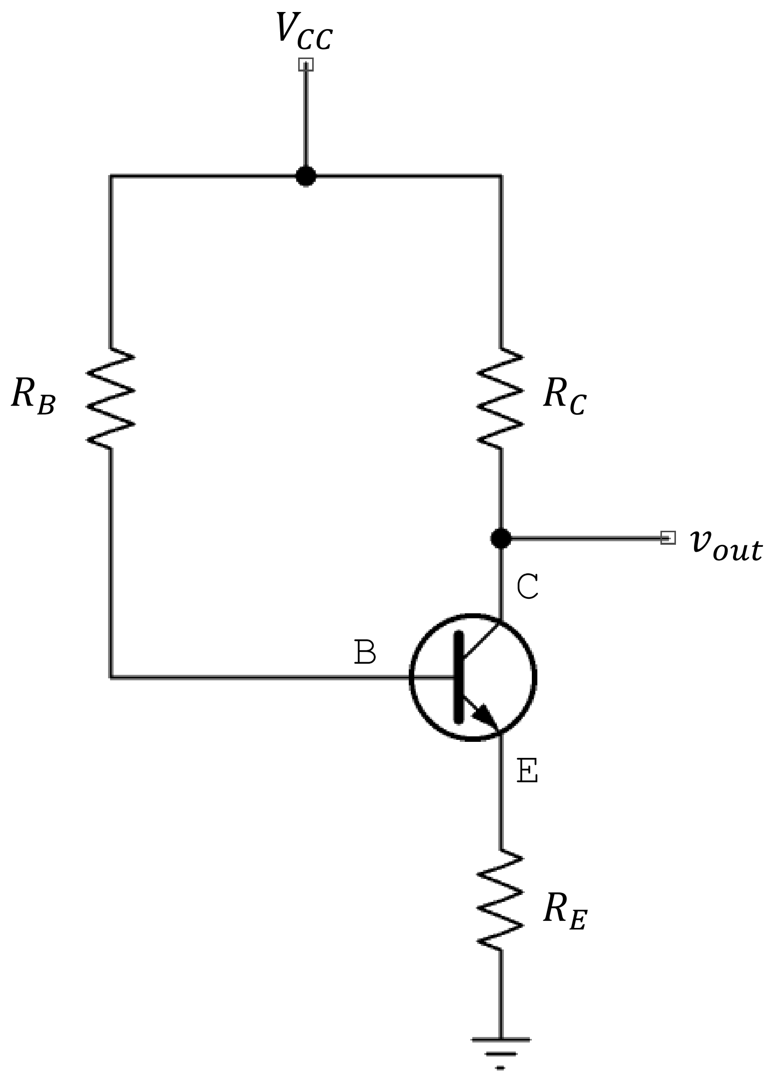
α is always less than 1 (typically 0.95 to 0.995)

Beta (β) is the ratio of the collector current to the base current.

Formula

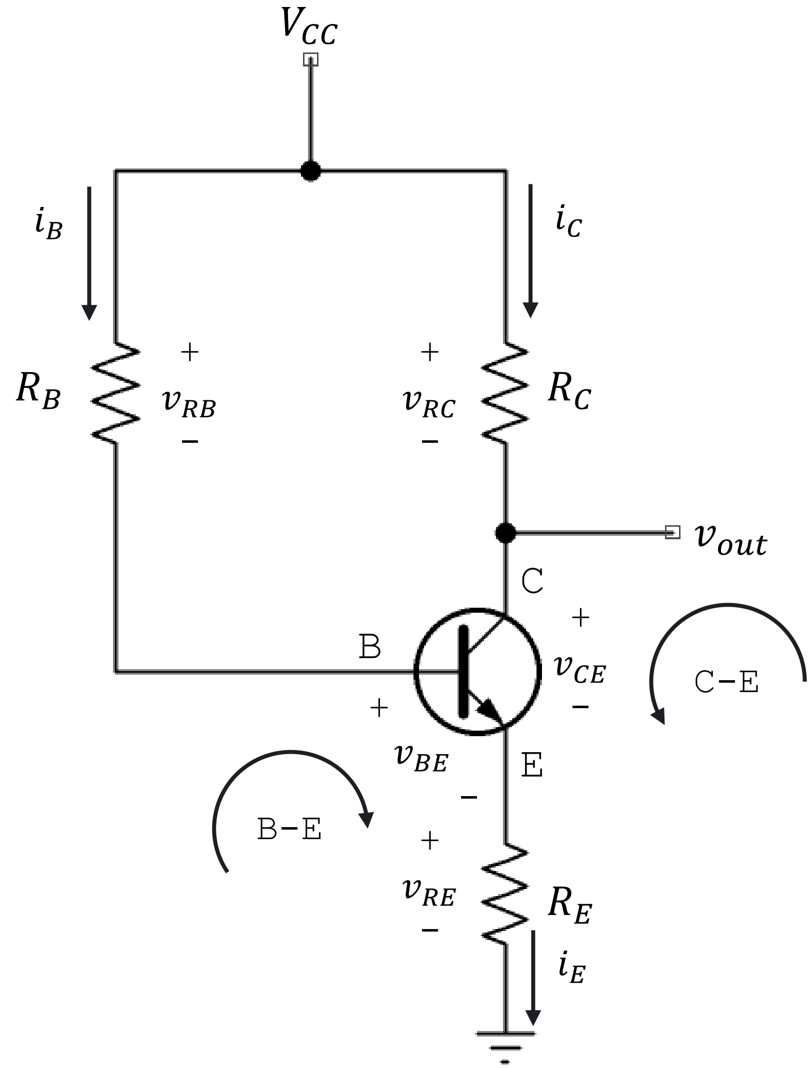
$$\beta = \frac{i_C}{i_B}$$

EMITTER-STABILIZED BIAS CIRCUIT



The **emitter-stabilized bias** is an improved biasing method by adding **resistor in the emitter** (R_E). This resistor introduces negative feedback, which helps stabilize the operating point against variations in temperature and transistor beta (β).

BASE-EMITTER LOOP



<u>KVL @B-E</u>

$$-v_{CC} + v_{RB} + v_{BE} + v_{RE} = 0$$

$$v_{RB} + v_{RE} = v_{CC} - v_{BE}$$

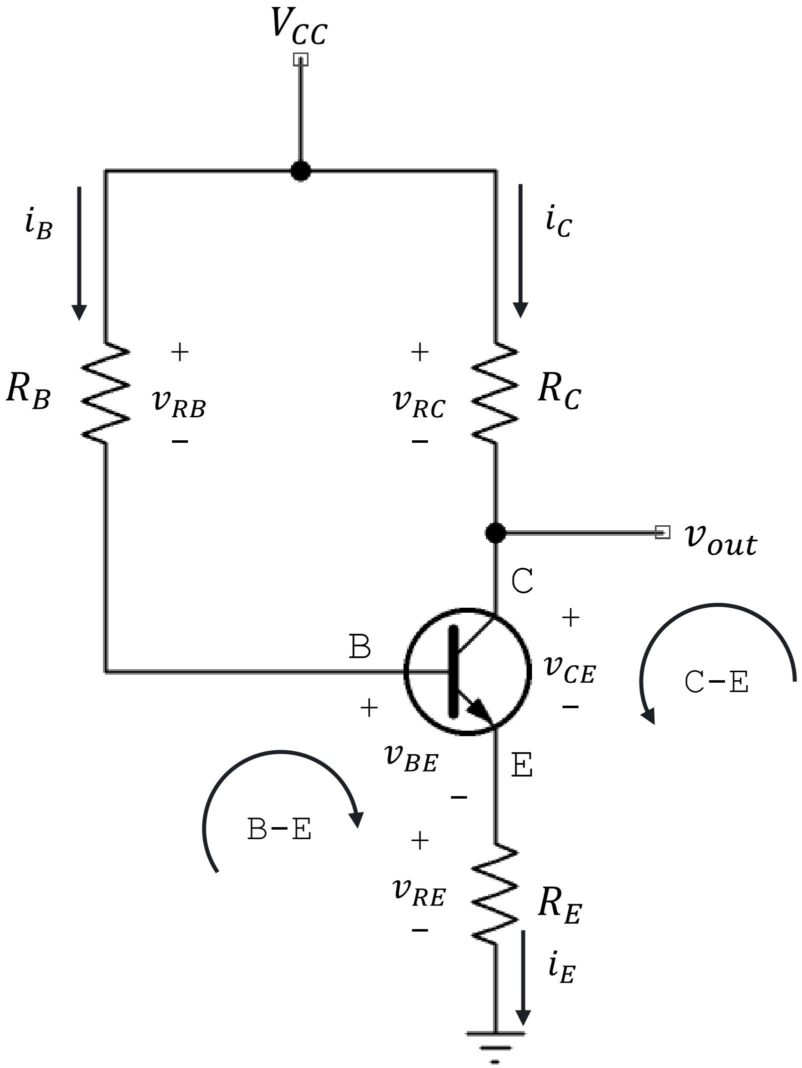
$$i_B R_B + i_E R_E = v_{CC} - v_{BE}$$

$$i_E = i_B + i_C$$

$$i_E = i_B + \beta i_B$$

$$i_E = i_B(\beta + 1)$$

BASE-EMITTER LOOP



KVL @B-E

$$-v_{CC} + v_{RB} + v_{BE} + v_{RE} = 0$$

$$v_{RB} + v_{RE} = v_{CC} - v_{BE}$$

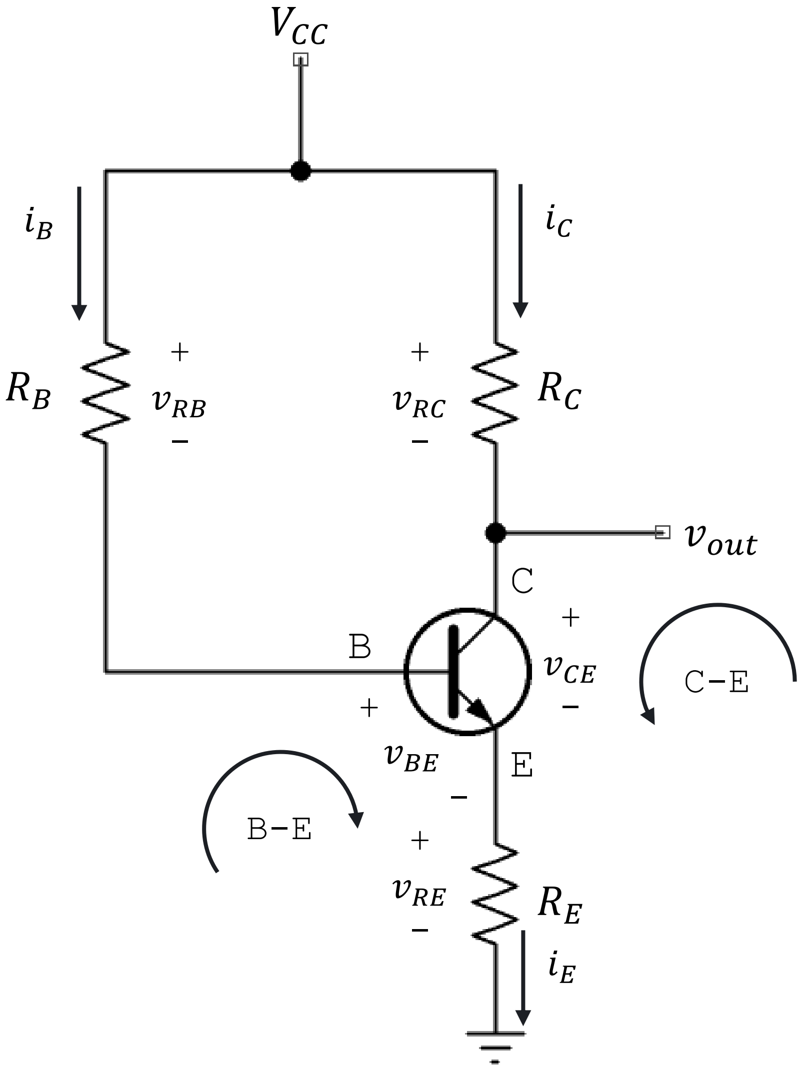
$$i_B R_B + i_E R_E = v_{CC} - v_{BE}$$

$$i_B R_B + i_B(\beta + 1)R_E = v_{CC} - v_{BE}$$

$$i_B(R_B + (\beta + 1)R_E) = v_{CC} - v_{BE}$$

$$i_B = \frac{v_{CC} - v_{BE}}{R_B + (\beta + 1)R_E}$$

COLLECTOR-EMITTER LOOP



<u>KVL @C-E</u>

$$-v_{CC} + v_{RC} + v_{CE} + v_{RE} = 0$$

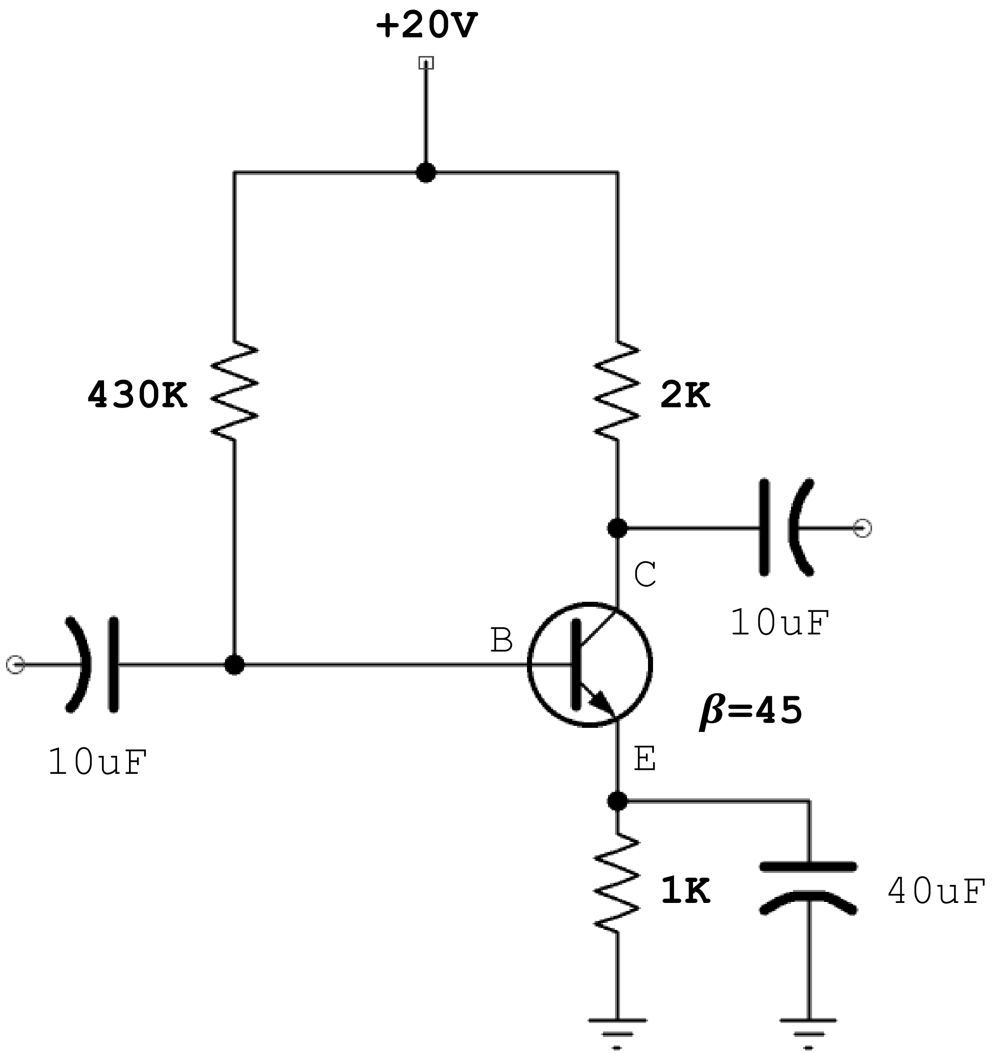
$$v_{CE} = v_{CC} - v_{RC} - v_{RE}$$

$$v_{CE} = v_{CC} - i_C R_C - i_E R_E$$

$$i_E \approx i_C$$

$$v_{CE} = v_{CC} - i_C(R_C + R_E)$$

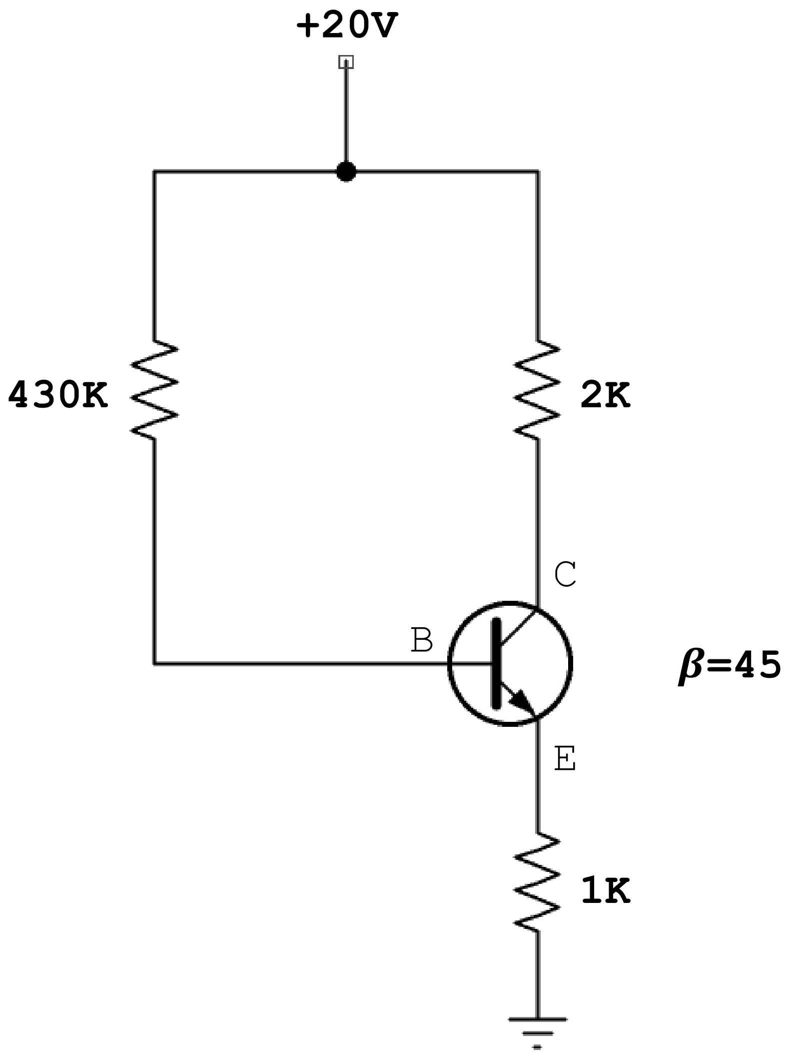
EXERCISE



For the given emitter-stabilized bias network, determine:

- Base current $\left(i_{BQ}\right)$
- Collector current $\left(i_{CQ}\right)$
- Collector-Emitter voltage $\left(v_{CEQ}\right)$
- Collector voltage $\left(v_C\right)$

EXERCISE



Solution

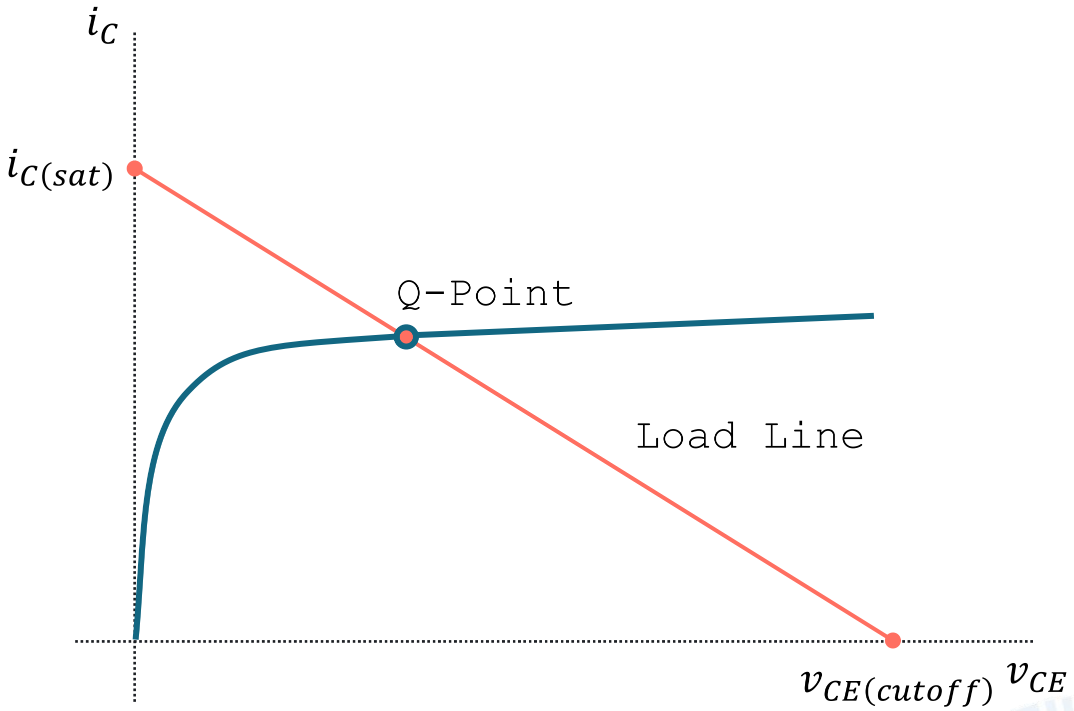
LOAD LINE ANALYSIS

SATURATION POINT

The **saturation point** is the operating state where BJT conducts the **maximum collector current** ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

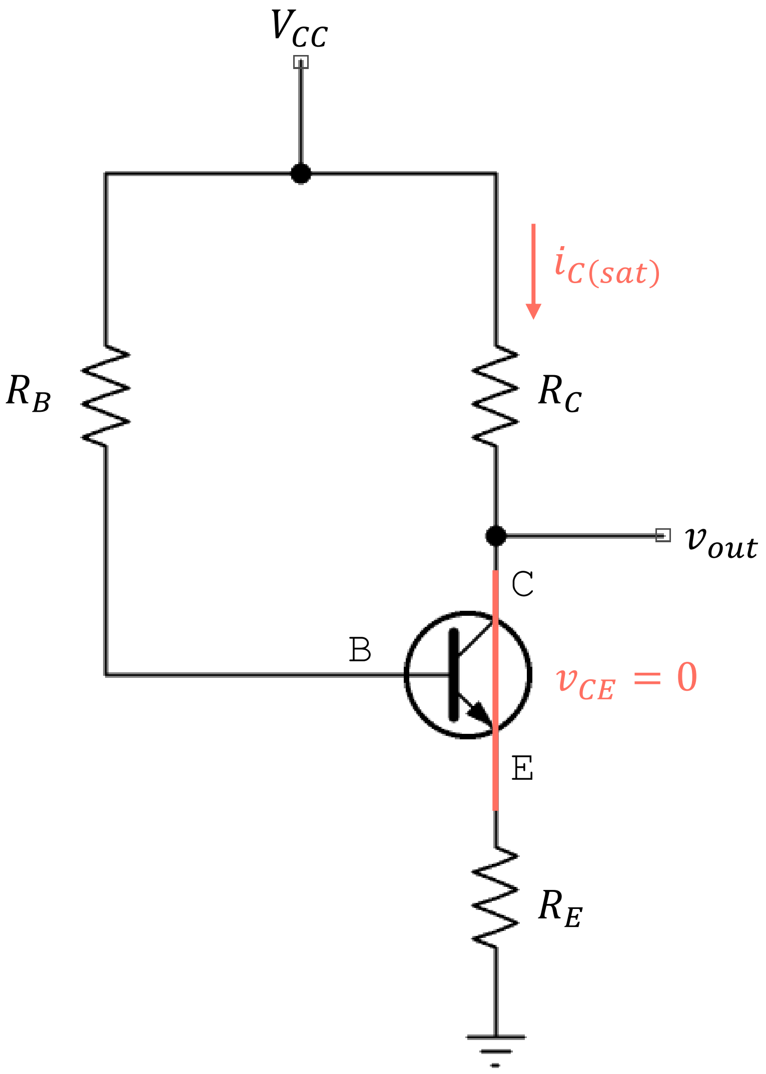
In this region the transistor acts like a **closed switch** (zero resistance between collector-emitter).

Collector Characteristic Curve

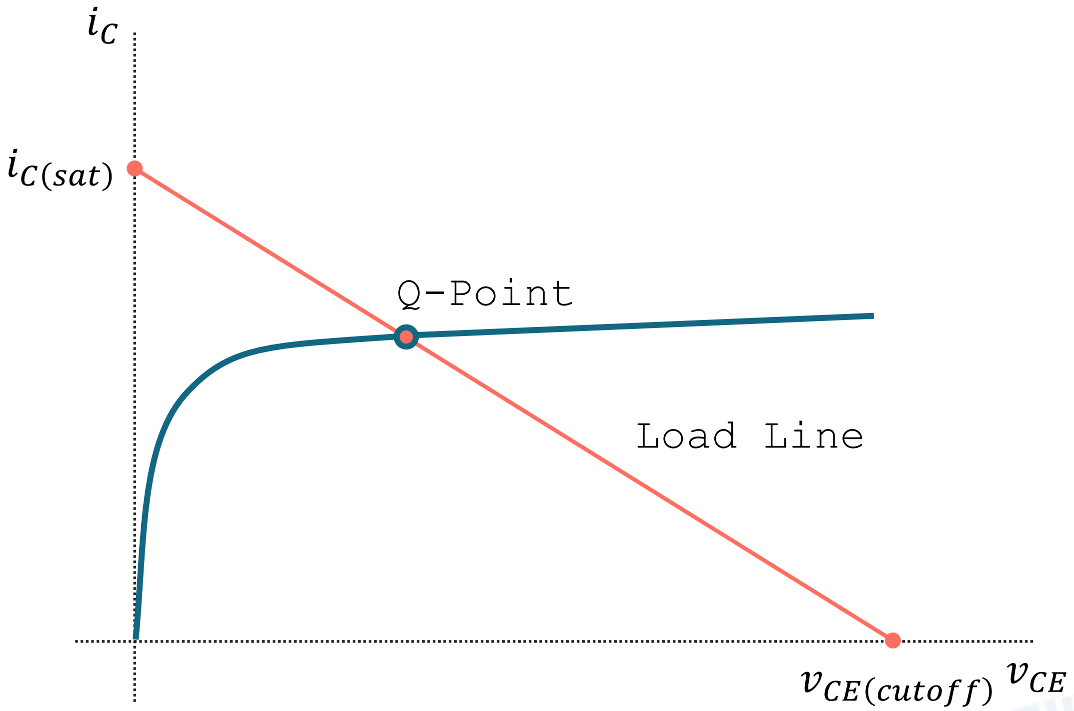


SATURATION POINT

Mentally Short



Collector Characteristic Curve

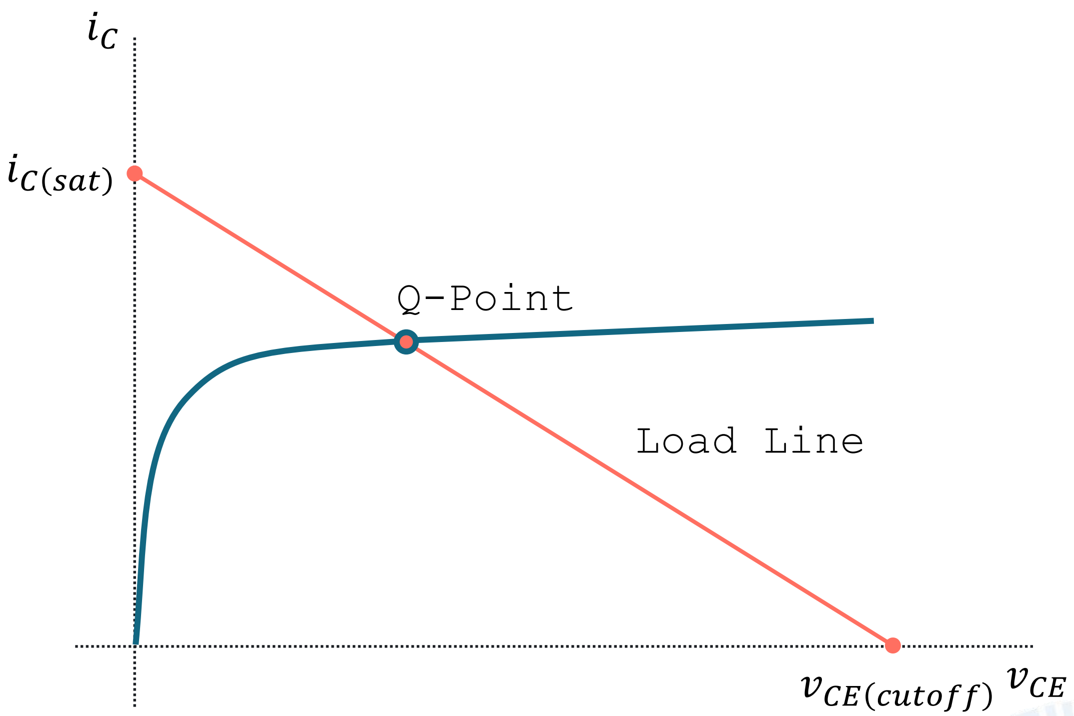


CUTOFF POINT

The **cutoff point** is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

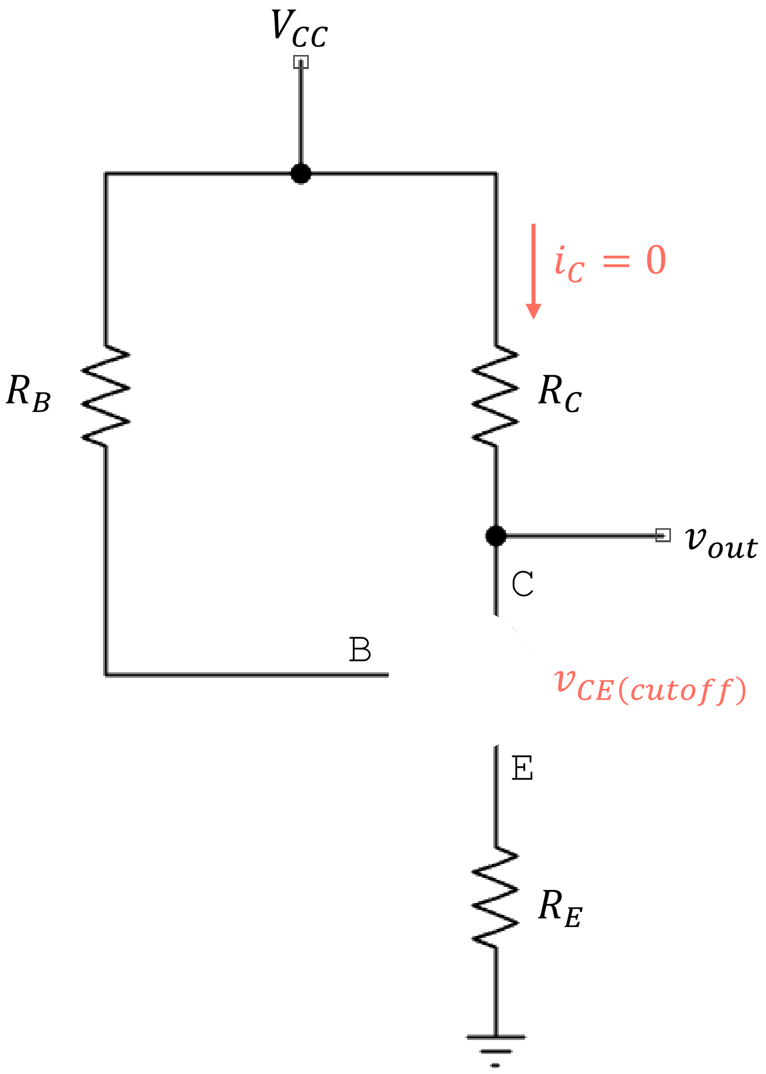
In this region the transistor acts like an **open switch** (infinite resistance between collector-emitter).

Collector Characteristic Curve

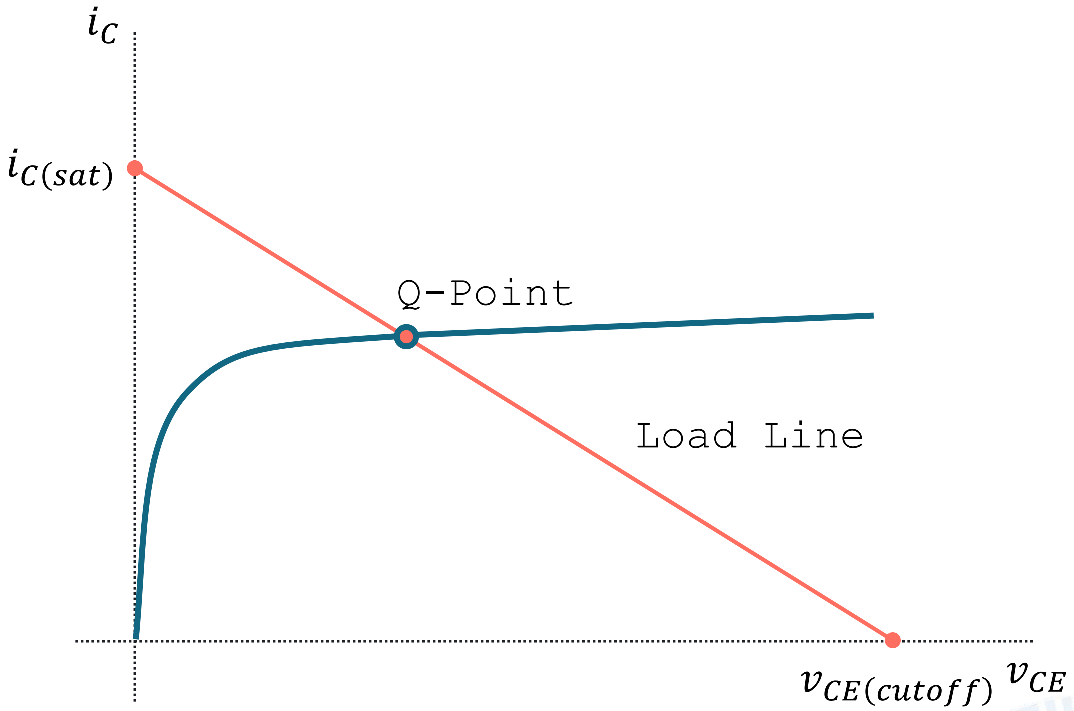


CUTOFF POINT

Mentally Open



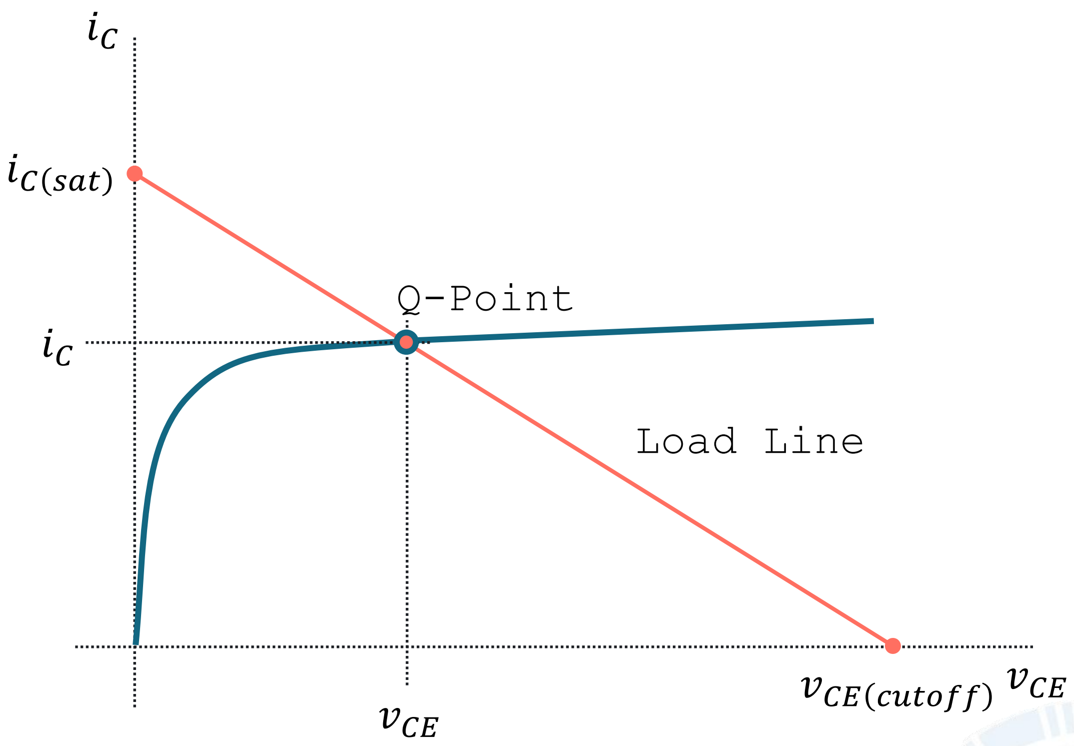
Collector Characteristic Curve



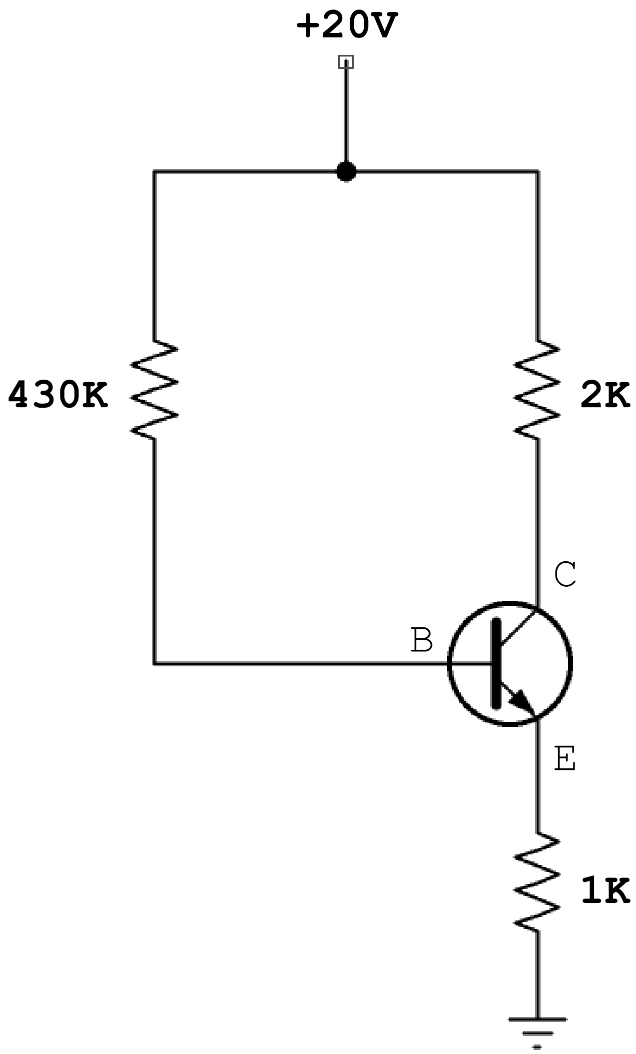
QUIESCENT POINT

The **Q-point** is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}).

Collector Characteristic Curve



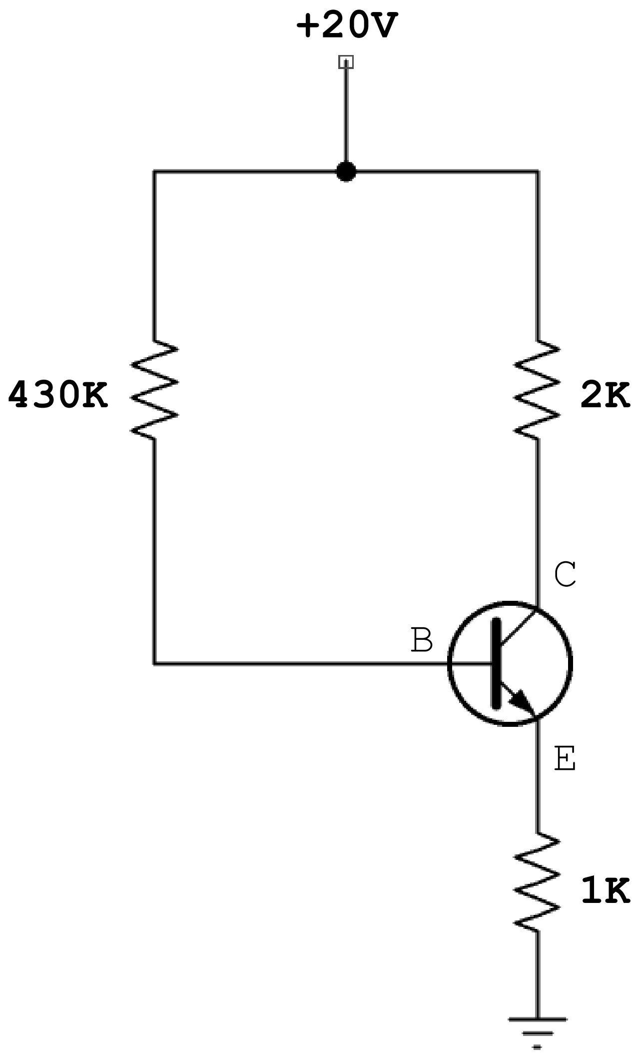
EXERCISE



Plot the DC load line analysis for the emitter-stabilized bias network, indicating:

- Saturation current ($i_{C(sat)}$)
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

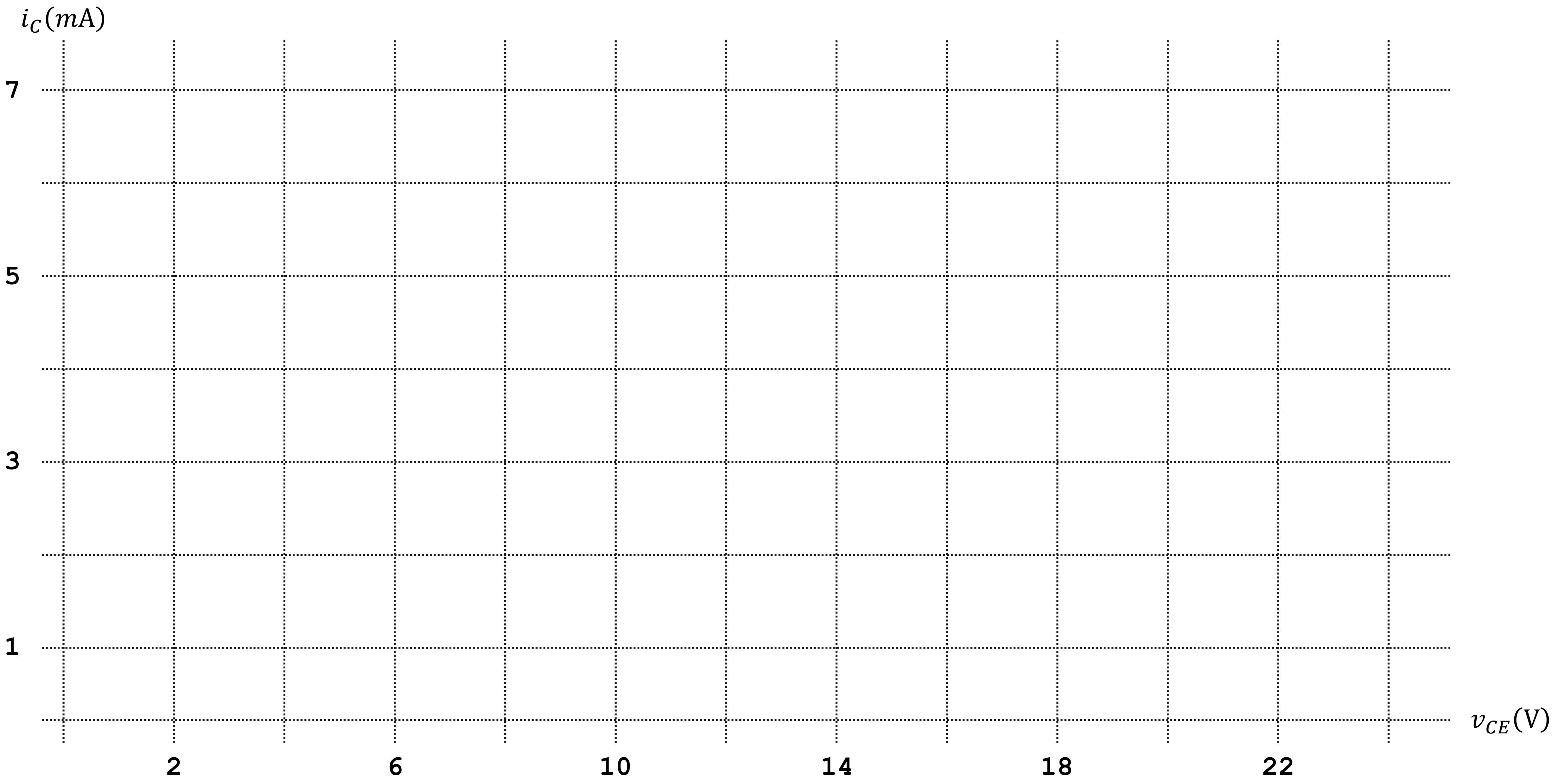
EXERCISE



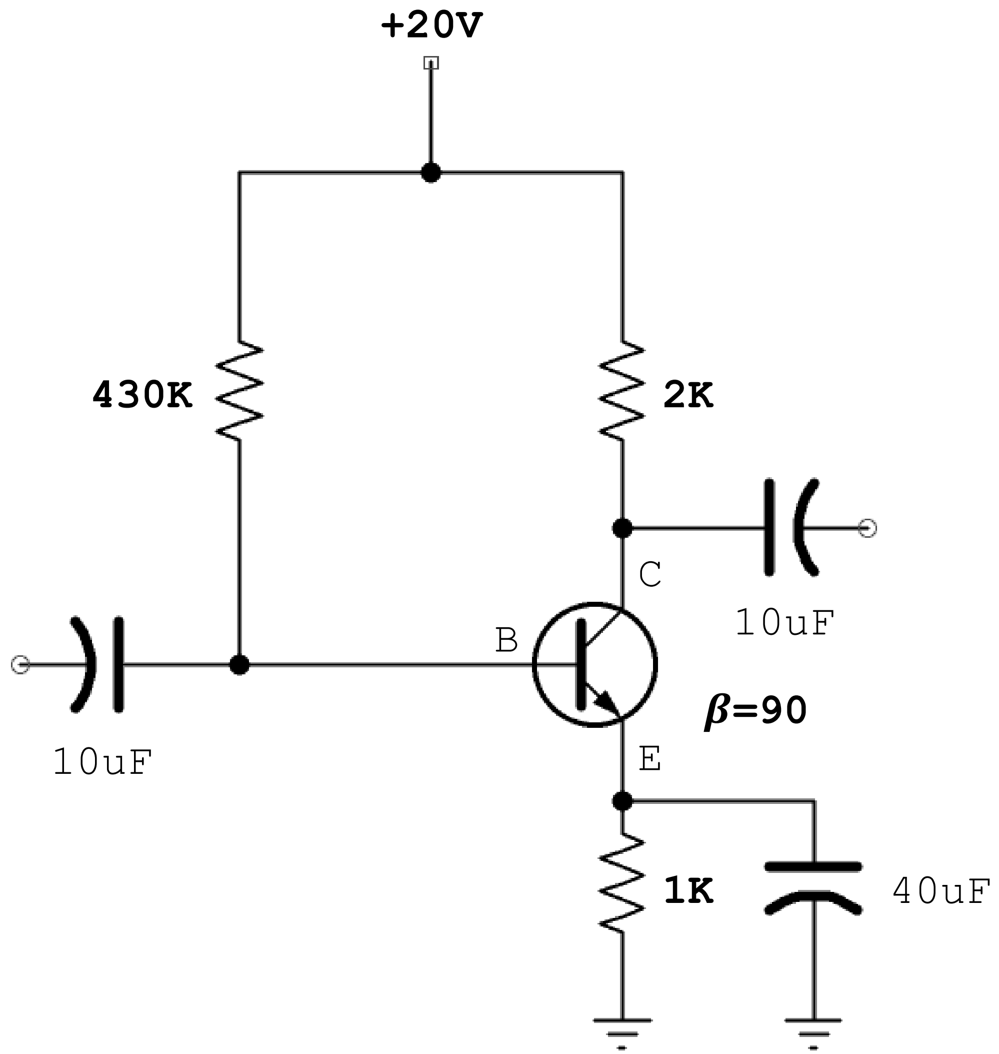
Solution

EXERCISE

Load Line Analysis



EXERCISE



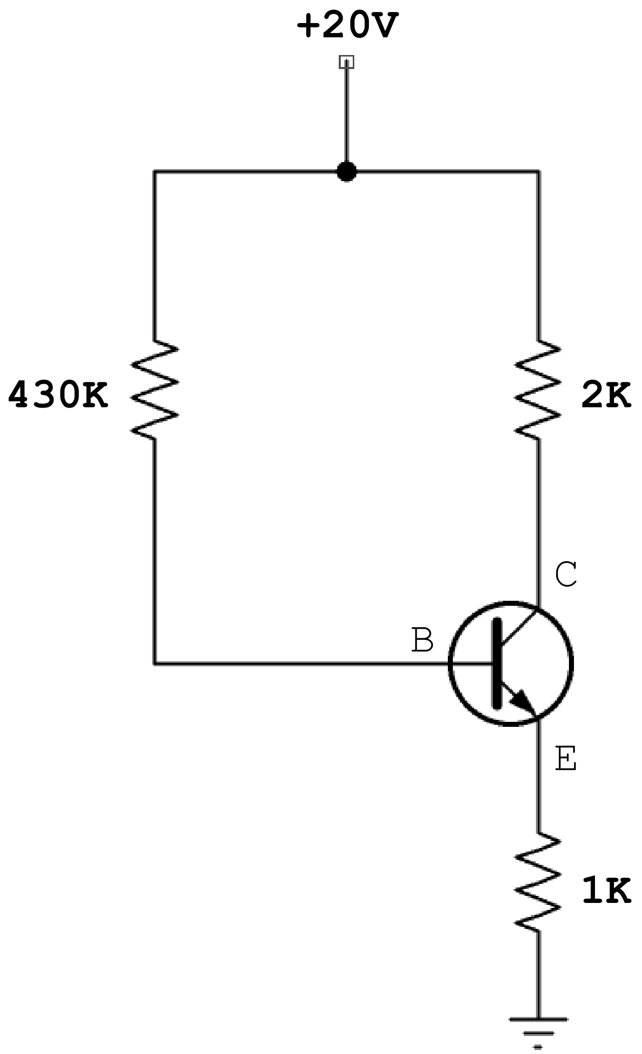
For the given emitter-stabilized bias network, determine:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})
- Emitter voltage (v_E)

and plot the DC load line analysis indicating:

- Saturation current $(i_{C(sat)})$
- Cutoff voltage $(v_{CE(cutoff)})$
- Operating Point (Q-Point)

EXERCISE

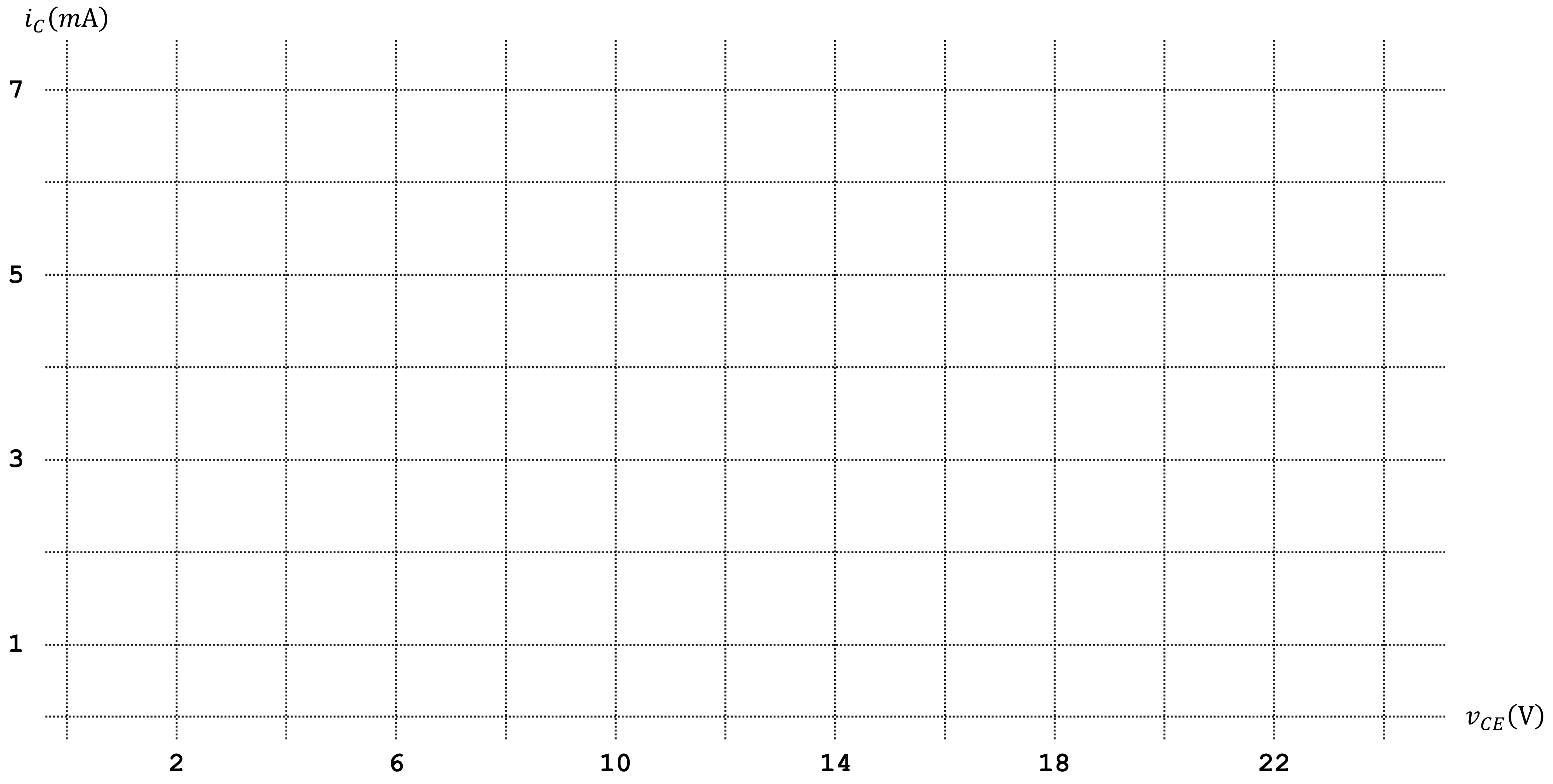


β=90

Solution

EXERCISE

Load Line Analysis



IMPROVE STABILITY

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{CE}$
Fixed-Bias	50	47.08	2.35	6.83	-76%
	100	47.08	4.71	1.64	
Emitter-Stabilized					
Voltage-Divider Bias					

LABORATORY