KIRCHHOFF'S CURRENT AND VOLTAGE LAW

BASIC CIRCUIT ANALYSIS METHOD

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TOPIC OUTLINE

Circuit Convention

Kirchhoff's Current Law (KCL)

Kirchhoff's Voltage Law (KVL)

CIRCUIT CONVENTION

CONVENTION

A **convention** is a widely accepted practice, method, or behavior that is followed by common **agreement** or tradition, rather than by formal rules.

example

Color coding in Offices

red – urgent documents
blue – general files
green – financial records

This is a common practice but not formally regulated.

STANDARD

A **standard** is a formal, established guideline, rule, or specification that is often **mandatory** and enforced by an authoritative body or organization.

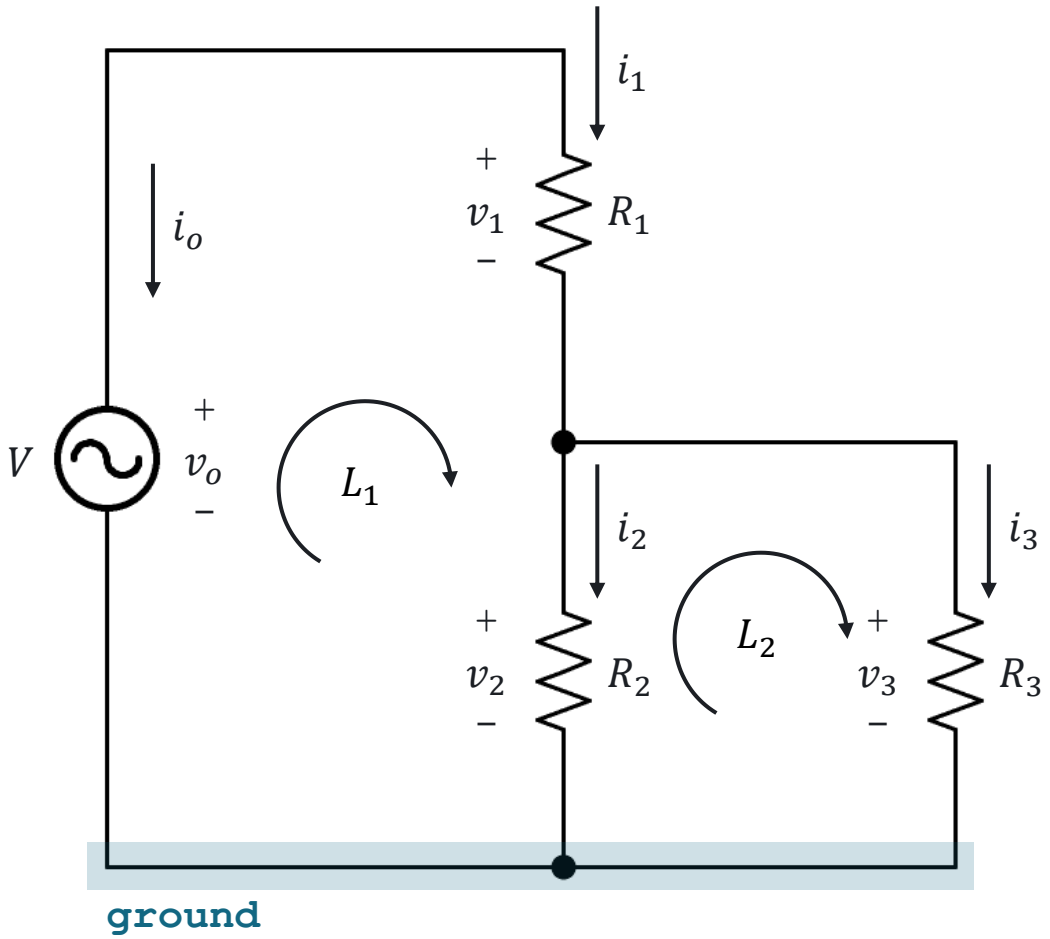
example

IEC 60062 Resistor Color Code

black – 0
brown – 1
red – 2
.
.
.
white – 9

Resistors have colored bands that represent specific digits, multipliers, and tolerance values.

LABELING VARIABLES



Steps in Labeling Variables

1. **Label the Reference Node** `(ground)`

Select a reference node with the most connections or the negative `(−)` terminal of a voltage source.

2. **Label Node Voltages**

Mark higher potentials as positive `(+)` relative to the reference node.

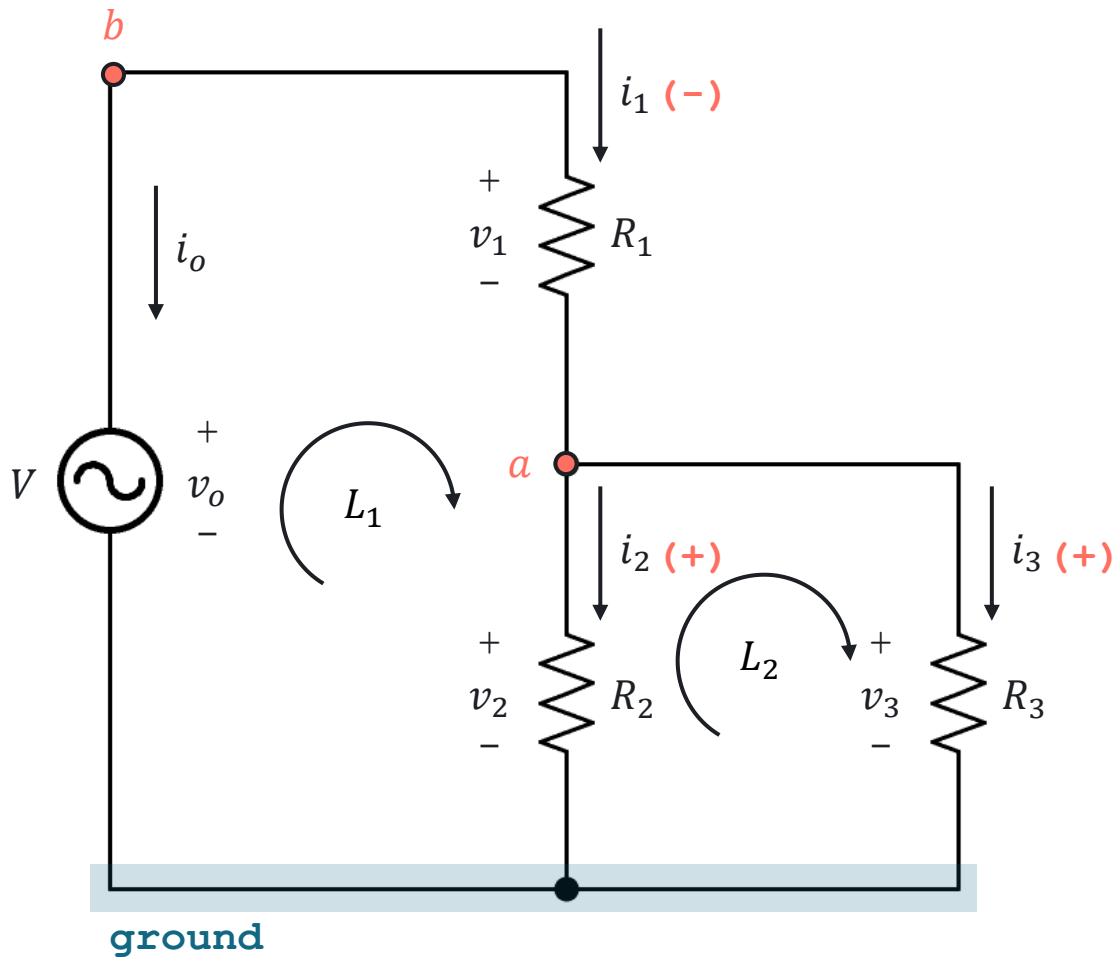
3. **Label Currents**

Entering the positive `(+)` terminal of a component.

4. **Create a voltage loop**

Follow the defined current directions.

CIRCUIT CONVENTION

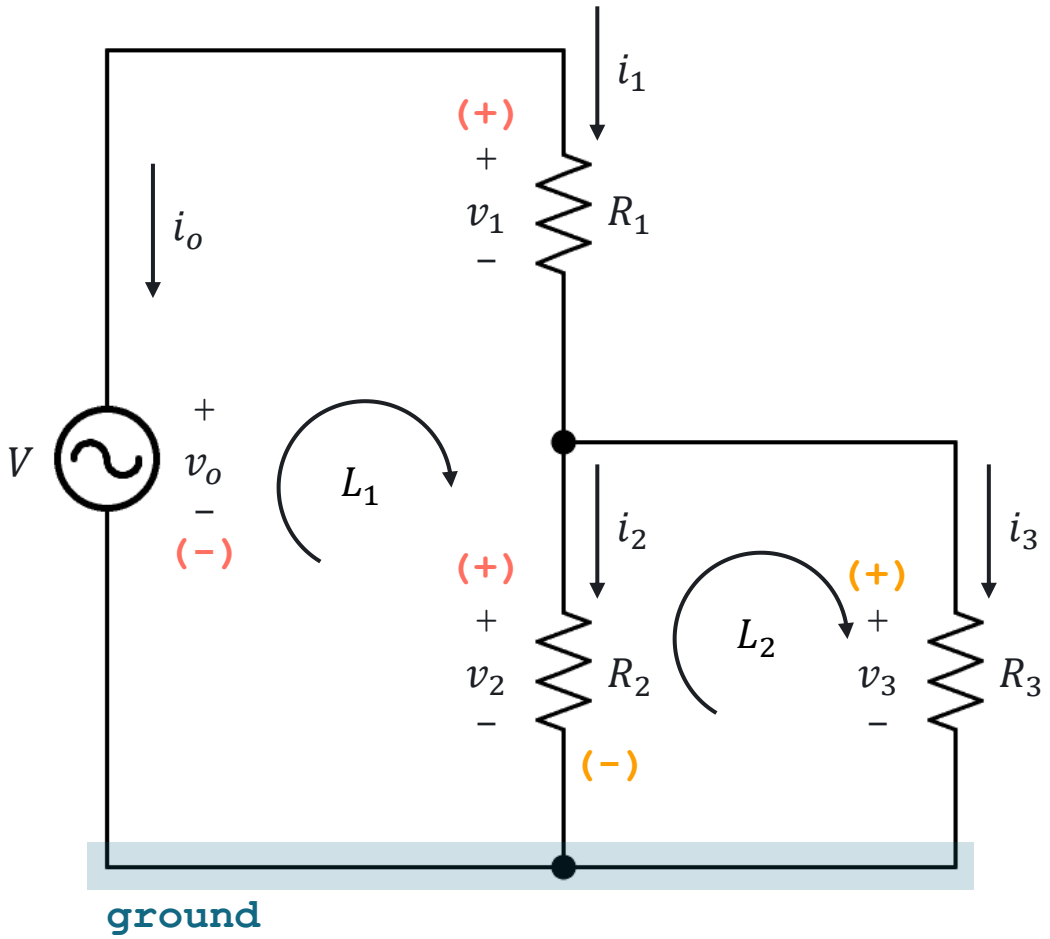


Current Flow Convention

- Current **entering** a node is negative **(−)**
- Current **leaving** a node is positive **(+)**

@***a***	@***b***
$-i_1$	$+i_o$
$+i_2$	$+i_1$
$+i_3$	

CIRCUIT CONVENTION



Voltage Loop Convention

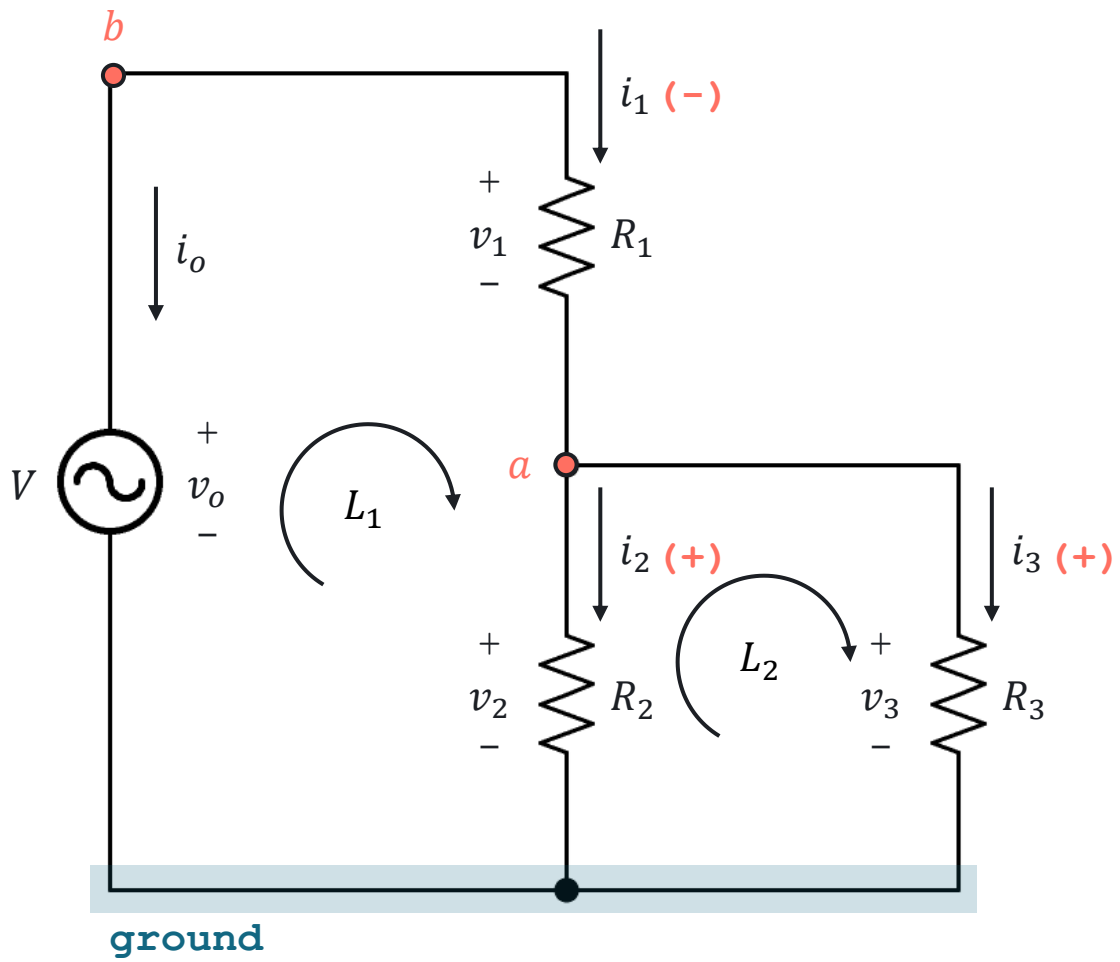
The "sign" of voltage of the element is the first sign the loop encounters.

@L_1	@L_2
$-v_o$	$-v_2$
$+v_1$	$+v_3$
$+v_2$	

KIRCHHOFF'S

CURRENT AND VOLTAGE LAW

KIRCHHOFF'S CURRENT LAW



Kirchhoff's current law states that summation of currents going-in and going-out a node is zero.

$$\sum i_j = 0$$

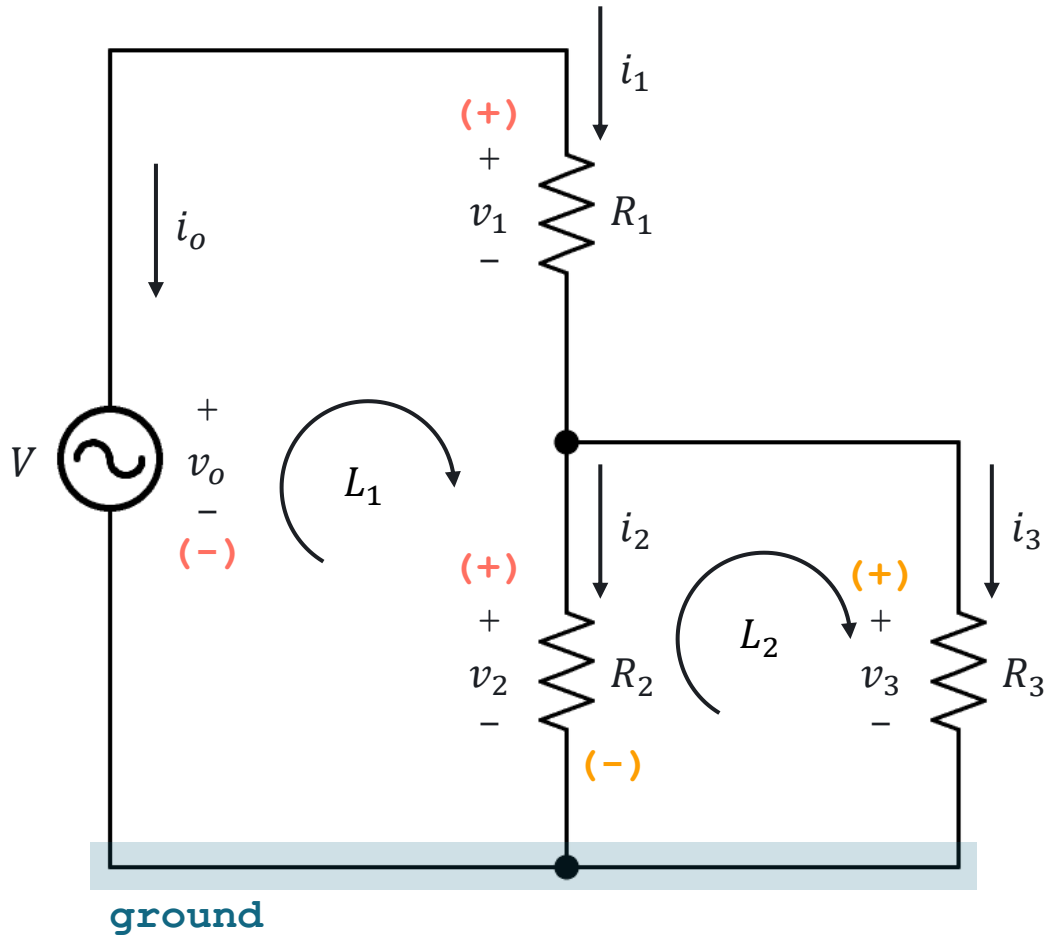
KCL @a

$$-i_1 + i_2 + i_3 = 0$$

KCL @b

$$i_o + i_1 = 0$$

KIRCHHOFF'S VOLTAGE LAW



Kirchhoff's voltage law states that the summation of voltages in a closed-loop is zero.

$$\sum v_j = 0$$

KVL @L_1

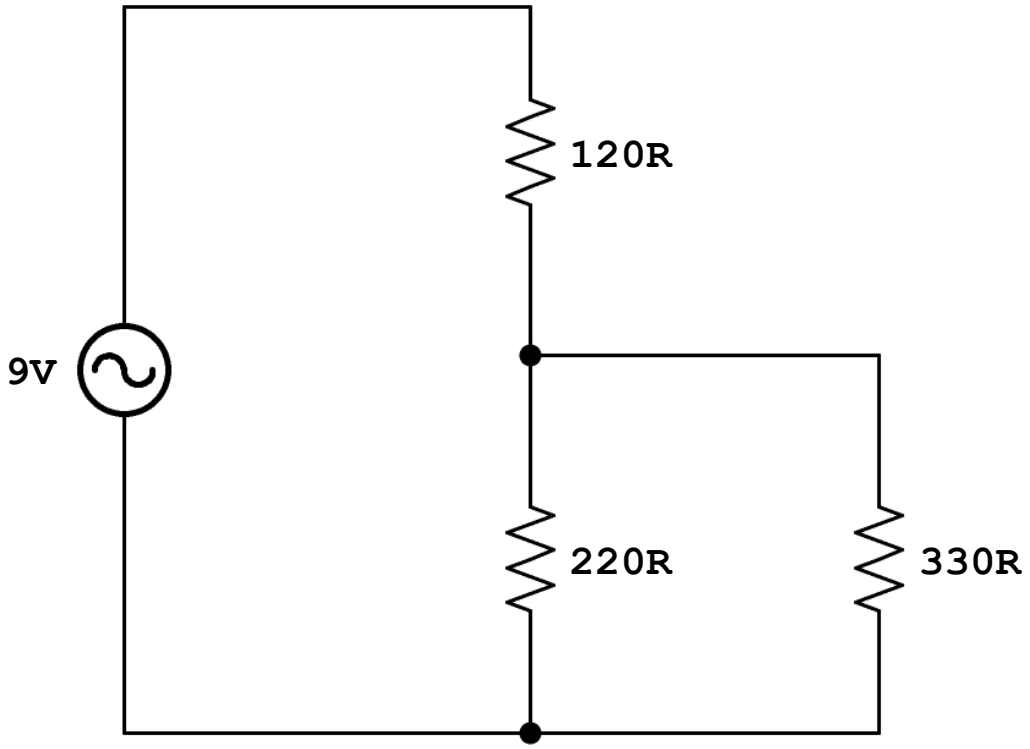
$$-v_o + v_1 + v_2 = 0$$

KVL @L_2

$$-v_2 + v_3 = 0$$

EXERCISE

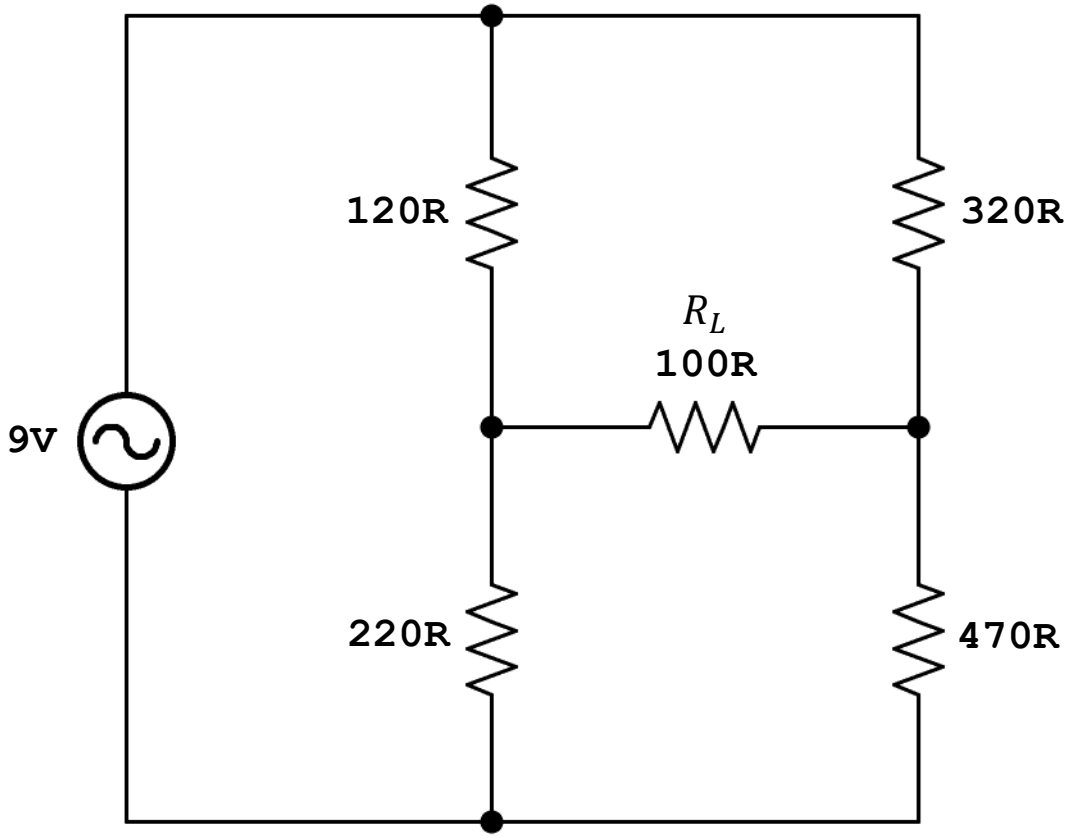
Analyze the given circuit to determine both the current through and the voltage drop across each resistor.



Solution

EXERCISE

Determine the voltage drop across the load resistor and the current flowing through it.



Solution

LABORATORY