EMITTER-STABILIZED BIAS

BJT DC BIASING

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TOPIC OUTLINE

Emitter-Stabilized Bias Circuit

- Base-Emitter Loop
- Collector-Emitter Loop
- Load Line Analysis

EMITTER-STABILIZED BIAS CIRCUIT

CURRENT GAIN

The current gain parameters **alpha** (α) and **beta** (β) describe the relationship between currents in the transistor's three terminals (emitter, base, and collector).

Alpha (α) is the ratio of the collector current to the emitter current.

Formula

$$\alpha = \frac{i_C}{i_E}$$

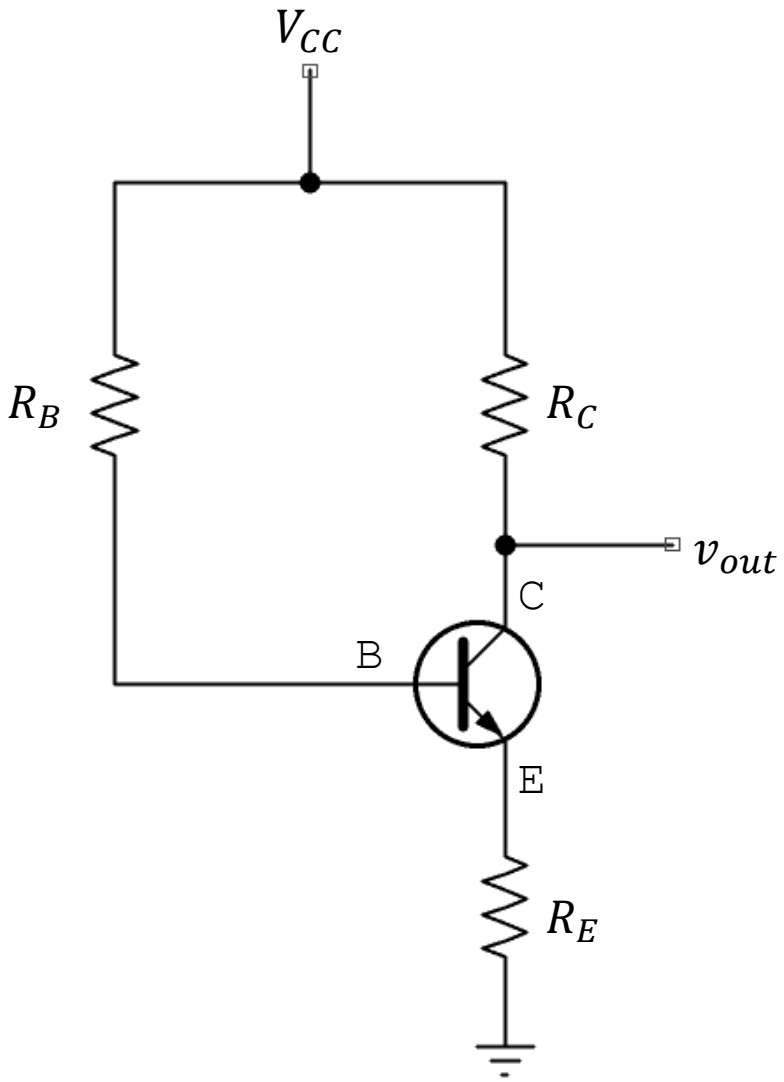
α is always less than 1 (typically 0.95 to 0.995)

Beta (β) is the ratio of the collector current to the base current.

Formula

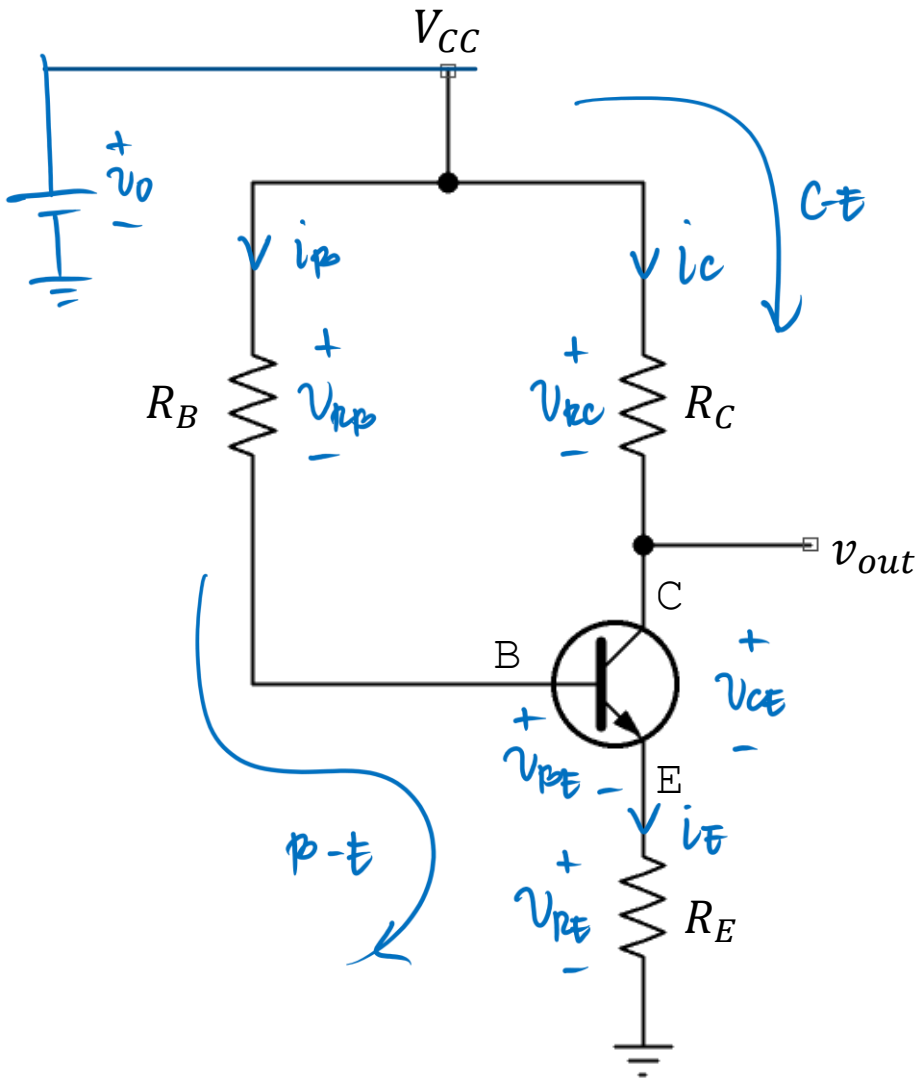
$$\beta = \frac{i_C}{i_B}$$

EMITTER-STABILIZED BIAS CIRCUIT



The **emitter-stabilized bias** is an improved biasing method by adding **resistor in the emitter** (R_E). This resistor introduces negative feedback, which helps stabilize the operating point against variations in temperature and transistor beta (β).

BASE-EMITTER LOOP



KVL @B-E

V_{CC}

$$-v_o + v_{RB} + v_{BE} + v_{RE} = 0$$

$$v_{RB} + v_{RE} = V_{CC} - v_{BE}$$

$$i_B R_B + i_E R_E = V_{CC} - v_{BE}$$

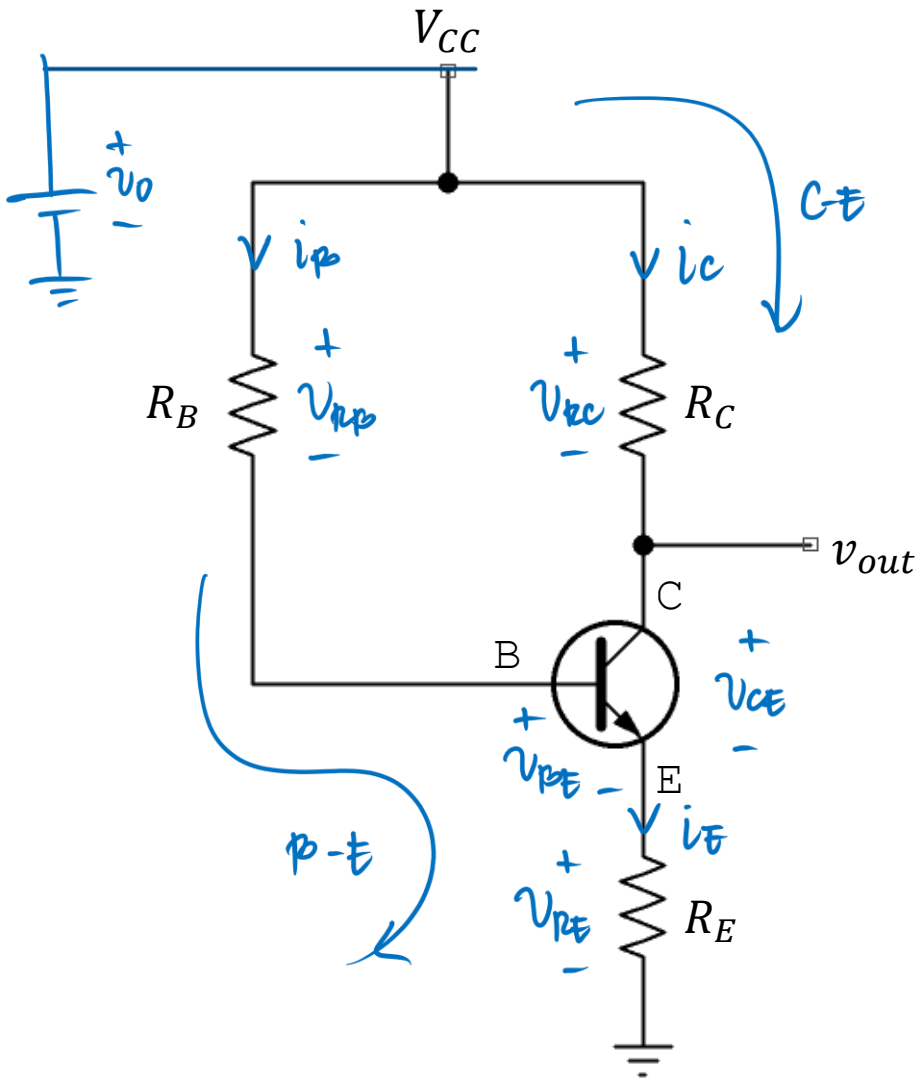
$$i_E = i_B + i_C \longrightarrow \beta = \frac{i_C}{i_B}$$

$$i_E = i_B + \beta i_B \qquad i_C = \beta i_B$$

$$i_E = i_B(\beta + 1)$$

$$i_B R_B + i_B(\beta+1) R_E = V_{CC} - v_{BE}$$

BASE-EMITTER LOOP



KVL @B-E

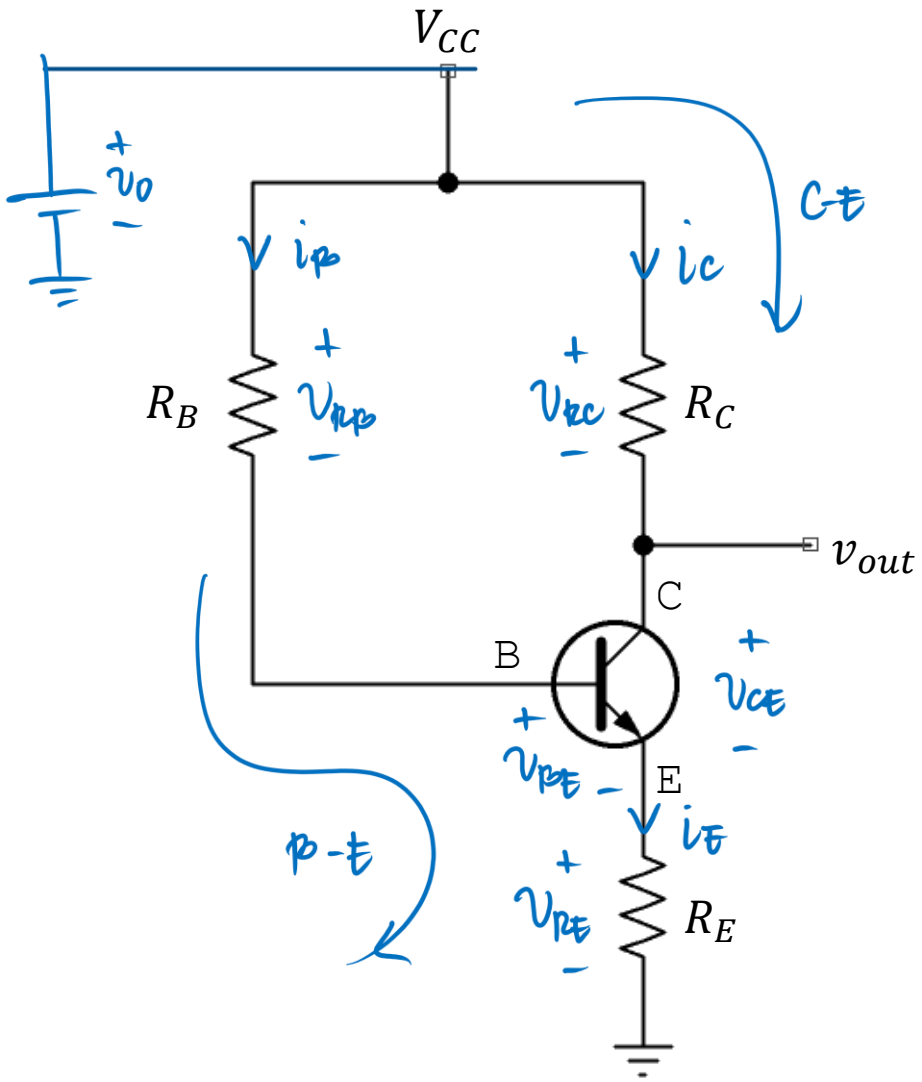
$$i_B R_B + i_B(\beta+1)R_E = V_{CC} - v_{BE}$$

$$i_B\left[R_B + (\beta+1)R_E\right] = V_{CC} - v_{BE}$$

$$i_B = \frac{V_{CC} - v_{BE}}{R_B + (\beta+1)R_E}$$

Emitter-stabilized bias

COLLECTOR-EMITTER LOOP



KVL @C-E

$$-v_{CC} + v_{R_C} + v_{CE} + v_{R_E} = 0$$

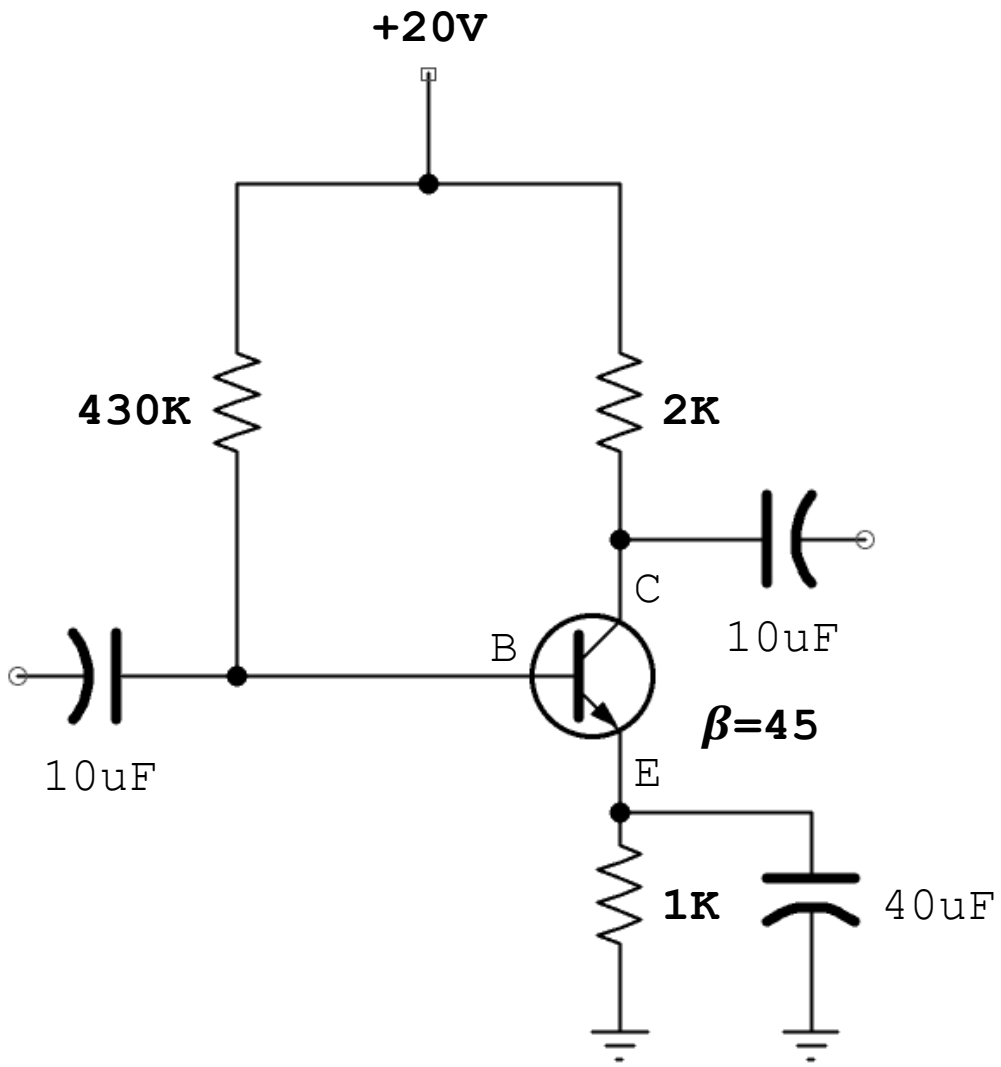
$$v_{CE} = V_{CC} - v_{R_C} - v_{R_E}$$

$$v_{CE} = V_{CC} - i_C R_C - i_E R_E \rightarrow i_C \approx i_E$$

$$\boxed{v_{CE} = V_{CC} - i_C (R_C + R_E)}$$

Emitter-stabilized bias

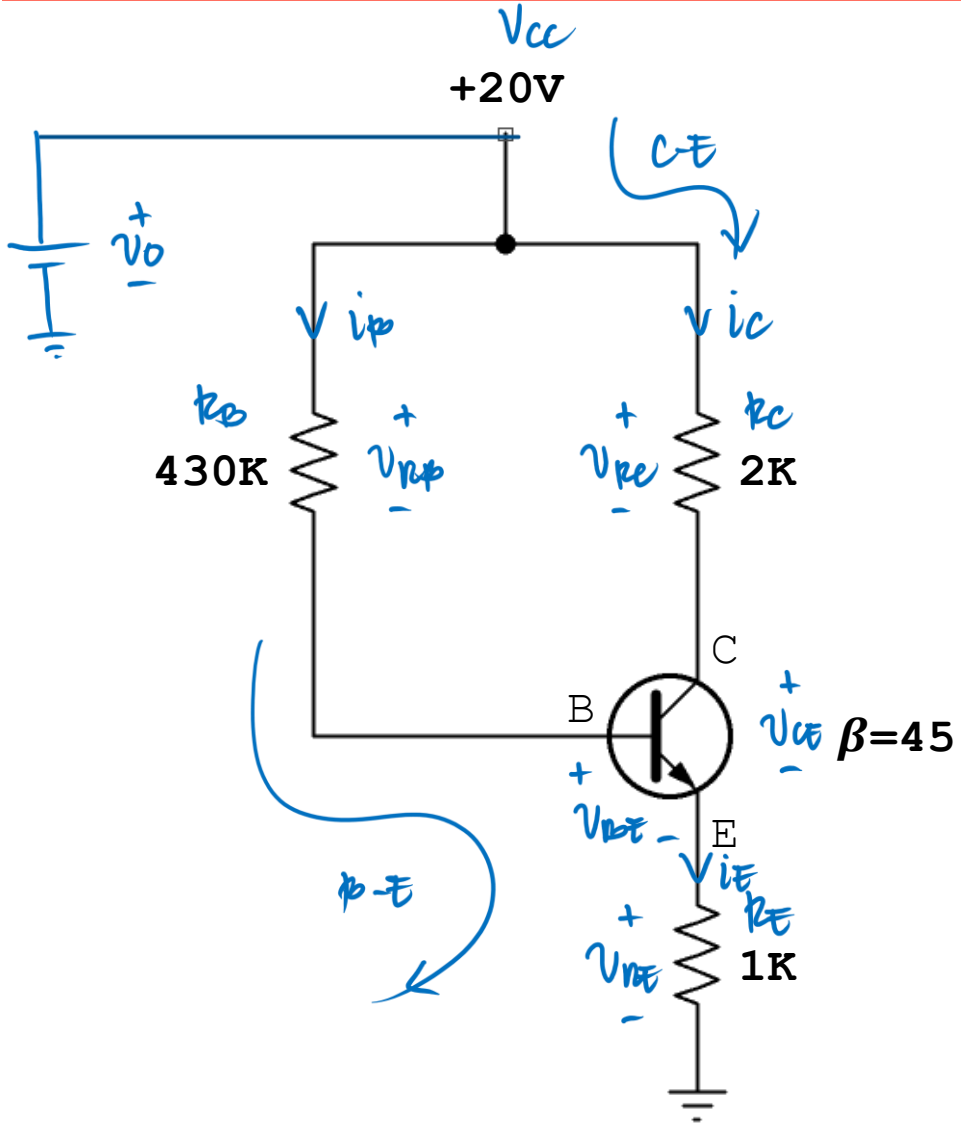
EXERCISE



For the given emitter-stabilized bias network, determine:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})
- Collector voltage (v_C)

EXERCISE



Solution

KVL @ B-E

$-V_{cc} + V_{RB} + V_{BE} + V_{RE} = 0$

$V_{RB} + V_{RE} = V_{cc} - V_{BE}$

$i_B R_B + i_E R_E = V_{cc} - V_{BE}$

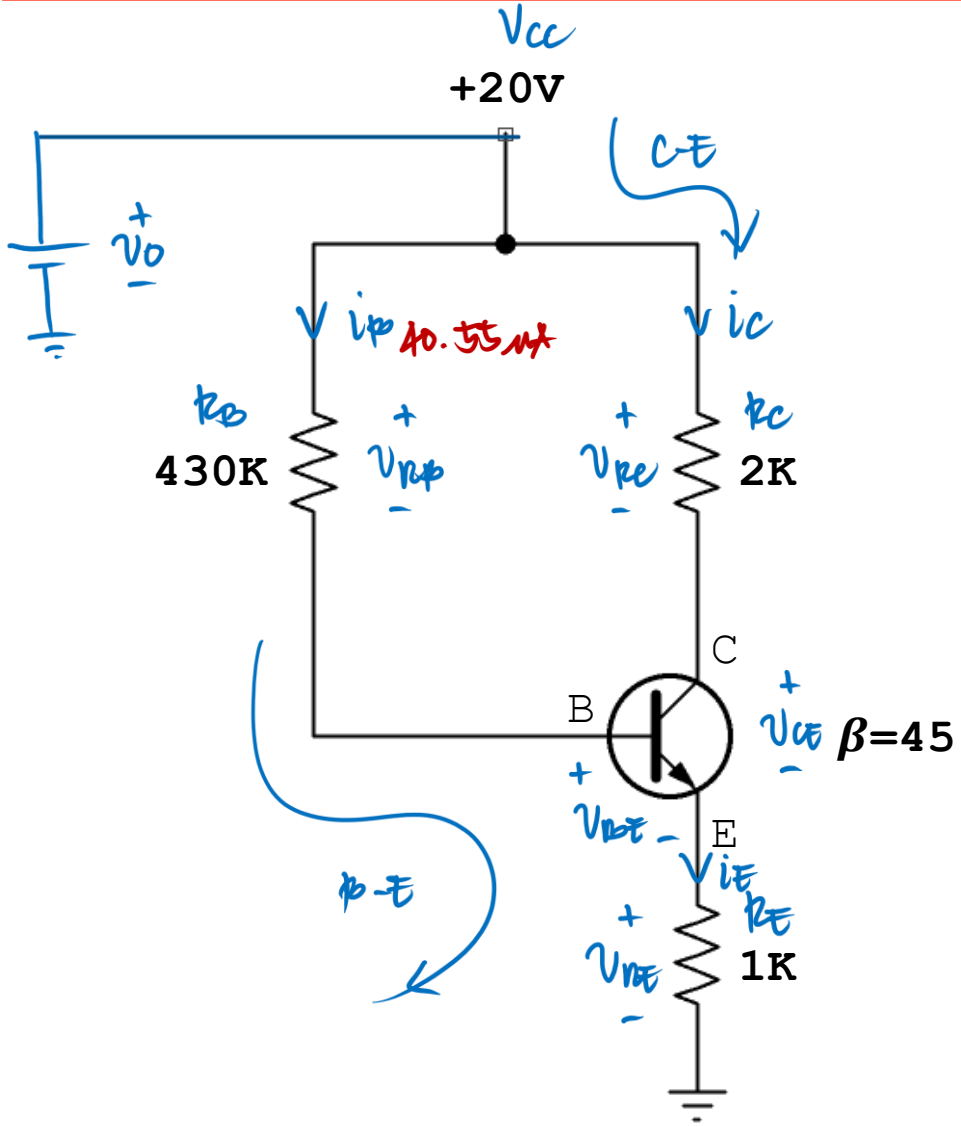
$i_E = i_B + i_C \rightarrow \beta = \frac{i_C}{i_B}$

$i_E = i_B + \beta i_B$ $\quad i_C = \beta i_B$

$i_E = i_B(\beta + 1)$

$i_B R_B + i_B(\beta+1) R_E = V_{cc} - V_{BE}$

EXERCISE



Solution

$$i_B R_B + i_B(\beta+1)R_E = V_{CC} - V_{BE}$$

$$i_B\left[R_B + (\beta+1)R_E\right] = V_{CC} - V_{BE}$$

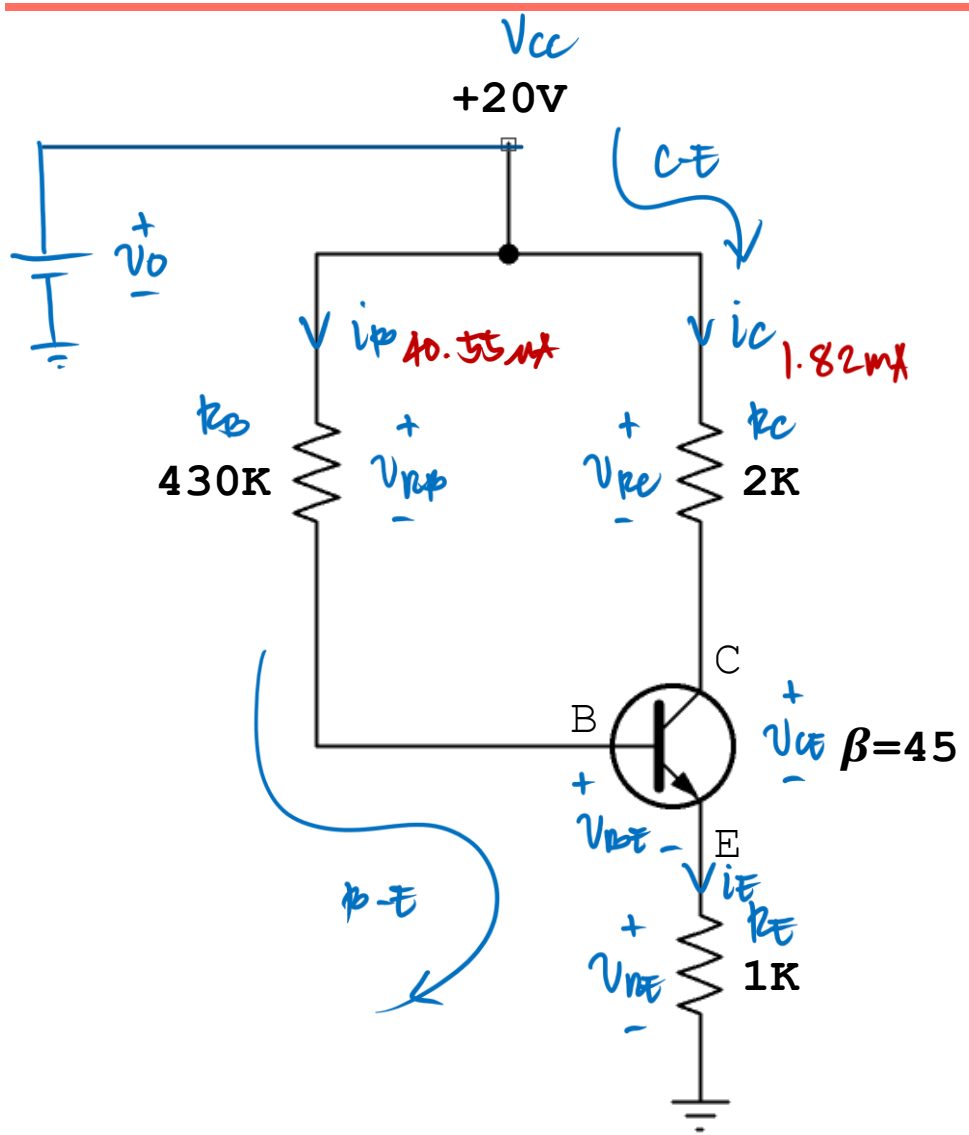
$$i_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E}$$

$$i_B = \frac{20 - 0.7}{430k + (45+1)\,1k}$$

$$i_{BQ} = 40.55\ \mu A$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_C}{i_B}$$

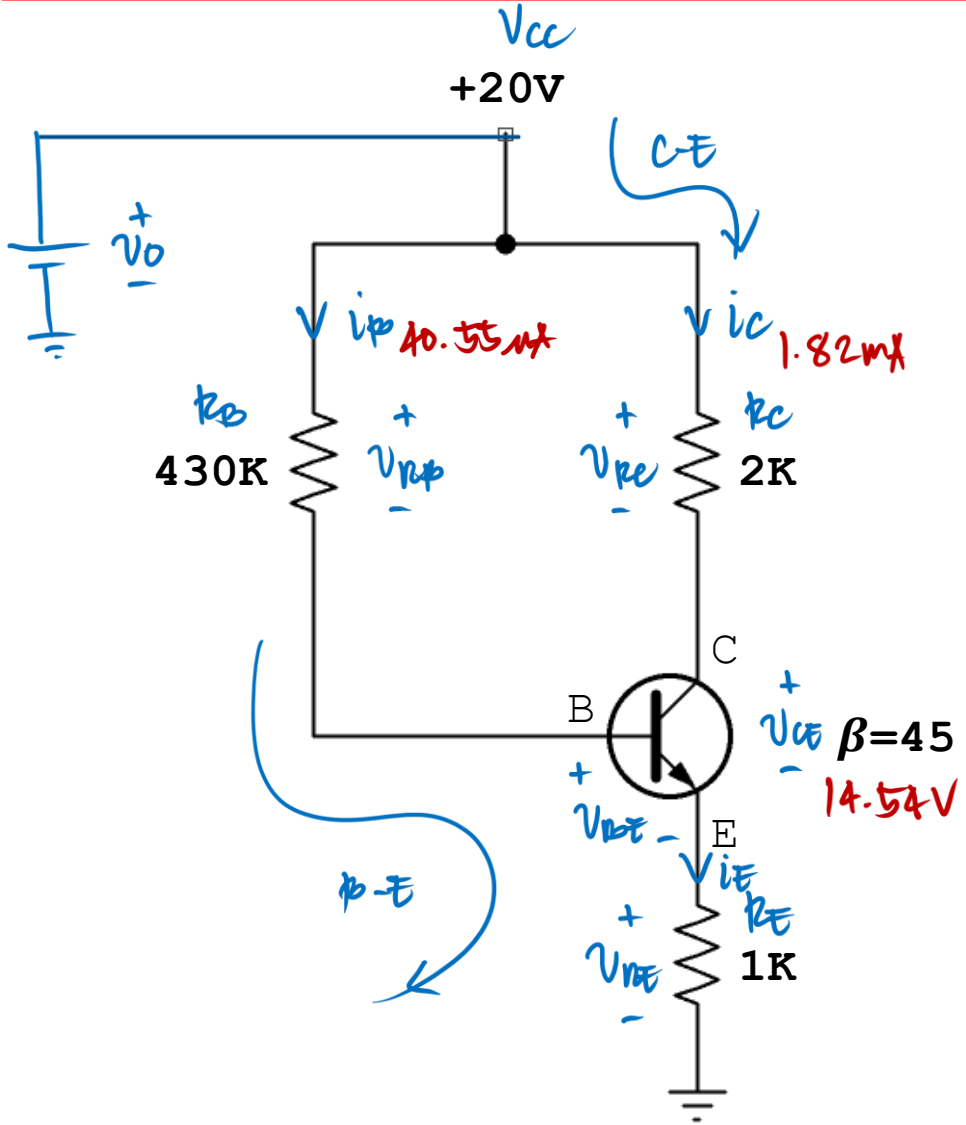
$$i_C = \beta i_B$$

$$i_C = 45(40.55\mu)$$

$$i_{CQ} = 1.82\,mA$$

ans

EXERCISE



Solution

KVL @ C-E

$$-V_{cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

$$V_{CE} = V_{cc} - V_{RC} - V_{RE}$$

$$V_{CE} = V_{cc} - i_c R_C - i_E R_E \rightarrow i_c \approx i_E$$

$$V_{CE} = V_{cc} - i_c(R_C + R_E)$$

$$V_{CE} = 20 - 1.82m(2K + 1K)$$

$$\boxed{V_{CEQ} = 14.54\ V}$$

ans

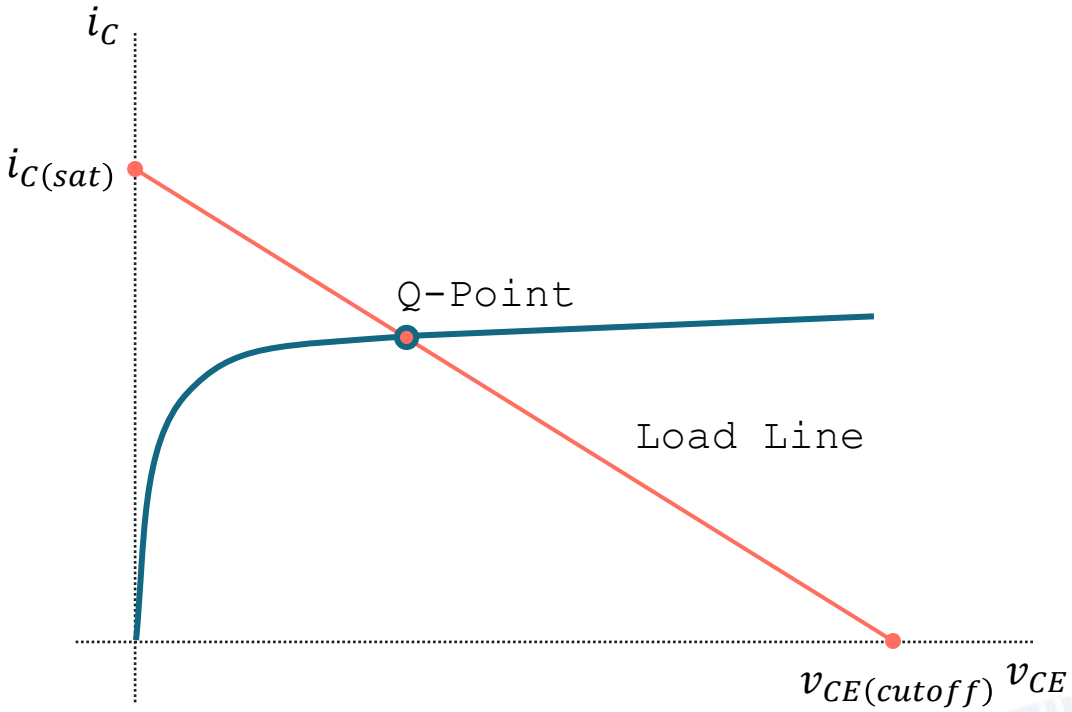
LOAD LINE ANALYSIS

SATURATION POINT

The **saturation point** is the operating state where BJT conducts the **maximum collector current** ($i_{C(sat)}$) with zero collector-emitter voltage ($v_{CE} = 0$).

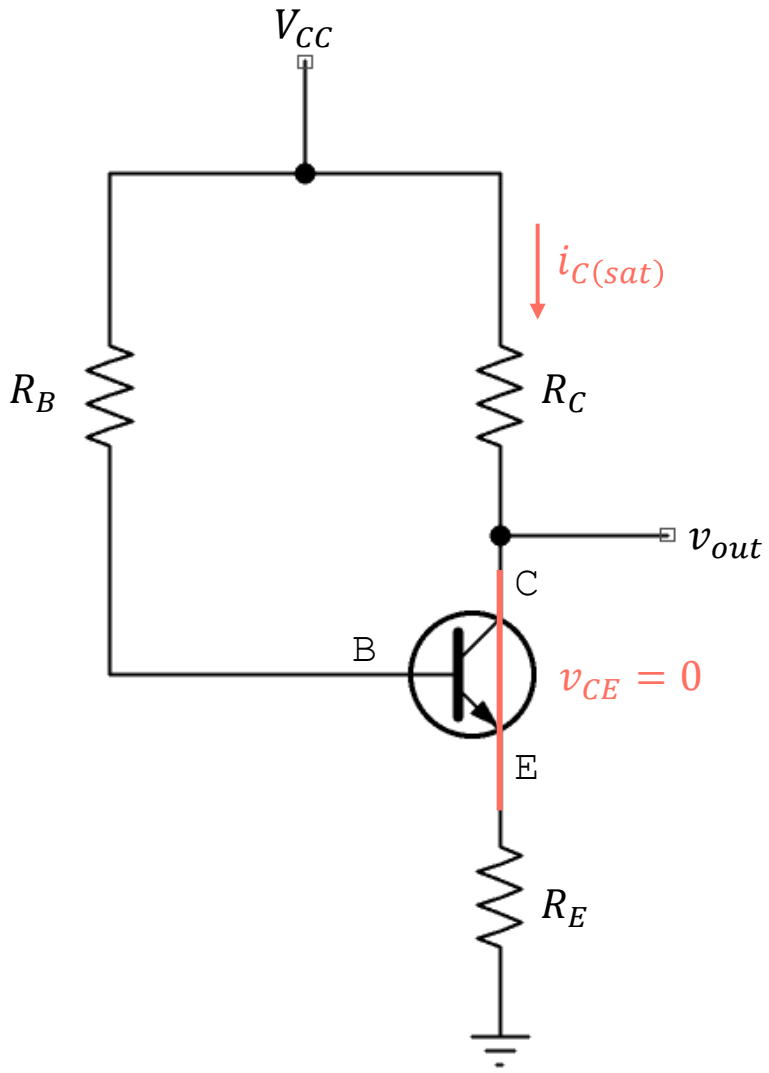
In this region the transistor acts like a **closed switch** (zero resistance between collector-emitter).

Collector Characteristic Curve

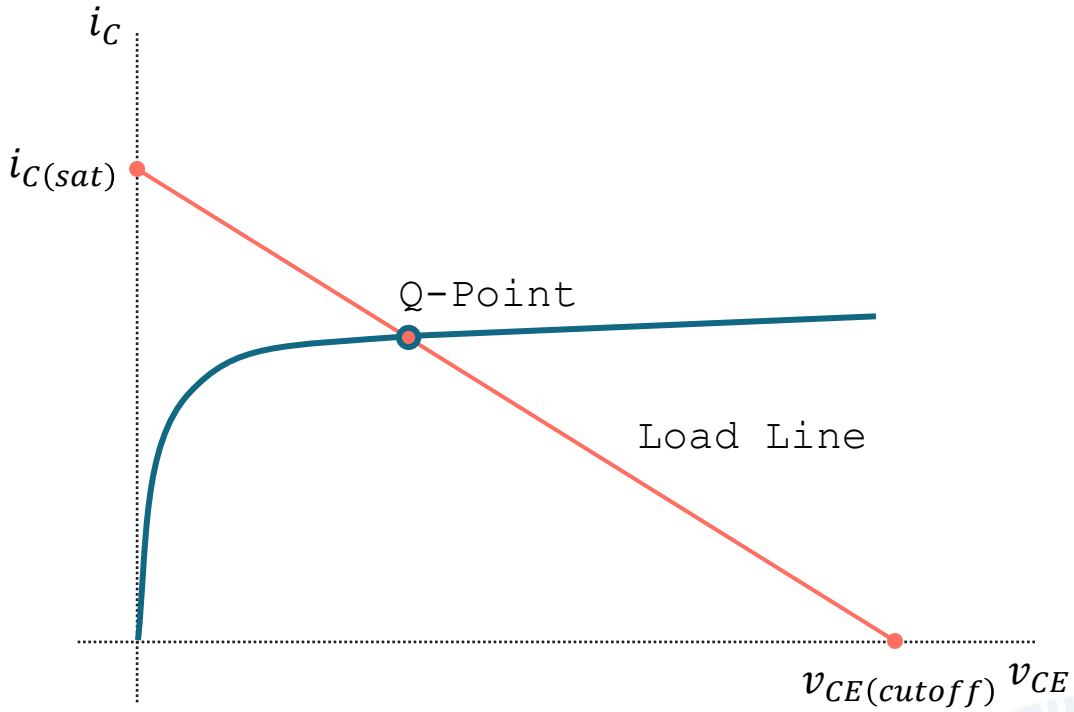


SATURATION POINT

Mentally Short



Collector Characteristic Curve

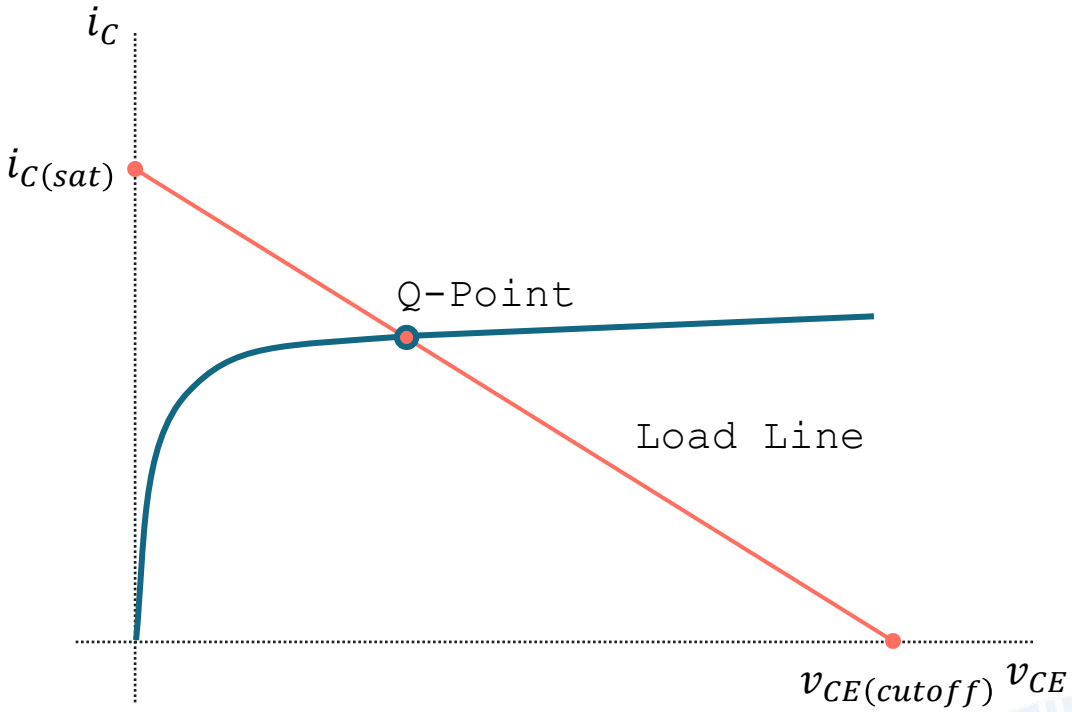


CUTOFF POINT

The **cutoff point** is the operating state where BJT conducts zero collector current ($i_C = 0$) with v_{CE} at its maximum ($v_{CE} = V_{CC}$).

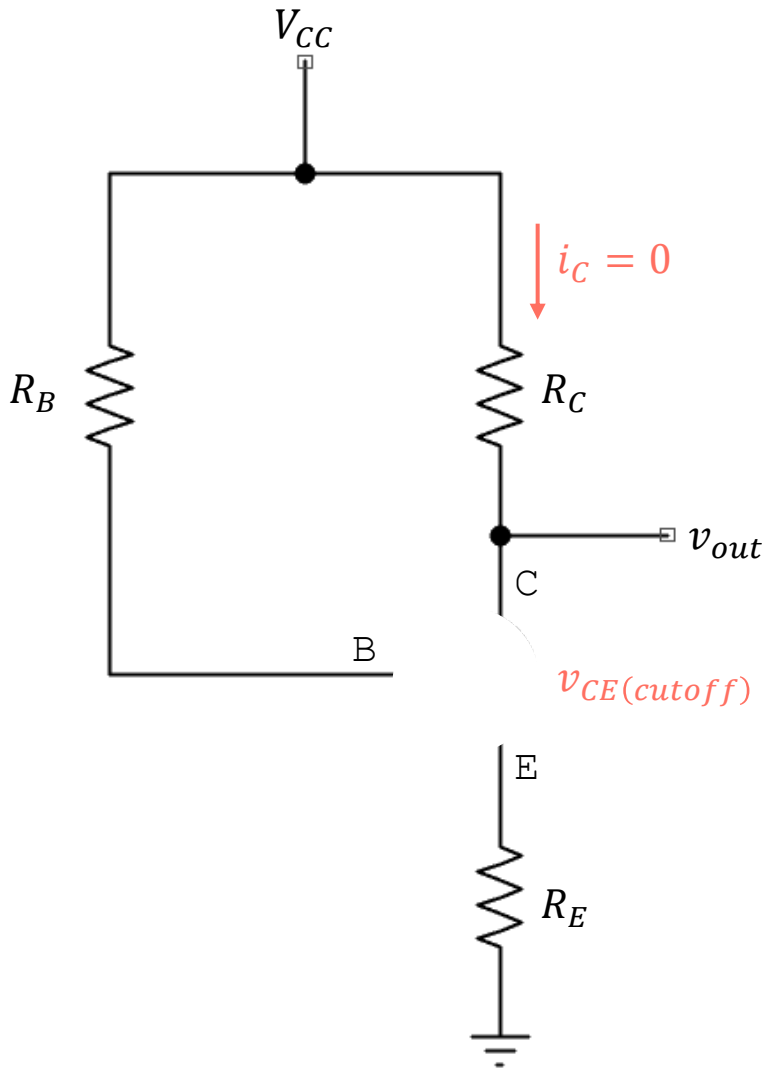
In this region the transistor acts like an **open switch** (infinite resistance between collector-emitter).

Collector Characteristic Curve

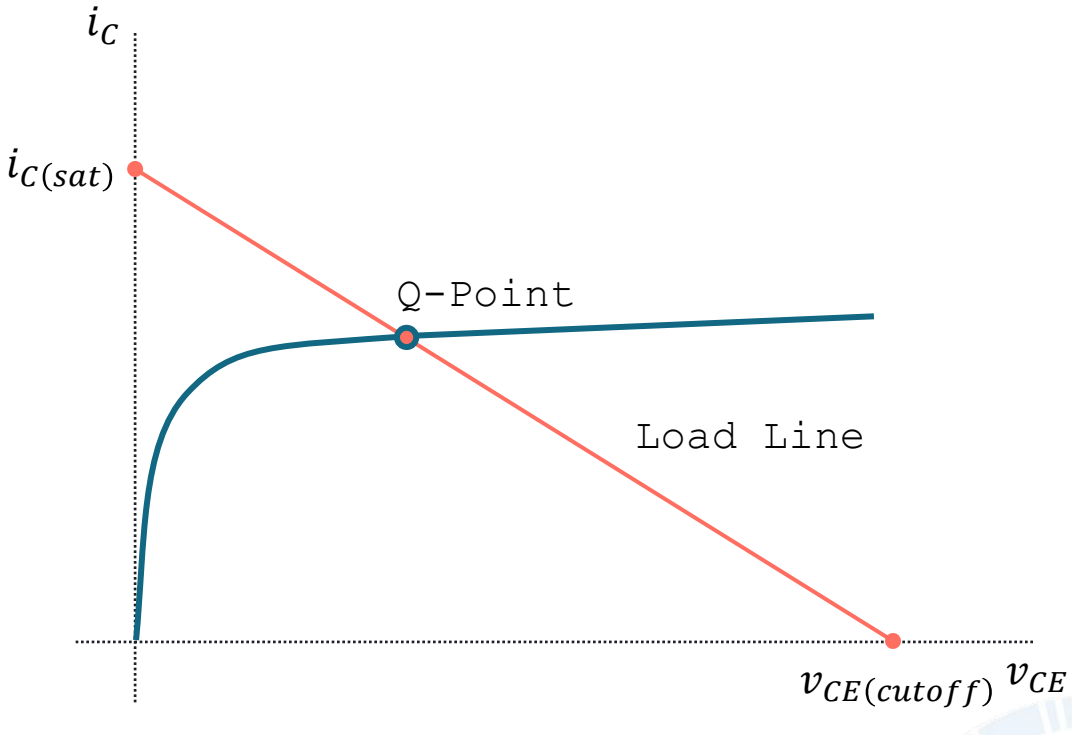


CUTOFF POINT

Mentally Open



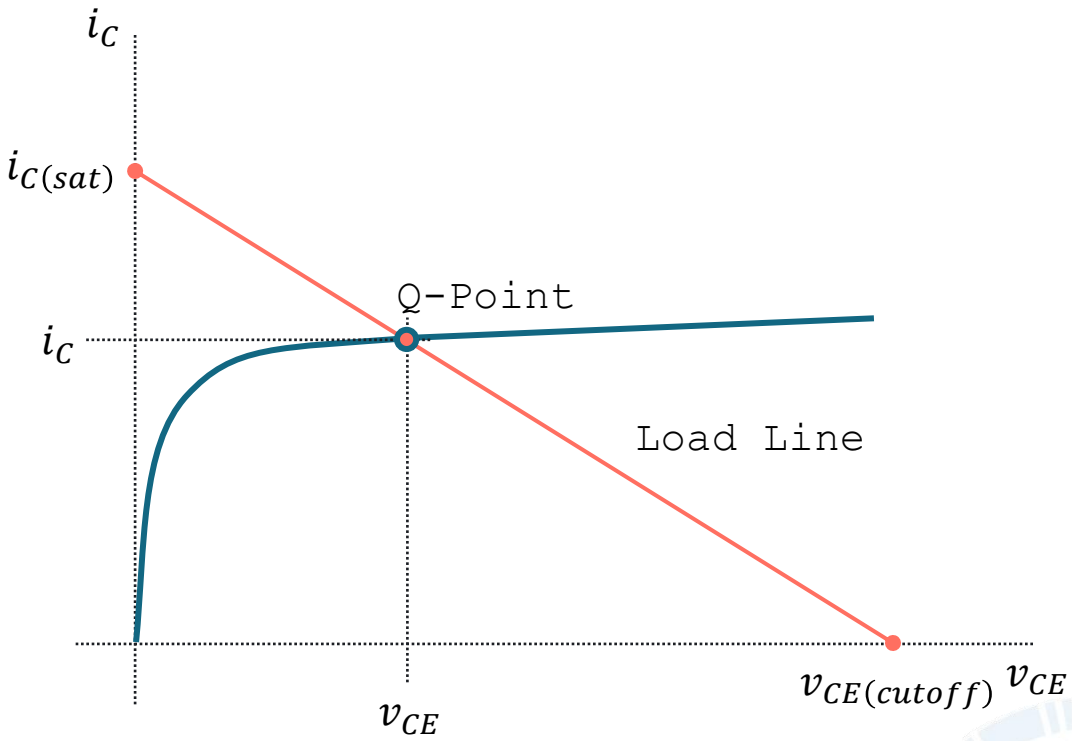
Collector Characteristic Curve



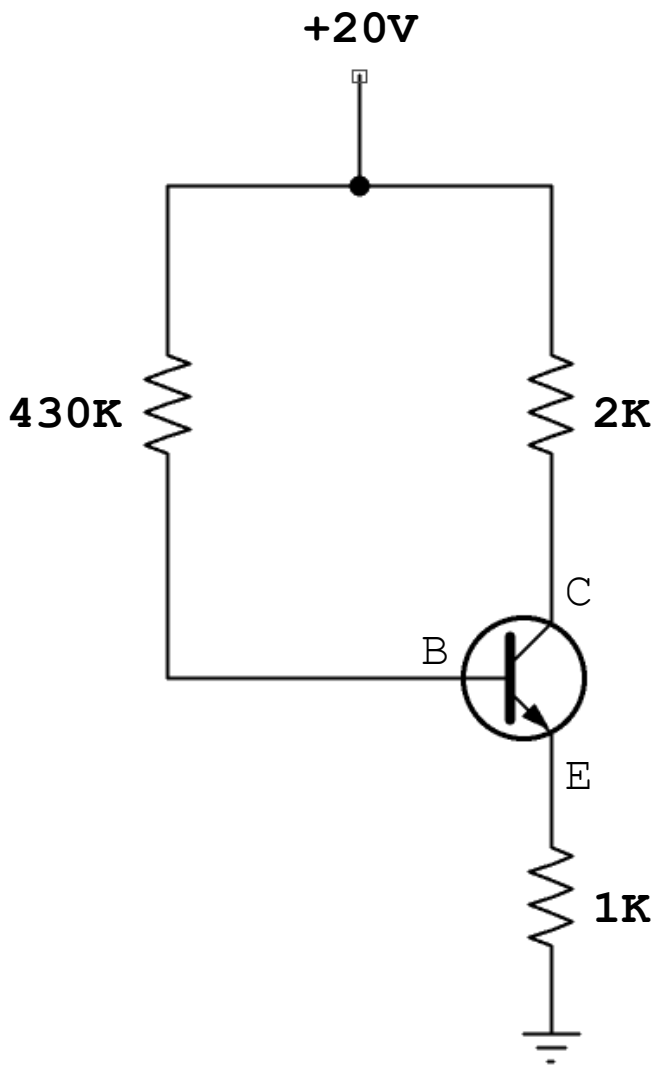
QUIESCENT POINT

The **Q-point** is the stable DC operating condition characterized by specific value of collector current (i_C) and collector-emitter voltage (v_{CE}).

Collector Characteristic Curve



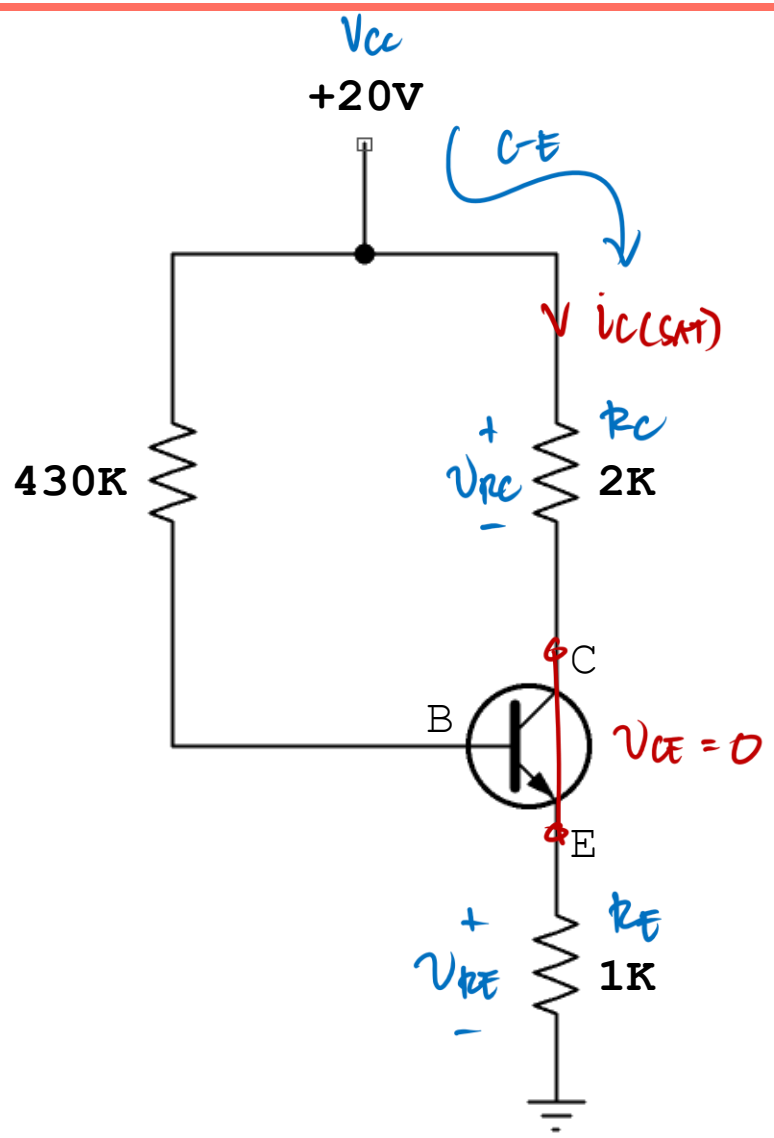
EXERCISE



Plot the DC load line analysis for the emitter-stabilized bias network, indicating:

- Saturation current ($i_{C(sat)}$)
- Cutoff voltage ($v_{CE(cutoff)}$)
- Operating Point (Q-Point)

EXERCISE



Solution

Saturation Point

KVL @ C-E

$$-V_{cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

$$V_{RC} + V_{RE} = V_{cc}$$

$$i_C R_C + i_E R_E = V_{cc}$$

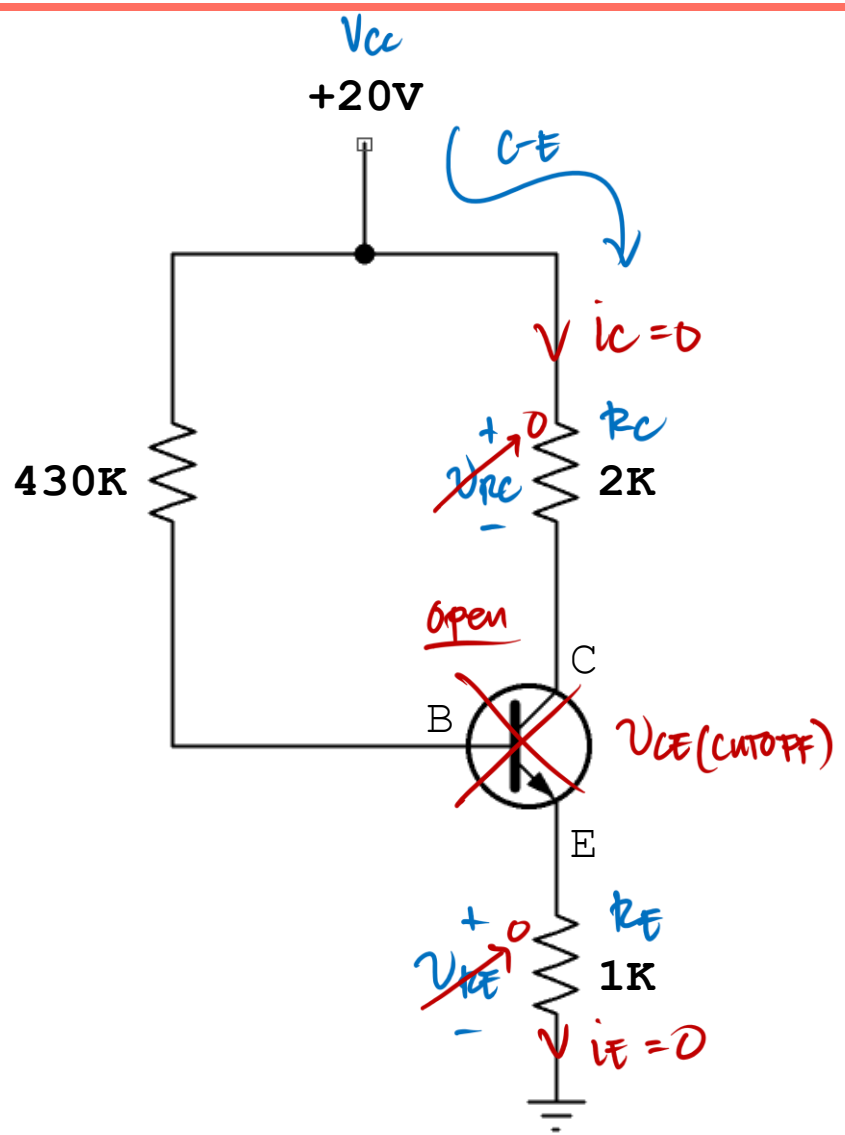
$$\frac{i_C(R_C + R_E)}{R_C + R_E} = \frac{V_{cc}}{R_C + R_E}$$

$$i_{C(SAT)} = \frac{20}{2K + 1K}$$

$$i_{C(SAT)} = 6.67\ mA$$

ans

EXERCISE



Solution

Cutoff Point

KVL @ C-E

$$-V_{cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

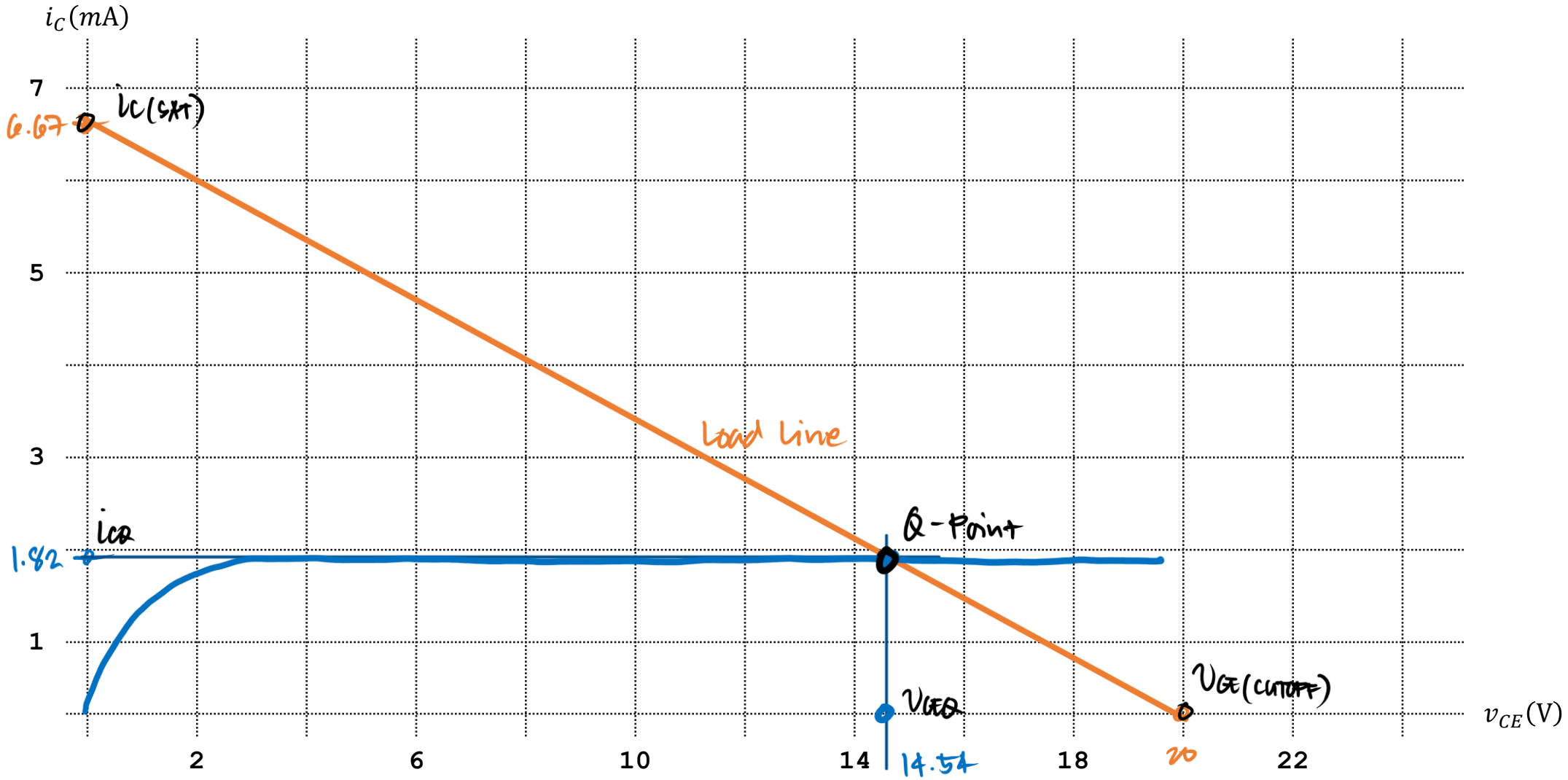
$$V_{CE(CUTOFF)} = V_{cc}$$

$$V_{CE(CUTOFF)} = 20V$$

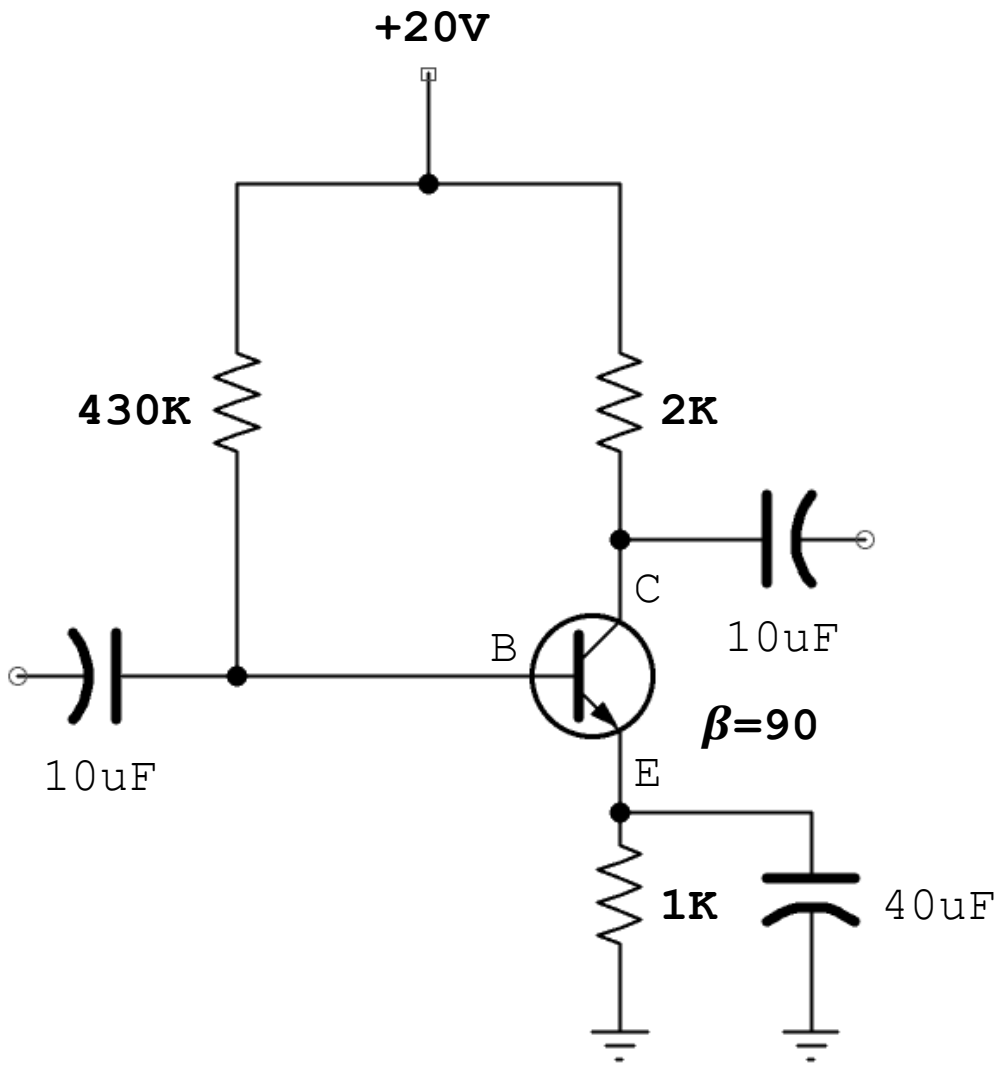
ans

EXERCISE

Load Line Analysis



EXERCISE



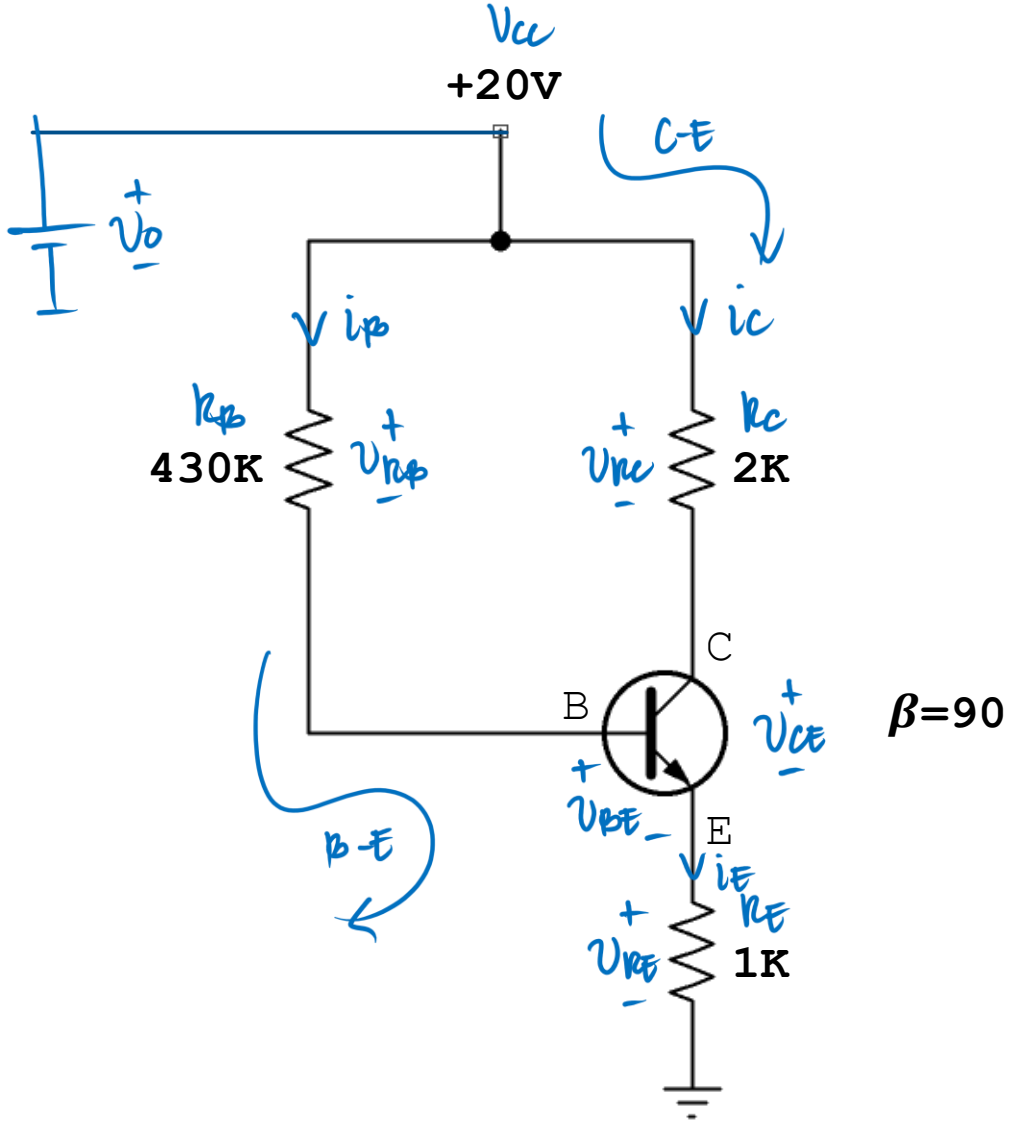
For the given emitter-stabilized bias network, determine:

- Base current (i_{BQ})
- Collector current (i_{CQ})
- Collector-Emitter voltage (v_{CEQ})
- Emitter voltage (v_E)

and plot the DC load line analysis indicating:

- Saturation current $(i_{C(sat)})$
- Cutoff voltage $(v_{CE(cutoff)})$
- Operating Point (Q-Point)

EXERCISE



Solution

KVL @ B-E

$$-V_{CC} + V_{RB} + V_{BE} + V_{RE} = 0$$

$$V_{RB} + V_{RE} = V_{CC} - V_{BE}$$

$$i_B R_B + i_E R_E = V_{CC} - V_{BE}$$

$$i_E = i_B + i_C \rightarrow \beta = \frac{i_C}{i_B}$$

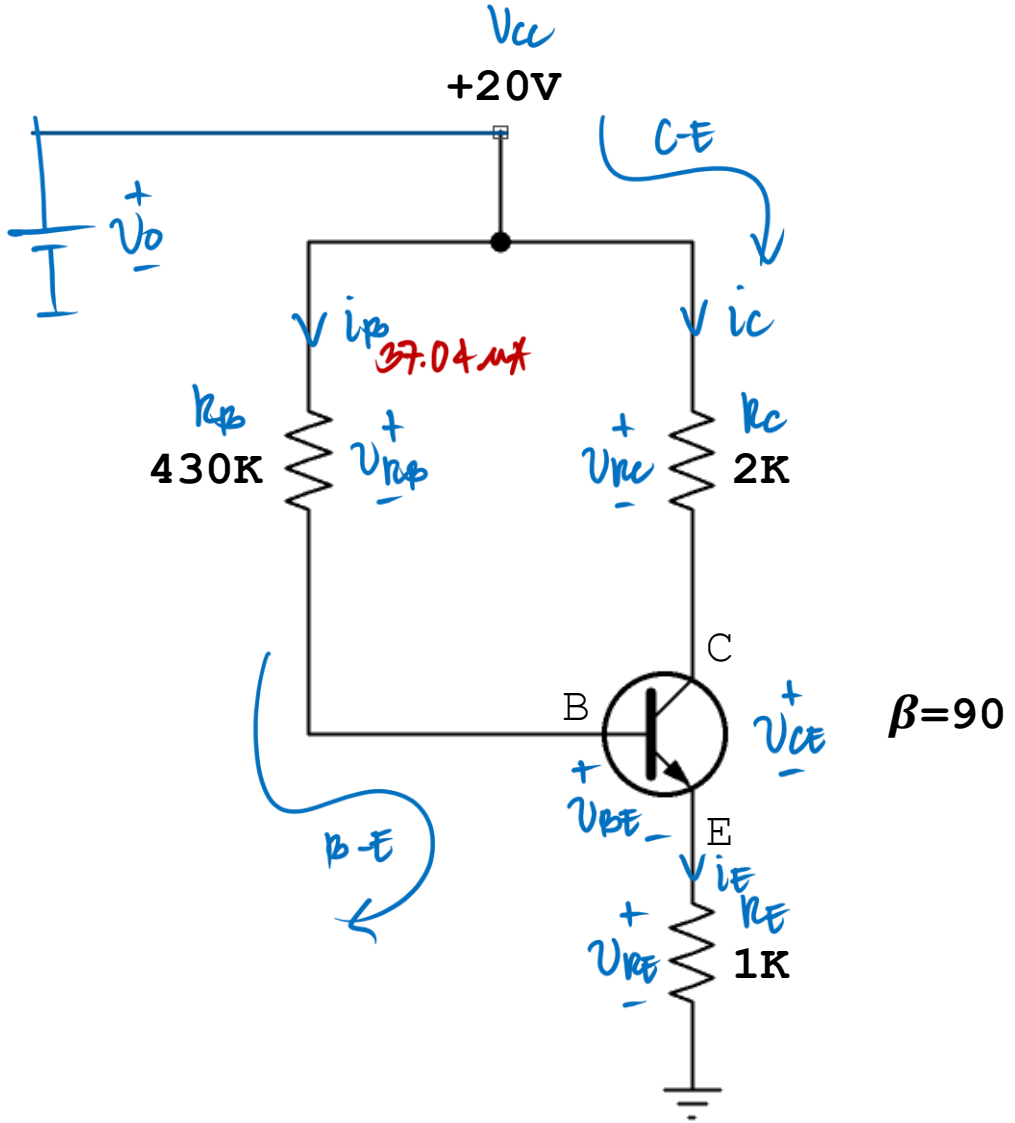
$$i_E = i_B + \beta i_B \qquad i_C = \beta i_B$$

$$i_E = i_B(\beta + 1)$$

$$i_B R_B + i_B(\beta+1) R_E = V_{CC} - V_{BE}$$

$$i_B\left[R_B + (\beta+1)R_E\right] = V_{CC} - V_{BE}$$

EXERCISE



$\beta = 90$

Solution

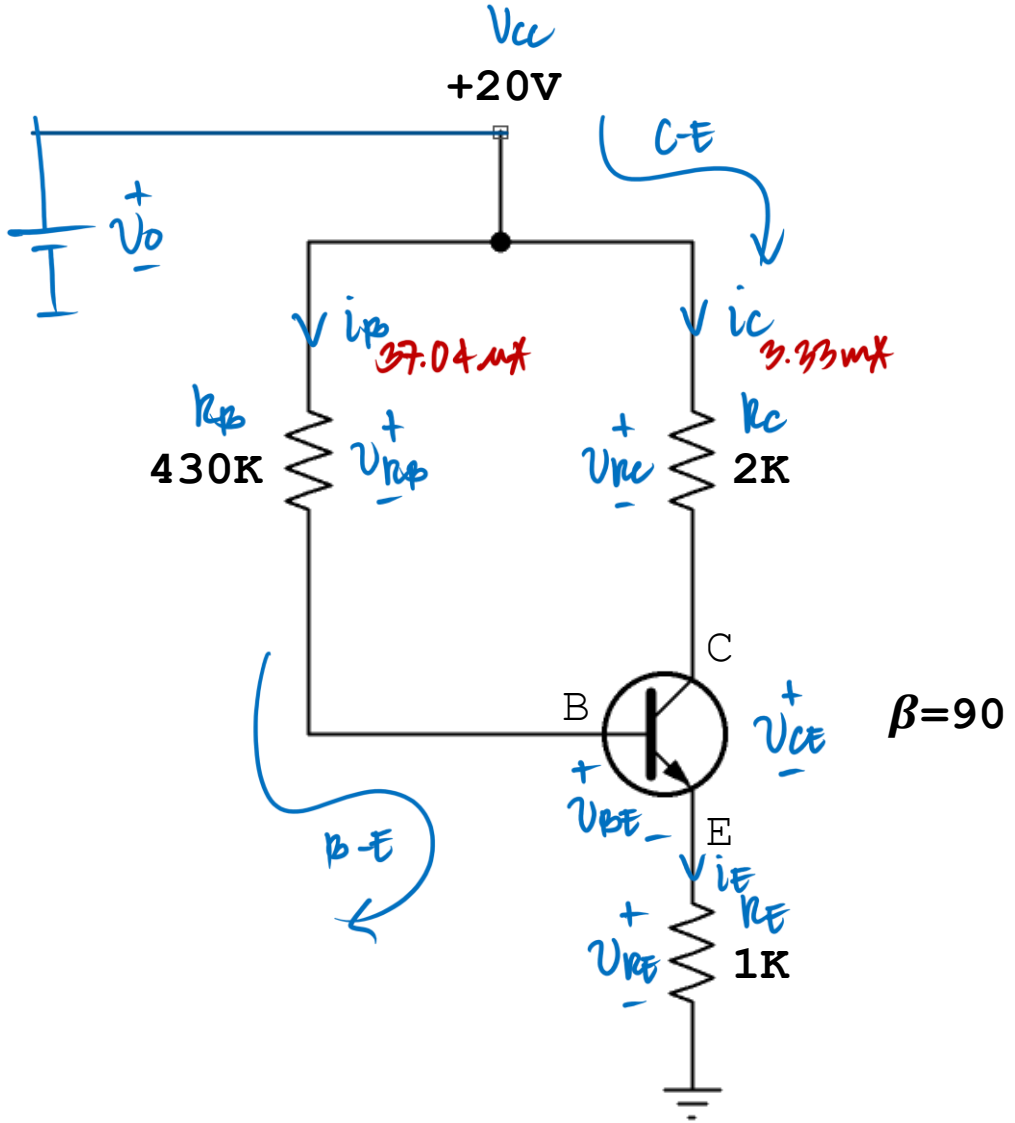
$$i_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}$$

$$i_B = \frac{20 - 0.7}{430k + (90+1)\,1k}$$

$$i_{BQ} = 37.04\ \mu A$$

ans

EXERCISE



Solution

Current Gain

$$\beta = \frac{i_C}{i_B}$$

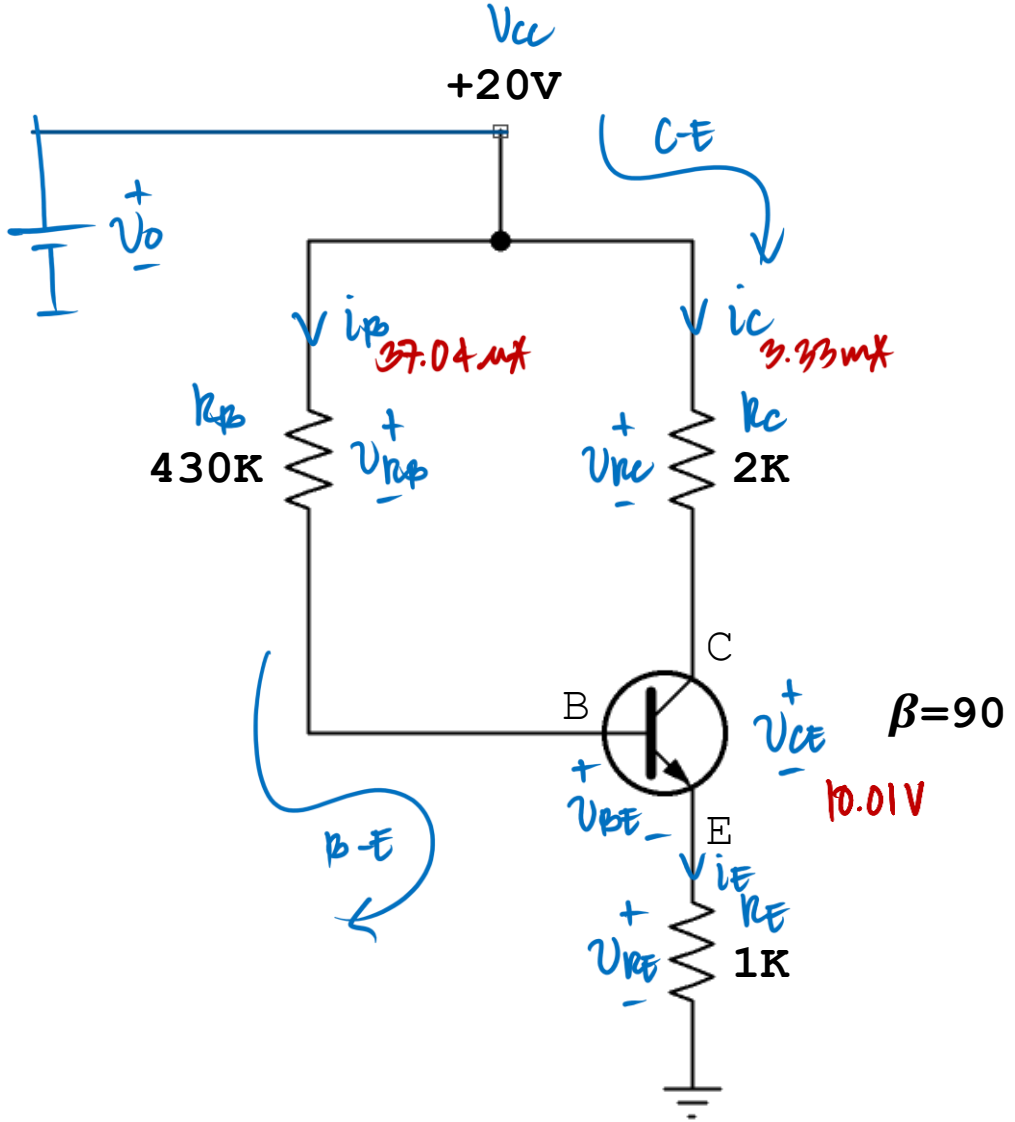
$$i_C = \beta i_B$$

$$i_C = 90(37.04\mu)$$

$$i_{CQ} = 3.33\ mA$$

ans

EXERCISE



Solution

KVL @ C-E

$$-V_{cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

$$V_{CE} = V_{cc} - V_{RC} - V_{RE}$$

$$V_{CE} = V_{cc} - i_c R_C - i_E R_E \rightarrow i_c \approx i_E$$

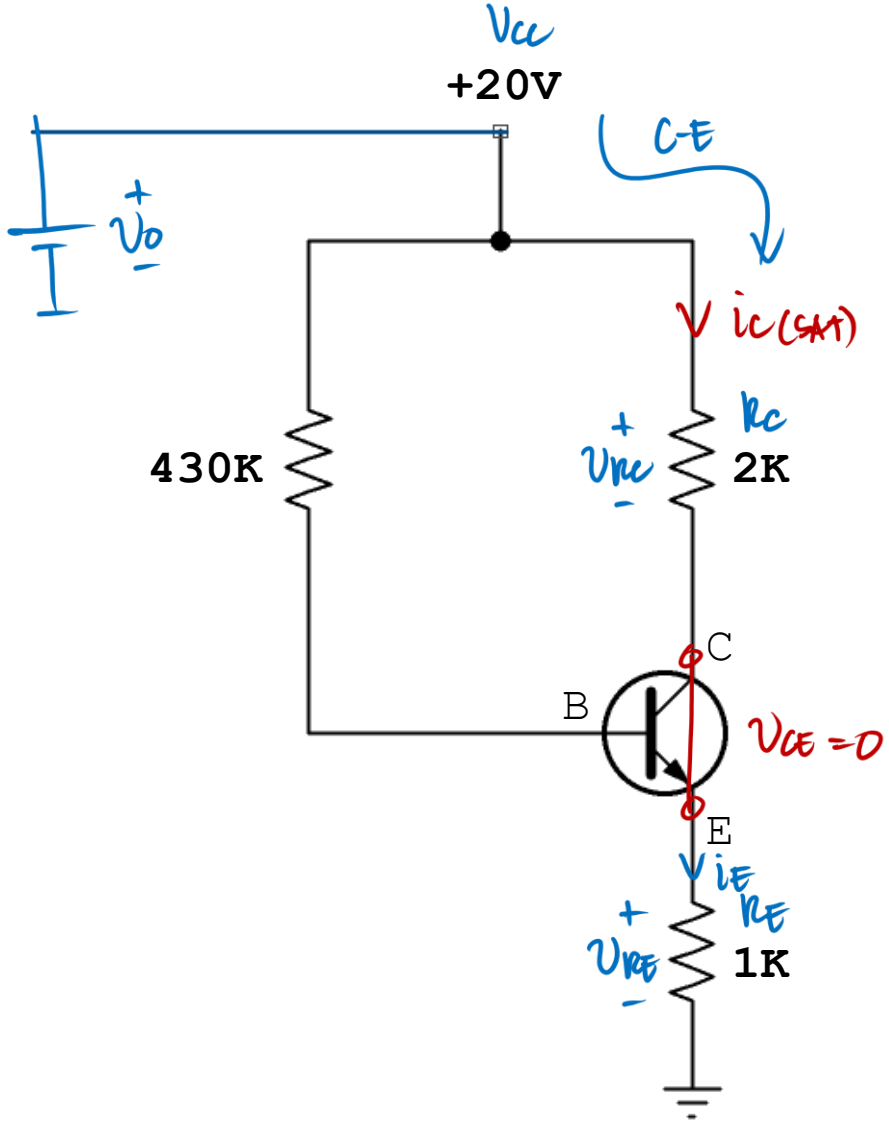
$$V_{CE} = V_{cc} - i_c (R_C + R_E)$$

$$V_{CE} = 20 - 3.33m(2K + 1K)$$

$$\boxed{V_{CEQ} = 10.01\,V}$$

ans

EXERCISE



Solution

Saturation Point

KVL @ C-E

$$-V_{cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

$$V_{RC} + V_{RE} = V_{cc}$$

$$i_c R_C + i_E R_E = V_{cc} \rightarrow i_c \approx i_E$$

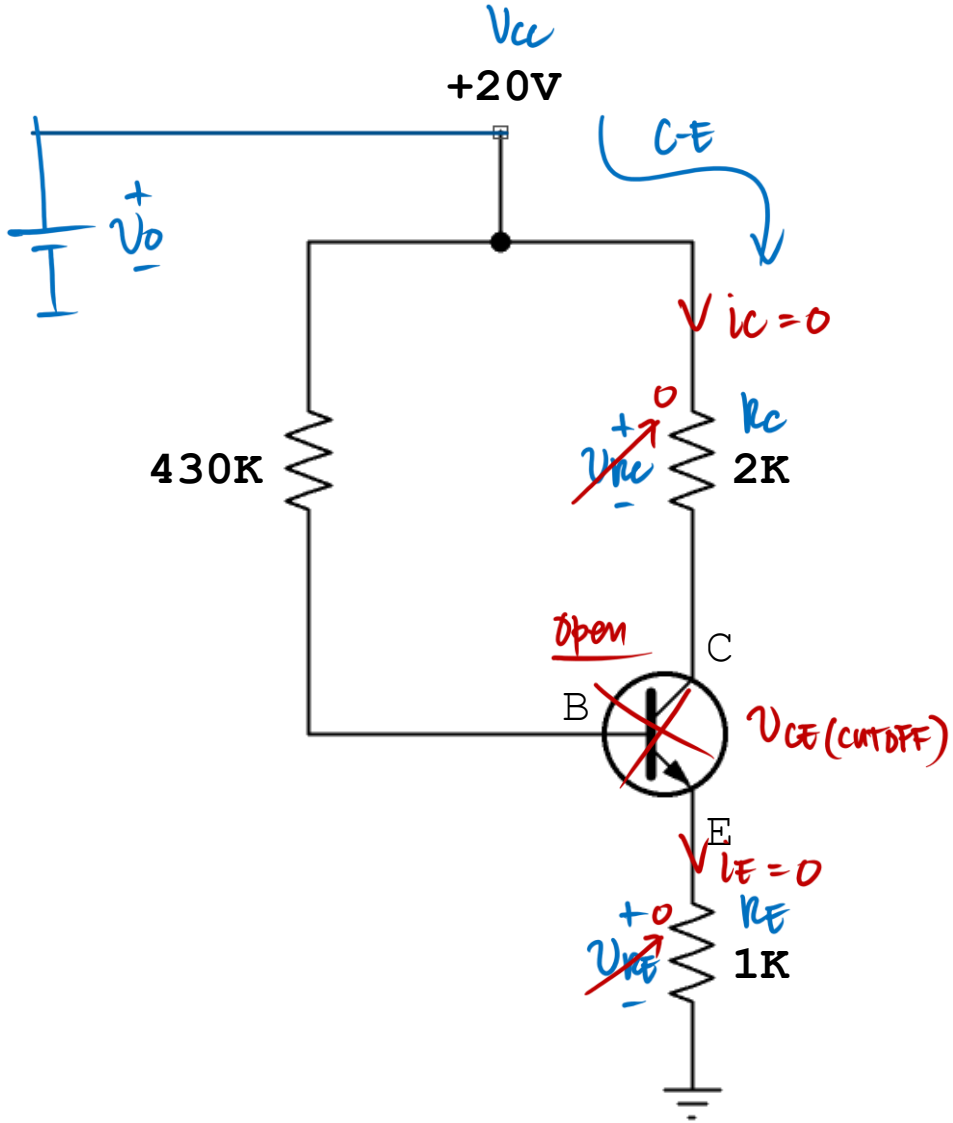
$$\frac{i_c(R_C + R_E)}{R_C + R_E} = \frac{V_{cc}}{R_C + R_E}$$

$$i_{c(SAT)} = \frac{20}{2K + 1K}$$

$$i_{c(SAT)} = 6.67\ mA$$

ans

EXERCISE



Solution

Cutoff Point

KVL @ C-E

$$-V_{Cc} + V_{RC} + V_{CE} + V_{RE} = 0$$

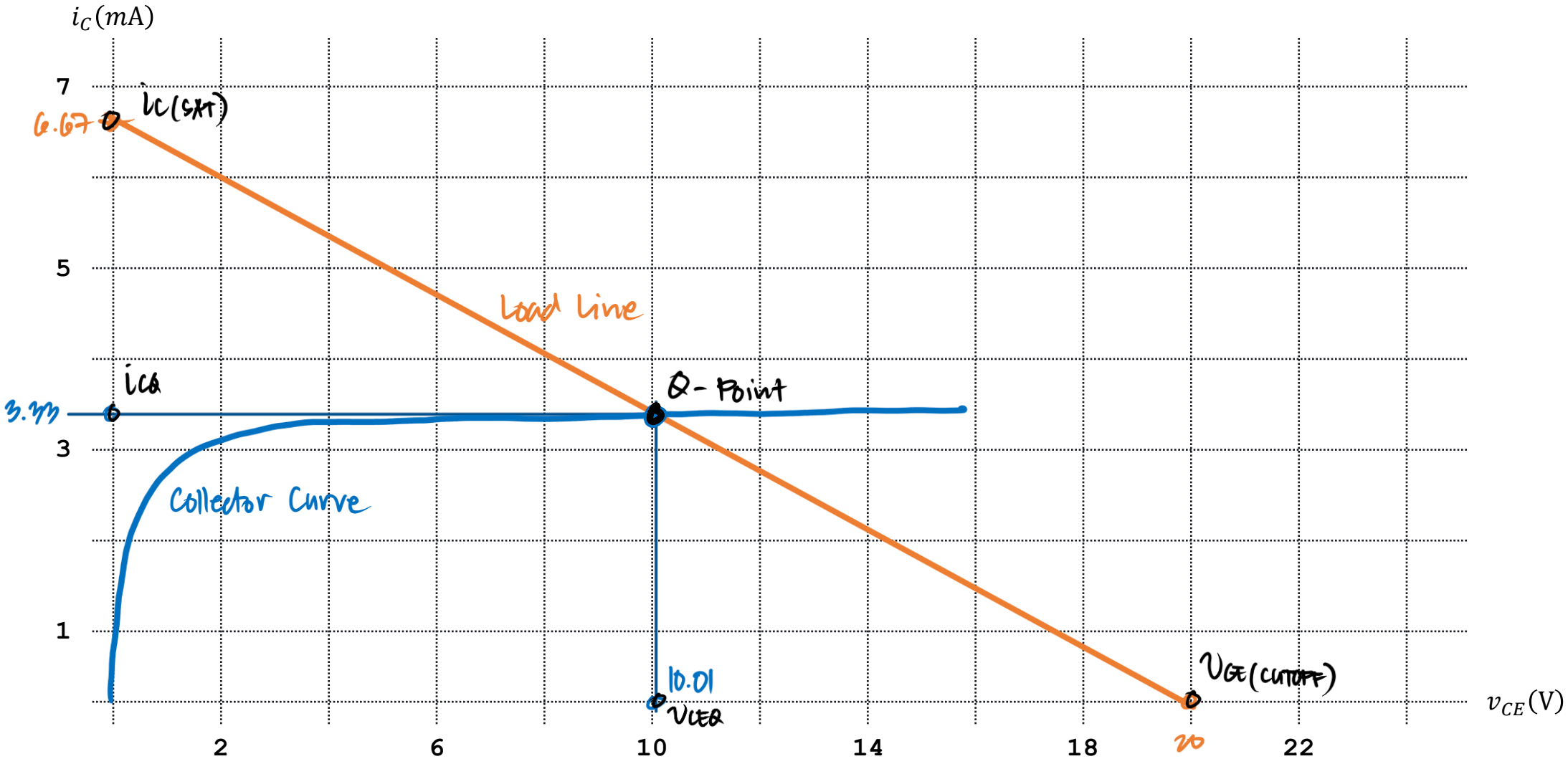
$$V_{CE} = V_{CC}$$

$$V_{CE(CUTOFF)} = 20V$$

ans

EXERCISE

Load Line Analysis



IMPROVE STABILITY

Bias	β	$i_B(\mu A)$	$i_C(mA)$	$v_{CE}(V)$	$\%\Delta v_{CE}$
Fixed-Bias	50	47.08	2.35	6.83	-76%
	100	47.08	4.71	1.64	
Emitter-Stabilized	45	40.55	1.82	14.54	-31%
	90	37.04	3.33	10.01	
Voltage-Divider Bias					

LABORATORY