
STM32
CubeMX

1. Description

1.1. Project

Project Name	Project_08_Protocol_Serial_Comunication
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	10/03/2022

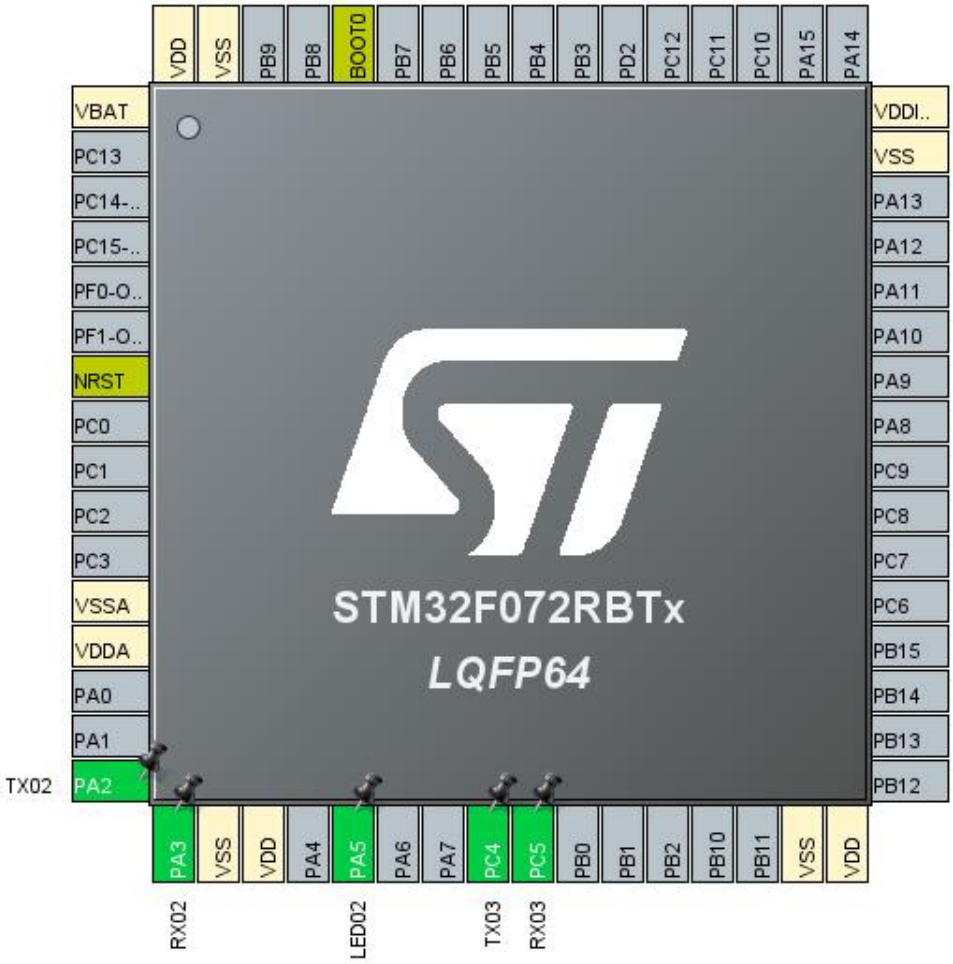
1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x2
MCU name	STM32F072RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M0

2. Pinout Configuration

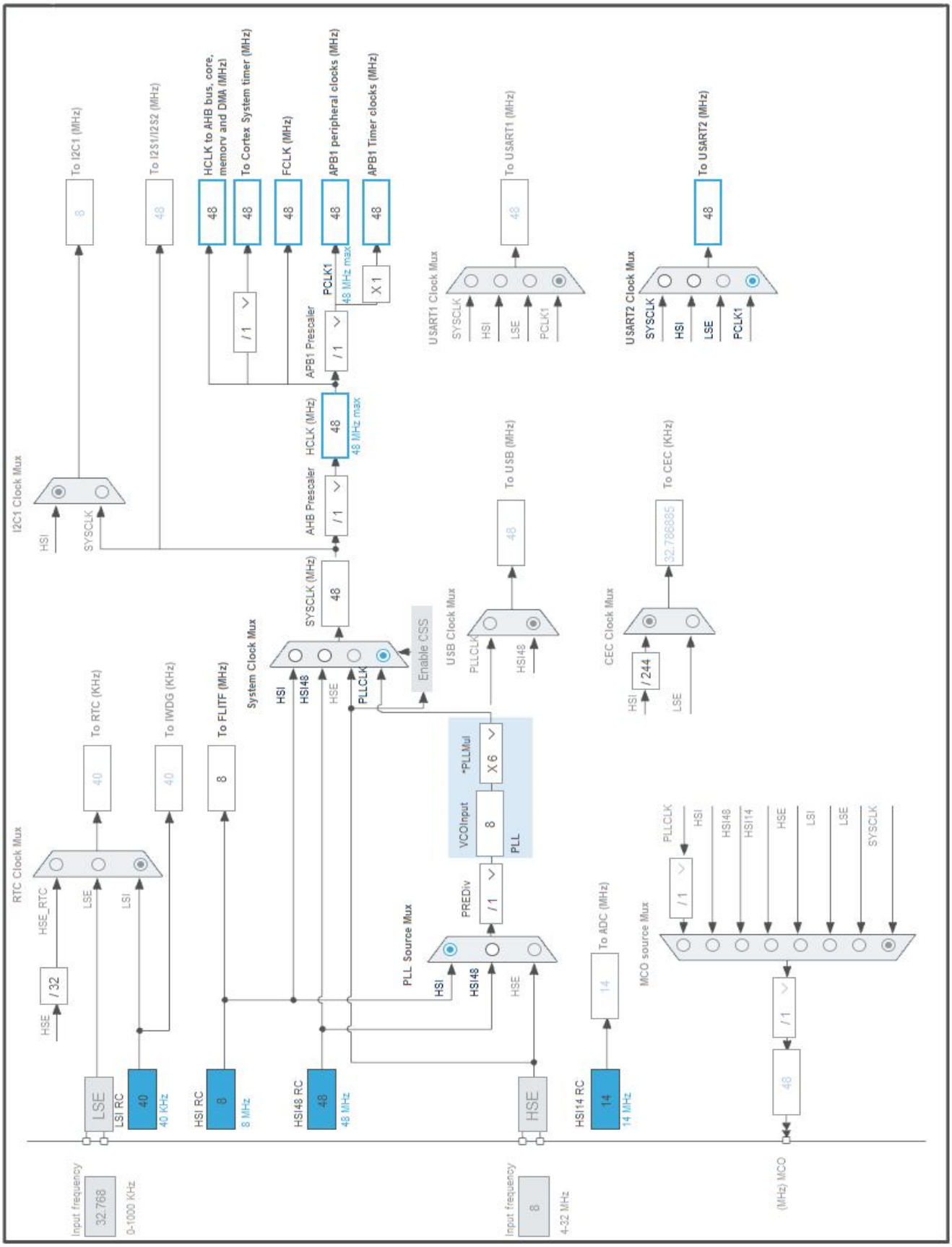


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	TX02
17	PA3	I/O	USART2_RX	RX02
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LED02
24	PC4	I/O	USART3_TX	TX03
25	PC5	I/O	USART3_RX	RX03
31	VSS	Power		
32	VDD	Power		
47	VSS	Power		
48	VDDIO2	Power		
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Project_08_Protocol_Serial_Comunication
Project Folder	C:\Users\rubens.araujo\STM32CubeIDE\workspace_1.10.1\Project_08_Protocol_
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F0 V1.11.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	Yes
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART2_UART_Init	USART2
4	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x2
MCU	STM32F072RBTx
Datasheet	DS9826_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

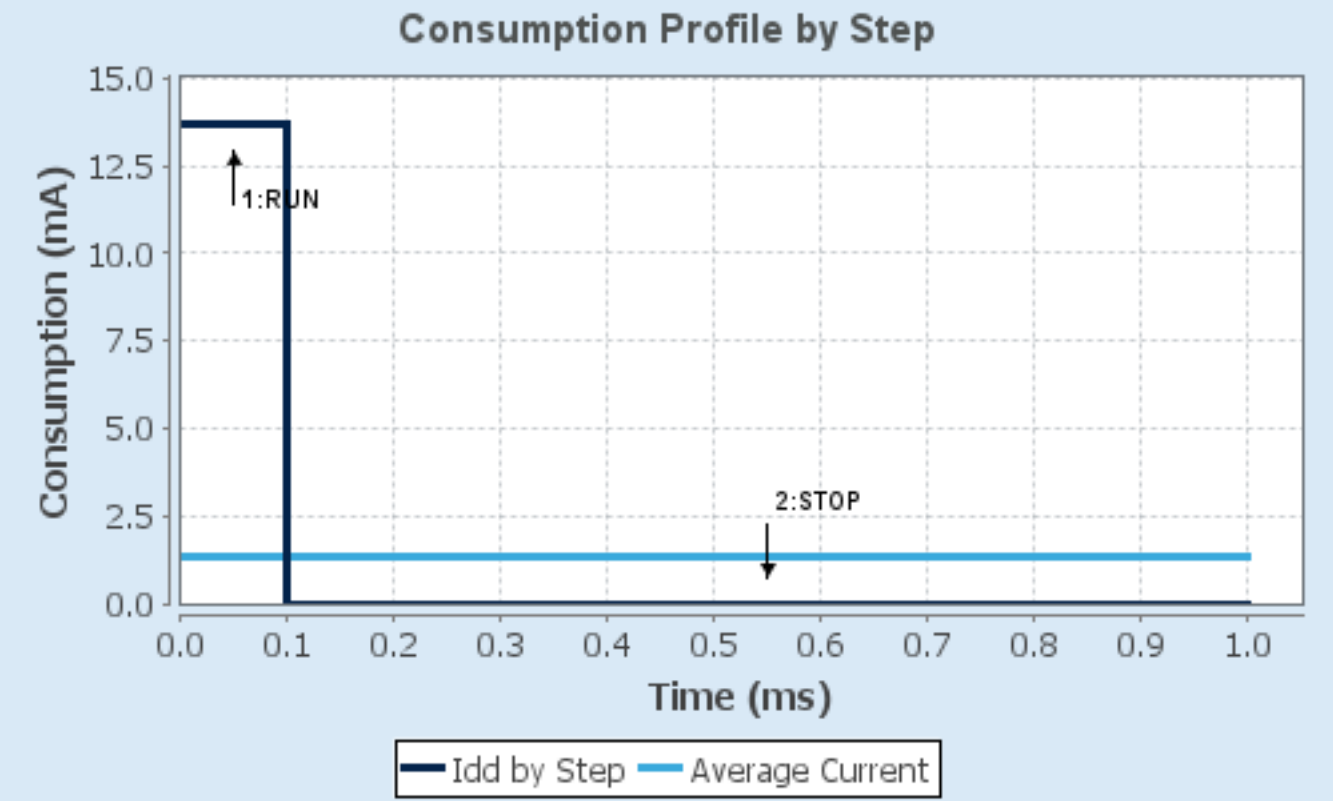
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	13.66 mA	6.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Ta Max	102.84	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.37 mA
Battery Life	3 months, 11 days, 17 hours	Average DMIPS	0.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. RCC

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.2. USART2

Mode: Asynchronous

7.2.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.3. USART3

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	TX02
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	RX02
USART3	PC4	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	TX03
	PC5	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	RX03
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED02

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	3	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
USART3 and USART4 global interrupts	true	0	0
PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31	unused		
Flash global interrupt	unused		
RCC and CRS global interrupts	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	false	true	true
USART3 and USART4 global interrupts	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link