ECE 551
Exercise03

This is a 10pt problem of HW1

Submit whatever you have for both the DUT and test results to the dropbox by end of the class period.

Submit a **structural** Verilog file that models a module that can synchronize a signal to our system clock (***clk***) and output a signal that is high for 1 clock cycle when that signal has a rising edge. Assume a D-FF is already defined that has an interface of:(D, clk,Q,&PRN) and a module name of ***dff***.

So essentially a circuit to solve metastability, then detect a rising edge.

Name your file **synch_detect.sv** and ensure the module name is also **synch_detect**.

Interface is:

asynch_sig_in ➔ input to synchronize and detect falling edge on
clk → clock signal
rst_n → global asynch active low reset (initialize the circuit) (preset flops in this case)
rise_edge → output of your block that is high for 1 clock cycle after falling edge occurs on

The code for **dff.v**, and a testbench are provided (**synch_detect_tb.v**) are provided in the Exercise03 folder table row.

Create a ModelSim project, and test your design. The test bench is self checking and should give a happy message in the console window if your DUT is good.

Watch the first 5min of Part I of Lecture02 video for hints on how to make this circuit.