Lab4 Notes

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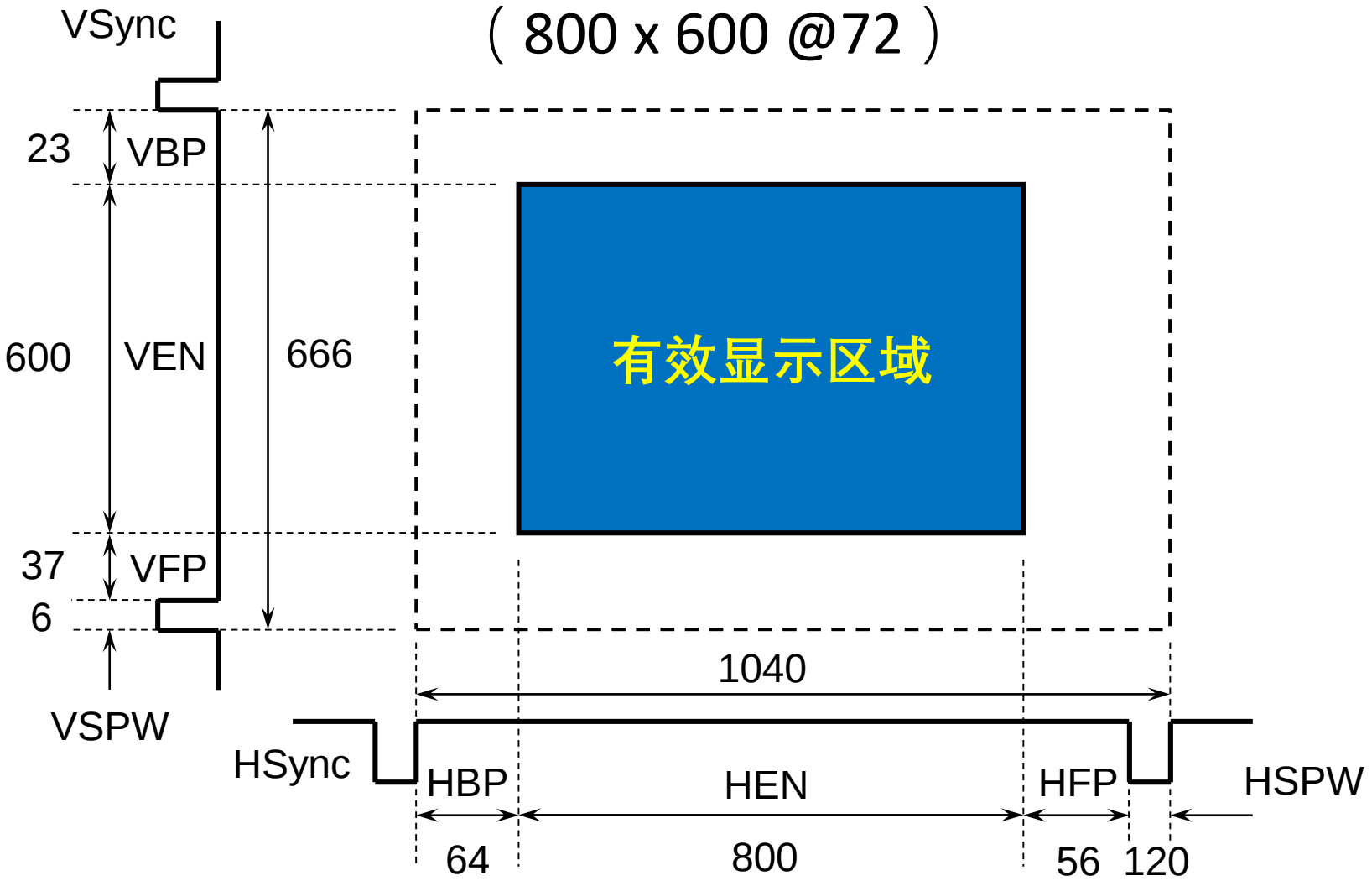
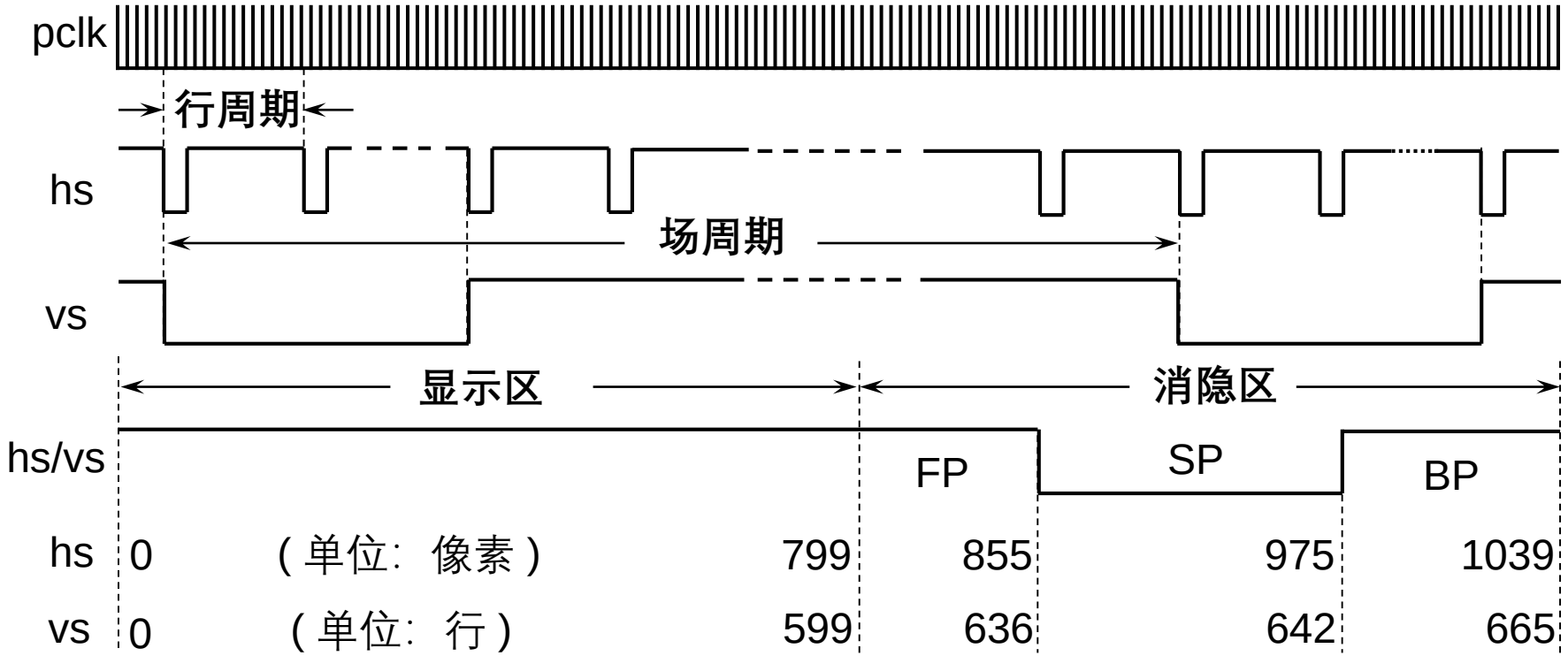
显示区域和定时参数


（800 x 600 @72）
VSync
23
VBP
600
VEN
666
37
VFP
6
VSPW
有效显示区域
1040
HSync
HBP
HEN
HFP
HSPW
64
800
56
120



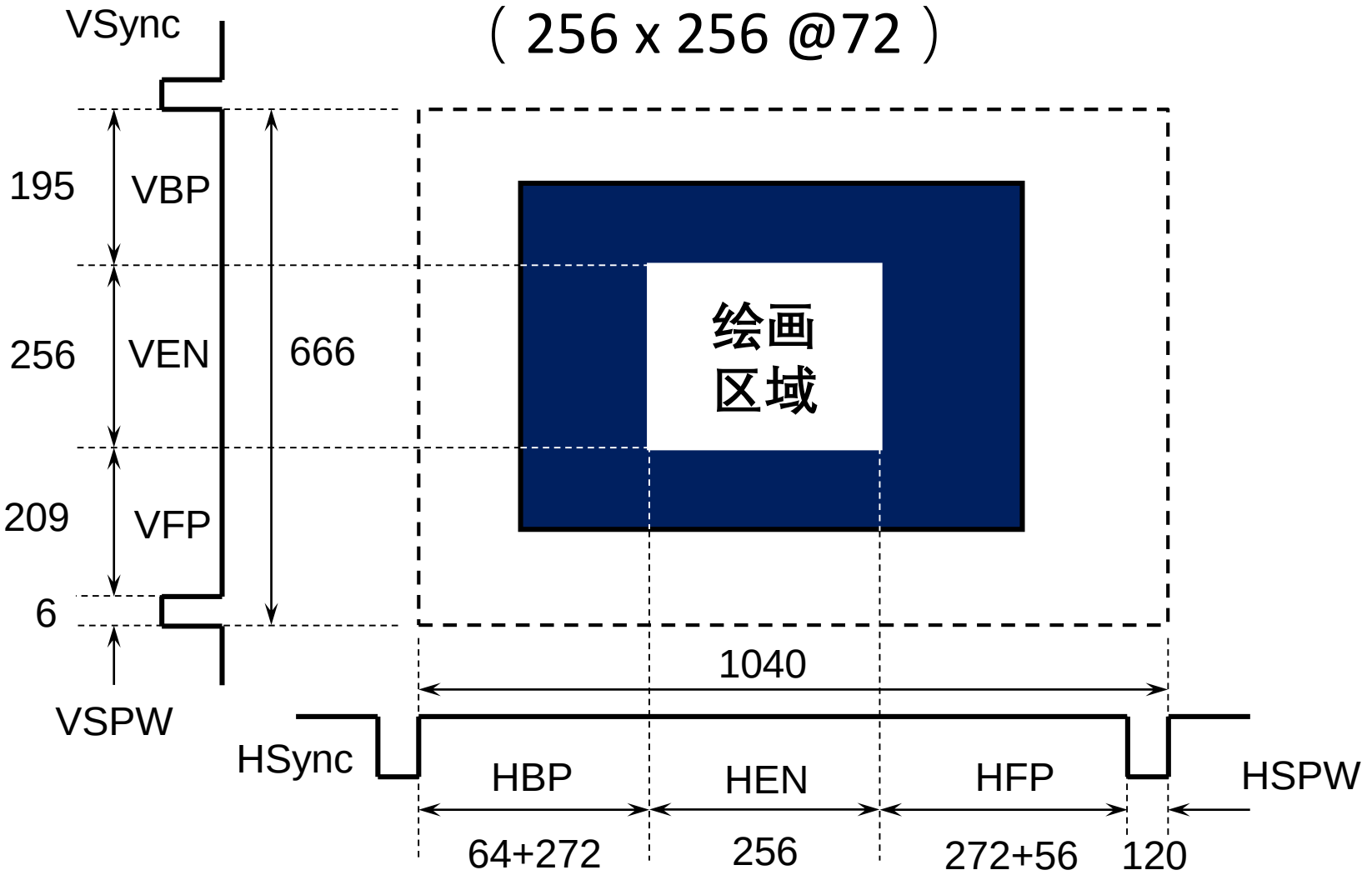

```
always @(posedge pclk, negedge rstn)
    if (!rstn) hcnt <= 856;
    else if (hcnt == 1039) hcnt <= 0;
    else hcnt <= hcnt + 1;
```

```
always @(posedge pclk, negedge rstn)
    if (!rstn) hs <= 0;
    else if (hcnt == 975) hs <= 1;
    else if (hcnt == 855) hs <= 0;
```

```
always @(posedge pclk, negedge rstn)
    if (!rstn) vcnt <= 637;
    else if (hcnt == 855) begin
        if (vcnt == 665) vcnt <= 0;
        else vcnt <= vcnt + 1;  end
```

```
assign hen = hcnt < 800;
assign ven = vcnt < 600;
assign vrgb = (vhen & hen) ? vdata : 0;
```

显示区域和定时参数


（256 x 256 @72）
VSync
195
VBP
256
VEN
666
209
VFP
6
VSPW
绘画
区域
1040
HSync
HBP
HEN
HFP
HSPW
64+272
256
272+56
120

Verilog 编码细节

- **行/场同步信号：建议用寄存器输出**
  - 出错现象：不显示
- **像素信号：注意消隐，建议用寄存器输出**
  - 出错现象：不显示，显示出现色散
  - 由于存储器和控制器速度限制导致，降低时钟频率，例如, 选择800x600@60Hz (40MHz)
- **其他疏忽**
  - if … else的匹配
  - begin … end语句块
  - 变量位宽的匹配

The End