74HC2G08; 74HCT2G08

Dual 2-input AND gate Rev. 04 — 7 May 2009

Product data sheet

General description 1.

The 74HC2G08 and 74HCT2G08 are high-speed Si-gate CMOS devices. They provide two 2-input AND gates.

The HC device has CMOS input switching levels and supply voltage range 2 V to 6 V.

The HCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. **Features**

- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

Ordering information 3.

Table 1. **Ordering information**

Type number	Package							
	Temperature range	Name	Description	Version				
74HC2G08DP	–40 °C to +125 °C	TSSOP8 plastic thin shrink small outline package; 8 leads;		SOT505-2				
74HCT2G08DP			body width 3 mm; lead length 0.5 mm					
74HC2G08DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads;	SOT765-1				
74HCT2G08DC			body width 2.3 mm					
74HC2G08GD	–40 °C to +125 °C	XSON8U	place of the control of the pastage, its reads,					
74HCT2G08GD			8 terminals; UTLP based; body $3 \times 2 \times 0.5$ mm					

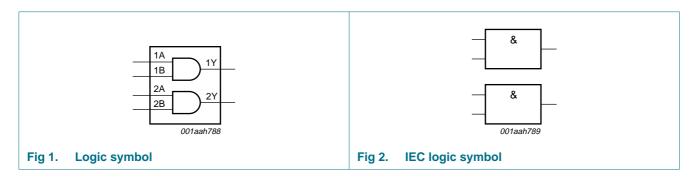


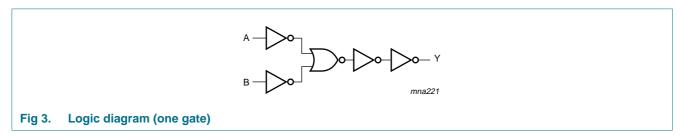
4. Marking

Table 2. Marking code

Type number	Marking code
74HC2G08DP	H08
74HCT2G08DP	T08
74HC2G08DC	H08
74HCT2G08DC	T08
74HC2G08GD	H08
74HCT2G08GD	T08

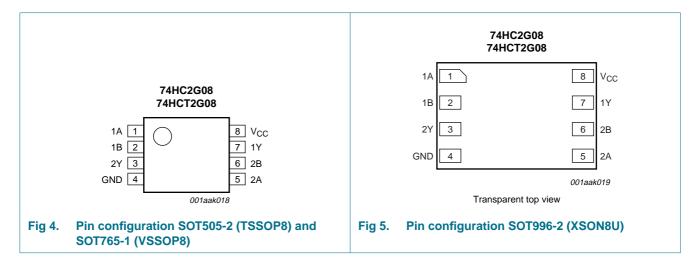
5. Functional diagram





6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table [1]

Input	Output	
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> -	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	[1] -	±20	mA
I _O	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	<u>[1]</u> -	25	mA
I _{CC}	supply current		<u>[1]</u> -	50	mA
I_{GND}	ground current		<u>[1]</u> –50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P_D	dynamic power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] -	300	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	7	4HC2G0	8	7	4HCT2G	08	Unit
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_{I}	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
	and fall rate	V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K. For XSON8U package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	–40 °C t	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
74HC2G0	8		•	'	•			'
V _{IH}	HIGH-level input	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	V
	voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output	$V_I = V_{IH}$ or V_{IL}						
	voltage	$I_O = -20 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	V
		$I_O = -20 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	V
		$I_O = -20 \mu A$; $V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.63	5.81	-	5.2	-	V
V_{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}						
	voltage	$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	per input pin; $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	10	-	20	μΑ
Cı	input capacitance		-	1.5	-	-	-	pF

Table 7. Static characteristics ...continued Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	–40 °C t	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
74HCT2G	808							
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	8.0	V
V _{OH}	HIGH-level output	$V_I = V_{IH}$ or V_{IL}						
	voltage	$I_O = -20 \mu A$; $V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	-	V
V_{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}						
	voltage	$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	10	-	20	μΑ
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V};$ $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A}$	-	-	375	-	410	μΑ
Cı	input capacitance		-	1.5	-	-	-	pF

^[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		-40	°C to +85	5 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	110 1 22 1 20 1	
74HC2G	08								
t _{pd}	propagation delay	nA and nB to nY; see Figure 6	[2]						
		V _{CC} = 2.0 V		-	26	95	-	110	ns
		V _{CC} = 4.5 V		-	9	19	-	22	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	9	-	-	-	ns
		V _{CC} = 6.0 V		-	8	16	-	20	ns
t _t	transition time	see Figure 6	[3]						
		$V_{CC} = 2.0 \text{ V}$		-	20	95	-	125	ns
		V _{CC} = 4.5 V		-	7	19	-	25	ns
		V _{CC} = 6.0 V		-	6	16	-	20	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	<u>[4]</u>	-	10	-	-	-	pF

 Table 8.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		-40 °C to +85 °C		Unit			
				Min	Typ[1]	Max	Min	Max	
74HCT20	G08		,						
t _{pd}	propagation delay	nA and nB to nY; see Figure 6	[2]						
•		V _{CC} = 4.5 V		-	14	30	-	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Figure 6</u>	[3]	-	7	19	-	22	ns
C_{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC} - 1.5 \text{ V}$	<u>[4]</u>	-	10	-	-	-	pF

- [1] All typical values are measured at $T_{amb} = 25$ °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_t is the same as t_{TLH} and t_{THL} .
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

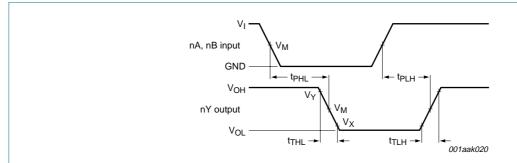
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



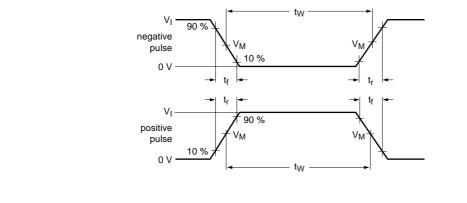
Measurement points are given in Table 9.

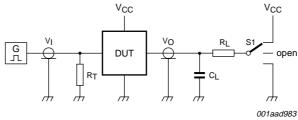
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Туре	Input	Output					
	V _M	V _M V _X V _Y					
74HC2G08	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}			
74HCT2G08	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}			





Test data is given in Table 10.

Definitions for test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

R_I = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Туре	Input		Load		S1 position
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}
74HC2G08	GND to V_{CC}	≤ 6 ns	15 pF, 50 pF	1 kΩ	open
74HCT2G08	GND to 3 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

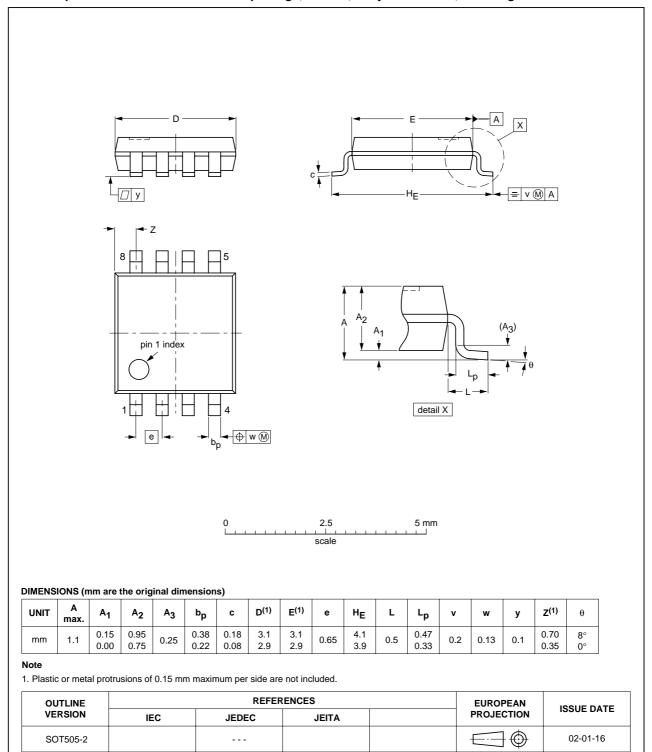
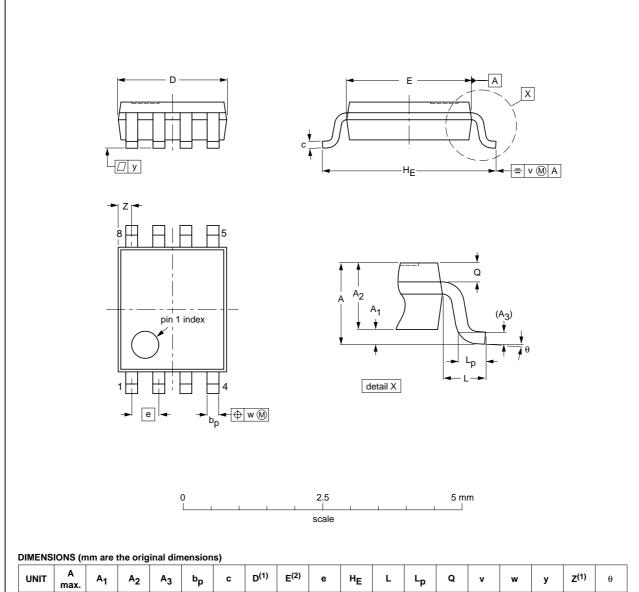


Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



U	INIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
r	mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT765-1		MO-187				02-06-07	

Fig 9. Package outline SOT765-1 (VSSOP8)

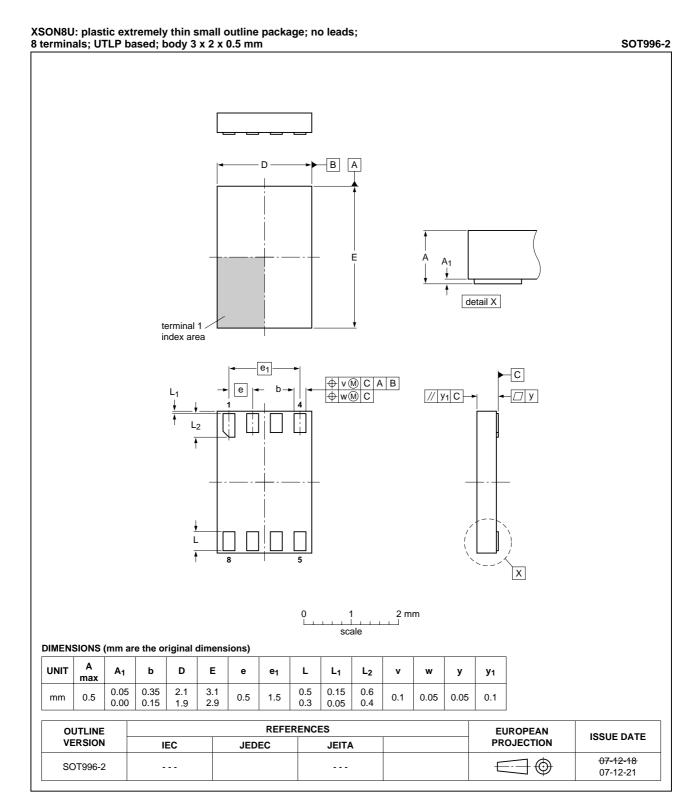


Fig 10. Package outline SOT996-2 (XSON8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC_HCT2G08_4	20090507	Product data sheet	-	74HC_HCT2G08_3				
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 							
	 Legal texts 	have been adapted to the n	ew company name whe	ere appropriate.				
	 Added type 	e number 74HC2G08GD and	174HCT2G08GD (XSC	N8U package)				
74HC_HCT2G08_3	20031022	Product specification	-	74HC_HCT2G08_2				
74HC_HCT2G08_2	20030203	Product specification	-	74HC_HCT2G08_1				
74HC_HCT2G08_1	20020710	Product specification	-	-				

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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