ET 438a
Automatic Control Systems Technology
Laboratory 3
Practical Integrator Response

Objective: Design a practical integrator circuit using common OP AMP circuits. Test the frequency response and phase shift of the integrator with a variable frequency sine wave signal. Compare the lab measurements to the theoretical calculations for the circuit to check the design. Observe the integrator output signals for various types of input signals commonly used in lab.

Theoretical Background

The mathematical operation of integration can be simulated by replacing the feedback resistor in an inverting OP AMP circuit and inserting a capacitor. This ideal integrator circuit is show in Figure 1.

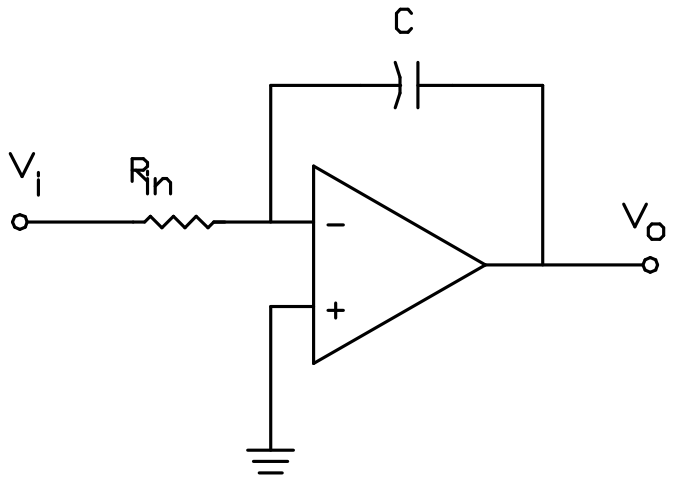

Figure 1. Ideal Integrator Circuit.

If ideal OP AMP circuit operation is assumed, no current will flow into the inverting terminal of the amplifier due to the infinite input impedance. Also, the voltage between the inverting and non-inverting terminal is equal due to the effects of the negative feedback. This means that the voltage at the inverting terminal is at ground potential. So:

$$I_f = -I_C$$

and

$$I_{in} = V_i/R_{in} \qquad (1)$$

The current in the capacitor is derived from:

$$i_c = -\ C\frac{dv}{dt}$$
$$V_o = -\ \frac{1}{C}\int\ i_c(t)\,dt \qquad (1)$$

Substituting Equation 1 into the integral equation above gives the input-output relationship of the ideal integrator circuit.

$$V_o(t) = -\frac{1}{R\,C}\int V_\in(t)\,dt \quad (a)$$
$$-\ \frac{1}{RC} = K_I \quad (b) \qquad (2)$$

The constant, K_I in Equation 2b is the integrator's gain. This integrator circuit sums current I_{in} into the feedback capacitor as long as a voltage is applied to the input. This current produces the output voltage of the circuit. In an ideal OP AMP, the output voltage will remain constant until a negative voltage is applied to the input. This will cause the voltage at the output to decrease. If the input voltage remains connected long enough, a practical OP AMP circuit will reach its power supply limits and saturate.

Another way of examining the circuit is to check its output gain response to sine waves of different frequencies. When the gain of these tests is represented in db and the frequency is plotted on a logarithmic scale, a Bode plot is produced. Bode plots are used to determine the stability of control systems and the frequency response of filter circuits.

To find the Bode plot of the ideal integrator circuit, the first step is to take the Lap7lace transform of the input-output relationship of Equation 2a. In the Laplace domain, integration in time converts to division by the complex variable s. (s represents the complex frequency - transient and sine response of a system.)

Taking the Laplace transform of 2a gives

$$L(v_o(t)) = V_o(s) \quad L(v_\in(t)) = V_\in(s) \quad (a)$$
$$V_o(s) = -\ \frac{1}{RC}\frac{1}{s}\ V_\in(s) \quad (b) \qquad (3)$$
$$\frac{V_o(s)}{V_\in(s)} = -\ \frac{1}{RCs} \quad (c)$$

Equation 3c is the transfer function of the ideal integrator circuit of Figure 1. To convert this to a Bode plot, we must replace the complex variable s with its imaginary part to find the change in circuit gain as frequency changes, and then the magnitude and phase shift of the transfer function can be found. The magnitude and phase of any complex quantity can be found from the following relationships:

$$|z| = \sqrt{Re(z)^2 + Im(z)^2} \qquad \phi = \tan^{-1}\left(\frac{Im(z)}{Re(z)}\right) \tag{4}$$

Where z = a complex value
Re(z) = the real part of z
Im(z) = the imaginary part of z
φ = the phase angle of z

The equations below show this theory applied to the ideal integrator circuit.
The equations in (5) show that the gain of this circuit increases as the frequency decreases. In fact, the circuit has an infinite gain to dc signals. The phase shift is a constant 90 degrees. This includes the 180 degree shift due to the inverting OP AMP configuration.

$$A_v(j\omega) = \frac{V_o(j\omega)}{V_{inn}(j\omega)} = -\frac{1}{RCj\omega}$$
$$|A_v(\omega)| = \frac{1}{RC\omega} \tag{5}$$
$$\phi = 180 - 90 = 90°$$

To construct the Bode plot the gain must be converted to db by using the formula

$$db(\omega) = 20 \log[A_v(\omega)]$$

The plot in Figure 2 shows the gain response of the ideal integrator circuit. The phase shift is a constant 90 degree over the entire range of frequency. Notice that the gain of the ideal integrator decreases with a constant rate over the range of the plot. The gain goes down 20 db for every decade (power of 10) in frequency increase. The value of 20 db is 1/10 of the initial gain value. As frequency continues to increase the gain will continue to diminish at the same rate. As frequency decrease, the gain will continue to increase. This increasing gain to lower frequencies produces a practical limit for using this circuit.

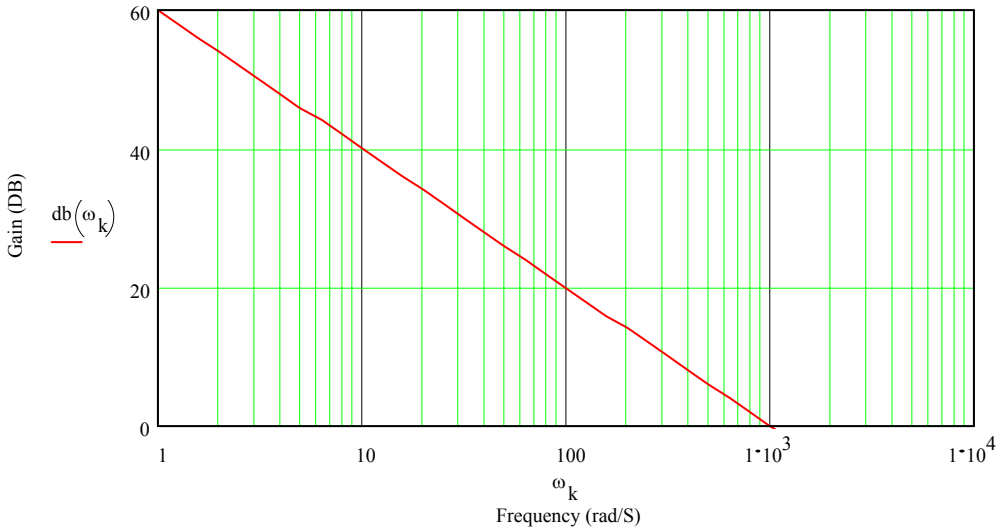

Figure 2. Frequency Response of an Idea Integrator **.**

The ideal integrator is not a practical circuit. The infinite gain to dc makes it impossible to construct because practical OP AMP require bias currents to flow in the inverting and non-inverting leads. These currents cause the capacitor to charge to the amplifier maximum output voltage even when on input is connect to the circuit. A practical OP AMP integrator approximates the characteristics of the ideal circuit, but has a fixed gain to dc.

Bias currents also produce offset voltage error in the output. This voltage error can be minimized by adding an appropriately sized resistor in the non-inverting input of the OP AMP. The bias currents flowing through these resistors will develop a common mode voltage (same magnitude and phase) at the inputs to the OP AMP. The common mode voltage will not be amplified.

Note that the gain of the circuit reaches 0 db (1) at the frequency given by the value

$$\omega_c = 1/RC$$

Where ω_c = the cutoff frequency of the device in rad/s

Practical OP AMP Integrators

Figure 3 shows a practical integrator circuit that overcomes the limitations of the ideal circuit and still simulates the integrator action that is useful in control applications. This

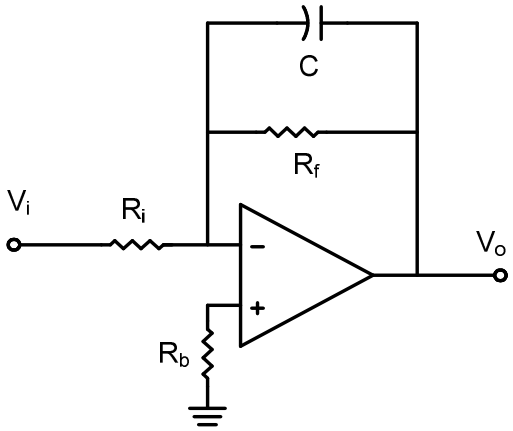

Figure 3. Practical Integrator Circuit with Bias Compensation.

circuit is also known as an active low pass filter. The value of resistor R_b is given by the parallel combination of the input and feed back resistances. In equation form this is:

$$R_b = R_i \,||\, R_f = R_f(R_i)/(R_f+R_i)$$

If the transfer characteristic of an inverting OP AMP circuit is written as the ratio of two impedances that have been converted using the rules of the Laplace transform, then the elements in the feedback branch can be combined using the rules of parallel impedances. The resulting value can then be substituted into the inverting gain formula and the transfer function written without a large amount of computation.
The following equations sketch out the mathematics used to find the transfer function for the practical integrator circuit.

$$v_o(t) = \frac{1}{C}\int i_c(t)\,dt \quad (a)$$

$$V_o(s) = \frac{1}{Cs}\, I_c(s) \quad (b) \qquad (6)$$

$$Z_f(s) = \frac{1}{Cs} \,||\, R_f = \frac{\frac{1}{Cs} \bullet R_f}{\frac{1}{Cs} + R_f} = \frac{R_f}{(1 + R_f C\, s)} \quad (c)$$

Taking the Laplace transform of 6a gives 6b. The term 1/Cs can be interpreted as impedance and used in the parallel resistance formula to give the simplified value of the resistor and capacitor in the feedback branch $Z_f(s)$ in 6c.

Substituting the value of $Z_f(s)$ into the gain gives the transfer function as a function of the complex variable s.

In the transfer function $A_v(s)$, the ratio of R_f/R_i, which is the same as the dc gain of an inverting OP AMP configuration, defines the gain the integrator has to a dc signal. This stabilizes the integrator and eliminates the saturation effects of the bias currents in the inverting terminal. The remainder of the transfer function defines the integrator action of the circuit.

$$\frac{V_o(s)}{V_i(s)} = \frac{-Z_f(s)}{Z_i(s)} \qquad Z_i(s) = R_i$$

$$\frac{V_o(s)}{V_i(s)} = \frac{\dfrac{-R_f}{1 + R_f C s}}{R_i} = \frac{-R_f}{R_i\,(1 + R_f C s)} = A_v(s) \tag{7}$$

If the variable s is replaced by $j\omega$, and the magnitude and phase angle determined from procedures similar to the ideal case, the gain and phase shift can be found for any sinusoidal input frequency. These relationships are

$$|A_v(\omega)| = \frac{R_f}{R_i} \bullet \left(\frac{1}{\sqrt{1 + R_f^2 C^2 \omega^2}} \right)$$

$$\phi(\omega) = 180° - \tan^{-1}(R_f C \omega) \tag{8}$$

The frequency in these equations is given in radians/sec. To convert the values to Hertz use the following relationship.

$$2\pi f = \omega$$

This function models the response of a low pass active filter. The ratio of R_f/R_i sets the gain in the pass band. The point where the gain begins to decrease is called the cutoff frequency. This is defined as the point where the gain is down 3 db from the gain in the pass band. A 3 db reduction in gain corresponds to a 0.707 reduction in the output voltage from the level in the pass band. This point is defined by

$$f_c = 1/2\pi R_f C \ \ Hz$$

$$\omega_c = 1/R_f C \ rad/S$$

After the cutoff point is reached, the gain of the circuit falls at a rate of -20 db/decade; just as in the ideal integrator circuit. To use the practical integrator as an integrator, the lowest frequency expected to be encountered in a control system must fall into this part of the circuit response. As "a rule of thumb" for designing a practical integrator in a control system, set f_c to be 1/10 of the lowest frequency encountered. Figures 4 and 5 show the Bode plots for the practical integrator circuit.

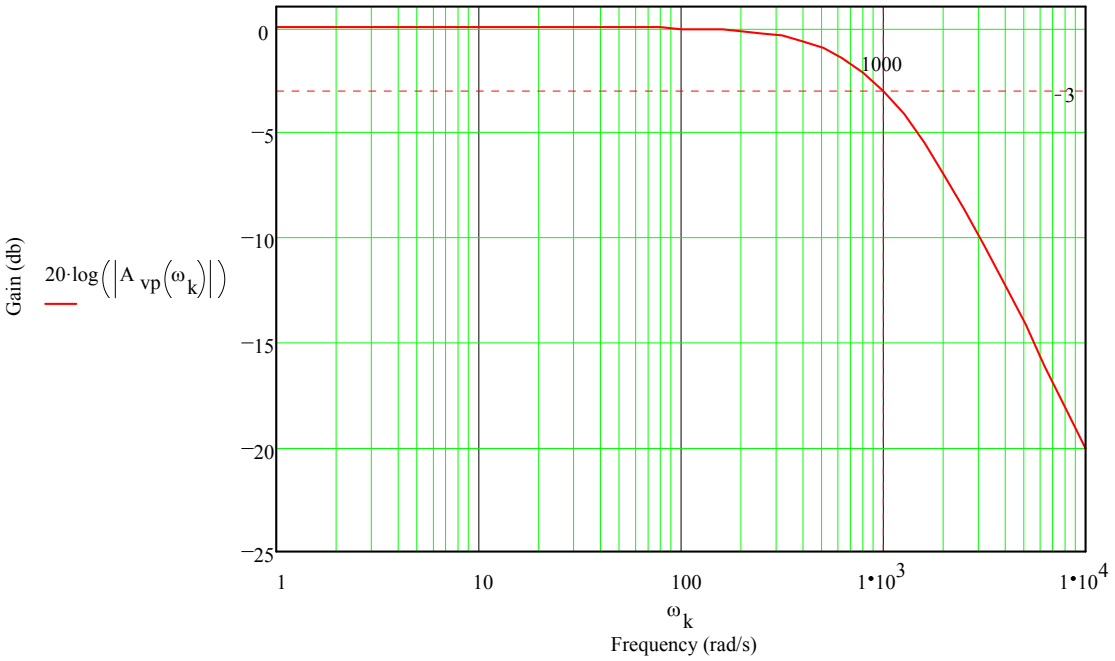

Figure 4. Gain Plot for Practical Integrator Circuit Showing Cutoff Frequency.

In this plot the dc gain of the integrator is 1 (0 db) and the cutoff frequency is 1000 rad/s (159.15 Hz). Increasing the dc gain of the practical integrator will increase this gain. Notice that the circuit's gain is relatively constant until 200 rad/s and then starts to decrease. It eventually takes the shape of the ideal integrator below the cutoff frequency.

The phase plot shown in Figure 5 includes the 180 degree phase shift due to the inverting action of the integrator circuit. The phase and the gain will both be important when the stability of control systems is examined.

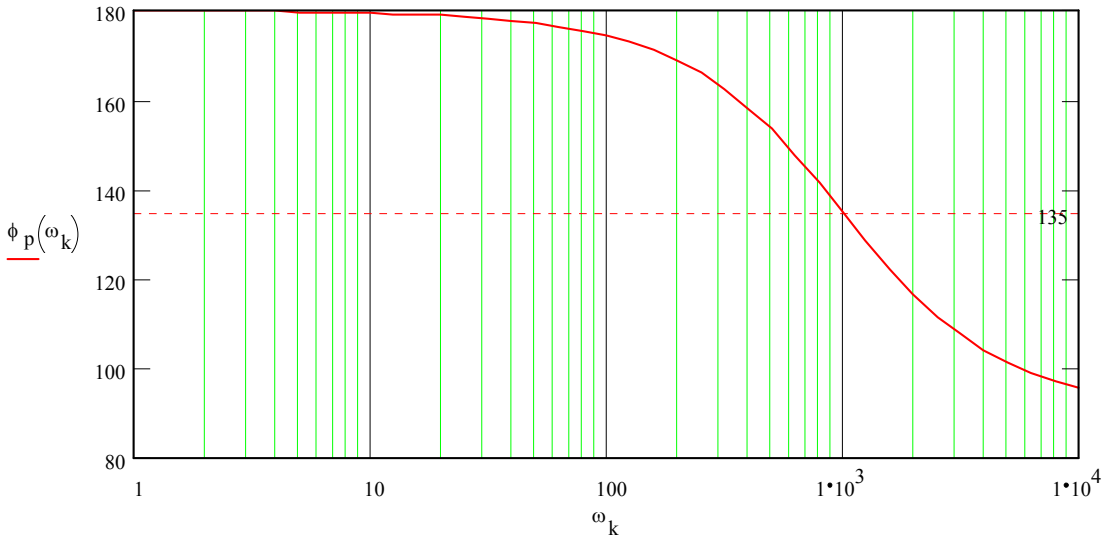

Figure 5. Phase Response of a Practical Integrator Circuit.

In the pass band, well below the frequency of 1000 rad/s, the only phase shift is from the inverting action of the OP AMP circuit. As the frequency increases the phase shift decreases to a value of 135 degrees at the cutoff frequency. The phase shift continues to decrease as the frequency increases and will asymptotically approach 90 degrees for high frequencies.

Time Response of a Practical Integrator to Common Waveforms

An integrator circuit simulates the mathematical operation of integration. Table 1 shows the results of applying common waveforms to the integrator and how these wave forms can be modeled using mathematical formulae.

Table 1. Integrator Time Response

Mathematical Model			Integrator Circuit	
Function	Equation	Integral (t)	Waveform In	Integrator Out
Constant	K	Kt	Square wave	Triangle
line	Kt	$Kt^2/2$	Triangle	Parabolic
sinusoidal	$A_{max}\sin(\omega t)$	$-A_{max}/\omega\cos(\omega t)$	Sine Wave	Shifted Sine

When an inverting integrator is used, the sign of the output will be opposite of the mathematical model integral. If a positive constant is applied to the practical integrator, (the positive half cycle of a square wave) the resulting output will be a negatively sloping part of a triangle wave.

To achieve the integral action on these wave forms the input frequency must follow the 1/10 f_c rule introduced above. The gain will be decreasing as the frequency increases as predicted by the Bode plots, so the magnitude of the output will be reduced.

Design Project - Practical Integrator Circuits and Responses.

Design a practical integrator circuit that has a dc gain of 5 and a cutoff frequency of 2.5 kHz. Document all the design values for the lab report. Test the design and compare it to the expected theoretical values.

1.) To check the frequency response, apply a 1 V_{p-p} sinusoidal ac signal to the input. Generate the test points for the Bode plot by applying the following signal frequencies:

100 Hz
200 Hz
500 Hz
700 Hz
1000 Hz
2.5 kHz
5 kHz
7 kHz
10 kHz
15 kHz
20 kHz

Maintain the input voltage constant and record the output voltage and phase shift for each of the listed frequencies. Use the input wave form as the reference for the phase measurements. Compute the integrator gain using the formula:

$$db = 20 \log[V_o / V_i]$$

Using the formula for the practical integrator derived above; compute the theoretical values of gain. Plot both the measured and theoretical values on the same semi-log (log scale on x-axis) plot. Discuss any deviations from the theoretical curve in the lab report.

Using the formula for the practical integrator phase shift, compute the theoretical values of phase shift (in degrees) and plot both the measured and theoretical values on the same semi-log plot (log scale on x-axis). Discuss any deviations from the theoretical curve in the lab report.

2a.) Apply a square wave signal with an amplitude of 1 Vp-p to the integrator. Use the following frequencies: 200 Hz, 1000 Hz, and 25 kHz. Sketch the changes in the output waveform as the frequency changes and note any changes in amplitude and shape. Discuss these data in the lab report. Determine the frequency where the integrator action begins to take place.

2b.) Apply a triangle wave signal with amplitude of 1 Vp-p to the integrator. Use the following frequencies: 200 Hz, 1000 Hz, and 25 kHz. Sketch the changes in the output waveform as the frequency changes and note any changes in amplitude and shape. Discuss these data in the lab report. Determine the frequency where the integrator action begins to take place.

3.) Derive the transfer function for the integrator designed in the lab by substituting the design values into the final formula in (7). Include the simplified transfer function in the lab report along with a schematic that shows all the computed design values.