

nRF52810 Objective Product Specification v0.5.4

Key features

- 2.4 GHz transceiver
 - -96 dBm sensitivity in Bluetooth® low energy mode
 - 2 Mbps Bluetooth® low energy mode
 - 1 Mbps, 2 Mbps supported data rates
 - TX power -20 to +4 dBm in 4 dB steps
 - Single-pin antenna interface
 - 4.6 mA peak current in TX (0 dBm)
 - 4.6 mA peak current in RX
 - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
 - 144 EEMBC CoreMark® score running from flash memory
 - 37.5 μA/MHz running from flash memory
 - 32.8 μA/MHz running from RAM
 - Serial wire debug (SWD)
 - Trace port
- Flexible power management
 - Supply voltage range 1.7 V-3.6 V
 - Fully automatic LDO and DC/DC regulator system
 - Fast wake-up using 64 MHz internal oscillator
 - 0.3 μA at 3 V in OFF mode, no RAM retention
 - $0.5~\mu\text{A}$ at 3 V in OFF mode with full 24 kB RAM retention
 - 1.3 µA at 3 V in ON mode, no RAM retention, wake on RTC
- Memory
 - 192 kB flash
 - 24 kB RAM
- Nordic SoftDevice ready
- Support for concurrent multi-protocol
- 12-bit, 200 ksps ADC 8 configurable channels with programmable gain
- 64 level comparator
- Temperature sensor
- 32 general purpose I/O pins
- 4-channel pulse width modulator (PWM) units with EasyDMA
- Digital microphone interface (PDM)
- 3x 32-bit timers with counter mode
- SPI master/slave with EasyDMA I2C compatible 2-Wire master/slave
- UART (CTS/RTS) with EasyDMA
- Programmable peripheral interconnect (PPI)
- Quadrature decoder (QDEC)
- AES HW encryption with EasyDMA
- Autonomous peripheral operation without CPU intervention using PPI and EasyDMA
- 2x real-time counter (RTC)
- External system
 - Single crystal operation
 - On-chip balun (single-ended RF)
 - Few external components
- Package variants
 - QFN48 package, 6 × 6 mm
 - QFN32 package, 5 × 5 mm

- Computer peripherals and I/O devices
 - Mouse
 - Keyboard
 - Mobile HID
 - CE remote controls
- Network processor
 - Wearables
 - Virtual reality headsets
- Health and medical
- Enterprise lighting
 - Industrial
 - Commercial
 - Retail
- Connectivity device in multi-chip solutions



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1 Revision history

Date	Version	Description
June 2017	0.5.4	Initial release



2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- · Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in Recommended operating conditions on page 17.

2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

Table 1: Defined document names

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 0.7.
Preliminary Product Specification (PPS)	This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0.
Product Specification (PS)	This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher.
	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id** (**Field Id**) row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.



Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value** Id, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.4 Registers

Table 2: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 **DUMMY**

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number		31	30	29 2	28 2	27 2	26 2!	5 2	24 2	3 22	2 21	20	19	18	17	16	15	14 :	13 :	12 :	11 1	10 9	9 8	3 7	6	5	4	3	2	1 0
Id						D	D C) [D					С	С	С							ı	3						А А
Reset 0x0005000	1	0	0	0	0	0	0 0) (0 (0	0	0	0	1	0	1	0	0	0	0	0	0 () (0	0	0	0	0	0	1 0
Id RW Field	Value Id	Va	lue						D	esci	ipti	on																		
A RW FIELD	A								Е	xam	ple	of a	fie	d w	/ith	sev	era	l er	ıun	era	ted	val	ues							
	Disabled	0							Т	he e	xan	ple	fea	tur	e is	dis	able	ed												
	Normal Mode	1							Т	he e	xam	ple	fea	tur	e is	ena	able	d ii	n no	rm	al n	nod	е							
	ExtendedMode	2							Т	he e	xam	ple	fea	tur	e is	ena	able	d a	lon	g w	ith	extr	a fı	ınct	ion	ality	,			
B RW FIELD	3								Ε	xam	ple	of a	de	ore	cate	d f	ield											Dep	rec	ated
	Disabled	0							Т	he c	ver	ride	fea	tur	e is	dis	able	ed												
	Enabled	1							Т	he c	ver	ride	fea	tur	e is	ena	able	d												
C RW FIELD									Ε	xam	ple	of a	fie	d w	/ith	a v	alid	rar	ige	of v	/alu	es								
	ValidRange	[2.	.7]						Ε	xam	ple	of a	llov	ved	val	ues	for	thi	s fi	eld										
D RW FIELD									Е	xam	ple	of a	fie	d w	/ith	no	res	tric	tior	on	the	e va	lue	5						



3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

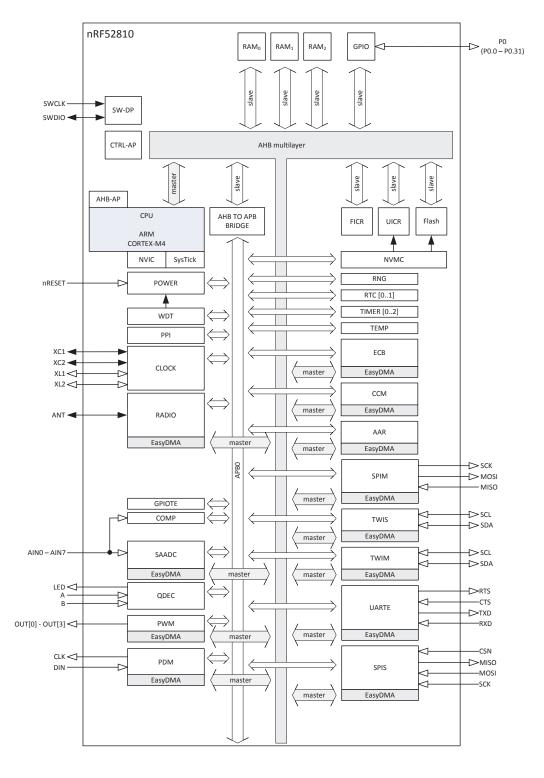


Figure 1: Block diagram



4 Pin assignments

The pin assignment figures and tables describe the pinouts for the product variants of the chip. There are also recommendations for how the GPIO pins should be configured, in addition to any usage restrictions.

4.1 QFN48 pin assignments

The nRF52810 QFN48 pin assignment table and figure describe the pinouts for this variant of the chip.

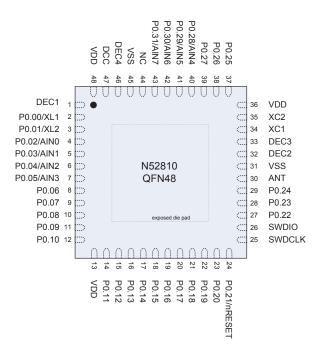


Figure 2: QFN48 pin assignments, top view

Table 3: QFN48 pin assignments

Di-	Name	Torres	Description
Pin	Name	Туре	Description
Left side of chip			
1	DEC1	Power	0.9 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AINO	Analog input	COMP input
			SAADC input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	COMP input
			SAADC input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	COMP input



Pin	Name	Туре	Description
			SAADC input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	COMP input
			SAADC input
8	P0.06	Digital I/O	General purpose I/O
9	P0.07	Digital I/O	General purpose I/O
10	P0.08	Digital I/O	General purpose I/O
11	P0.09	Digital I/O	General purpose I/O
12	P0.10	Digital I/O	General purpose I/O
Bottom side of chip			
13	VDD	Power	Power supply
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
10	DO 1E	Digital I/O	General purpose I/O
18	P0.15	Digital I/O	General purpose I/O
19	P0.16	Digital I/O	General purpose I/O
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
24	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
Right side of chip			G
25	SWDCLK	Digital input	Serial wire debug clock input for debug
		Ç ,	and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and
			programming
27	P0.22	Digital I/O	General purpose I/O
28	P0.23	Digital I/O	General purpose I/O
29	P0.24	Digital I/O	General purpose I/O
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground (radio supply)
32	DEC2	Power	1.3 V regulator supply decoupling (radio
			supply)
33	DEC3	Power	Power supply decoupling
34	XC1	Analog input	Connection for 32 MHz crystal
35	XC2	Analog input	Connection for 32 MHz crystal
36	VDD	Power	Power supply
Top side of chip			
37	P0.25	Digital I/O	General purpose I/O ¹
38	P0.26	Digital I/O	General purpose I/O ¹
39	P0.27	Digital I/O	General purpose I/O ¹
40	P0.28	Digital I/O	General purpose I/O ¹
	AIN4	Analog input	COMP input
		-	
41	DO 20	Digital I/O	SAADC input General purpose I/O ¹
41	P0.29	Digital I/O	
	AIN5	Analog input	COMP input
			SAADC input
42	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	COMP input
	Allivo	Analog Input	
43	P0.31	Digital I/O	SAADC input General purpose I/O pin



Pin	Name	Туре	Description
	AIN7	Analog input	COMP input
			SAADC input
44	NC		No connect
			Leave unconnected
45	VSS	Power	Ground
46	DEC4	Power	1.3 V regulator supply decoupling
			Input from DC/DC regulator
			Output from 1.3 V LDO
47	DCC	Power	DC/DC regulator output
48	VDD	Power	Power supply
Bottom of chip			
Die pad	VSS	Power	Ground pad
			Exposed die pad must be connected to ground (VSS) for proper device
			operation.
			operation.

4.2 QFN32 pin assignments

The nRF52810 QFN32 pin assignment table and figure describe the pinouts for this variant of the chip.

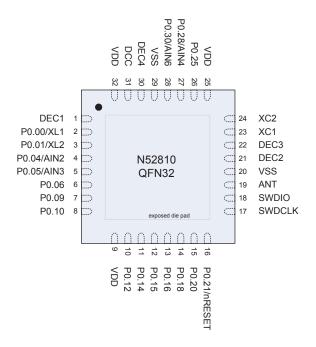


Figure 3: QFN32 pin assignments, top view

Table 4: QFN32 pin assignments

Pin	Name	Туре	Description
Left side of chip			

See GPIO pins located near the radio on page 15 for more information.



Pin	Name	Туре	Description
1	DEC1	Power	0.9 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	COMP input
	7.11.12	, manag mipat	
5	P0.05	Digital I/O	SAADC input
3		Digital I/O	General purpose I/O
	AIN3	Analog input	COMP input
			SAADC input
6	P0.06	Digital I/O	General purpose I/O
7	P0.09	Digital I/O	General purpose I/O ²
8	P0.10	Digital I/O	General purpose I/O ²
Bottom side of chip			
9	VDD	Power	Power supply
10 11	P0.12 P0.14	Digital I/O Digital I/O	General purpose I/O General purpose I/O
12	P0.15	Digital I/O	General purpose I/O
13	P0.16	Digital I/O	General purpose I/O
14	P0.18	Digital I/O	General purpose I/O
		- ·	
15	P0.20	Digital I/O	Single wire output General purpose I/O
16	P0.21	Digital I/O	General purpose I/O
Disha side of ship	nRESET		Configurable as pin reset
Right side of chip 17	SWDCLK	Digital input	Serial wire debug clock input for debug
17	SWEEK	Digital Input	and programming
18	SWDIO	Digital I/O	Serial wire debug I/O for debug and
		-	programming
19	ANT	RF	Single-ended radio antenna connection
20	VSS	Power	Ground (radio supply)
21	DEC2	Power	1.3 V regulator supply decoupling (radio
			supply)
22	DEC3	Power	Power supply decoupling
23	XC1	Analog input	Connection for 32 MHz crystal
24 Top side of chip	XC2	Analog input	Connection for 32 MHz crystal
25	VDD	Power	Power supply
26	P0.25	Digital I/O	General purpose I/O ²
27	P0.28	Digital I/O	General purpose I/O ²
		-	
	AIN4	Analog input	COMP input
			SAADC input
28	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	COMP input
			SAADC input
29	VSS	Power	Ground
30	DEC4	Power	1.3 V regulator supply decoupling
			Input from DC/DC regulator
31	DCC	Power	Output from 1.3 V LDO DC/DC regulator output
32	VDD	Power	Power supply
			. o supp.y



Pin	Name	Туре	Description
Die pad	VSS	Power	Ground pad
			Exposed die pad must be connected
			to ground (VSS) for proper device
			operation.

4.3 GPIO pins located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Table 5: GPIO recommended usage on page 15 identifies some GPIO pins that have recommended usage guidelines for maximizing radio performance in an application.

Table 5: GPIO recommended usage

GPIO	QFN48 pin	QFN32 pin	Recommended usage
P0.25	37	26	Low drive, low frequency I/O only.
P0.26	38		
P0.27	39		
P0.28	40	27	
P0.29	41		

² See *GPIO pins located near the radio* on page 15 for more information.



5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 6: Absolute maximum ratings

V V
V
V
V
dBm
°C
kV
V
Write/erase cycles





6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 7: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t _{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
TĀ	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.



7 CPU

The ARM® Cortex®-M4 processor has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- · Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- · Hardware divide
- 8 and 16-bit single instruction multiple data (SIMD) instructions

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. The section *Electrical specification* on page 18 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

The ARM System Timer (SysTick) is present on the device. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

7.1 Electrical specification

7.1.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark® benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Тур.	Max.	Units
W _{FLASH}	CPU wait states, running from flash	0		2	
W_{RAM}	CPU wait states, running from RAM			0	
I _{DDFLASH}	CPU current, running from flash, LDO		4.0		mA
I _{DDFLASHDCDC}	CPU current, running from flash, DCDC 3V		2.4		mA
I _{DDRAM}	CPU current, running from RAM, LDO		3.8		mA
I _{DDRAMDCDC}	CPU current, running from RAM, DCDC 3V		2.1		mA
I _{DDFLASH/MHz}	CPU efficiency, running from flash, LDO		62.5		μΑ/
					MHz
I _{DDFLASHDCDC/MHz}	CPU efficiency, running from flash, DCDC 3V		37.5		μΑ/
					MHz
CM_{FLASH}	CoreMark ³ , running from flash		144		CoreN
CM _{FLASH/MHz}	CoreMark per MHz, running from flash		2.25		CoreN
					MHz
CM _{FLASH/mA}	CoreMark per mA, running from flash, DCDC 3V		60		CoreN
					mA

7.2 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

³ Using IAR v6.50.1.4452 with flags --endian=little --cpu=Cortex-M4 -e --fpu=VFPv4 sp -Ohs --no size constraints



Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	30 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little endian
Bit-banding	Bit banded memory	NO
DWT	Data watchpoint and trace	NO
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating-point unit	NO
DAP	Debug access port	YES
ETM	Embedded trace macrocell	NO
ITM	Instrumentation trace macrocell	NO
TPIU	Trace port interface unit	NO
ETB	Embedded trace buffer	NO
FPB	Flash patch and breakpoint unit	YES
HTM	AMBA® AHB trace macrocell	NO



8 Memory

The nRF52810 contains flash and RAM that can be used for code and data storage.

The amount of RAM and flash will vary depending on variant, see Table 8: Memory variants on page 20.

Table 8: Memory variants

Device name	RAM	Flash	Comments
nRF52810-QFAA	24 kB	192 kB	

The CPU and the EasyDMA can access memory via the AHB multilayer interconnect. The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 4: Memory layout* on page 20.

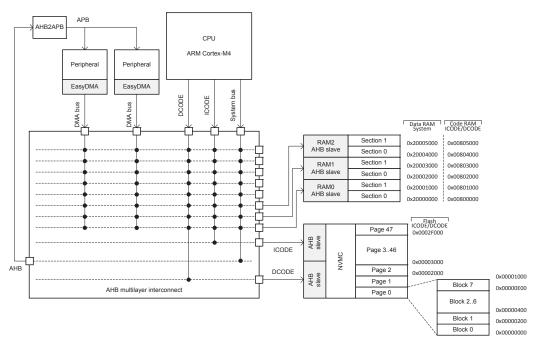


Figure 4: Memory layout

See *AHB multilayer* on page 23 and *EasyDMA* on page 24 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into multiple RAM AHB slaves.

Each RAM AHB slave is connected to two 4-kilobyte RAM sections, see Section 0 and Section 1 in *Figure 4: Memory layout* on page 20.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 67).

8.2 Flash - Non-volatile memory

The flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased, and also on how it can be written.



Writing to flash is managed by the non-volatile memory controller (NVMC), see *NVMC* — *Non-volatile memory controller* on page 26.

The flash is divided into multiple 4 kB pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in, *Figure 4: Memory layout* on page 20. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 5: Memory map* on page 21. As described in *Memory* on page 20, Code RAM and Data RAM are the same physical RAM.

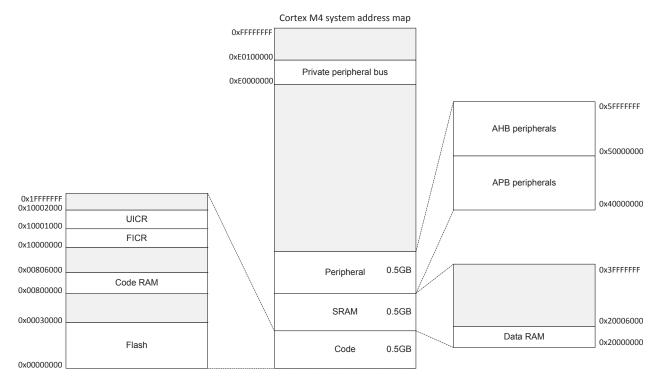


Figure 5: Memory map

8.4 Instantiation

Table 9: Instantiation table

ID	Base Address	Peripheral	Instance	Description
0	0x40000000	CLOCK	CLOCK	Clock control
0	0x40000000	BPROT	BPROT	Block protect
0	0x40000000	POWER	POWER	Power control
1	0x40001000	RADIO	RADIO	2.4 GHz radio
2	0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA
3	0x40003000	TWIS	TWIS0	Two-wire interface slave
3	0x40003000	TWIM	TWIM0	Two-wire interface master
4	0x40004000	SPIS	SPIS0	SPI slave
4	0x40004000	SPIM	SPIM0	SPI master
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events
7	0x40007000	SAADC	SAADC	Analog-to-digital converter
8	0x40008000	TIMER	TIMER0	Timer 0
9	0x40009000	TIMER	TIMER1	Timer 1
10	0x4000A000	TIMER	TIMER2	Timer 2
11	0x4000B000	RTC	RTC0	Real-time counter 0
12	0x4000C000	TEMP	TEMP	Temperature sensor



ID	Base Address	Peripheral	Instance	Description
13	0x4000D000	RNG	RNG	Random number generator
14	0x4000E000	ECB	ECB	AES Electronic Codebook (ECB) mode block encryption
15	0x4000F000	CCM	CCM	AES CCM mode encryption
15	0x4000F000	AAR	AAR	Accelerated address resolver
16	0x40010000	WDT	WDT	Watchdog timer
17	0x40011000	RTC	RTC1	Real-time counter 1
18	0x40012000	QDEC	QDEC	Quadrature decoder
19	0x40013000	COMP	COMP	General purpose comparator
20	0x40014000	SWI	SWI0	Software interrupt 0
20	0x40014000	EGU	EGU0	Event generator unit 0
21	0x40015000	EGU	EGU1	Event generator unit 1
21	0x40015000	SWI	SWI1	Software interrupt 1
22	0x40016000	SWI	SWI2	Software interrupt 2
23	0x40017000	SWI	SWI3	Software interrupt 3
24	0x40018000	SWI	SWI4	Software interrupt 4
25	0x40019000	SWI	SWI5	Software interrupt 5
28	0x4001C000	PWM	PWM0	Pulse-width modulation unit 0
29	0x4001D000	PDM	PDM	Pulse-density modulation (digital microphone interface)
30	0x4001E000	NVMC	NVMC	Non-volatile memory controller
31	0x4001F000	PPI	PPI	Programmable peripheral interconnect
0	0x50000000	GPIO	P0	General purpose input and output
N/A	0x10000000	FICR	FICR	Factory information configuration
N/A	0x10001000	UICR	UICR	User information configuration



9 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to the slave devices using an interconnection matrix. The bus masters are assigned priorities. Priorities are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority
 is granted the access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- · Bus masters that have the same priority are mutually exclusive, thus cannot be used concurrently.

Below is a list of bus masters in the system and their priorities.

Table 10: AHB bus masters (listed in priority order, highest to lowest)

Bus master name	Description
CPU	
SPIMO/SPISO	Same priority and mutually exclusive
RADIO	
CCM/ECB/AAR	Same priority and mutually exclusive
SAADC	
UARTE0	
TWIM0/TWIS0	Same priority and mutually exclusive
PDM	
D\M/M	

Defined bus masters are the CPU and the peripherals with implemented EasyDMA, and the available slaves are RAM AHB slaves. How the bus masters and slaves are connected using the interconnection matrix is illustrated in *Memory* on page 20.



10 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in *Figure 6: EasyDMA example* on page 24.

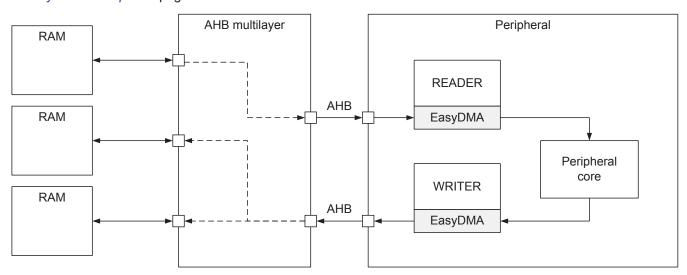


Figure 6: EasyDMA example

An EasyDMA channel is usually implemented like illustrated by the code below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000.
- · Process the data.
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005.

The memory layout of these buffers is illustrated in Figure 7: EasyDMA memory layout on page 25.



0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 7: EasyDMA memory layout

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

10.1 EasyDMA array list

EasyDMA is able to operate in a mode called array list.

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA array list can be implemented by using the data structure ArrayList_type as illustrated in the code example below:

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

The data structure only includes a buffer with size equal to the size of READER.MAXCNT register. EasyDMA uses the READER.MAXCNT register to determine when the buffer is full.

READER.PTR = &ReaderList

T .				
0x20000000 : ReaderList[0]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000004 : ReaderList[1]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000008 : ReaderList[2]	buffer[0]	buffer[1]	buffer[2]	buffer[3]

Figure 8: EasyDMA array list



11 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing of the internal flash memory and the UICR (user information configuration registers).

The CONFIG register is used to enable the NVMC for writing (CONFIG.WEN) and erasing (CONFIG.EEN), see *CONFIG* on page 27. The user must make sure that writing and erasing are not enabled at the same time. Having both enabled at the same time may result in unpredictable behavior.

11.1 Writing to flash

When writing is enabled, full 32-bit words are written to word-aligned addresses in flash.

As illustrated in *Memory* on page 20, the flash is divided into multiple pages that in turn are divided into multiple blocks. The same block in flash can only be written n_{WRITE} number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 20 for block size.

The NVMC is only able to write 0 to bits in the flash that are erased (set to 1). It cannot rewrite a bit back to 1. Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits, write the data as a full 32-bit word and set all the bits that should remain unchanged in the word to 1. Note that the restriction on the number of writes (see above) still applies in this case.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

The time it takes to write a word to flash is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to flash.

11.2 Erasing a page in flash

When erase is enabled, the flash memory can be erased page by page using the ERASEPAGE register.

After erasing a flash page, all bits in the page are set to 1. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.

11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR or ERASEALL. The time it takes to write a word to UICR is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to UICR.

11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to 1. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.

11.5 Erase all

When erase is enabled, flash and UICR can be erased completely in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).



The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted while the NVMC performs the erase operation.

11.6 Registers

Table 11: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non-volatile memory controller	

Table 12: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPCR1	0x508	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEPAGE	0x508	Register for erasing a page in code area	
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing user information configuration registers	

11.6.1 READY

Address offset: 0x400

Ready flag

Bit	numbe	er		31 30	29	28	27 2	26 2	25 2	4 2	3 2	2 2:	1 20	19	18	17	16	15	14 1	3 1	2 11	. 10	9	8	7	6	5	4	3	2 2	1 0
Id																															Α
Res	et OxC	0000000		0 0	0	0	0	0	0 0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	2					D	esc	ript	ion																		
Α	R	READY								Ν	IVM	1C is	rea	dy (or b	usy															
			Busy	0						Ν	IVM	1C is	bus	sy (c	ngo	oing	wr	ite	or e	ase	оре	erati	ion)								
			Ready	1						Ν	IVM	1C is	rea	dy																	

11.6.2 **CONFIG**

Address offset: 0x504 Configuration register

Bit	numbe	er		31	1 30	29	28	3 27	26	25	24	1 23	3 22	2 2:	1 2	0 1	9 1	18	17	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	ript	tion	1																				
Α	RW	WEN										Pr	ogı	ram	n m	em	ory	/ a	cce	ss r	no	de.	It is	s st	ron	gly	rec	omi	ner	nde	d					Τ
												to	ac	tiva	ite	era	ise	an	d w	/rit	e n	nod	es (only	y w	hen	the	y a	re a	acti	vely	/				
												us	ed																							
			Ren	0								Re	ead	on	ly a	ICCE	ess																			
			Wen	1								W	rite	e er	nab	led																				
			Een	2								Er	ase	e en	nabl	led																				

11.6.3 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in code area. Equivalent to ERASEPAGE.



Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																			
Α	RW	ERASEPCR1										Reg	iste	er fo	or e	ras	ing	ар	age	in	coc	le a	rea	. Ec	viup	/ale	nt t	to						
												ER/	SFI	PAG	iF																			

11.6.4 ERASEPAGE

Address offset: 0x508

Register for erasing a page in code area

Bit	numbe	er		31	30	29	28 2	27	26 2	25 2	4 23	3 22	21	20	19 3	18	17 1	.6 1	15 1	4 13	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				А	Α	Α	Α	Α	Α /	ДД	A A	Α	Α	Α	Α	Α	Α ,	Δ,	A A	Д Д	. A	A	Α	Α	Α	Α	Α	Α	A	Α Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																		
Α	RW	ERASEPAGE									Re	egist	er fo	or s	tart	ing	era	se o	of a	pag	e ir	coo	de a	rea								
											Tł	ne va	alue	is t	he a	add	ress	to	the	pag	ge t	o be	era	sed	(ad	dre	esse	s o	f			
											fir	st w	ord	in	page	e). I	Note	e th	nat t	he e	eras	e m	ust	be e	enab	oled	d us	ing				
											C	ONF	IG.W	VEN	l bet	for	e the	e pa	age	can	be	eras	ed.	Att	emp	ots	to e	ras	e			
											pa	ages	tha	t ar	e ou	utsi	de t	he	cod	e ar	ea ı	may	res	ult i	n ur	nde	sira	ble	9			
											be	ehav	iour	r, e.	g. tł	he v	wroi	ng p	page	e ma	y b	e er	ase	d.								

11.6.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory

Bit r	umbe	r		31	30 2	29	28	27	26	25	24	1 2	3 2	2 2	21	20	19	18	1	7 1	6 1	.5	L4	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	C	C)	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue							D	esc	rip	otic	n																					
Α	RW	ERASEALL										Е	ase	e a	ll n	on-	-vc	lat	ile	me	m	ory	ind	clud	din	g U	ICR	reg	iste	rs.	No	te					
												tł	at	th	e e	ras	e n	nus	t b	e e	na	ble	dι	ısin	ıg (ON	IFIG	i.W	EN	bef	ore	th	е				
												n	on-	vo	lati	le i	me	mc	ry	ca	n b	e e	ras	ed													
			NoOperation	0								N	0 0	pe	rat	ion	1																				
			Erase	1								Si	art	eı	rase	e of	f cl	nip																			

11.6.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in code area. Equivalent to ERASEPAGE.

Bit	numbe	er		31	30	29	28	27	26	25	24	23 2	22 2	21 :	20 :	19 :	18 1	.7 1	6 1	5 1	4 1	3 1:	2 1	1 10) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A A	Α Α	Α Α	. Δ	\ <i>A</i>	A	Α	Α	Α	Α	Α	Α	A	Δ.	А А
Res	et 0 x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0) () (0) (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	ERASEPCR0										Reg	iste	r fo	or st	art	ing	era	se o	of a	pag	e ir	n cc	de a	area	a. Ed	quiv	ale	nt to)			
												ERA	SEF	PAG	ŝΕ.																		

11.6.7 ERASEUICR

Address offset: 0x514

Register for erasing user information configuration registers



Bit	numbe	er		31	1 30	29	28	8 27	7 26	5 2!	5 2	4 2	3 2	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0x0	0000000		0	0	0	0	0	0	0) (0 (0 () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							0	esc	rip	tio	n																				
Α	RW	ERASEUICR										F	legi	ster	r sta	arti	ing	era	ise	of a	all u	ıseı	inf	orr	nat	ion	cor	nfig	ura	tior	1					
												r	egis	ter	s. N	lot	e tł	nat	the	er	ase	mı	ıst	be	ena	ble	d us	sing	5							
												C	ON	FIG	i.W	ΕN	be	fore	e th	ie l	JICI	R ca	n b	e e	ras	ed.										
			NoOperation	0								١	lo o	per	rati	on																				
			Erase	1								S	tart	era	ase	of	UIC	CR																		

11.7 Electrical specification

11.7.1 Flash programming

Symbol	Description	Min.	Тур.	Max.	Units
n _{WRITE,BLOCK}	Amount of writes allowed in a block before erase				
n _{WRITE}	Number of times an address can be written between erase ⁴				
t _{WRITE}	Time to write one 32-bit word	67.5		338	μs
t _{ERASEPAGE}	Time to erase one page		80		ms
t _{ERASEALL}	Time to erase all flash		80		ms
I _{write}	Flash write current				mA
l _{erasepage}	Flash erase page current				mA
I _{eraseall}	Flash erase all current				mA

⁴ The page must be erased when either of $n_{WRITE,BLOCK}$ or n_{WRITE} is not satisfied



12 BPROT — Block protection

The mechanism for protecting non-volatile memory can be used to prevent erroneous application code from erasing or writing to protected blocks.

Non-volatile memory can be protected from erases and writes depending on the settings in the CONFIG registers. One bit in a CONFIG register represents one protected block of 4 kB. There are multiple CONFIG registers to cover the whole range of the flash. *Figure 9: Protected regions of program memory* on page 30 illustrates how the CONFIG bits map to the program memory space.

Important: If an erase or write to a protected block is detected, the CPU will hard fault. If an ERASEALL operation is attempted from the CPU while any block is protected it will be blocked and the CPU will hard fault.

On reset, all the protection bits are cleared. To ensure safe operation, the first task after reset must be to set the protection bits. The only way of clearing protection bits is by resetting the device from any reset source.

The protection mechanism is turned off when in debug mode (a debugger is connected) and the DISABLEINDEBUG register is set to disable.

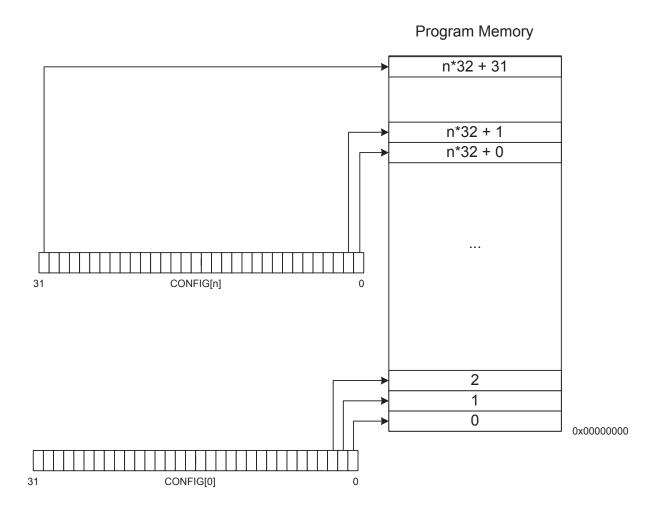


Figure 9: Protected regions of program memory



12.1 Registers

Table 13: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	BPROT	BPROT	Block protect	

Table 14: Register Overview

Register	Offset	Description	
CONFIG0	0x600	Block protect configuration register 0	
CONFIG1	0x604	Block protect configuration register 1	
DISABLEINDEBUG	0x608	Disable protection mechanism in debug mode	
	0x60C		Reserved

12.1.1 CONFIG0

Address offset: 0x600

Block protect configuration register 0

Bit	numbe	er		3	1 30	29	28	27	26	25	24	23	3 22	21	20	19	18	17	16	15	14	13	12	2 1	1 10) 9	8	7	6	5	4	3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	V	U	Т	S	R	Q	Р	О	Ν	N	1 L	. K	J	-1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	(0	C	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue	9						De	escri	ptic	n																				
Α	RW	REGION0										Er	nable	pro	ote	ctio	on f	for	reg	ion	٥. ١	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	I																	
В	RW	REGION1										Er	nable	pro	ote	ctio	on f	for	reg	ion	1. \	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	ı																	
С	RW	REGION2										Er	nable	pro	ote	ctio	on f	for	reg	ion	2. ۱	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	I																	
D	RW	REGION3										Er	nable	pro	ote	ctio	on f	for	reg	ion	3. ۱	Nri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	ł																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	ı																	
Е	RW	REGION4										Er	nable	pro	ote	ctio	on f	for	reg	ion	4. ۱	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	ı																	
F	RW	REGION5										Er	nable	pro	ote	ctio	on f	for	reg	ion	5. ۱	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	ł																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	ı																	
G	RW	REGION6										Er	nable	pro	ote	ctio	on f	for	reg	ion	6. ۱	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	1																	
Н	RW	REGION7										Er	nable	pro	ote	ctio	on f	for	reg	ion	7. ۱	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	ł																	
			Enabled	1								Pr	rotec	tior	n er	nab	led	l																	
I	RW	REGION8											nable						reg	ion	8. ۱	٧ri	te '	'0'	has	no	effe	ct.							
			Disabled	0								Pr	rotec	tior	n di	isab	lec	t																	
			Enabled	1									rotec																						
J	RW	REGION9											nable						reg	ion	9.١	۷ri	te '	'0'	has	no	effe	ct.							
			Disabled	0									rotec																						
			Enabled	1									rotec																						
K	RW	REGION10											nable						reg	ion	10.	Wı	rite	9 '0	ha:	s n	o ef	fect							
			Disabled	0									rotec																						
			Enabled	1									rotec																						
L	RW	REGION11										Er	nable	pro	ote	ctio	on f	for	reg	ion	11.	Wı	rite	9 '0	ha:	s n	ef	fect							



Bit r	numbe	er		31 30	29 28	3 27 2	26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z \	'XWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0	0 0	0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	:			Description
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
M	RW	REGION12						Enable protection for region 12. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
N	RW	REGION13						Enable protection for region 13. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
0	RW	REGION14						Enable protection for region 14. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Р	RW	REGION15						Enable protection for region 15. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Q	RW	REGION16						Enable protection for region 16. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
R	RW	REGION17						Enable protection for region 17. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
S	RW	REGION18						Enable protection for region 18. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Т	RW	REGION19						Enable protection for region 19. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
U	RW	REGION20						Enable protection for region 20. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
V	RW	REGION21						Enable protection for region 21. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
W	RW	REGION22	5					Enable protection for region 22. Write '0' has no effect.
			Disabled	0				Protection disabled
.,	5144	250101100	Enabled	1				Protection enabled
Χ	RW	REGION23	8:-11-1	0				Enable protection for region 23. Write '0' has no effect.
			Disabled	0				Protection disabled
V	DVA	DECIONA	Enabled	1				Protection enabled
Υ	KVV	REGION24	Disabled	0				Enable protection for region 24. Write '0' has no effect. Protection disabled
			Disabled	0				Protection enabled
7	DVA	DECIONAL	Enabled	1				
Z	RVV	REGION25	Disabled	0				Enable protection for region 25. Write '0' has no effect.
			Disabled	0				Protection disabled
	DVA	DECIONAC	Enabled	1				Protection enabled
а	KVV	REGION26	Disabled	0				Enable protection for region 26. Write '0' has no effect.
			Disabled	0				Protection disabled
h	D\A/	PEGION27	Enabled	1				Protection enabled Enable protection for region 27. Write '0' has no effect
b	r(VV	REGION27	Disabled	0				Enable protection for region 27. Write '0' has no effect.
			Disabled	0				Protection enabled
	Ditt	DECIONAS	Enabled	1				Protection enabled
С	кW	REGION28	Disabled	0				Enable protection for region 28. Write '0' has no effect.
			Disabled	0				Protection disabled
		250101100	Enabled	1				Protection enabled
d	RW	REGION29	P: 11 1	0				Enable protection for region 29. Write '0' has no effect.
			Disabled	0				Protection disabled



Bit	number		31	. 30	29	28 2	7 2	6 25	5 24	4 23	3 22	21	20	19	18	17 :	16	15 :	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id			f	е	d	c ł	о а	a Z	Y	×	W	٧	U	Т	S	R	Q	Р	О	N I	M	_ K	J	-1	Н	G	F	Ε	D (C E	3 A
Res	et 0x00000000		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0) (0
Id	RW Field	Value Id	Va	lue						D	escr	iptio	on																		
		Enabled	1							Pr	ote	ctio	n er	nabl	ed																
е	RW REGION30									Er	nabl	e pr	ote	ctio	n f	or re	egic	on 3	٥. ١	Vrit	e '0	' ha	s no	eff	ect.						
		Disabled	0							Pr	ote	ctio	n di	sab	led																
		Enabled	1							Pr	ote	ctio	n er	nabl	ed																
f	RW REGION31									Er	nabl	e pr	ote	ctio	n f	or re	egic	on 3	1. \	Vrit	e '0	' ha	s no	eff	ect.						
		Disabled	0							Pr	ote	ctio	n di	sab	led																
		Enabled	1							Pr	ote	ctio	n er	nabl	ed																

12.1.2 CONFIG1

Address offset: 0x604

Block protect configuration register 1

	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
A	RW	REGION32			Enable protection for region 32. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
В	RW	REGION33			Enable protection for region 33. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
С	RW	REGION34			Enable protection for region 34. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
D	RW	REGION35			Enable protection for region 35. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
E	RW	REGION36			Enable protection for region 36. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
F	RW	REGION37			Enable protection for region 37. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
G	RW	REGION38			Enable protection for region 38. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Н	RW	REGION39			Enable protection for region 39. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
ı	RW	REGION40			Enable protection for region 40. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
J	RW	REGION41			Enable protection for region 41. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
K	RW	REGION42			Enable protection for region 42. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
L	RW	REGION43			Enable protection for region 43. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
М	RW	REGION44			Enable protection for region 44. Write '0' has no effect.
			Disabled	0	Protection disabled



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id		P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Enabled	1 Protection enabled
N RW REGION45		Enable protection for region 45. Write '0' has no effect.
	Disabled	0 Protection disabled
	Enabled	1 Protection enabled
O RW REGION46		Enable protection for region 46. Write '0' has no effect.
	Disabled	0 Protection disabled
	Enabled	1 Protection enabled
P RW REGION47		Enable protection for region 47. Write '0' has no effect.
	Disabled	0 Protection disabled
	Enabled	1 Protection enabled

12.1.3 DISABLEINDEBUG

Address offset: 0x608

Disable protection mechanism in debug mode

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	3 12	2 13	10) 9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																				
Α	RW	DISABLEINDEBUG										Dis	sabl	e th	ne p	rot	ect	ion	me	ech	ani	sm	for	N۷	M ı	regi	ons	wh	ile	in					
												de	bug	mo	ode	. Th	nis r	egi	ste	r w	ill c	nly	dis	ab	e tl	ne p	rot	ect	ion						
												me	echa	anis	m i	f th	e d	evi	ce i	s in	de	bu	g m	od	e.										
			Disabled	1								Dis	sabl	ed i	in d	lebı	Jg																		
			Enabled	0								En	able	ed ii	n de	ebu	g																		



13 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

13.1 Registers

Table 15: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x10000000	FICR	FICR	Factory information configuration		

Table 16: Register Overview

CODEFASEZE 0.0101 Code memory size OFVICEID(1) 0.064 Device identifier OFVICEID(1) 0.0684 Device identifier ER(0) 0.080 Device identifier ER(1) 0.0684 Encryption root, word 0 ER(1) 0.068 Encryption root, word 1 ER(2) 0.068 Encryption root, word 3 IR(3) 0.090 Identity root, word 3 IR(3) 0.090 Identity root, word 2 IR(3) 0.090 Identity root, word 2 IR(3) 0.090 Identity root, word 3 IR(3) 0.000 Device address 1 IR(4) 0.000 Part code IR(4) 0.000 Part code	Register	Offset	Description	
DEVICED 0	CODEPAGESIZE	0x010	Code memory page size	
DEVICEID[1] 0x064 Device identifier ER[0] 0x080 Encyption root, word 1 ER[1] 0x084 Encyption root, word 2 ER[2] 0x08C Encyption root, word 3 IR[0] 0x090 Identity root, word 3 IR[1] 0x094 Identity root, word 1 IR[2] 0x098 Identity root, word 2 IR[3] 0x09C Identity root, word 3 DEVICEADDRYPE 0x00A Device address 0 DEVICEADDRYPE 0x0A0 Device address 1 DEVICEADD	CODESIZE	0x014	Code memory size	
ER(I)1 0x084 Encryption root, word 1 ER(I)1 0x084 Encryption root, word 2 ER(I)2 0x085 Encryption root, word 2 ER(I)3 0x08C Encryption root, word 3 IR(I) 0x090 Identity root, word 1 IR(I)1 0x094 Identity root, word 2 IR(I)3 0x09C Identity root, word 3 DEVICEADDRYPE 0x000 Device address type DEVICEADDRYPE 0x004 Device address 5 DEVICEADDRYII 0x0A8 Device address 1 INFO PARAM 0x100 Part code INFO PARAM 0x100 Part code INFO PARAM 0x104 Part variant, hardware version and production configuration INFO PARAM 0x100 Part code INFO PARAM 0x101 Flash variant INFO PARAM 0x101 Flash variant INFO PARAM 0x102 Reserved TEMP A0 0x404 Slope definition A0 TEMP A1 0x406 Slope definition A2 TEMP A2	DEVICEID[0]	0x060	Device identifier	
ER(I) 0x084 Encryption root, word 1 ER(2) 0x088 Encryption root, word 2 ER(3) 0x08C Encryption root, word 3 IR(0) 0x090 Identity root, word 0 IR(1) 0x094 Identity root, word 1 IR(2) 0x098 Identity root, word 3 IR(2) 0x009 Identity root, word 3 DEVICEADDR(IP) 0x0A0 Device address type DEVICEADDR(II) 0x0A04 Device address 0 DEVICEADDR(II) 0x0A04 Device address 1 INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PARM 0x104 Part variant, hardware version and production configuration INFO.PARM 0x100 Part variant, hardware version and production configuration INFO.PARM 0x110 Flash variant INFO.PARM 0x110 Flash variant INFO.PARM 0x110 Flash variant TEMP.A0 0x404 Slope definition A1 TEMP.A1 <	DEVICEID[1]	0x064	Device identifier	
ER[2] 0x088 Encryption root, word 2 ER[3] 0x08C Encryption root, word 3 IR[0] 0x090 Identity root, word 1 IR[1] 0x094 Identity root, word 1 IR[2] 0x098 Identity root, word 2 IR[3] 0x09C Identity root, word 3 DEVICEADDRYPE 0x0A0 Device address type DEVICEADDR[0] 0x0A4 Device address 1 INFO.PART 0x100 Part code INFO.PART 0x100 Part code INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PART 0x100 Part code INFO.PART 0x101 Flash variant INFO.PART 0x101 Flash variant INFO.PART 0x110 Flash variant INFO.PART 0x110 Flash variant INFO.PART 0x114 Reserved TEMP.A1 0x404 Slope definition A0 TEMP.A2 0x40C S	ER[0]	0x080	Encryption root, word 0	
ER[3] 0x80C Encryption root, word 3 IR[0] 0x909 Identity root, word 0 IR[1] 0x908 Identity root, word 2 IR[2] 0x908 Identity root, word 2 IR[3] 0x90C Identity root, word 3 DEVICEADDRIP[0] 0x0A0 Device address type DEVICEADDRIP[1] 0x0A8 Device address 1 INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PARXARIANT 0x104 Part variant, hardware version and production configuration INFO.PARXAGE 0x180 Package option INFO.PARXAGE 0x180 Package option INFO.PARXAGE 0x110 Flash variant INFO.PARXAGE 0x110 Flash variant INFO.PARXAGE 0x110 Flash variant INFO.PARXAGE 0x110 Specerved TEMP.A1 0x10 Specerved TEMP.A2 0x010 Specerved TEMP.A3 0x10 Specerved	ER[1]	0x084	Encryption root, word 1	
IR(O) 0x090 Identity root, word 0 IR(1) 0x094 Identity root, word 1 IR(2) 0x098 Identity root, word 2 IR(3) 0x09C Identity root, word 3 DEVICEADDRTYPE 0x0A0 Device address type DEVICEADDR[1] 0x0A4 Device address 0 DEVICEADDR[1] 0x0A8 Device address 1 INFO PART 0x100 Part code INFO PART 0x100 Part code INFO PART 0x104 Part variant, hardware version and production configuration INFO PARTA 0x100 Package option INFO PARTA 0x101 Flash variant INFO PARTA 0x110 Flash variant INFO PARTA 0x10 Slope definition A0 TEMP A2 0x4	ER[2]	0x088	Encryption root, word 2	
IR[1] 0x094 Identity root, word 1 IR[2] 0x098 Identity root, word 2 IR[3] 0x09C Identity root, word 3 DEVICEADORTYPE 0x0A0 Device address type DEVICEADOR[0] 0x0A4 Device address 1 DEVICEADOR[1] 0x0A8 Device address 1 INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PACKAGE 0x108 Package option INFO.PACKAGE 0x100 Reserved Reserved Reserved RESERVED Reserved RESERVED Reserved TEMP.A3 0x404 Slope definition A2 T	ER[3]	0x08C	Encryption root, word 3	
R[2]	IR[0]	0x090	Identity root, word 0	
IR[3] 0x09C Identity root, word 3 DEVICEADDRIVE 0x0A0 Device address type DEVICEADDRIJI 0x0A4 Device address 0 DEVICEADDRIJI 0x0A8 Device address 1 INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PACKAGE 0x108 Package option INFO.FLASH 0x110 Flash variant INFO.FLASH 0x110 Flash variant INFO.FLASH 0x1114 Reserved NEST Nation Reserved Reserved Reserved Reserved TEMP.AI 0x112 Reserved TEMP.AI 0x404 Slope definition AQ TEMP.A2 0x400 Slope definition A3 TEMP.A3 0x410 Slope definition A3 TEMP.A3 0x418 Slope definition A3 TEMP.B3 0x420 V-intercept B1 TEMP.B3 0x420 V-intercept B3 TEMP.B3 0x428 V-inte	IR[1]	0x094	Identity root, word 1	
DEVICEADDRIVPE Ox0A0 Device address type	IR[2]	0x098	Identity root, word 2	
DEVICEADDR(0) 0x0A4 Device address 0 DEVICEADDR[1] 0x0A8 Device address 1 INFO.PART 0x100 Part code INFO.PARIANT 0x104 Part variant, hardware version and production configuration INFO.PACKAGE 0x108 Package option INFO.RAM 0x100 RAM variant INFO.FLASH 0x110 Flash variant 0x112 Reserved 0x118 Reserved TEMP.A0 0x404 Slope definition A0 TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x400 Slope definition A2 TEMP.A3 0x410 Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A3 0x414 Slope definition A5 TEMP.B0 0x412 Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B3 0x430 Y-intercept B3 TEMP.T	IR[3]	0x09C	Identity root, word 3	
DEVICEADDR[1] 0x00 Part code INFO.PART 0x100 Part code INFO.PART 0x104 Part variant, hardware version and production configuration INFO.PACKAGE 0x108 Package option INFO.RAM 0x10C RAM variant INFO.FLASH 0x110 Flash variant CM118 Reserved Ox112 Reserved TEMP.AO 0x404 Slope definition AO TEMP.AI 0x408 Slope definition AI TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A5 0x418 Slope definition A4 TEMP.B0 0x41C Y-intercept B0 TEMP.B0 0x41C Y-intercept B1 TEMP.B2 0x420 Y-intercept B2 TEMP.B3 0x420 Y-intercept B3 TEMP.B5 0x430 Y-intercept B5 TEMP.B5 0x430 Y-intercept B5 TEMP.T1 0x438 Segment end T0 TEMP.T2 0x430<	DEVICEADDRTYPE	0x0A0	Device address type	
INFO_PART	DEVICEADDR[0]	0x0A4	Device address 0	
INFO.VARIANT	DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PACKAGE	INFO.PART	0x100	Part code	
INFO.RAM	INFO.VARIANT	0x104	Part variant, hardware version and production configuration	
NFO.FLASH	INFO.PACKAGE	0x108	Package option	
0x114 Reserved 0x11B Reserved 0x11C Reserved TEMP.A0 0x404 Slope definition A0 TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T1 0x438 Segment end T0 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	INFO.RAM	0x10C	RAM variant	
0x118 Reserved TEMP.A0 0x404 Slope definition A0 TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T1 0x438 Segment end T0 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	INFO.FLASH	0x110	Flash variant	
Reserved TEMP.A0 0x404 Slope definition A0 TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3		0x114		Reserved
TEMP.A0 0x404 Slope definition A0 TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A4 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3		0x118		Reserved
TEMP.A1 0x408 Slope definition A1 TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3		0x11C		Reserved
TEMP.A2 0x40C Slope definition A2 TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A0	0x404	Slope definition A0	
TEMP.A3 0x410 Slope definition A3 TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A1	0x408	Slope definition A1	
TEMP.A4 0x414 Slope definition A4 TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A2	0x40C	Slope definition A2	
TEMP.A5 0x418 Slope definition A5 TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A3	0x410	Slope definition A3	
TEMP.B0 0x41C Y-intercept B0 TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A4	0x414	Slope definition A4	
TEMP.B1 0x420 Y-intercept B1 TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.A5	0x418	Slope definition A5	
TEMP.B2 0x424 Y-intercept B2 TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B0	0x41C	Y-intercept B0	
TEMP.B3 0x428 Y-intercept B3 TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B1	0x420	Y-intercept B1	
TEMP.B4 0x42C Y-intercept B4 TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B2	0x424	Y-intercept B2	
TEMP.B5 0x430 Y-intercept B5 TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B3	0x428	Y-intercept B3	
TEMP.T0 0x434 Segment end T0 TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B4	0x42C	Y-intercept B4	
TEMP.T1 0x438 Segment end T1 TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.B5	0x430	Y-intercept B5	
TEMP.T2 0x43C Segment end T2 TEMP.T3 0x440 Segment end T3	TEMP.TO	0x434	Segment end TO	
<i>TEMP.T3</i> 0x440 Segment end T3	TEMP.T1	0x438	Segment end T1	
,	TEMP.T2	0x43C	Segment end T2	
TEMP.T4 0x444 Segment end T4	TEMP.T3	0x440	Segment end T3	
	TEMP.T4	0x444	Segment end T4	



13.1.1 CODEPAGESIZE

Address offset: 0x010 Code memory page size

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	R	CODEPAGESIZE		Code memory page size

13.1.2 CODESIZE

Address offset: 0x014 Code memory size

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	15 1	4 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α.	A A	Δ,	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	A	A A	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 1	1 1	1	1	1	1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	CODESIZE										Со	de r	ner	nor	y siz	e ir	n nu	ımb	er o	of p	age	!S										

Total code space is: CODEPAGESIZE * CODESIZE

13.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

Bit	numbe	er		31	30	29	28	27	26	25 2	24 2	3 2	2 21	. 20	19	18	17	16	15 1	L4 1	3 12	11	10	9	8	7 6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α.	A A	Δ Δ	A	Α	Α	Α	Α	Α	A	A A	A	Α	Α	A	Δ,	4 Α	A	Α	Α	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1 1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1 1	. 1	1	1	1	1	1
Id	RW	Field	Value Id Value Description																													
Α	R	DEVICEID 64 bit unique device identifier																														
	DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the																															
											ic	dent	ifier	r. Di	EVIC	CEIC	[1]	cor	ntain	is th	e m	ost :	sign	ifica	nt k	oits (of th	ne				
											d	evic	e id	ent	ifier	٠.																

13.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field Value Id	Value Description
A R DEVICEID	64 bit unique device identifier

DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

13.1.5 ER[0]

Address offset: 0x080 Encryption root, word 0



Bit r	umbe	er		31	30	29	28	27	⁷ 26	25	24	23	22	21	20	19 :	18	17 1	16 :	15 :	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α.	Α,	4 A	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	R	ER										End	ryp	tior	n ro	ot,	wo	rd n	1														

13.1.6 ER[1]

Address offset: 0x084 Encryption root, word 1

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	L9 1	.8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 4	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 A	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	. 1	1	1	1	1	1	1	1	1	1	1	1	l 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	R	ER										Enc	ryp	tion	ro	ot, v	vor	d n															

13.1.7 ER[2]

Address offset: 0x088 Encryption root, word 2

Bit	ทเ	ımb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15 1	L4 1	L3 1	.2 1	1 10) 9	8	7	6	5	4	3	2 :	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A .	Δ,	Δ Δ	Α	Α	Α	Α	Α	Α	Α	A A	А А
Re	se	0xF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1
Id		RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α		R	ER										End	rvr	otio	n rc	ot.	wο	rd r	1														

13.1.8 ER[3]

Address offset: 0x08C Encryption root, word 3

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	4 Α	A	Α	Α	Α	Α	Α	Α .	A ,	А А
Rese	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																		
Α	R	ER										Enc	ryp	tio	n ro	ot,	wo	rd ı	า														

13.1.9 IR[0]

Address offset: 0x090 Identity root, word 0

Bit numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18	17 :	16	15 1	L4 1	3 1	2 1	1 1	0 9	8	7	6	5	4	3 2	2 :	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 /	Δ Α	\ A	A	Α	Α	Α	Α	Α	A A	Δ Α	А А
Reset 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	۱ 1	. 1	1	1	1	1	1	1	1 :	1 1
Id RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
A R	IR										Ide	ntit	y rc	ot,	wo	rd ı	n															

13.1.10 IR[1]

Address offset: 0x094 Identity root, word 1

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 :	16	15	14 :	13 :	12 :	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
^	D	ID.										1-1-																						

A R IR Identity root, word n



13.1.11 IR[2]

Address offset: 0x098 Identity root, word 2

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	L7 1	L6 1	.5 1	4 1	3 12	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ ,	A A	A	. Δ	A	Α	Α	Α	Α	Α	Α	A	Δ ,	АА
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	. 1	. 1	. 1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																		
Α	R	IR										Ide	ntit	y ro	ot,	wo	rd r	ı															

13.1.12 IR[3]

Address offset: 0x09C Identity root, word 3

Reset 0xFFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Id	
	1 1
51 30 25 20 27 20 25 24 25 22 21 20 15 10 17 10 15 14 15 12 11 10 5 0 7 0 5 4 5 2	А А
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0

13.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit	numbe	er		31 30	29	28	27	26	25	24	23	22 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1	1	1	1	1	1 1	L 1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Value							Des	crip	tio	n																	
Α	R	DEVICEADDRTYPE									Dev	ice :	add	lres	s ty	ре															
			Public	0							Pub	lic a	ddı	ress																	
			Random	1							Ran	don	n ac	ddre	ess																

13.1.14 **DEVICEADDR**[0]

Address offset: 0x0A4
Device address 0

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	1 2	0 19	18	17	16	15	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Α	A	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	L 1	. 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1	l 1	1
Id	RW	Field	Value Id	Va	alue							Des	crip	tior	1																	
Α	R	DEVICEADDR										48 I	bit d	evic	e ac	ldre	ess															
																•				leas	Ŭ								ė			

the device address. Only bits [15:0] of ${\tt DEVICEADDR[1]}$ are used.

13.1.15 **DEVICEADDR**[1]

Address offset: 0x0A8

Device address 1

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	R	DEVICEADDR		48 bit device address

TO BEVICEADURE 40 BIT GEVICE AUGIT



Bit number	31 30	29 28 27 2	26 25 24	23 22 21	20 19 18	3 17 16	15 14 1	L3 12 1	1 10	9 8	7	6 5	5 4	3 2	2 1 0
Id	A A	A A A	A A A	A A A	ААА	. A A	A A	АА	4 A	А А	Α	A	4 А	A A	A A A
Reset 0xFFFFFFF	1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1	1 1	1 1 :	1 1	1 1	1	1 :	1 1	1 1	l 1 1
Id RW Field Val	ue Id Value			Descriptio	n										

DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

13.1.16 INFO.PART

Address offset: 0x100

Part code

Bit	numbe	er		31	. 30	29	28	27	26	25	24 :	23 2	22 2	1 20	0 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Д Д	Α.	Α	Α
Res	et 0x0	0052810		0	0	0	0	0	0	0	0	0	0 0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0 :	1 0	0	0	0
Id	RW	Field	Value Id	Va	lue						- 1	Des	cript	ion	1																		
Α	R	PART									- 1	Part	cod	le																			
			N52810	0x	528	10					-	nRF	5282	10																			
			N52832	0x	528	32					-	nRF	5283	32																			
			Unspecified	0x	FFFF	FFI	FF					Jns	peci	fied	ł																		

13.1.17 INFO.VARIANT

Address offset: 0x104

Part variant, hardware version and production configuration

Bit	numb	er		31	. 30 :	29	28 2	27 2	26 2	5 2	24 2	3 2	2 21	20	19	18	17	16	15	14 :	13 1	2 1:	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α.	A A	Δ.	A	4 Δ	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Re	et 0x4	11414142		0	1	0	0	0	0 0)	1 (0 1	0	0	0	0	0	1	0	1	0 (0	0	0	1	0	1	0	0	0 0	1	0
Id	RW	Field	Value Id	Va	lue						D)esc	ripti	on																		
Α	R	VARIANT									Р	art	varia	nt,	har	dw	are	ver	sior	n an	ıd pı	odu	ctio	n co	onfig	gura	atio	n,				
											е	nco	ded	as A	ASC	II																
			AAAA	0x	4141	41	41				Δ	AAA	A																			
			AAAB	0x	4141	41	42				Δ	AAE	3																			
			AABA	0x	4141	.42	241				Δ	ABA	A																			
			AABB	0x	4141	.42	242				Δ	ABE	3																			
			Unspecified	0x	FFFF	FFI	FF				ι	Jnsp	ecifi	ed																		

13.1.18 INFO.PACKAGE

Address offset: 0x108

Package option

Bit number		31 30 29 28 27 26 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		AAAAAA	A A A A A A A A A A A A A A A A A A A
Reset 0x00002000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A R PACKAGE			Package option
	QF	0x2000	QFxx - 48-pin QFN
	QC	0x2003	QCxx - 32-pin QFN
	Unspecified	0xFFFFFFF	Unspecified

13.1.19 INFO.RAM

Address offset: 0x10C

RAM variant



Bit	numbe	er		31	30 2	9	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6 5	5 ,	4 3	2	. 1	0
Id				Α	Α .	Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	۸ ,	ДД	. A	A	Α
Res	et 0x0	0000018		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	1 1	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																			
Α	R	RAM										RA	Mν	/aria	ant																			
			K16	0x	10							16	kBy	/te	RAN	Λ																		
			K24	0x	18							24	kBy	/te	RAN	Λ																		
			K32	0x	20							32	kBy	/te	RAN	Λ																		
			K64	0x	40							64	kBy	/te	RAN	Λ																		
			Unspecified	0x	FFFF	FF	F					Un	spe	cifi	ed																			

13.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

Bit r	umbe	er		31	30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	19 1	L8 1	L7 1	16 :	15 1	14 1	.3 1	2 1	1 10) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ,	A	Α.	Α.	Α	Α	A A	Δ,	Δ Α	. Δ	A	Α	Α	Α	Α	Α	Α	Α.	АА
Res	et 0x0	00000C0		0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0 (0 (0	0	0	1	1	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	า																		
Α	R	FLASH										Flas	h va	aria	nt																		
			K128	0x	80							128	kBy	yte f	flas	h																	
			K192	0x	C0							192	kBy	yte f	flas	h																	
			K256	0x	100							256	kBy	yte f	flas	h																	
			K512	0x	200							512	kBy	yte f	flas	h																	
			Unspecified	0x	FFFF	FFF	FF					Uns	pec	ifie	d																		

13.1.21 TEMP.A0

Address offset: 0x404 Slope definition A0

-	3it n	umb	er		31	30	29	28 2	27 2	6 2	5 2	4 2	3 22	2 2 1	. 20	19	18	17	16	15	14	13	12	11 1	.0	9	8 7	7 (5 5	4	3	2	1	0
1	d																							Α	Δ ,	Δ.	Α Α	۱ ۸	4 <i>A</i>	A	Α	Α	Α	Α
ı	Rese	t Ox	00000320		0	0	0	0	0 0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	1	1 () (0 1	. 0	0	0	0	0
ı	d	RW	Field	Value Id	Va	lue						D	esc	ripti	ion																			
7	Α .	R	Α									Α	(slc	ре	def	init	ion') re	gist	er														

13.1.22 TEMP.A1

Address offset: 0x408 Slope definition A1

Bit r	umbe	er		31 30 29 28 27	26 25 24 23 22 21 20 19	9 18 17 16 15 14 13 12	11 10 9 8	7 6	5 4	4 3 2	2 1 0
Id							A A A A	А А	A	A A A	A A A
Rese	et OxO	0000343		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 1 1	0 1	0 (0 0	0 1 1
Id	RW	Field	Value Id	Value	Description						
Α	R	Α			A (slope definiti	ion) register					

13.1.23 TEMP.A2

Address offset: 0x40C Slope definition A2



Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																							,	A A	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000035D		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	1	1	0	1	0	1	1	1	0 1
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	R	А										Α (slop	e d	efir	nitic	n)	reg	iste	er													

13.1.24 TEMP.A3

Address offset: 0x410 Slope definition A3

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	l8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A
Res	et 0x(00000400		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	1	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	Α										A (s	lope	e de	efin	itio	n) r	egis	ter														

13.1.25 TEMP.A4

Address offset: 0x414 Slope definition A4

Bit n	umbe	er		31	30 2	9 2	28 2	7 26	25	24	23	22	21 2	20 2	19 1	8 1	7 16	15	14	13 1	2 11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A
Rese	t OxO	0000452		0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0 0	1	0	0	0	1	0	1	0 () 1	1 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																	
Α	R	Α									Α (slop	e d	efin	itio	n) re	gist	er													

13.1.26 TEMP.A5

Address offset: 0x418 Slope definition A5

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17	16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Id					A A A A A	
Reset 0x0000037B		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 1 1 0	1 1 1 1 0 1 1
Id RW Field	Value Id	Value	Description			
A R A			A (slope definition) res	gister		

13.1.27 TEMP.B0

Address offset: 0x41C

Y-intercept B0

Bit	t nı	umbe	er		31	30	29	28 2	7 26	5 25	24	23	22	21	20	19 1	L8 1	17 1	.6 1	.5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	0
Id																					А	. A	Α	Α	Α	Α	Α	Α	Α	Α	A	ДД	АА
Re	se	t OxC	0003FCC		0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 (0 () 1	1	1	1	1	1	1	1	0	0	1	1 0	0
Id		RW	Field	Value Id	Va	lue						De	scri	ptic	n																		
Α		R	В									В (y-in	tero	ept	:)																	

13.1.28 TEMP.B1

Address offset: 0x420

Y-intercept B1



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
1.J		31 33 23 20 27	20 23 2 1 23 22 21 20 13 10 1		
Id				AAAA	A A A A A A A A A
Reset 0x00003F98		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1	1 1 1 0 0 1 1 0 0 0
Id RW Field	Value Id	Value	Description		
A R B			B (v-intercent)		

13.1.29 TEMP.B2

Address offset: 0x424

Y-intercept B2

Bit number		31 30 29 28 2	27 26 25 24 23 22 21 20 19 18	17 16 15 14	13 12 11	10 9	8 7	6 5	5 4	3 2	1 0
Id					A A A	АА	A A	A	A A	А А	A A
Reset 0x00003F98		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	1 1 1	1 1	1 1	0 () 1	1 0	0 0
Id RW Field	Value Id	Value	Description								
A R B			B (y-intercept)								

13.1.30 TEMP.B3

Address offset: 0x428

Y-intercept B3

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 1	.7 16 15 14 13 12 1	11 10 9 8 7	6 5 4 3 2 1 0
Id				АА	AAAAA	A A A A A A
Reset 0x00000012		0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 1 0 0 1 0
Id RW Field	Value Id	Value	Description			
A R B			B (y-intercept)			

13.1.31 TEMP.B4

Address offset: 0x42C

Y-intercept B4

Bit	num	per		31	. 30	29	28 27	7 26	25	24	23 2	22 2	1 2	0 19	18	17	16	15	14 :	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																				Α ,	4 A	Α	Α	Α	Α	Α	Α	A	4 A	А	Α
Res	et 0	0000004D		0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0	0	0	0	1	0	0 :	1 1	0	1
Id	RV	/ Field	Value Id	Va	lue						Des	crip	tior	1																	
Α	R	В									В (у	-inte	erce	pt)																	

13.1.32 TEMP.B5

Address offset: 0x430

Y-intercept B5

Bit number		31 30 29 28 2	27 26 25 24 23 22 21 20 19 18	17 16 15 14 13 12	11 10 9 8 7	7 6 5 4 3 2 1 0
Id				A A	A A A A	A A A A A A A
Reset 0x00003E10		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1	1 1 1 0 0	0 0 1 0 0 0 0
Id RW Field	Value Id	Value	Description			
A R B			B (y-intercept)			

13.1.33 TEMP.T0

Address offset: 0x434 Segment end T0



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	18 2	L7 1	.6 1	15 1	.4 1	3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																											Α	Α	Α	Α	Α	Α	АА
Res	et OxC	00000E2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0	0	0	0	0	1	1	1	0	0	0	1 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	Т										T (s	egn	nen	t er	ıd) ı	reg	iste	r														

13.1.34 TEMP.T1

Address offset: 0x438 Segment end T1

Bit r	umbe	er		31	30	29 2	28 2	7 26	5 25	24	23	22	21 2	0 1	9 18	8 17	7 16	15	14	13	12 1	1 1	0 9	8	7	6	5	4	3 2	2 1	1 0
Id																									Α	Α	Α	Α	A A	\ <i>A</i>	A A
Rese	et OxO	0000000		0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Val	lue						Des	cri	otio	n																	
Α	R	Т									T (s	egr	nent	t en	d) r	egis	ter														

13.1.35 TEMP.T2

Address offset: 0x43C Segment end T2

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9 8	8 7 6 5 4 3 2 1 0
14					
Id					A A A A A A A
Reset 0x00000014		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 1 0 1 0 0
Id RW Field	Value Id	Value	Description		
A R T			T (segment end) registe	ar.	

13.1.36 TEMP.T3

Address offset: 0x440 Segment end T3

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000019		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0000000	0 0 0 0 1 1 0 0 1
Id RW Field	Value Id	Value	Description		
A R T			T (segment end) register		

13.1.37 TEMP.T4

Address offset: 0x444 Segment end T4

Bit	numb	er		31	30	29	28 2	27 2	26 2	25 2	24 :	23 2	22 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12 1	1 1	9	8	7	6	5	4	3 2	2 :	1 0	
Id																										Α	Α	Α	Α	A A	۱ ۸	А А	
Re	set 0x	00000050		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	1	0	1	0 0) (0 0	
Id	RW	Field	Value Id	Va	lue						-	Des	crip	tio	n																		
Α	R	Т										Γ (s	egn	en	t en	d) r	egis	ter															١



14 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the *NVMC* — *Non-volatile memory controller* on page 26 and *Memory* on page 20 chapters.

14.1 Registers

Table 17: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10001000	UICR	UICR	User information configuration	

Table 18: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	



Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access port protection

14.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

E	3it ni	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17	16	15 :	14 :	13 :	12 1	11 1	10	9	8 7	7 6	5 5	4	3	2	1	0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ Α	A A	A A	A	Α	Α	Α	Α
ı	Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	. 1	1	1	1	1
ı	d	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																			
	۸	D\A/	NIDEENA										Dag		امما	for	NIO	.di.c	£:		~~~	مامه													

A RW NRFFW Reserved for Nordic firmware design

14.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit number	31 30	0 29 28 27 2	26 25 24 23 22 21 20 19	9 18 17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A	AAAA	A A A A A A A	A A A A A A A A A	A A A A A A A A
Reset 0xFFFFFFF	1 1	1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1
ld RW Field Value	ue Id Value	е	Description		

RW NRFFW Reserved for Nordic firmware design

14.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design



Bit	numb	er		31	30	29	28	27	26	25	24	23 2	22 2	21 :	20 1	19 1	l8 1	17 1	16 1	15 1	L4 1	L3 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	A A	Α,	A ,	Α.	A A	Δ,	4 Δ	. A	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	NRFFW										Res	erv	ed t	for I	Nor	dic	firn	nwa	are	des	ign											

14.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFFW										Res	serv	/ed	for	No	rdic	fir	mw	are	de	sigr	n											

14.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	AAAAAA	A A A A A A A A A	A A A A A A A A	A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 :	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		
A RW NRFFW	·	Reserved for Nordic firn	nware design	

14.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

Bit n	umbe	er		31	30 2	29 2	28 :	27 :	26	25 :	24	23 2	22 2	21 2	0 1	9 1	8 1	7 10	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ /	A /	Α Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Δ	A A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	L 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Val	lue							Des	crip	tio	n																		
Α	RW	NRFFW										Rese	erve	ed f	or N	lord	lic f	irm	war	e d	esig	n											

14.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description

RW NRFFW Reserved for Nordic firmware design



14.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bi	t ni	umb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4
R	ese	t Ox	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L
Id		RW	Field	Value Id	Va	lue							De	scri	ipti	on																				
Α		RW	NRFFW										Re	ser	ved	for	No	rdic	fir	mw	are	de	sig	า												ī

14.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	АА
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	NRFFW										Res	erv	ed f	for I	Nor	dic 1	firm	war	e d	esig	n											

14.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	17 1	6 1	.5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	NRFFW										Res	erv	ed 1	for	Nor	dic	firn	nwa	re d	esig	n											

14.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number		31	30	29	28	27	26	25	24	23 :	22	21 2	20 1	19 1	18 1	17 1	6 1	.5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	! 1	. 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α,	A A	Δ ,	4 4	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ A	A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	l 1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id RW Field	Value Id	Va	lue							Des	cri	otio	n																		

A RW NRFFW Reserved for Nordic firmware design

14.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	15 1	14 1	L3 1	.2 1	1 1	0 9	8	7	6	5	4	3	2	1 0	ĺ
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	Α .	Α,	4 4	. Δ	. A	Α	Α	Α	Α	Α	Α.	А А	l
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1	l
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																			l
Α	RW	NRFFW										Res	erv	ed	for	Nor	dic	firr	nwa	are	des	ign												

14.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit r	numb	er		31	1 30	29	28	27	⁷ 26	25	24	23	22	21 :	20 1	19 1	.8 1	.7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 Α	Α Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Δ	Α	Α	Α
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	l 1	1	1	1	1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																		
Α	RW	NRFHW										Res	erv	ed t	for I	Nor	dic	har	dwa	are o	lesi	gn											_

14.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	AAAAA	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description

RW NRFHW Reserved for Nordic hardware design



14.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

1	Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17	16	15 :	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 Α	Α	A A
1	Rese	t OxF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
ı	ld	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
_	Д	RW	NRFHW										Res	serv	red	for	Nor	dic	ha	rdw	are	de	sig	n											

Reserved for Nordic hardware design

14.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number		31 30 29 28 3	27 26 25 24 2	3 22 21 20 19 :	18 17 16 15 14 13 12	2 11 10 9 8 7	6 5 4 3 2 1 0
Id		A A A A	A A A A	A A A A A	A A A A A A	. A A A A A	A A A A A A
Reset 0xFFFFF	FF	1 1 1 1	1 1 1 1 1	1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1	1 1 1 1 1 1 1
Id RW Fie	l Value Id	Value	D	escription			
A RW NR	HW		R	eserved for Nor	rdic hardware design		

14.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21 :	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	Α Α	A	Α	Α	Α	Α	Α.	Α	Α.	Α	Α.	A A	4 A	Α	Α	Α
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	scri	otio	n																		
Α	RW	NRFHW										Res	erv	ed t	for I	Vor	dic l	hard	dwa	re d	esig	gn											

14.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	17 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	4 А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	1	1	1	1	1	1	1	1	1	1	1 1	L :	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed 1	for	Nor	dic	har	dwa	are o	desi	gn											

14.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

A RW NRFHW	Value Id	Value Description Reserved for Nordic hardware design	
Id RW Field	Malue Id	Malua Danadatian	
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
Id		A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A
Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 3	11 10 9 8 7 6 5 4 3 2 1 0

14.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	l8 1	.7 1	6 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Δ,	Δ Α	Δ ,	Δ Α	λ Α	Α Α	A	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1 1	L 1	ا 1	. 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	NRFHW										Res	erv	ed 1	for	Nor	dic	har	dwa	are	des	ign											

14.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	.9 1	.8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	ДД	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	. Д	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	NRFHW										Res	erv	ed 1	for I	Vor	dic ł	narc	war	e d	esig	n											

14.1.28 CUSTOMER[0]

Address offset: 0x080 Reserved for customer

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.29 CUSTOMER[1]

Address offset: 0x084 Reserved for customer

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.30 CUSTOMER[2]

Address offset: 0x088 Reserved for customer

Bit number Id																												2 A		
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1 :	1 1	1	1	1
Id RW Field	Value Id	Va								_		tion																		

RW CUSTOMER Reserved for customer



14.1.31 CUSTOMER[3]

Address offset: 0x08C Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW CUSTOMER	Reserved for customer

14.1.32 CUSTOMER[4]

Address offset: 0x090 Reserved for customer

Bit	nu	mbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ą
Res	set	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L
Id	-	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α		RW	CUSTOMER										Res	serv	/ed	for	cus	ton	ner																	_

14.1.33 CUSTOMER[5]

Address offset: 0x094 Reserved for customer

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.34 CUSTOMER[6]

Address offset: 0x098 Reserved for customer

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	.8 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α ,	ДД	A	Α.	Α	Α	A A	Α Α	Α	Α	Α	Α	Α .	A	4 A	Α	Α
Rese	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1 1	1	1	1	1	1	1	l 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																	
Α	RW	CUSTOMER										Res	erv	ed 1	for c	ust	ome	er														

14.1.35 CUSTOMER[7]

Address offset: 0x09C Reserved for customer

Bit number		31	30	29	28	27	26	25	24	23 :	22	21 2	20 1	19 1	.8 1	7 16	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	4 Δ	A	. A	Α	Α	Α	A A	Δ Δ	A	Α	Α	Α	Α	Α .	A ,	А А
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 1
Id RW Field	Value Id	Va	lue							Des	cri	otio	n																	

A RW CUSTOMER Reserved for customer

14.1.36 CUSTOMER[8]

Address offset: 0x0A0
Reserved for customer



Bit nu	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner																

14.1.37 CUSTOMER[9]

Address offset: 0x0A4
Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	15 1	L4 1	L3 1	.2 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A	Α .	Δ ,	4 Δ	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	CUSTOMER										Res	erv	ed	for	cus	tom	ner															

14.1.38 CUSTOMER[10]

Address offset: 0x0A8
Reserved for customer

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	7 1	6 15	14	13	12	11 :	10	9	8	7 6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A A	Α	Α	Α	Α	A	Α.	Δ ,	Α Α	A A	A	Α	Α	A A	À
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	۱ 1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1 :	Ĺ
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	CUSTOMER										Res	serv	ed	for	cus	tom	er															-

14.1.39 CUSTOMER[11]

Address offset: 0x0AC Reserved for customer

-	3it ni	umbe	er		3	1 30	29	9 28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
1	d				Α	Д	. A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	l
1	Rese	t OxF	FFFFFF		1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	
1	d	RW	Field	Value Id	V	alu	е						De	scri	ptic	on																				ı
7	Α .	RW	CUSTOMER										Re	serv	ved	for	cus	ton	ner																	ī

14.1.40 CUSTOMER[12]

Address offset: 0x0B0 Reserved for customer

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	19 1	18 1	17 1	16 1	15 1	14 1	L3 :	12 :	11 :	10	9	8	7	6	5	4	3	2 (1 0	,
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A ,	Α.	Α.	Α.	A .	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A /	А А	,
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	L 1	1 1	
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																				
Α	RW	CUSTOMER										Res	erv	ed 1	for o	cust	tom	ner																	

14.1.41 CUSTOMER[13]

Address offset: 0x0B4 Reserved for customer

Bit number		31	30	29	28	27	26	25	24	23 2	22 2	1 2	0 19	18	17	16	15 1	L4 13	3 12	11	10	9	8 7	' 6	5	4	3	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A	Α	Α	Α	Α	А А	Α	Α	A	A ,	Δ /	A	Α	Α	Α .	A A	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1 1	1	1	1	1	1 1	. 1	1	1	1	1 1	1 1
Id RW Field	Value Id	Va	lue							Des	crip	tior	1																

A RW CUSTOMER Reserved for customer



14.1.42 CUSTOMER[14]

Address offset: 0x0B8 Reserved for customer

E	Bit n	umbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	d				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
F	Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	d	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																				
1	١	RW	CUSTOMER										Re	serv	ed	for	cus	ton	ner																	_

14.1.43 CUSTOMER[15]

Address offset: 0x0BC Reserved for customer

Bit	nu	mbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ą
Res	set	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L
Id	-	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α		RW	CUSTOMER										Res	serv	/ed	for	cus	ton	ner																	_

14.1.44 CUSTOMER[16]

Address offset: 0x0C0 Reserved for customer

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.45 CUSTOMER[17]

Address offset: 0x0C4
Reserved for customer

Bit r	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	17 1	6 1	.5 1	4 13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 Α	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	А А	
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	n																			
Α	RW	CUSTOMER										Res	erv	ed	for	cus	tom	ier																

14.1.46 CUSTOMER[18]

Address offset: 0x0C8
Reserved for customer

Bit	numbe	er		31	30	29 2	28 2	7 26	25	24	23 :	22 2	21 2	20 19	18	17	16	15	14	13	12 1	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id				А	Α	Α.	ΑА	А	Α	Α	Α	A	Α.	A A	Α	Α	Α	Α	Α	Α	Α	A ,	Δ Δ	A	A	Α	Α	Α	Α.	Δ.	А А
Res	et 0xF	FFFFFF		1	1	1	1 1	. 1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Val	lue						Des	crip	tio	n																	
Α	RW	CUSTOMER									Res	erve	ed f	or cu	ısto	mei	-														

14.1.47 CUSTOMER[19]

Address offset: 0x0CC Reserved for customer



Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 3	18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id		AAAAA	A A A A A A A A	A A A A A A A A	A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description		
A RW CUSTON	ER		Reserved for cust	tomer	

14.1.48 CUSTOMER[20]

Address offset: 0x0D0 Reserved for customer

Bit	numb	er		31	1 30	29	9 28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	. A	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	А А
Res	et 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	2						De	scri	ptic	on																			
Α	RW	CUSTOMER							Re	serv	/ed	for	cus	ton	ner																			

14.1.49 CUSTOMER[21]

Address offset: 0x0D4 Reserved for customer

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	L6 1	l5 1	4 13	12	11	10	9	8	7	6 !	5 4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	A A	A	Α	Α	Α	Α	Α	Α	Α ,	Δ Δ	A	Α	A A	į.
Rese	t 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	1 1	. 1	1	1 :	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		ı
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner															

14.1.50 CUSTOMER[22]

Address offset: 0x0D8 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.51 CUSTOMER[23]

Address offset: 0x0DC Reserved for customer

Bit r	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et Ox	FFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.52 CUSTOMER[24]

Address offset: 0x0E0 Reserved for customer

Bit number		31	30	29	28	27	26	25	24	23 2	22 2	1 2	0 19	18	17	16	15 1	L4 13	3 12	11	10	9	8 7	' 6	5	4	3	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A	Α	Α	Α	Α	А А	Α	Α	A	A ,	Δ /	A	Α	Α	Α .	A A	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1 1	1	1	1	1	1 1	. 1	1	1	1	1 1	1 1
Id RW Field	Value Id	Va	lue							Des	crip	tior	1																

A RW CUSTOMER Reserved for customer



14.1.53 CUSTOMER[25]

Address offset: 0x0E4
Reserved for customer

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 1	.3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ,	Δ,	4 Α	. A	Α	Α	Α	Α	Α	Α	Α	Α .	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Re	serv	ed	for	cus	ton	ner																

14.1.54 CUSTOMER[26]

Address offset: 0x0E8
Reserved for customer

Bit	nu	mbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ą
Res	set	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L
Id	-	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α		RW	CUSTOMER										Res	serv	/ed	for	cus	ton	ner																	_

A RW CUSTOMER Reserved for custor

14.1.55 CUSTOMER[27]

Address offset: 0x0EC Reserved for customer

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Re	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.56 CUSTOMER[28]

Address offset: 0x0F0
Reserved for customer

Bit number		31	30	29	28	27	26	25	24	23 :	22	21	20	19 :	18 1	17 :	16	15 :	14	13 1	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Δ	A	Α	Α	Α	Α	Α .	Α.	А А
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 1
Id RW Field	Value Id	Va	lue							Des	cri	ptic	n																		

A RW CUSTOMER Reserved for customer

14.1.57 CUSTOMER[29]

Address offset: 0x0F4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 2	22 21 20 19 18 17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A		A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Desc	cription	

A RW CUSTOMER Reserved for customer

14.1.58 CUSTOMER[30]

Address offset: 0x0F8
Reserved for customer



Bi	t nı	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			 А А
D.																																			
R	ese	t UXF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id		RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α		RW	CUSTOMER										Re	serv	/ed	for	cus	ton	ner																

14.1.59 CUSTOMER[31]

Address offset: 0x0FC Reserved for customer

Bi	t nı	umbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Re	ese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id		RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
Α		RW	CUSTOMER										Re	ser	ved	for	cus	stor	ner																	

14.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If values are not the same, there will be no nRESET function exposed on a GPIO. As a result, the device will always start independently of the levels present on any of the GPIOs.

Bit r	numbe	er		31	L 30	29	28	3 27	26	5 25	5 24	4 23	3 22	21	20	19	18	17	16	15	14	13	12 :	l1 1	.0 9) 8	3 7	6	5	4	3	2	1	0
Id				В																									Α	Α	Α	Α	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	L 1	. 1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue	2						D	esci	ipti	on																			
Α	RW	PIN		21	L							G	PIO	nur	nbe	er Po	0.n	ont	o w	hicl	h re	set	is e	хро	sed									
В	RW	CONNECT										C	onn	ecti	on																			
			Disconnected	1								D	isco	nne	ct																			
			Connected	0								C	onn	ect																				

14.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If values are not the same, there will be no nRESET function exposed on a GPIO. As a result, the device will always start independently of the levels present on any of the GPIOs.

Bit	numbe	er		31	. 30	29	28	27	26	25	5 24	4 2:	3 22	2 2:	1 2	0 1	9 1	.8 1	7 1	16 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				В																											Α	Α	A	A A	А А	
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	. 1	. 1	. 1	. 1	. 1	. 1	1	1 :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Va	lue							D	esc	ript	ion	1																				
Α	RW	PIN		21								G	PIO	nu	mb	er	P0.	n o	nto	wł	nich	n re	set	is	exp	ose	ed									
В	RW	CONNECT										C	onn	ect	ion	ı																				
			Disconnected	1								D	isco	nne	ect																					
			Connected	0								C	onn	ect																						

14.1.62 APPROTECT

Address offset: 0x208
Access port protection



Bi	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Re	set 0xF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PALL			Enable or disable access port protection.
					See <i>Debug</i> on page 61 for more information.
			Disabled	0xFF	Disable
			Enabled	0x00	Enable



15 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

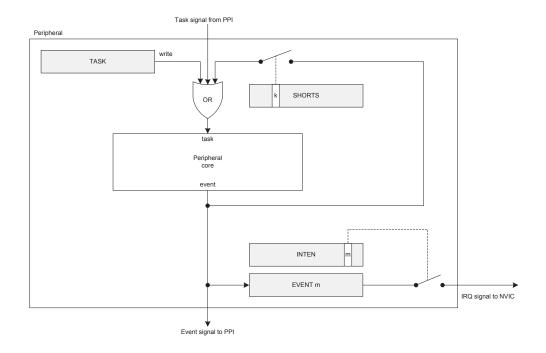


Figure 10: Tasks, events, shortcuts, and interrupts

15.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 21 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

15.2 Peripherals with shared ID

In general, and with the exception of ID 0, peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one at the time on this specific ID.

When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:

Disable the previously used peripheral



- · Remove any PPI connections set up for the peripheral that is being disabled
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- Enable the now configured peripheral.

See *Instantiation* on page 21 to see which peripherals are sharing ID.

15.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

15.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the "set-and-clear" pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map where the main register is followed by a dedicated SET and CLR register in that order.

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing a '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing a '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

15.5 Tasks

Tasks are used to trigger actions in a peripheral, for example, to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes a '1' to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 58.

15.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example, a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 58. An event register is only cleared when firmware writes a '0' to it.

Events can be generated by the peripheral even when the event register is set to '1'.

15.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.



Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

15.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the Nested Vectored Interrupt Controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 10: Tasks, events, shortcuts, and interrupts* on page 58.

15.8.1 Interrupt clearing

When clearing an interrupt by writing "0" to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

Important: To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.



16 Debug

The debug system offers a flexible and powerful mechanism for non-intrusive debugging.

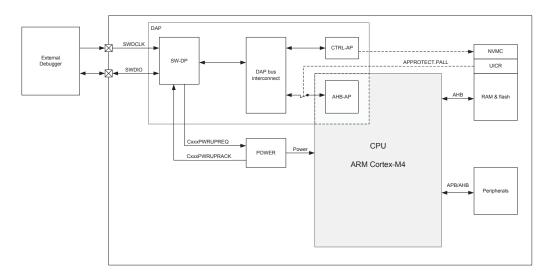


Figure 11: Overview

The main features of the debug system are:

- Two-pin Serial Wire Debug (SWD) interface
- Flash Patch and Breakpoint Unit (FPB) supports:
 - Two literal comparators
 - Six instruction comparators

16.1 DAP - Debug Access Port

An external debugger can access the device via the DAP.

The DAP implements a standard ARM® CoreSight™ Serial Wire Debug Port (SW-DP).

The SW-DP implements the Serial Wire Debug protocol (SWD) that is a two-pin serial interface, see SWDCLK and SWDIO in *Figure 11: Overview* on page 61.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom Control Access Port (CTRL-AP). The CTRL-AP is described in more detail in *CTRL-AP - Control Access Port* on page 61.

Important:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

16.2 CTRL-AP - Control Access Port

The Control Access Port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 56 for more information about enabling access port protection.

This access port enables the following features:



- Soft reset, see Reset on page 70 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase the Flash, UICR, and RAM.

16.2.1 Registers

Table 19: Register Overview

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP Identification Register, IDR

RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit nu	ımbe	r		31 3	0 29	9 28	3 27	7 26	25	24	23	22 2	21 2	0 19	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5 4	4 3	2	1	0
Id																															Α
Rese	0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Valu	e						Des	crip	tior	1																	
Α	RW	RESET									Sof	t res	et t	rigg	ere	d th	rou	gh (CTRI	-AP	. Se	e Re	set l	Beh	avio	ur i	in				
											PO	WER	cha	apte	r fo	r m	ore	det	ails.												
			NoReset	0							Res	et is	s no	t act	tive																
			Reset	1							Res	et is	act	ive.	De	vice	is h	eld	in r	eset											
			Reset	1							Res	et is	act	ive.	De	vice	is h	eld	in r	eset											

ERASEALL

Address offset: 0x004

Erase all

Bit	numbe	er		31 30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0 x0	0000000		0 0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	9						Des	crip	tio	n																	
Α	W	ERASEALL									Eras	se a	II FL	.ASF	l ar	nd R	ΑM														
			NoOperation	0							No	ope	rati	on																	
			Erase	1						1	Eras	se a	II FL	.ASF	l ar	nd R	ΑM														

ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation

В	it nur	mbe	r		3	1 3	0 29	9 2	8 2	7 2	26 2	25 2	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
lo																																					Α
R	eset	0x0	0000000		0	0	0	0) () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
lo	l F	RW	Field	Value Id	٧	/alu	е							De	scri	ptic	on																				
Α	F	3	ERASEALLSTATUS											Sta	tus	reg	ist	er fo	or t	he	ER/	SE	٩LL	ор	erat	tion											
				Ready	0)								ERA	ASE	ALL	is	read	dy																		
				Busy	1									ERA	ASE	ALL	is	bus	y (c	n-g	oin	g)															

APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection



Bit	numb	er		3	1 3	0 2	9 2	8 2	27 2	26	25	24	23	22	21	20	19	18	17	16	15	14	1 13	3 1:	2 1:	1 10	9	8	7	6	5	4	3	2	1)
Id																																				4
Res	et 0x(0000000		0) () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	٧	/alu	e							De	scr	ipti	on																				
Α	R	APPROTECTSTATUS											Sta	atus	s re	gist	er	or	acc	ess	ро	rt p	rot	ect	ion											
			Enabled	0)								Ac	ces	s p	ort	pro	tec	tioi	n er	nab	led														
			Disabled	1									Ac	ces	s p	ort	pro	tec	tioi	n no	ot e	nak	ole	b												

IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21 :	20 -	19 1	18 -	17 1	16 '	15 1	14 1	3 1	2 1	1 10) 9	8	7	6	5	4	3) 1	1 0
Id									D																	Ī					Α /	Δ Δ	Δ Α
	at OvO	2880000							0															۱	٥	٥					0		0 0
Id		Field	Value Id	_	alue	•	Ü	Ü	Ü	-	•	-	scri	-	-	•		•	•	•		•	,	, ,	Ū	Ü	Ü	Ü	•	•			, ,
Iu	IV V V	rieiu	value lu	Vd	iiue							De	SCIII	ptio	"																		
Α	R	APID										ΑP	Ide	ntifi	cat	ion																	
В	R	CLASS										Acc	ess	noq	t (/	AP)	clas	SS															
			NotDefined	0x	0							No	def	ine	d cl	ass																	
			MEMAP	0x	8							Me	emo	ry A	cce	ss F	or	t															
С	R	JEP106ID										JEC	DEC.	JEP:	106	ide	nti	ty c	ode	9													
D	R	JEP106CONT										JEC	DEC .	JEP:	106	COI	ntin	nuat	ion	СО	de												
Е	R	REVISION										Rev	visio	n																			

16.2.2 Electrical specification

Control access port

Symbol	Description	Min.	Тур.	Max.	Units
R _{pull}	Internal SWDIO and SWDCLK pull up/down resistance				kΩ

16.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the Control Access Port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 73 will be set.

16.4 Real-time debug

The nRF52810 supports real-time debugging.

Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or



sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.



17 Power and clock management

Power and clock management in nRF52810 is optimized for ultra-low power applications.

The core of the power and clock management system is the power management unit (PMU) illustrated in *Figure 12: Power management unit* on page 65.

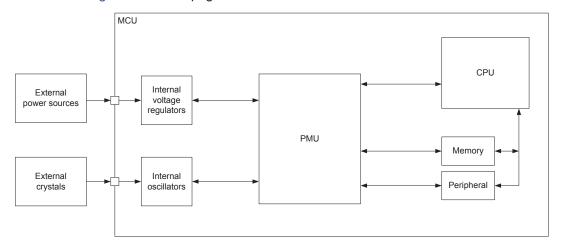


Figure 12: Power management unit

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

17.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. To aid that, a set of current consumption scenarios are provided to show average current drawn from the VDD supply for the application.

See *Electrical specification* on page 65 for application scenarios. Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 20: Current consumption scenarios, common conditions* on page 65 shows a set of conditions commonly used for the scenarios, unless otherwise is stated in the scenario description.

Table 20: Current consumption scenarios, common conditions

Condition	Value
VDD	3 V
Temperature	25°C
CPU	WFI (wait for interrupt)/WFE (wait for event) sleep
Peripherals	All idle
Clock	Not running
Regulator	DC/DC

17.1.1 Electrical specification

Current consumption: Radio

Symbol	Description	Min.	Тур.	Max.	Units
I _{RADIO_TX0}	0 dBm TX @ 1 Mbps Bluetooth low energy mode, Clock = HFXO		TBD		mA
I _{RADIO_TX1}	-40 dBm TX @ 1 Mbps Bluetooth low energy mode, Clock =		TBD		mA
	HFXO				
I _{RADIO_RXO}	Radio RX @ 1 Mbps Bluetooth low energy mode, Clock = HFXO		TBD		mA



Current consumption: Ultra-low power

Symbol	Description	Min.	Тур.	Max.	Units
I _{ON_RAMOFF_EVENT}	System ON, No RAM retention, Wake on any event		0.6		μΑ
I _{ON_RAMON_EVENT}	System ON, Full 24 kB RAM retention, Wake on any event		0.8		μΑ
I _{ON_RAMOFF_RTC}	System ON, No RAM retention, Wake on RTC		1.3		μΑ
I _{OFF_RAMOFF_RESET}	System OFF, No RAM retention, Wake on reset		0.3		μΑ
I _{OFF_RAMOFF_GPIO}	System OFF, No RAM retention, Wake on GPIO		0.3		μΑ
I _{OFF_RAMON_RESET}	System OFF, Full 24 kB RAM retention, Wake on reset		0.5		μΑ



18 POWER — Power supply

This device has the following power supply features:

- On-chip LDO and DC/DC regulators
- · Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- · Supervisor HW to manage power on reset, brownout, and power fail
- · Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- · Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

Note: Two additional external passive components are required to use the DC/DC regulator.

18.1 Regulators

The following internal power regulator alternatives are supported:

- · Internal LDO regulator
- · Internal DC/DC regulator

The LDO is the default regulator.

The DC/DC regulator can be used as an alternative to the LDO regulator and is enabled through the *DCDCEN* on page 75 register. Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in *Figure 14: DC/DC regulator setup* on page 68.

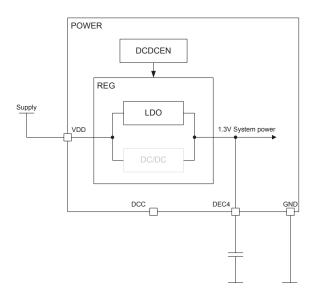


Figure 13: LDO regulator setup



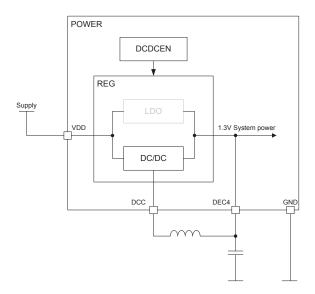


Figure 14: DC/DC regulator setup

18.2 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following:

- 1. The DETECT signal, optionally generated by the GPIO peripheral
- 2. A reset

When the system wakes up from System OFF mode, it gets reset. For more details, see *Reset behavior* on page 71.

One or more RAM sections can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers.

RAM[n].POWER are retained registers, see *Reset behavior*. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. This is usually accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF.

18.2.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug* on page 61 for more information. Required resources needed for debugging include the following key components: *Debug* on page 61, *CLOCK* — *Clock control* on page 87, *POWER* — *Power supply* on page 67, *NVMC* — *Non-volatile memory controller* on page 26, CPU, Flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.

18.3 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.



Register *RESETREAS* on page 73 provides information about the source that caused the wakeup or reset.

The system can switch on and off the appropriate internal power sources, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

18.3.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- · Constant latency
- Low power

In constant latency mode the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by forcing a set of base resources on while in sleep. The advantage of having a constant and predictable latency will be at the cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode the automatic power management system, described in *System ON mode* on page 68, ensures the most efficient supply option is chosen to save the most power. The advantage of having the lowest power possible will be at the cost of having varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it will, by default, reside in the low power sub-power mode.

18.4 Power supply supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure.

In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in *Figure 15: Power supply supervisor* on page 69.

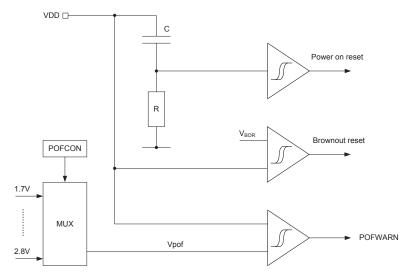


Figure 15: Power supply supervisor

18.4.1 Power-fail comparator

The power-fail comparator (POF) can provide the CPU with an early warning of impending power failure. It will not reset the system, but give the CPU time to prepare for an orderly power-down.



The comparator features a hysteresis of V_{HYST} , as illustrated in *Figure 16: Power-fail comparator (BOR = Brownout reset)* on page 70. The threshold V_{POF} is set in register *POFCON* on page 74. If the POF is enabled and the supply voltage falls below V_{POF} , the POFWARN event will be generated. This event will also be generated if the supply voltage is already below V_{POF} at the time the POF is enabled, or if V_{POF} is reconfigured to a level above the supply voltage.

If power-fail warning is enabled and the supply voltage is below V_{POF} the power-fail comparator will prevent the NVMC from performing write operations to the NVM. See $NVMC - Non-volatile \ memory \ controller$ on page 26 for more information about the NVMC.

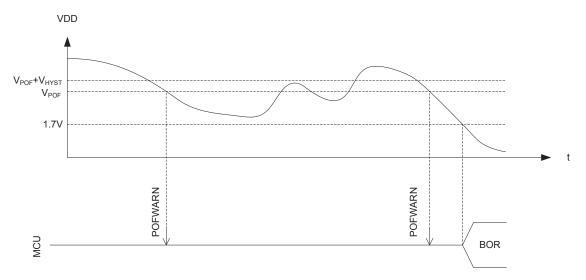


Figure 16: Power-fail comparator (BOR = Brownout reset)

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.

18.5 RAM sections

RAM section power control is used for retention in System OFF mode and for powering down unused sections in System ON mode.

Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* on page 20 for more information on RAM sections.

18.6 Reset

There are multiple sources that may trigger a reset.

After a reset has occurred, register *RESETREAS* can be read to determine which source generated the reset.

18.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

18.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.



Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

Note: Pin reset is not available on all pins.

18.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode. Refer to chapter *Debug* on page 61 for more information.

18.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

Refer to ARM documentation for more details.

A soft reset can also be generated via the RESET on page 62 register in the CTRL-AP.

18.6.5 Watchdog reset

A Watchdog reset is generated when the watchdog times out.

Refer to chapter WDT — Watchdog timer on page 388 for more information.

18.6.6 Brown-out reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

Refer to section *Power fail comparator* on page 86 for more information.

18.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.

18.8 Reset behavior

Reset source	Reset target CPU	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup ⁵	X	X	X						
Soft reset	х	X	X						
Wakeup from System OFF mode reset	Х	Х		x ⁶		x ⁷			
Watchdog reset ⁸	х	X	Х	X		X	Х	X	
Pin reset	x	х	х	х		х	х	х	
Brownout reset	x	X	X	X	X	X	X	X	X
Power on reset	х	х	х	х	х	X	х	х	х

Note: The RAM is never reset, but depending on reset source, RAM content may be corrupted.

^a All debug components excluding SWJ-DP. See *Debug* on page 61 chapter for more information about the different debug components in the system.

Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

⁶ The Debug components will not be reset if the device is in debug interface mode.

RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM register parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

⁸ Watchdog reset is not available in System OFF.



18.9 Registers

Table 21: Instances

Base address	Peripheral	Instance	Description Configuration		
0x40000000	POWER	POWER	Power control	For 24 kB RAM variant, only RAM[0].x to	
				RAM[2].x registers are in use.	

Table 22: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
DCDCEN	0x578	DC/DC enable register	
RAM[0].POWER	0x900	RAMO power control register	
RAM[0].POWERSET	0x904	RAMO power control set register	
RAM[0].POWERCLR	0x908	RAMO power control clear register	
RAM[1].POWER	0x910	RAM1 power control register	
RAM[1].POWERSET	0x914	RAM1 power control set register	
RAM[1].POWERCLR	0x918	RAM1 power control clear register	
RAM[2].POWER	0x920	RAM2 power control register	
RAM[2].POWERSET	0x924	RAM2 power control set register	
RAM[2].POWERCLR	0x928	RAM2 power control clear register	
RAM[3].POWER	0x930	RAM3 power control register	
RAM[3].POWERSET	0x934	RAM3 power control set register	
RAM[3].POWERCLR	0x938	RAM3 power control clear register	
RAM[4].POWER	0x940	RAM4 power control register	
RAM[4].POWERSET	0x944	RAM4 power control set register	
RAM[4].POWERCLR	0x948	RAM4 power control clear register	
RAM[5].POWER	0x950	RAM5 power control register	
RAM[5].POWERSET	0x954	RAM5 power control set register	
RAM[5].POWERCLR	0x958	RAM5 power control clear register	
RAM[6].POWER	0x960	RAM6 power control register	
RAM[6].POWERSET	0x964	RAM6 power control set register	
RAM[6].POWERCLR	0x968	RAM6 power control clear register	
RAM[7].POWER	0x970	RAM7 power control register	
RAM[7].POWERSET	0x974	RAM7 power control set register	
RAM[7].POWERCLR	0x978	RAM7 power control clear register	

18.9.1 INTENSET

Address offset: 0x304

Enable interrupt



Bit r	umbe	or .		31	30	29 2	28 2	7 2	6 2	5 24	23 2	22 :	21 2	0 1	9 1:	8 1 ⁻	7 16	5 1	5 14	1 13	12	11	10	9	8	7	6 !	5 4	3	2	1 0
Id				-	,			_										-	_								C I	3	J	A	
	et 0x0	0000000		0	0	0	0 (0 (0 0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0			0 0	0		0 0
Id	RW	Field	Value Id	Va	lue						Des	crip	otio	n																	
Α	RW	POFWARN									Wri	te '	1' to	En	able	e int	terr	upt	fo	r PO	FW	/ARI	V ev	ent							
											See	EV	ENT	S_P	OFV	NAI	RN														
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: [Disal	bled	ł																
			Enabled	1							Rea	d: E	Enab	led																	
В	RW	SLEEPENTER									Wri	te '	1' to	En	able	e int	terr	upt	fo	r SLE	EEP	ENT	ER	eve	nt						
											See	EV	ENT	S_S	LEE	PΕN	ITE	?													
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: [Disal	bled	ł																
			Enabled	1							Rea	d: E	Enab	led																	
С	RW	SLEEPEXIT									Wri	te '	1' tc	En	able	e int	terr	upt	fo	SLE	EP	EXI	Гev	ent							
											See	EV	ENT	s_s	LEE	PEX	ΊΤ														
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: [Disal	bled	ł																
			Enabled	1							Rea	d: E	Enab	led																	

18.9.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	umbe	er		31	30	29 2	28 2	27 2	26 2	25 2	4 23	3 22	21	20	19	18	17 1	16 :	15 :	14 1	.3 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id																											C E	3		Α	
Rese	et OxO	0000000		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escri	ipti	on																	
Α	RW	POFWARN									W	/rite	'1'	to D	isal	ble	inte	rru	pt f	or F	OF	NAF	RN e	ven	t						
											Se	ee <i>E</i> l	VEN	ITS_	POI	FW/	4RN														
			Clear	1							Di	isabl	le																		
			Disabled	0							Re	ead:	Dis	able	ed																
			Enabled	1							Re	ead:	Ena	able	d																
В	RW	SLEEPENTER									W	/rite	'1'	to D	isal	ble	inte	rru	pt f	or S	LEE	PEN	TER	eve	nt						
											Se	ee <i>E</i> l	VEN	ITS	SLE	EPE	NTE	ER													
			Clear	1							Di	isabl	le																		
			Disabled	0							Re	ead:	Dis	able	ed																
			Enabled	1							Re	ead:	Ena	able	d																
С	RW	SLEEPEXIT									W	/rite	'1'	to D	isal	ble	inte	rru	pt f	or S	LEE	PEX	IT e	vent							
											Se	ee <i>E</i> l	VEN	ITS	SLE	EPE	XIT														
			Clear	1								isabl		_																	
			Disabled	0							Re	ead:	Dis	able	ed																
			Enabled	1							Re	ead:	Ena	able	d																

18.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW RESETPIN		Reset from pin-reset detected
	NotDetected	0 Not detected
	Detected	1 Detected
B RW DOG		Reset from watchdog detected
	NotDetected	0 Not detected
	Detected	1 Detected
C RW SREQ		Reset from soft reset detected
	NotDetected	0 Not detected
	Detected	1 Detected
D RW LOCKUP		Reset from CPU lock-up detected
	NotDetected	0 Not detected
	Detected	1 Detected
E RW OFF		Reset due to wake up from System OFF mode when wakeup is
		triggered from DETECT signal from GPIO
	NotDetected	0 Not detected
	Detected	1 Detected
F RW DIF		Reset due to wake up from System OFF mode when wakeup is
		triggered from entering into debug interface mode
	NotDetected	0 Not detected
	Detected	1 Detected

18.9.4 SYSTEMOFF

Address offset: 0x500 System OFF register

Bit r	numb	er		31 30 29 28 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Res	et OxC	0000000		0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	W	SYSTEMOFF			Enable System OFF mode
			Enter	1	Enable System OFF mode

18.9.5 POFCON

Address offset: 0x510

Power failure comparator configuration

Bit n	umbe	er		31	30 2	9 :	28 2	27 :	26 2	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8 7	6	5	4	3	2	1 0
Id																														В	В	В	ВА
Rese	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ipti	on																		
Α	RW	POF										Ena	ble	10 9	dis	ab	le p	ow	er f	ailu	re o	om	npar	rato	r								
			Disabled	0								Disa	abl	e																			
			Enabled	1								Ena	ble	e																			
В	RW	THRESHOLD										Pov	ver	r fa	lur	e co	omp	oara	ator	th	resh	olo	se	tting	S								
			V17	4								Set	th	res	holo	d to	1.	7 V															
			V18	5								Set	th	res	holo	d to	1.	3 V															
			V19	6								Set	th	res	holo	d to	1.9	9 V															
			V20	7								Set	th	res	holo	d to	2.0) V															
			V21	8								Set	th	res	holo	d to	2.:	1 V															
			V22	9								Set	th	res	holo	d to	2.:	2 V															
			V23	10	1							Set	th	res	holo	d to	2.:	3 V															
			V24	11								Set	th	res	holo	d to	2.4	1 V															
			V25	12								Set	th	res	holo	d to	2.	5 V															



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B B B B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	V26	13	Set threshold to 2.6 V
	V27	14	Set threshold to 2.7 V
	V28	15	Set threshold to 2.8 V

18.9.6 GPREGRET

Address offset: 0x51C

General purpose retention register

Bit number			31 30	0 29	28 27	7 26	25 2	24 2	3 22	21	20 1	19 1	8 17	16	15 3	14 1	.3 12	2 11	10	9	8	7 6	5	4	3	2	1 0
Id																					A	A A	A A	Α	Α	Α	А А
Reset 0x00	000000	(0	0	0 0	0	0	0 (0 0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 () (0	0	0	0	0 0
ld RW	Field Val	ue Id	/alu	е				D	escr	iptic	on																
A RW	GPREGRET							G	iene	ral n	urpo	ose r	eter	ntio	n res	ziste	r										

This register is a retained register

18.9.7 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit	numbe	er		31 30 29 28 27	26 25 24	23 22 3	21 20	19 1	8 17	16 1	.5 14	13 1	L2 11	. 10	9	8	7	6	5 4	4 3	2	1 ()
Id																	Α	Α	Α /	4 A	Α	A A	A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0	0 0	0 (0	0	0 0	0	0 0	0	0	0	0	0	0 (0 0	0	0 ()
Id	RW	Field	Value Id	Value		Descrip	tion																I
Α	RW	GPREGRET				Genera	l pur	pose i	eten	tion	regis	ster											

This register is a retained register

18.9.8 DCDCEN

Address offset: 0x578 DC/DC enable register

Bit	numb	er		31 30	29	28	27	26	25 :	24	23 2	22 2	21 2	0 19	9 1	8 17	7 16	15	14	13	12	11 1	10 9	9 8	3 7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x	00000000		0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•					- 1	Des	crip	tior	ı																	
Α	RW	DCDCEN									Ena	ble	or d	lisak	ole	DC/	DC	con	vert	er											
			Disabled	0						-	Disa	ble																			
			Enabled	1						-	Ena	ble																			

18.9.9 RAM[0].POWER

Address offset: 0x900

RAM0 power control register

Bit r	umbe	r		31	. 30	29	28	27	7 26	25	5 24	1 23	3 22	2 2:	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			D	С															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	() (0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	llue							D	esc	ript	ior	1																				
Α	RW	SOPOWER										Ke	еер	RA	М	sec	ctio	n S	0 0	NC	or	OFF	in	Sys	ten	10 r	N m	ode	₽.							
												R	AM	l sec	tio	ns	are	e al	lwa	ys	ret	ain	ed v	vhe	n C	N,	but	car	n als	o b	e					
												re	etaiı	ned	w	her	n O	FF	de	per	nde	nt o	n t	he	set	ing	s in	SOI	RET	EN	ГΙΟ	N.				
												Α	II RA	AM	se	ctic	ons	wi	II b	e C	FF	in S	syst	em	OF	Fm	od	э.								
			Off	0								0	ff																							



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C
Res	et 0x0	0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
			On	1	On
В	RW	S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
С	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On

18.9.10 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	. 30	29	28 2	27 2	26 2	5 2	24 2	3 2	2 2	1 20	0 1	9 1	.8 :	17 1	16	15	14 1	L3 1	2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id																		D	С														В А
Res	et 0x0	000FFFF		0	0	0	0	0	0 (0	0 (0) (0) (0 (0	0	0	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						0	esc	rip	tion	1																		
Α	W	SOPOWER									K	еер	R/	AM s	sec	tio	n Si	of C	R/	\M(on (or	off	in S	yste	m (NC	mod	de				
			On	1							C)n																					
В	W	S1POWER									K	еер	R/	AM s	sec	tio	n S	1 of	R/	AM(on (or	off	in S	yste	m (NC	mod	de				
			On	1							C)n																					
С	W	SORETENTION									K	еер	re	tent	tior	n or	n R.	ΑM	se	ctic	n S	0 w	nen	RA	M s	ecti	on	S					
											S	wito	che	d of	f																		
			On	1							C)n																					
D	W	S1RETENTION									K	еер	re	tent	tior	n or	n R.	ΑM	se	ctic	n S	1 w	nen	RA	M s	ecti	on	S					
											S	wite	che	d of	f																		
			On	1							C)n																					

18.9.11 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	1 30	29	28 2	7 2	6 2	5 2	4 2:	3 22	2 21	20	19	18	17	16	15 1	14 1	.3 1	2 1:	1 10	9	8	7	6	5	4	3 2	. 1	. 0
Id																	D	С													В	Α
Rese	et OxO	000FFFF		0	0	0	0 () (0 0) (0	0	0	0	0	0	0	0	1	1	1 1	1	. 1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	alue						D	esci	riptio	on																		
Α	W	SOPOWER									K	eep	RAN	1 se	ctio	n S	0 о	f R/	M	on (or	off i	n Sy	/ste	m C)N r	nod	le				
			Off	1							0	ff																				
В	W	S1POWER									K	еер	RAN	1 se	ctio	n S	1 o	f RA	MA	on (or	off i	n Sy	/ste	m C)N r	nod	le				
			Off	1							0	ff																				
С	W	SORETENTION									K	еер	rete	ntic	on o	n R	ΑN	l se	ctio	n S) wł	nen	RAI	VI se	ecti	on i	S					
											S۱	vitc	hed	off																		
			Off	1							0	ff																				
D	W	S1RETENTION									K	еер	rete	ntic	on o	n R	ΑN	l se	ctio	n S	L wh	nen	RAI	VI se	ecti	on i	S					
											S۱	vitc	hed	off																		



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id			D C
Reset 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description
	Off	1	Off

18.9.12 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

Bit	numbe	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000FFFF		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 &$
Id	RW	Field	Value Id	Value	Description
Α	RW	SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in SORETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
В	RW	S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
С	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On

18.9.13 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	30 2	29 2	28 2	7 2	6 25	24	23 2	22 :	21 2	0 1	9 1	8 1	7 16	5 15	14	13 1	2 1	1 10	9	8	7	6	5 .	4 3	2	1	0
Id																[) C													В	Α
Res	et 0x0	000FFFF		0	0	0	0 0) (0 0	0	0	0	0 0) (0 0) (0	1	1	1	1 1	1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue						Des	crip	ption	1																	
Α	W	SOPOWER									Kee	p R	: MA	sec	tion	s SC	of	RAN	11 o	n or	off i	n Sy	ster	n Ol	N m	node	9				
			On	1							On																				
В	W	S1POWER									Kee	p R	: MA	sec	tion	S1	of	RAN	11 o	n or	off i	n Sy	ster	n Ol	N m	node	9				
			On	1							On																				
С	W	SORETENTION									Kee	p re	eten	tio	n on	R/	Ms	ecti	on S	0 w	hen	RAN	1 se	ctio	n is						
											swit	tche	ed of	ff																	
			On	1							On																				
D	W	S1RETENTION									Kee	p re	eten	tio	n on	R/	Ms	ecti	on S	1 w	hen	RAN	1 se	ctio	n is						
											swit	tche	ed of	ff																	
			On	1							On																				

18.9.14 RAM[1].POWERCLR

Address offset: 0x918



RAM1 power control clear register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	30 2	9 28	8 27	26 2	25 2	4 23	3 22	21	20	19 :	18	17	16 1	.5 1	4 13	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id																D	С													В	Α
Rese	et OxO	0000FFFF		0	0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	1 :	l 1	1	1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Val	ue					D	escri	iptio	n																		
Α	W	SOPOWER								Κe	ep l	RAM	se	ctio	n S	0 o	f RA	M1	on (or o	ff in	Sy	ster	n O	N n	node	9				
			Off	1						Of	ff																				
В	W	S1POWER								Κe	ep l	RAM	se	ctio	n S	1 o	f RA	M1	on (or o	ff in	Sy	ster	n O	N n	node	9				
			Off	1						Of	ff																				
С	W	SORETENTION								Κe	ері	retei	ntic	on o	n R	ΑM	sec	tio	s0	wh	en F	RAIV	1 se	ctio	n is						
										sv	vitch	ned o	off																		
			Off	1						Of	ff																				
D	W	S1RETENTION								Ke	ері	retei	ntic	on o	n R	AM	sec	tio	1 S1	wh	en F	RAN	l se	ctio	n is						
										SV	vitch	ned o	off																		
			Off	1						Of	ff																				

18.9.15 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

D:+	numbe			21	20	20	20	27	20	. 25		4.35		2 22	1 20	2 1	0 10	2 1	7 1	C 1	г 1	1 1	2 1	2 1	1 1	0 0		7	-	_	4	2	2	1	0
	numbe	er		31	. 3L) 29	28	27	26) 25) Z	4 23	5 22	2 2.	L 2C	JΙ	9 18				.5]	L4 .	13 1	.2 1	11	0 9	' 8	, /	Ь	5	4	3	2	1	
Id) (В	
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	C	0 0	0	0	0	(0	() () :	1	1	1 :	1 :	1 1	. 1	. 1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	llue)						De	esc	ript	ion	1																			
Α	RW	SOPOWER										Ke	eep	RA	M s	sec	tion	SC	ON	lo	r O	FF i	n Sy	ste	m C	ı NC	noc	le.							
												RA	٩M	sec	tior	ns	are	alw	ays	re	tai	nec	l wh	en	ON	, bu	t ca	ın a	lso l	эe					
												re	taiı	ned	wh	nen	OF	F d	ере	nd	ent	or	the	e se	ttin	gs i	n S(ORE	ΓEΝ	TIO	N.				
												Αl	I RA	MΑ	sec	tio	ns v	vill	be	OF	F ir	ı Sy	ster	n C	FF I	mod	de.								
			Off	0								Of	ff																						
			On	1								Oı	n																						
В	RW	S1POWER										Ke	еер	RA	M s	sec	tion	S1	ON	lo	r O	FF i	n Sy	ste	m C	ı NC	noc	le.							
												RA	٩M	sec	tior	ns	are	alw	ays	re	tai	nec	l wh	en	ON	, bu	t ca	ın a	lso l	эe					
												re	taiı	ned	wh	nen	OF	F d	ере	nd	ent	or	the	e se	ttin	gs i	n Sí	LRE	TEN	TIO	N.				
												Αl	I RA	١M	sec	tio	ns v	vill	be	OF	F ir	ı Sy	ster	n C	FF I	mod	de.								
			Off	0								Of	ff																						
			On	1								Oı	n																						
С	RW	SORETENTION										Ke	eep	ret	ent	ior	n on	RA	M	sec	tio	n S) wl	nen	RA	M s	ect	ion	is in	OF	F				
			Off	0								Of	ff																						
			On	1								Oı	n																						
D	RW	S1RETENTION										Ke	eep	ret	ent	ior	n on	RA	M:	sec	tio	n S	1 wl	nen	RA	M s	ect	ion	is in	OF	F				
			Off	0								Of	ff																						
			On	1								Oı	n																						

18.9.16 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C
Reset 0x0000FFFF		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description
A W SOPOWER			Keep RAM section S0 of RAM2 on or off in System ON mode
	On	1	On



Bit r	numbe	er		31	. 30	29 :	28 2	7 2	6 2	5 2	4 23	3 22	21	20	19	18	17 :	16 1	L5 1	4 1	3 12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id																	D	С													В	Α
Res	et 0 x0	000FFFF		0	0	0	0 0) (0) (0 0	0	0	0	0	0	0	0	1 :	1 1	. 1	1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	on																		
В	W	S1POWER									Ke	еер	RAN	1 se	ctic	n S	1 o	f RA	M2	on	or of	ff in	Sys	ten	10 n	l m	ode	è				
			On	1							0	n																				
С	W	SORETENTION									Ke	еер	rete	ntio	on c	n R	AM	sec	ctio	n SO	whe	en R	AM	sec	ction	ı is						
											SV	vitcl	hed	off																		
			On	1							0	n																				
D	W	S1RETENTION									Ke	еер	rete	ntio	on c	n R	AM	sec	ctio	n S1	whe	en R	AM	sec	ction	ı is						
											SV	vitcl	hed	off																		
			On	1							0	n																				

18.9.17 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	30	29	28 2	27 :	26 2	25 2	4 23	3 22	21	20	19	18	17	16	5 1!	5 1	4 13	3 12	11	. 10	9	8	7	6	5	4	3	2	1 0
Id																	D	С															ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						De	escr	ipti	on																			
Α	W	SOPOWER									Ke	ер	RAN	∕l se	ecti	on	S0	of I	RAI	VI2	on (or o	ff ir	n Sy	ste	m C)N r	noc	de				
			Off	1							Of	ff																					
В	W	S1POWER									Ke	ер	RAN	∕l se	ecti	on	S1	of I	RAI	VI2	on (or o	ff ir	n Sy	ste	m C)N r	noc	de				
			Off	1							Of	ff																					
С	W	SORETENTION									Ke	ер	rete	enti	on	on	RAI	M s	ect	tior	S0	wh	en l	RAN	/I se	ectio	on i	S					
											SW	vitc	ned	off																			
			Off	1							Of	ff																					
D	W	S1RETENTION									Ke	ер	rete	enti	on	on	RAI	M s	ect	tior	S1	wh	en I	RAN	/I se	ectio	on i	S					
											SW	vitc	ned	off																			
			Off	1							Of	ff																					

18.9.18 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit r	umbe	r		31	30	29 2	28 2	27 2	26 2	5 2	24 23	3 22	2 21	20	19	18	3 17	16	15	14	13 1	2 11	10	9	8	7	6	5 4	4 3	2	1	0
Id																	D	С													В	Α
Res	et OxO	000FFFF		0	0	0	0 (0	0 0)	0 0	0	0	0	0	0	0	0	1	1	1	1 1	1	1	1	1	1	1 :	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue						De	escr	ripti	on																		
Α	RW	SOPOWER									Ke	еер	RAN	VI se	ect	ion	S0	ON	or C	FF	in Sy	ster	10 n	N m	ode							
											R/	AM	sect	tion	ıs a	re a	alwa	ays	reta	ine	d wh	en (ON, I	but	can	als	o be	9				
											re	etair	ned	whe	en	OFF	de	per	der	nt o	n the	e set	ting	s in	SOR	ETE	ENT	ION				
											Αl	II RA	AM s	sect	tior	ns w	/ill b	oe C	FF i	n S	/stei	n Ol	Fm	ode	2.							
			Off	0							Of	ff																				
			On	1							10	n																				
В	RW	S1POWER									Ke	еер	RAN	VI se	ect	ion	S1	ON	or C)FF	in Sy	ster	10 n	N m	ode							
											R/	AM	sect	tion	ıs a	re a	alwa	ays	reta	ine	d wh	en (ON, I	but	can	als	o be	9				
											re	etair	ned	whe	en	OFF	de	per	der	nt o	n the	e set	ting	s in	S1R	ETE	ENT	ION				
											Αl	II RA	AM s	sect	tior	าร พ	/ill b	oe C	FFi	n S	/stei	n Ol	F m	ode	2.							
			Off	0							Of	ff																				
			On	1							10	n																				
С	RW	SORETENTION									Ke	еер	rete	enti	on	on	RA	VI s	ecti	on S	0 w	nen	RAN	1 se	ctio	n is	in (OFF				
			Off	0							Of	ff																				
			On	1							10	n																				



Bit r	numbe	er		31 30	29	28	27	26 2	25 2	24 :	23 2	22 2	1 2	0 1	9 1	3 17	16	15	14	13 :	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																D	С													В	Α
Res	et 0x0	000FFFF		0 0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1	l 1	. 1	1
Id	RW	Field	Value Id	Value	9					- 1	Des	crip	tior	1																	
D	RW	S1RETENTION								- 1	Kee	p re	ten	tior	n on	RA	M s	ecti	on S	1 w	hen	RAN	1 se	ctio	n is	in (OFF				
			Off	0						(Off																				
			On	1						(On																				

18.9.19 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	. 30	29	28	27	26	25 2	24 2	3 22	21	20	19 :	18	17	16	15	14 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																	D	С													В	3 A
Res	et 0 x0	0000FFFF		0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	on																		
Α	W	SOPOWER									K	еер	RAN	1 se	ctio	n S	0 о	f RA	AM:	3 on	or	off i	n Sy	ste	m C	N n	nod	e				
			On	1							C	n																				
В	W	S1POWER									K	еер	RAN	1 se	ctio	n S	1 o	f RA	AM3	3 on	or	off i	n Sy	ste	m C	N n	nod	е				
			On	1							C	n																				
С	W	SORETENTION									K	еер	rete	ntic	on o	n R	ΑN	1 se	ctic	n SC) w	nen	RAI	√l se	ctio	n is	5					
											S	witc	ned	off																		
			On	1							C	n																				
D	W	S1RETENTION									K	еер	rete	ntic	on o	n R	ΑN	1 se	ctic	n S1	L w	nen	RAI	√l se	ctio	n is	5					
											S	witc	ned	off																		
			On	1							С	n																				

18.9.20 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	30	29	28 2	27 2	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14	13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																	D	С														В	3 A
Rese	et 0x0	000FFFF		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	alue						D	escr	ipti	on																			
Α	W	SOPOWER									K	еер	RAN	Λse	ecti	on	S0 (of F	RAN	13 (on d	or o	ff in	Sys	sten	n O	N n	node	e				
			Off	1							0	ff																					
В	W	S1POWER									K	еер	RAN	∕l se	ecti	on	S1 (of F	RAN	13 (on d	or o	ff in	Sys	sten	n O	N n	node	e				
			Off	1							0	ff																					
С	W	SORETENTION									K	еер	rete	nti	on (on	RAI	VI s	ecti	on	S0	wh	en F	RAIV	1 se	ctio	n is						
											S١	witcl	hed	off																			
			Off	1							0	ff																					
D	W	S1RETENTION									K	еер	rete	enti	on (on	RAI	VI s	ecti	on	S1	wh	en F	RAIV	l se	ctio	n is						
											S۱	witcl	hed	off																			
			Off	1							0	ff																					

18.9.21 RAM[4].POWER

Address offset: 0x940

RAM4 power control register



Bit n	umbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C
Rese	t 0x0	000FFFF		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 &$
Id	RW	Field	Value Id	Value	Description
Α	RW	SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in SORETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
В	RW	S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
С	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On

18.9.22 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	L 30	29	28	27	26	25 2	24 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	2	1	0
Id																	D	С														В	Α
Res	et Ox0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1 :	. 1	1	1
Id	RW	Field	Value Id	Va	alue						0	esci	ripti	on																			
Α	W	SOPOWER									K	еер	RAN	VI se	ecti	on	S0	of R	AM	4 o	า	r of	f in	Sys	ten	n Ol	N n	nod	е				
			On	1							C)n																					
В	W	S1POWER									K	еер	RAN	VI se	ecti	on	S1	of R	AM	4 o	า	r of	f in	Sys	ten	n Ol	N n	nod	е				
			On	1							C)n																					
С	W	SORETENTION									K	еер	rete	enti	on	on	RAI	M s	ecti	on S	0 v	vhe	n R	AM	se	ctio	n is	5					
											S	witc	hed	off																			
			On	1							C)n																					
D	W	S1RETENTION									K	еер	rete	enti	on	on	RAI	M s	ecti	on S	1 v	vhe	n R	AM	se	ctio	n is						
											S	witc	hed	off																			
			On	1							C)n																					

18.9.23 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register

When read, this register will return the value of the POWER register.

Bit	numb	er		31 30	29 2	28 27	7 26	25 2	4 2	3 22	21	20	19	18 1	7 1	6 15	5 14	13	12 1	11 1	0 9	8	7	6	5	4	3	2 1	1 0
Id														[) (2												E	3 A
Res	et 0x(0000FFFF		0 0	0 (0 0	0	0 0) (0	0	0	0	0 () () 1	1	1	1	1 :	1 1	1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Value					D	escr	ipti	on																	
Α	W	SOPOWER							K	еер	RAN	VI se	ctic	n S0	of	RAN	Л4 c	n o	roff	in S	yste	m ()N r	nod	le				
			Off	1					0	ff																			
В	W	S1POWER							K	еер	RAN	VI se	ctic	n S1	of	RAN	Л4 c	n o	roff	in S	yste	m C)N r	nod	le				



Bit	numbe	er		31	. 30	29	28	3 27	26	25	24	4 23	3 2	2 2	21 2	20	19	18	17	16	15	5 14	1 13	3 12	2 1:	1 10) 9	8	7	6	5	4	3	2	1	0
Id																			D	С															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							D	esc	rip	tio	n																				
			Off	1								0	ff																							
С	W	SORETENTION										Ke	eep	re	ten	itic	on c	on	RAI	M s	ect	ion	S0	wh	en	RAI	√l s	ecti	on i	S						
												SV	vito	che	d o	ff																				
			Off	1								0	ff																							
D	W	S1RETENTION										Ke	eep	re	ten	ntic	on c	on	RAI	M s	ect	ion	S1	wh	en	RAI	√l s	ecti	on i	S						
												SV	vito	che	d o	ff																				
			Off	1								0	ff																							

18.9.24 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

																	_																
	numbe	er		31	. 30	29	28	27	26	25	24	23	22 .	21 2	20 :	19 1				15	14 :	L3 1:	2 1:	L 10	9	8	7	6	5	4 3	3 2	1	0
Id																		D	С													В	Α
Res	et 0 x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1 1	. 1	1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	RW	SOPOWER										Kee	p R	AM	se	ctio	n S	0 C	N c	or O	FF i	n Sy	ster	n Ol	l m	ode							
												RAN	√l s	ecti	ons	are	al	wa	ys r	eta	ined	l wh	en (ON, I	out	can	als	o b	e				
												reta	ine	d w	/he	n Ol	FF (dep	en	den	t or	the	set	ting	s in	SOR	ETI	ENT	ION	١.			
												All I	RAN	∕l se	ecti	ons	wil	ll b	e O	FF i	n Sy	sten	n Ol	FF m	ode	2.							
			Off	0								Off																					
			On	1								On																					
В	RW	S1POWER										Kee	p R	AM	se	ctio	n S	1 C)N c	or O	FF i	n Sy	ster	n Ol	N m	ode							
												RAN	√l s	ecti	ons	are	al	wa	ys r	eta	nec	l wh	en (ON, I	out	can	als	o b	е				
												reta	ine	d w	/he	n Ol	FF (dep	en	den	t or	the	set	ting	s in	S1R	ETI	ENT	ION	١.			
												All I	RAN	∕l se	ecti	ons	wil	ll b	e O	FF i	n Sy	sten	n Ol	FF m	ode	<u>.</u>							
			Off	0								Off																					
			On	1								On																					
С	RW	SORETENTION										Kee	p r	eter	ntic	n o	n R	ΑN	1 se	ctic	n S	0 wh	en	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					
D	RW	S1RETENTION										Kee	p r	eter	ntic	n o	n R	ΑN	1 se	ctic	n S	1 wh	en	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					

18.9.25 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		3	1 30	29	28	3 27	26	25	2	4 23	3 22	2 2	1 2	0 1	19 1	18	17	16	15	14	13	12	2 1	1 1	0 9	9 :	8	7	6	5	4	3	2	1	0
Id																			D	С																В	Α
Res	et 0 x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0) ()	0	0	0	0	1	1	1	1	1	. 1	L 1	1	1 :	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alue							De	esc	ript	tior	1																					
Α	W	SOPOWER										Ke	ep	RA	M	sec	tio	n S	60 o	f R	AN	15 (n o	or o	ff i	n S	yst	em	O١	l m	ode	9					
			On	1								10	n																								
В	W	S1POWER										Ke	ep	RA	M	sec	tio	n S	61 o	f R	AN	15 (on o	or o	ff i	n S	yst	em	٥N	l m	ode	e					
			On	1								10	n																								
С	W	SORETENTION										Ke	ep	ret	ten	tio	n o	n F	RAN	1 s	ecti	on	S0	wh	en	RA	M s	sec	tion	is							
												SW	vito	he	d o	ff																					
			On	1								01	n																								



Bit r	umbe	er		31 30	29	28	27	26	25 :	24	23	22	21	20	19	18	17	16	15 :	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																	D	С														ВА
Res	et 0x0	000FFFF		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Value	9						De	scri	ptic	on																		
D	W	S1RETENTION									Kee	ep r	ete	ntic	on c	n R	AM	se	ctio	n S	l wl	nen	RAN	∕l s∈	ctic	n is	5					
											swi	itch	ed (off																		
			On	1							On																					

18.9.26 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

	umbe	er		31	L 30	29	28	27	26 2	25 2	4 23	22	21	20	19				15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	. 0
ld Res	et OxO	000FFFF		0	0	0	0	0	0	0 0	0	0	0	0	0	0	D 0	0	1	1 1	. 1	1	1	1	1	1	1	1	1	1 1	В L 1	3 A 1 1
Id	RW	Field	Value Id	Va	alue						De	scri	iptic	n																		
Α	W	SOPOWER									Ke	ер I	RAIV	1 se	ctio	n S	О 0	f RA	AM5	on	or c	ff ir	ı Sy	ster	n O	N m	nod	е				
			Off	1							Of	f																				
В	W	S1POWER									Ke	ер I	RAIV	1 se	ctio	n S	1 o	f RA	AM5	on	or c	ff ir	Sy	ster	n O	N m	nod	е				
			Off	1							Of	f																				
С	W	SORETENTION									Ke	ері	rete	ntic	on o	n R	AN	1 se	ctio	n SO	wh	en l	RAN	1 se	ctio	n is						
											SW	itch	ned (off																		
			Off	1							Of	f																				
D	W	S1RETENTION									Ke	ері	rete	ntic	on o	n R	AN	1 se	ctio	n S1	wh	en l	RAN	1 se	ctio	n is						
											SW	itch	ned (off																		
			Off	1							Of	f																				

18.9.27 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

Reset 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	Bit n	umbe	er		31 3	0 29	9 28 2	27 2	6 25	5 24	23	22	21 2	20 1	.9 18	3 17	' 16	15	14 1	3 1	2 11	. 10	9	8 7	7 6	5 5	4	3	2	1 0
Id RW Field Value Id Value Description A RW SOPOWER Keep RAM section SO ON or OFF in System ON mode. RAM sections are always retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.	Id															D	С													ВА
A RW SOPOWER Keep RAM section SO ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.	Rese	et 0x0	000FFFF		0	0 0	0	0 (0 0	0	0	0	0	0	0 0	0	0	1	1	1 1	. 1	1	1	1 1	1 1	۱ 1	1	1	1	1 1
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.	Id	RW	Field	Value Id	Valu	ie					Des	scri	iptio	n																
retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.	Α	RW	SOPOWER								Kee	ep l	RAM	sec	tion	S0	ON	or C)FF i	n Sy	ster	n ON	l mo	ode.						
All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.											RAI	M s	ecti	ons	are a	alwa	ays	reta	inec	wh	en (ON, k	out	can a	also	be				
Off 0 Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.											ret	ain	ed w	hei	n OFI	- de	per	ider	nt or	the	set	tings	in	SORE	TEI	NTIC	N.			
On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.											All	RA	M se	ctio	ns v	vill k	oe C)FF i	n Sy	ster	n OF	Fm	ode							
B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.				Off	0						Off																			
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION.				On	1						On																			
retained when OFF dependent on the settings in S1RETENTION.	В	RW	S1POWER								Kee	ep l	RAM	sec	tion	S1	ON	or C)FF i	n Sy	ster	n ON	l mo	ode.						
											RAI	M s	ecti	ons	are a	alwa	ays	reta	inec	wh	en (ON, b	out	can a	also	be				
All RAM sections will be OFF in System OFF mode.											ret	ain	ed w	hei	n OFI	- de	per	ıder	nt or	the	set	tings	in	S1RE	TEI	NTIC	N.			
·											All	RA	M se	ctio	ns v	vill k	oe C)FF i	n Sy	ster	n Of	F m	ode							
Off 0 Off				Off	0						Off																			
On 1 On				On	1						On																			
C RW SORETENTION Keep retention on RAM section SO when RAM section is in OFF	С	RW	SORETENTION								Kee	g q	reter	itio	n on	RAI	M s	ectio	on S) wh	ien	RAM	se	ction	is i	n Ol	F			
Off 0 Off				Off	0						Off																			
On 1 On				On	1						On																			
D RW S1RETENTION Keep retention on RAM section S1 when RAM section is in OFF	D	RW	S1RETENTION								Kee	ı qe	reter	itio	n on	RAI	M s	ectio	on S	l wh	en	RAM	se	ction	is i	n Ol	F			
Off 0 Off				Off	0						Off																			
On 1 On				On	1						On																			



18.9.28 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	. 30	29	28 2	27 2	26 2	25 2	24 2	23 2	22 2	21 2	0 1	19 1	18	17	16	15	14 1	.3 1	2 1	1 10	0 9	8	3 7	6	5	4	3	2	1 0	I
Id																		D	С														ВА	ı
Res	et 0x0	000FFFF		0	0	0	0	0	0 (0	0	0 (0 (0 (0	0	0	0	0	1	1	1 :	L 1	. 1	. 1	1	. 1	1	1	1	1	1	1 1	ı
Id	RW	Field	Value Id	Va	lue							Desc	crip	tior	n																			l
Α	W	SOPOWER									k	Keep	p RA	AM	sec	ctio	n S	0 o	f R	AM6	on	or	off i	n S	yste	m	ON	mo	de					
			On	1							(Эn																						
В	W	S1POWER									k	Keep	p RA	AM	sec	ctio	n S	1 o	f R	AM6	on	or	off i	n S	yste	m	ON	mo	de					
			On	1							(On																						
С	W	SORETENTION									k	Keep	p re	eten	tio	n o	n R	AV	l se	ctic	n S() wl	nen	RA	M s	ect	ion	is						
											S	wit	che	ed of	ff																			
			On	1							C	Эn																						
D	W	S1RETENTION									k	Keep	p re	eten	tio	n o	n R	AV	l se	ctic	n S	l wl	nen	RA	M s	ect	ion	is						
											S	wit	che	ed of	ff																			
			On	1							(Эn																						

18.9.29 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	. 30	29	28 2	27 2	26 2	25 2	24 2	3 22	2 21	20	19	18	3 17	7 16	5 15	5 14	4 13	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																	D	С														Е	ВА
Res	et 0 x0	000FFFF		0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	1	1	. 1	1	1	1	1	1	1	1	1	1	1 :	L 1	1 1
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																			
Α	W	SOPOWER									K	еер	RAI	VI se	ect	ion	S0	of I	RAN	Л6	on	or o	ff i	ı Sy	ster	n O	Νn	nod	e				
			Off	1							C	ff																					
В	W	S1POWER									K	еер	RAI	VI se	ect	ion	S 1	of I	RAN	Л6	on	or o	ff i	ı Sy	ster	n O	Νn	nod	е				
			Off	1							C	ff																					
С	W	SORETENTION									K	еер	ret	enti	ion	on	RA	M s	ect	ion	SO	wh	en	RAN	1 se	ctio	n is	5					
											S	witc	hed	off	F																		
			Off	1							C	ff																					
D	W	S1RETENTION									K	еер	ret	enti	ion	on	RA	M s	ect	ion	S1	wh	en	RAN	1 se	ctio	n is						
											S	witc	hed	off																			
			Off	1							C	ff																					

18.9.30 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

Bit r	numbe	er		31	. 30	29	2	8 27	7 2	26 2	5 2	24 2	23	22	21	20	19	18	3 1	7 1	6 1	.5 1	L4 :	13	12	11	10	9	8	7	6	5	4	3	2	1	. 0
Id																			D) (2															В	3 A
Res	et 0x0	000FFFF		0	0	0	C	0 0)	0 () (0	0	0	0	0	0	0	0	()	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	. 1
Id	RW	Field	Value Id	Va	lue								Des	scr	iptio	on																					
Α	RW	SOPOWER										ŀ	Kee	ер	RAN	/I se	ect	ion	S0	10	١o	r O	FF i	n S	yst	em	١٥	۱m	ode	Э.							
												F	RAI	M s	sect	ion	ıs a	re	alw	ays	s re	tai	neo	w b	hei	n O	N, ł	out	car	n al	so	be					
												r	reta	ain	ed v	wh	en	OF	F de	ере	end	ent	t or	n th	ie s	ett	ings	s in	SO	RE1	ΈN	TIC	N.				
												A	ΑII	RA	M s	ect	ior	ns v	vill	be	OF	F ir	n Sy	/ste	m	OF	m	od	e.								
			Off	0								(Off	F																							
			On	1								(On																								
В	RW	S1POWER										ŀ	Kee	ер	RAN	/I se	ect	ion	S 1	10	١o	r O	FF i	n S	yst	em	01	۱m	ode	е.							



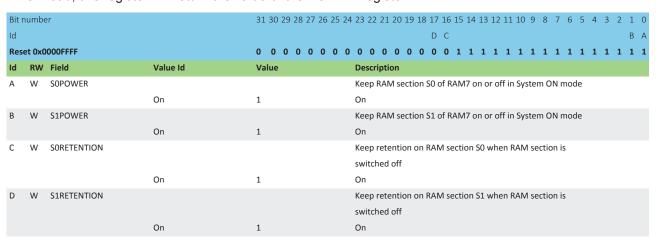
Bit	numbe	r		31	30 29	28	27	26 2	5 2	4 23	22	21 20) 1	9 18	3 1	7 16	5 15	5 14	13	12	11	10	9	8	7	6 !	5 4	3	2	1 0	
Id															0) C														ВА	
Res	et 0x0	000FFFF		0	0 0	0	0	0 (0	0	0	0 0	(0 0	C	0	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1 1	
Id	RW	Field	Value Id	Val	ue					Des	scri	ption	ı																		
										RAI	M s	ectio	ns	are a	alw	ays	ret	aine	ed v	her	n O	N, b	ut	can	also	be					
										ret	aine	ed wh	nen	OF	F d	ере	nde	nt c	n t	ne s	etti	ngs	in	S1R	ETE	NTI	ON.				
										All	RAI	M sec	tio	ns v	vill	be (OFF	in S	yst	em	OF	mc	ode								
			Off	0						Off	:																				
			On	1						On																					
С	RW	SORETENTION								Kee	ep r	etent	ior	n on	RΑ	M s	ect	ion	S0 ۱	vhe	n R	AM	se	ction	ı is	in C	FF				
			Off	0						Off	:																				
			On	1						On																					
D	RW	S1RETENTION								Kee	ep r	etent	ior	n on	RA	M s	ect	ion	S1 ۱	vhe	n R	AM	se	ction	ı is	in C	FF				
			Off	0						Off																					
			On	1						On																					

18.9.31 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.



18.9.32 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	30 2	9 2	8 27	26	25	24	23 2	2 21	L 20	19	18	17	16	15	14 :	L3 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																D	С													В	Α
Res	et 0x0	000FFFF		0	0 0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Val	ue						Desc	ripti	ion																		
Α	W	SOPOWER									Keep	RAI	M se	ecti	ion	S0 (of R	AM	7 or	or	off i	n Sy	ster	n O	N n	nod	е				
			Off	1							Off																				
В	W	S1POWER									Кеер	RAI	M se	ecti	ion	S1 (of R	AM	7 or	or	off i	n Sy	ster	n O	N n	nod	е				
			Off	1							Off																				
С	W	SORETENTION									Keep	ret	enti	on	on	RAI	VI se	ectio	on S	0 w	hen	RAN	1 se	ctio	n is						
											switc	ched	off																		
			Off	1							Off																				
D	W	S1RETENTION									Кеер	ret	enti	on	on	RAN	VI se	ectio	on S	1 w	hen	RAN	1 se	ctio	n is						
											switc	ched	off																		
			Off	1							Off																				



18.10 Electrical specification

18.10.1 Current consumption, sleep

Symbol	Description	Min.	Тур.	Max.	Units
I _{OFF}	System OFF current, no RAM retention		0.3		μΑ
I _{ON}	System ON base current, no RAM retention		0.6		μΑ
I _{RAM}	Additional RAM retention current per 4 KB RAM section		30		nA

18.10.2 Device startup times

Symbol	Description	Min.	Тур.	Max.	Units
t _{POR}	Time in Power on Reset after VDD reaches 1.7 V for all supply				
	voltages and temperatures. Dependent on supply rise time. ⁹				
t _{POR,10us}	VDD rise time 10us		1		ms
t _{POR,10ms}	VDD rise time 10ms		9		ms
t _{POR,60ms}	VDD rise time 60ms		23		ms
t_{PINR}	If a GPIO pin is configured as reset, the maximum time taken				
	to pull up the pin and release reset after power on reset.				
	Dependent on the pin capacitive load (C) 10 : t=5RC, R = 13kOhm				
t _{PINR,500nF}	C = 500nF			32.5	ms
t _{PINR,10uF}	C = 10uF			650	ms
t _{R2ON}	Time from reset to ON (CPU execute)				
t _{R2ON,NOTCONF}	If reset pin not configured	tPOR			ms
t _{R2ON,CONF}	If reset pin configured	tPOR +			ms
		tPINR			
t _{OFF2ON}	Time from OFF to CPU execute		16.5		μs
t _{IDLE2CPU}	Time from IDLE to CPU execute		3.0		μs
t _{EVTSET,CL1}	Time from HW event to PPI event in Constant Latency System		0.0625		μs
	ON mode				
t _{EVTSET,CLO}	Time from HW event to PPI event in Low Power System ON		0.0625		μs
	mode				

18.10.3 Power fail comparator

	Min.	Тур.	Max.	Units
Current consumption when enabled ¹¹		<4		μΑ
Nominal power level warning thresholds (falling supply voltage).	1.7		2.8	V
evels are configurable between Min. and Max. in 100mV				
ncrements.				
Fhreshold voltage tolerance		±1	±5	%
Fhreshold voltage hysteresis		50		mV
Brown out reset voltage range SYSTEM OFF mode	1.2		1.7	V
Brown out reset voltage range SYSTEM ON mode	1.5		1.7	V
	Nominal power level warning thresholds (falling supply voltage). Levels are configurable between Min. and Max. in 100mV Increments. Threshold voltage tolerance Threshold voltage hysteresis Brown out reset voltage range SYSTEM OFF mode	Nominal power level warning thresholds (falling supply voltage). 1.7 Levels are configurable between Min. and Max. in 100mV Increments. Threshold voltage tolerance Threshold voltage hysteresis Brown out reset voltage range SYSTEM OFF mode 1.2	Nominal power level warning thresholds (falling supply voltage). Levels are configurable between Min. and Max. in 100mV Increments. Threshold voltage tolerance ±1 Threshold voltage hysteresis Srown out reset voltage range SYSTEM OFF mode 1.2	Nominal power level warning thresholds (falling supply voltage). 1.7 2.8 Levels are configurable between Min. and Max. in 100mV Increments. Threshold voltage tolerance ±1 ±5 Threshold voltage hysteresis 50 Brown out reset voltage range SYSTEM OFF mode 1.2 1.7

⁹ A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

To save power, POF will not operate nor consume in System OFF, or while HFCLK is not running, even if left enabled by software



19 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- · 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-500 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- · 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of oscillator activity for low latency start up
- · Automatic oscillator and clock control, and distribution for ultra-low power

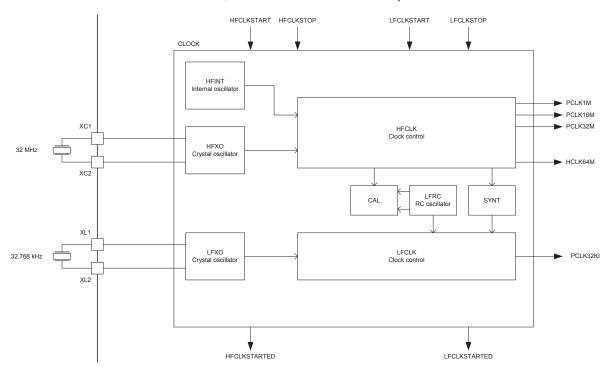


Figure 17: Clock control

19.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see Figure 17: Clock control on page 87.



When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started. The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event will be generated when the HFXO has started and its frequency is stable.

The HFXO must be running to use the RADIO or the calibration mechanism associated with the 32.768 kHz RC oscillator.

19.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 18: Circuit diagram of the 64 MHz crystal oscillator on page 88 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

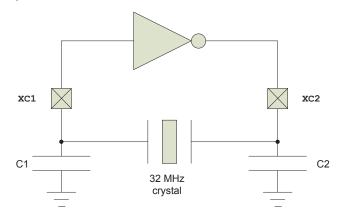


Figure 18: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 434. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the xc1 and xc2 pins. See table *64 MHz crystal oscillator (HFXO)* on page 94. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table 64 MHz crystal oscillator (HFXO) on page 94. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.



19.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 17: Clock control* on page 87, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- · 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 93 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

It is not allowed to write to register *LFCLKSRC* on page 93 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 93 indicates a 'LFCLK running' state.

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

19.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. See Table 32.768 kHz RC oscillator (LFRC) on page 95 for details on the default and calibrated accuracy of the LFRC oscillator. The LFRC oscillator does not require additional external components.

19.2.2 Calibrating the 32.768 kHz RC oscillator

After the 32.768 kHz RC oscillator is started and running, it can be calibrated by triggering the CAL task. In this case, the HFCLK will be temporarily switched on and used as a reference.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

It is not allowed to stop the LFRC during an ongoing calibration.

19.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32,768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

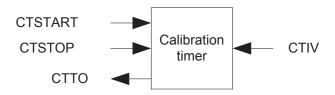


Figure 19: Calibration timer

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.



19.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the XL1 pin. The XL2 pin shall then be grounded.
- Rail-to-rail clock signal applied to the XL1 pin. The XL2 pin shall then be grounded or left unconnected.

The *LFCLKSRC* on page 93 register controls the clock source, and its allowed swing. The truth table for various situations is as follows:

Table 23: LFCLKSRC configuration depending on clock source

SRC	EXTERNAL	BYPASS	Comment
0	0	0	Normal operation, RC is source
0	0	1	DO NOT USE
0	1	X	DO NOT USE
1	0	0	Normal XTAL operation
1	1	0	Apply external low swing signal to XL1, ground XL2
1	1	1	Apply external full swing signal to XL1, leave XL2 grounded or unconnected
1	0	1	DO NOT USE
2	0	0	Normal operation, synth is source
2	0	1	DO NOT USE
2	1	X	DO NOT USE

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. *Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator* on page 90 shows the LFXO circuitry.

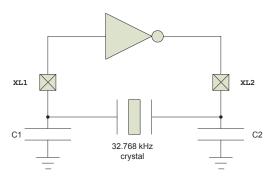


Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins (see 32.768 kHz crystal oscillator (LFXO) on page 95). The load capacitors C1 and C2 should have the same value.

For more information, see Reference circuitry on page 434.

19.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.



Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

19.3 Registers

Table 24: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	CLOCK	CLOCK	Clock control		

Table 25: Register Overview

Register	Offset	Description	
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator	
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator	
TASKS_LFCLKSTART	0x008	Start LFCLK source	
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source	
TASKS_CAL	0x010	Start calibration of LFRC oscillator	
TASKS_CTSTART	0x014	Start calibration timer	
TASKS_CTSTOP	0x018	Stop calibration timer	
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started	
EVENTS_LFCLKSTARTED	0x104	LFCLK started	
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event	
EVENTS_CTTO	0x110	Calibration timer timeout	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered	
HFCLKSTAT	0x40C	HFCLK status	
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered	
LFCLKSTAT	0x418	LFCLK status	
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered	
LFCLKSRC	0x518	Clock source for the LFCLK	
CTIV	0x538	Calibration timer interval	Retained

19.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25 2	14 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW HFCLKSTARTED			Write '1' to Enable interrupt for HFCLKSTARTED event
				See EVENTS_HFCLKSTARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW LFCLKSTARTED			Write '1' to Enable interrupt for LFCLKSTARTED event
				See EVENTS_LFCLKSTARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW DONE			Write '1' to Enable interrupt for DONE event
				See EVENTS_DONE
		Set	1	Enable
		Disabled	0	Read: Disabled



Bit r	numbe	er		31 3	0 29	9 2	8 27	7 26	25	24	1 23	22	21	20	19	18	17	16	15	14	13	12 1	l1 1	0 9	8	7	6	5	4	3 2	<u> </u>	0
Id																													D	С	P	3 A
Res	et 0 x0	0000000		0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Valu	e						De	escr	iptio	on																		
			Enabled	1							Re	ad:	Ena	ble	ed																	
D	RW	СТТО									W	rite	'1' t	to E	nak	ole	inte	rru	pt f	or (CTT	O e	vent									
											Se	e <i>E</i>	VEN	TS_	CT	ТО																
			Set	1							En	abl	e																			
			Disabled	0							Re	ad:	Disa	able	ed																	
			Enabled	1							Re	ad:	Ena	ble	ed																	

19.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	. 30	29	28	27	26 2	25 :	24 2	23	22 2	21 2	20 1	9 1	8 1	7 1	5 1	5 14	1 13	3 12	2 11	. 10	9	8	7	6 5	5 4	1 3	2	1	0
Id																													[ОС		В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	C	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0
Id	RW	Field	Value Id	Va	llue						ı	Des	scrip	otio	n																		
Α	RW	HFCLKSTARTED									١	Wr	ite ':	1' to	o Dis	sabl	e in	iter	rup	t fo	r HI	CLI	KST	ART	ED	eve	nt						
											9	See	e EVI	ENT	rs_h	IFCL	.KS1	TAR	TEL)													
			Clear	1							[Dis	able																				
			Disabled	0							F	Rea	ad: D	Disa	bled	t																	
			Enabled	1							F	Rea	ad: E	nat	bled																		
В	RW	LFCLKSTARTED									١	Wr	ite ':	1' to	o Dis	sabl	e in	ter	rup	t fo	r LF	CLk	(ST/	ARTI	ED 6	ever	nt						
											9	See	e <i>EVI</i>	ENT	rs_L	FCL	KST.	AR	TED														
			Clear	1							[Dis	able																				
			Disabled	0							F	Rea	ad: D	Disa	bled	t																	
			Enabled	1							F	Rea	ad: E	nak	bled																		
С	RW	DONE									١	Wr	ite ':	1' to	o Dis	sabl	e in	iter	rup	t fo	r D	ONE	E ev	ent									
											9	See	e <i>EVI</i>	ENT	rs_D	ON	Ε																
			Clear	1							[Dis	able																				
			Disabled	0							F	Rea	ad: D	Disa	bled	t																	
			Enabled	1							F	Rea	ad: E	nak	bled																		
D	RW	СТТО									١	Wr	ite ':	1' to	o Dis	sabl	e in	iter	rup	t fo	r C	ТО	eve	ent									
											9	See	e <i>EVI</i>	ENT	rs_c	TTC)																
			Clear	1							[Dis	able																				
			Disabled	0							F	Rea	ad: D	Disa	bled	t																	
			Enabled	1							F	Rea	ad: E	nak	bled																		

19.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit	numb	oer			3	1 30	29	28	27	26	25	24	23 2	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12 1	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0x	000000	00		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0
Id	RW	/ Field		Value Id	٧	alue	•						Des	crip	tior	1																	
Α	R	STAT	JS										HFC	LKS	TAR	T ta	isk 1	rigg	ere	d o	r no	t											
				NotTriggered	0								Task	c no	t tri	gge	red																
				Triggered	1								Task	k tri	ggei	red																	

19.3.4 HFCLKSTAT

Address offset: 0x40C



HFCLK status

Bit	numbe	er		31	. 30	29	28	27	26	25	5 24	4 2	3 22	2 21	20	19	9 18	3 17	7 16	15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																			В															Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							D	esci	ripti	on																			
Α	R	SRC										S	our	e o	f HF	CL	.K																	
			RC	0								6	4 M	Hz i	nte	rna	al os	scill	ato	r (H	IFIN	IT)												
			Xtal	1								6	4 M	Hz c	rys	tal	osc	illa	tor	(HF	ХО)												
В	R	STATE										Н	FCL	K sta	ate																			
			NotRunning	0								Н	FCL	K nc	t ru	unr	ning																	
			Running	1								Н	FCL	K ru	nni	ng																		

19.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit	numbe	er		31 30	29	28	27 2	26 2	25 2	4 2	23 2	2 2	1 20	19	18	17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0 (0 0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	9					D	esc	cript	tion																		
Α	R	STATUS								L	.FCL	.KST	ART	tas	k tr	igge	erec	or	not	:											
			NotTriggered	0						Т	ask	not	t trig	ger	ed																
			Triggered	1						Т	ask	trig	ger	ed																	

19.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit	numbe	er		31	30	29 :	28 2	7 2	26 25	5 2	4 23	3 22	21 2	20	19 1	.8 1	7 16	5 15	14	13	12 1	11 10	9	8	7	6	5	4 3	2	1 0
Id																	В													A A
Res	et 0x0	0000000		0	0	0	0 (0	0 0	(0 0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	n																
Α	R	SRC									Sc	urc	e of	LFC	LK															
			RC	0							32	2.76	8 kH	z R	C os	cilla	tor													
			Xtal	1							32	2.76	8 kH	z cr	ysta	ıl os	cilla	tor												
			Synth	2							32	2.76	8 kH	z sy	nth	esiz	ed f	rom	HF	CLK										
В	R	STATE									LF	CLK	stat	e																
			NotRunning	0							LF	CLK	not	rur	nin	g														
			Running	1							LF	CLK	runi	ning	3															

19.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bit n	umbe	er		31	1 30	29	28	27	26	25	24	23	22 :	21 :	20	19	18	17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1	0
Id																																	Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																			
Α	R	SRC										Clo	ck s	our	ce																			
			RC	0								32.	768	kH	z R	C os	cill	ato	r															
			Xtal	1								32.	768	kH	z cr	yst	al o	scil	late	or														
			Synth	2								32.	768	kH	z sy	nth	esi	zec	fro	m	HFC	CLK												

19.3.8 LFCLKSRC

Address offset: 0x518



Clock source for the LFCLK

Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C B A A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW SRC		Clock source
		RC	0 32.768 kHz RC oscillator
		Xtal	1 32.768 kHz crystal oscillator
		Synth	2 32.768 kHz synthesized from HFCLK
В	RW BYPASS		Enable or disable bypass of LFCLK crystal oscillator with external
			clock source
		Disabled	O Disable (use with Xtal or low-swing external source)
		Enabled	1 Enable (use with rail-to-rail external source)
С	RW EXTERNAL		Enable or disable external source for LFCLK
		Disabled	O Disable external source (use with Xtal)
		Enabled	1 Enable use of external source instead of Xtal (SRC needs to be
			set to Xtal)

19.3.9 CTIV (Retained)

Address offset: 0x538

This register is a retained register

Calibration timer interval

Bit	numl	ber			31	30	29 2	28 2	7 26	25	24	23	22 2	1 20	19	18	17	16 1	.5 1	4 13	3 12	11	10	9	8 7	7	6 5	5 4	3	2	1	0
Id																											A A	A A	Α	Α	Α	Α
Re	set 0	x000000	0		0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0	0	0 (כ	0 (0	0	0	0	0
Id	RV	V Field	١	Value Id	Va	lue						Des	crip	tion																		
Α	RV	V CTIV										Cal	ibrat	ion	time	r in	terv	al ir	n mı	ultip	le o	f 0.2	25 se	co	nds.	Ra	nge	:				

0.25 seconds to 31.75 seconds.

19.4 Electrical specification

19.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFINT}	Nominal output frequency		64		MHz
f _{TOL_HFINT}	Frequency tolerance		<±1.5	<±6	%
I _{HFINT}	Run current		60		μΑ
I _{START_HFINT}	Average startup current		I_HFINT		μΑ
t _{START_HFINT}	Startup time		3		us

19.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFXO}	Nominal output frequency		64		MHz
f _{XTAL_HFXO}	External crystal frequency		32		MHz
f _{TOL_HFXO}	Frequency tolerance requirement for 2.4 GHz proprietary radio applications			±60	ppm
f _{TOL_HFXO_BLE}	Frequency tolerance requirement, Bluetooth low energy applications			±40	ppm
C _{L_HFXO}	Load capacitance			12	pF
C _{0_HFXO}	Shunt capacitance			7	pF
R _{S_HFXO_7PF}	Equivalent series resistance C0 = 7 pF			60	ohm
R _{S_HFXO_5PF}	Equivalent series resistance C0 = 5 pF			80	ohm
R _{S_HFXO_3PF}	Equivalent series resistance CO = 3 pF			100	ohm



Symbol	Description	Min.	Тур.	Max.	Units
P _{D_HFXO}	Drive level			100	uW
C _{PIN_HFXO}	Input capacitance XC1 and XC2		4		pF
I _{STBY_X32M}	Core standby current ¹²		50		μΑ
I _{HFXO}	Run current		250		μΑ
I _{START_HFXO}	Average startup current, first 1 ms		0.4		mA
t _{START_HFXO}	Startup time		0.36		ms

19.4.3 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Тур.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f _{TOL_LFRC}	Frequency tolerance			±2	%
$f_{TOL_CAL_LFRC}$	Frequency tolerance for LFRC after calibration 13			±500	ppm
I _{LFRC}	Run current for 32.768 kHz RC oscillator		0.6	1	μΑ
t _{START LFRC}	Startup time for 32.768 kHz RC oscillator		600		us

19.4.4 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFXO}	Crystal frequency		32.768		kHz
f _{TOL_LFXO_BLE}	Frequency tolerance requirement for BLE stack			±250	ppm
f _{TOL_LFXO_ANT}	Frequency tolerance requirement for ANT stack			±50	ppm
C _{L_LFXO}	Load capacitance			12.5	pF
C _{0_LFXO}	Shunt capacitance			2	pF
R _{S_LFXO}	Equivalent series resistance			100	kohm
P _{D_LFXO}	Drive level			1	uW
C _{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I _{LFXO}	Run current for 32.768 kHz crystal oscillator		0.25		μΑ
t _{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.25		S
V _{AMP_IN_XO_LOW}	Peak to peak amplitude for external low swing clock. Input	200		1000	mV
	signal must not swing outside supply rails.				

19.4.5 32.768 kHz synthesized from HFCLK (LFSYNT)

Symbol	Description	Min.	Тур.	Max.	Units
f_{NOM_LFSYNT}	Nominal frequency		32.768		kHz
f _{TOL_LFSYNT}	Frequency tolerance in addition to HFLCK tolerance ¹⁴		8		ppm
I _{LFSYNT}	Run current for synthesized 32.768 kHz		100		μΑ
t _{START_LFSYNT}	Startup time for synthesized 32.768 kHz		100		us

Current drawn if HFXO is forced on through for instance using the low latency power mode.

Constant temperature within ±0.5 °C and calibration performed at least every 8 seconds

Frequency tolerance will be derived from the HFCLK source clock plus the LFSYNT tolerance



20 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port might vary with product variant and package. Refer to *Registers* on page 98 and *Pin assignments* on page 11 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- · Configurable output drive strength
- · Internal pull-up and pull-down resistors
- · Wake-up from high or low level triggers on all pins
- · Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- · One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- · All pins can be individually mapped to interface blocks for layout flexibility
- · GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- · Drive strength
- · Enabling of pull-up and pull-down resistors
- Pin sensing
- · Input buffer disconnect
- · Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER* — *Power supply* on page 67 chapter for more information about retained registers.

20.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 21*: *GPIO Port and the GPIO pin details* on page 97. This mechanism is functional in both ON and OFF mode.



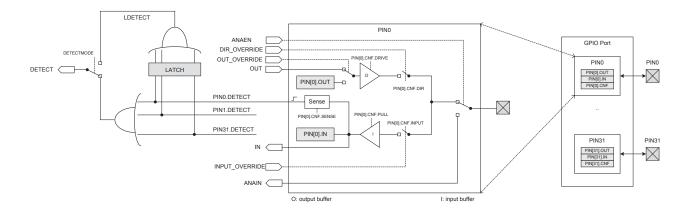


Figure 21: GPIO Port and the GPIO pin details

Figure 21: GPIO Port and the GPIO pin details on page 97 illustrates the GPIO port containing 32 individual pins, where PINO is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE* — *GPIO tasks and events* on page 142.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 22: DETECT signal behavior* on page 98.

Important: The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 21: GPIO Port and the GPIO pin details* on page 97. *Figure 22: DETECT signal behavior* on page 98 illustrates the DETECT signals behaviour for these two alternatives.

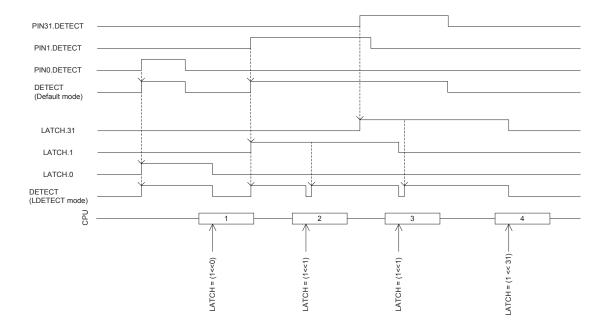


Figure 22: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 21: GPIO Port and the GPIO pin details* on page 97. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 21: GPIO Port and the GPIO pin details* on page 97.

Selected pins also support analog input signals, see ANAIN in *Figure 21: GPIO Port and the GPIO pin details* on page 97. The assignment of the analog pins can be found in *Pin assignments* on page 11.

Important: When a pin is configured as digital input, care has been taken in the nRF52810 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

20.2 GPIO located near the RADIO

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Refer to *Pin assignments* on page 11 for recommended usage guidelines to maximize radio performance in an application.

20.3 Registers

Table 26: Instances

Base address	Peripheral	Instance	Description	Configuration
0x50000000	GPIO	PO	General purpose input and output	



Table 27: Register Overview

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE
		registers
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

20.3.1 OUT

Address offset: 0x504 Write GPIO port

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2	1 0	
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N	M	L K	J	-1	Н	G	F	Ε	D	С	ВА	
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	PIN0										Pir	n 0																					
			Low	0								Pir	dri	ver	is l	ow																		
			High	1								Pir	dri	ver	is h	nigh																		
В	RW	PIN1										Pir	1																					



Bit r	numbe	er		31 30	29 28	27 26	25 2	24 2	3 22 21	20	19 1	L8 17	' 16	15	14 1	3 12	11	10	9 8	7	6	5	4 3	2	1	0
Id				f e	d c	b a	ΖV	Y)	x w v	U	Т	S R	Q	Р	0 N	I M	L	K	J I	Н	G	F	E C) С	В	Α
Res		0000000		0 0	0 0	0 0	0 (0 0 0		0	0 0	0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value					escript																	
			Low	0					in drive																	
	DIA	DINIO	High	1					in drive	ris	high															
С	KVV	PIN2	Low	0					in 2 in drive	ric	low															
			High	1					in drive																	
D	RW	PIN3	6	-					in 3	5	6															
			Low	0					in drive	r is	low															
			High	1				Р	in drive	r is	high															
Е	RW	PIN4						Р	in 4																	
			Low	0				Р	in drive	r is	low															
			High	1				Р	in drive	r is	high															
F	RW	PIN5						Р	in 5																	
			Low	0				Р	in drive	r is	low															
			High	1					in drive	r is	high															
G	RW	PIN6							in 6																	
			Low	0					in drive																	
	DIA	DINIZ	High	1					in drive	ris	high															
Н	RW	PIN7	Low	0					in 7 in drive	. i.	lavu															
			High	1					in drive																	
1	RW/	PIN8	riigii	1					in 8	1 13	mgn															
	11.00	TINO	Low	0					in drive	r is	low															
			High	1					in drive																	
J	RW	PIN9	0						in 9																	
			Low	0				Р	in drive	r is	low															
			High	1				Р	in drive	r is	high															
K	RW	PIN10						Р	in 10																	
			Low	0				Р	in drive	r is	low															
			High	1				Р	in drive	r is	high															
L	RW	PIN11						Р	in 11																	
			Low	0				Р	in drive	r is	low															
			High	1					in drive	r is	high															
М	RW	PIN12		_					in 12																	
			Low	0					in drive																	
N	D\A/	PIN13	High	1					in drive in 13	rıs	nıgn															
IN	KVV	PIN13	Low	0					in drive	ric	low															
			High	1					in drive																	
0	RW	PIN14	6	-					in 14	5																
			Low	0					in drive	r is	low															
			High	1				Р	in drive	r is	high															
Р	RW	PIN15						Р	in 15																	
			Low	0				Р	in drive	r is	low															
			High	1				Р	in drive	r is	high															
Q	RW	PIN16						Р	in 16																	
			Low	0				P	in drive	r is	low															
			High	1					in drive	r is	high															
R	RW	PIN17							in 17																	
			Low	0					in drive																	
_	D	DINIAO	High	1					in drive	r is	high															
S	RW	PIN18	Law	0					in 18	. :	la::															
			Low	0					in drive																	
Т	D\A/	PIN19	High	1					in drive in 19	1 15	nign															
	IVV	1 11473	Low	0					in drive	r ic	low															
			2011	J				r	unive	. 13	.0 00															



Bit r	numbe	er		31 30	29	28	27	26	25	24	23	3 22	21	20	19	18	3 17	16	15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2	1
Id				f e	d	С	b	а	Z	Υ	Х	w	٧	U	Т	S	R	Q	Р	С	N	М	L	K	J	1	Н	G	F	Ε	D (2	В.
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value							D	escri	iptio	on																			
			High	1							Pi	in dr	iver	is	higl	h																	
U	RW	PIN20									Pi	in 20)																				
			Low	0							Pi	n dr	iver	is	low	,																	
			High	1							Pi	n dr	iver	is	higl	h																	
V	RW	PIN21									Pi	in 21	L																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	
W	RW	PIN22									Pi	n 22	2																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	higl	h																	
Χ	RW	PIN23									Pi	in 23	}																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	
Υ	RW	PIN24									Pi	in 24	ļ																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	n dr	iver	is	higl	h																	
Z	RW	PIN25									Pi	in 25	;																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	
a	RW	PIN26									Pi	in 26	5																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	higl	h																	
b	RW	PIN27									Pi	in 27	7																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	higl	h																	
С	RW	PIN28									Pi	n 28	3																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	
d	RW	PIN29									Pi	in 2 9)																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	
е	RW	PIN30									Pi	in 30)																				
			Low	0							Pi	in dr	iver	is	low	/																	
			High	1							Pi	in dr	iver	is	hig	h																	
f	RW	PIN31									Pi	in 31	L																				
			Low	0							Pi	in dr	iver	is	low	,																	
			High	1							Pi	in dr	iver	is	hig	h																	

20.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number		31 30 29 28 2	7 26 25 2	24 23	22 21	20	19 1	.8 1	7 16	15	14 1	3 12	11	10 9	8	7	6	5	4 3	2	1 0
Id		f e d c	o a Z	Y X	W V	U	Т 5	S R	Q	Р	0 1	N M	L	K J	-1	Н	G	F	E D	С	ВА
Reset 0x00000000		0 0 0 0	0 0	0 0	0 0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0 0
Id RW Field	Value Id	Value		Des	cripti	on															
A RW PINO				Pin	0																
	Low	0		Rea	d: pin	driv	ver is	s lov	V												
	High	1		Rea	d: pin	driv	ver is	s hig	gh												
	Set	1		Wr	te: wr	iting	g a '1	l' se	ts th	ne pi	n hi	gh; w	ritin	g a '()' ha	s no	eff	ect			
B RW PIN1				Pin	1																
	Low	0		Rea	d: pin	driv	ver is	s lov	v												



Bit r	numbe	er		31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b	a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0 x0	0000000		0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value		Description
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN2		0		Pin 2
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
D	R\M	PIN3	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect Pin 3
0	11.44	11113	Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
E	RW	PIN4				Pin 4
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
F	RW	PIN5				Pin 5
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
G	RW	PIN6				Pin 6
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Н	RW	PIN7				Pin 7
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
	DIA	DINIO	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
1	KVV	PIN8	Low	0		Pin 8
			Low	1		Read: pin driver is low Read: pin driver is high
			High Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
J	RW	PIN9		_		Pin 9
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
K	RW	PIN10				Pin 10
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
L	RW	PIN11				Pin 11
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
M	RW	PIN12				Pin 12
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
	DIA	DINI42	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
N	KW	PIN13	Low	0		Pin 13
			Low	0		Read: pin driver is low
			High Set	1		Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
0	R/v/	PIN14	Jet	1		Pin 14
J	11.44		Low	0		Read: pin driver is low
			High	1		Read: pin driver is low
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Р	RW	PIN15				Pin 15
		-				



Bit r	numbe	er		31 30	29 28	27 2	6 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Q	RW	PIN16		^				Pin 16
			Low	0				Read: pin driver is low
			High Set	1				Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
R	RW/	PIN17	Jei	1				Pin 17
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
S	RW	PIN18						Pin 18
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Т	RW	PIN19						Pin 19
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
\ /	DVA	DINI24	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
V	KVV	PIN21	Low	0				Pin 21 Read: pin driver is low
			High	1				Read: pin driver is low
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
W	RW	PIN22		-				Pin 22
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Χ	RW	PIN23						Pin 23
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Υ	RW	PIN24						Pin 24
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
_	2111		Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Z	RW	PIN25	Laur	0				Pin 25
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
a	R\M/	PIN26	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect Pin 26
u	1100	111120	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
b	RW	PIN27						Pin 27
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN28						Pin 28
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3	2 :	1 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N	M	L I	(J	- 1	Н	G	F	Ε	D	C E	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																		
d	RW	PIN29										Pin	29																				
			Low	0								Rea	ad: p	pin	dri	ver	is l	ow															
			High	1								Rea	ad: p	pin	dri	ver	is h	nigh															
			Set	1								Wr	ite:	wri	itin	g a	'1'	sets	th	e pi	n h	igh;	wri	ting	a '0)' ha	s no	o ef	fect				
е	RW	PIN30										Pin	30																				
			Low	0								Rea	ad: p	pin	dri	ver	is l	ow															
			High	1								Rea	ad: p	pin	dri	ver	is h	nigh															
			Set	1								Wr	ite:	wri	itin	g a	'1'	sets	th	e pi	n h	igh;	wri	ting	a 'C)' ha	s no	o ef	fect	:			
f	RW	PIN31										Pin	31																				
			Low	0								Rea	ad: p	pin	dri	ver	is l	ow															
			High	1								Rea	ad: p	pin	dri	ver	is h	nigh															
			Set	1								Wr	ite:	wri	itin	g a	'1'	sets	th	e pi	n h	igh;	wri	ting	a 'C)' ha	s no	o ef	fect				

20.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port Read: reads value of OUT register.

Bit	numb	er		31 30	0 29	28 2	7 26	25 2	4 2	23 22 21	20 19	18	17 1	6 15	14	13	12 1	1 10	9	8	7	6 5	5 4	3	2	1 0
Id				f e	e d	c l	о а	Z۱	/	x w v	U T	S	R (Q P	0	N	М	L K	J	1	Н	G I	E	D	С	ВА
Res	et 0x0	0000000		0 0	0	0 (0 0	0 ()	0 0 0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Valu	е					Description	on															
Α	RW	PIN0							F	Pin 0																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	w;	writ	ing a	'0' l	has	no e	effe	t			
В	RW	PIN1							F	Pin 1																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
С	RW	PIN2							F	Pin 2																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
D	RW	PIN3							F	Pin 3																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
Е	RW	PIN4							F	Pin 4																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
F	RW	PIN5							F	Pin 5																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
G	RW	PIN6							F	Pin 6																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													
			Clear	1					١	Write: wr	riting a	'1' s	ets	the p	oin lo	ow;	writ	ing a	'0' l	has	no e	effe	t			
Н	RW	PIN7								Pin 7																
			Low	0					F	Read: pin	drive	is lo	w													
			High	1					F	Read: pin	drive	is h	igh													



Bit r	umbe	er		31 30 2	9 28 2	7 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d	d c l	оа	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Res	et 0x0	0000000		0 0 0	0 0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
I	RW	PIN8						Pin 8
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	RW	PIN9	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect Pin 9
J	IV V V	FINS	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
K	RW	PIN10		_				Pin 10
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
L	RW	PIN11						Pin 11
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
М	RW	PIN12						Pin 12
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
N	RW	PIN13						Pin 13
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
0	D\A/	PIN14	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect Pin 14
U	NVV	PIN14	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Р	RW	PIN15						Pin 15
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Q	RW	PIN16						Pin 16
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
R	RW	PIN17						Pin 17
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
_	D\A/	DIN 10	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
S	r(VV	PIN18	Low	0				Pin 18 Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Т	RW	PIN19		-				Pin 19
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
V	RW	PIN21						Pin 21
			Low	0				Read: pin driver is low



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
W	RW	PIN22			Pin 22
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Χ	RW	PIN23			Pin 23
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Υ	RW	PIN24			Pin 24
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Z	RW	PIN25			Pin 25
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
а	RW	PIN26			Pin 26
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
b	RW	PIN27			Pin 27
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
	DIA	DINIO	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN28			Pin 28
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
d	D\A/	DINIO	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
d	RW	PIN29	Low	0	Pin 29
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
	D\A/	DINIO	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
е	KVV	PIN30	Low	0	Pin 30 Read: pin driver is low
			Low High	1	Read: pin driver is low
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
f	R/V/	PIN31	Cical		Pin 31
	IVVV	1 11431	Low	0	Read: pin driver is low
			High	1	Read: pin driver is low
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
			cicai	1	write. writing a 1 sets the pin low, writing a 0 has no effect

20.3.4 IN

Address offset: 0x510 Read GPIO port

Bit	number				1 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	L3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U 1	ΓS	R	Q	Р	0	N N	1 L	K	J	1	Н	G	F	Ε	D C	В	Α
Res	et Ox	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue	:						Des	scri	ptio	n																	
Α	R	PIN0										Pin	0																			
			Low	0								Pin	inp	ut is	s lov	V																
			High	1							Pin input is high																					



Bit n	umbe	r		31 30	29 28	27 26	5 25 24	4 23 2	22 21 :	20 19	18	17 1	6 15	14 :	L3 12	11	10 9	8	7	6 5	5 4	3 2	1	0
Id									w v															
Rese	t 0x0	0000000		0 0	0 0	0 0	0 0	0	0 0	0 0	0	0 (0	0	0 0	0	0 (0	0	0 (0 0	0 (0	0
Id	RW	Field	Value Id	Value				Des	criptio	n														
В	R	PIN1						Pin	1															
			Low	0				Pin	input i	s low														
			High	1				Pin	input i	s high	1													
С	R	PIN2						Pin																
			Low	0					input i															
			High	1					input i	s high	1													
D	R	PIN3						Pin																
			Low	0					input i															
_			High	1					input i	s high	1													
E	R	PIN4						Pin																
			Low	0					input i															
г	D	DINE	High	1					input i	s nign	1													
۲	R	PIN5	Low	0				Pin																
			Low	0					input i															
G	R	PIN6	High	1				Pin		s mgn														
J	17	I IIVU	Low	0					input i	s low														
			High	1					input i															
Н	R	PIN7	111811	_				Pin		3 mgm	'													
••			Low	0					input i	s low														
			High	1					input i															
I	R	PIN8	Ü					Pin		. 0														
			Low	0					input i	s low														
			High	1					input i															
J	R	PIN9	_					Pin	9															
			Low	0				Pin	input i	s low														
			High	1				Pin	input i	s high	1													
K	R	PIN10						Pin	10															
			Low	0				Pin	input i	s low														
			High	1				Pin	input i	s high	1													
L	R	PIN11						Pin	11															
			Low	0				Pin	input i	s low														
			High	1				Pin	input i	s high	1													
M	R	PIN12						Pin	12															
			Low	0					input i															
			High	1					input i	s high	1													
N	R	PIN13						Pin																
			Low	0					input i															
		DINIA	High	1					input i	s high	1													
0	R	PIN14	Low	0				Pin		a I -														
			Low	0					input i															
Р	D	PIN15	High	1				Pin		s mgn														
۲	R	CINII	Low	0					input i	s low														
			High	1					input i															
Q	R	PIN16	6''					Pin		- mg1														
٠.			Low	0					input i	s low														
			High	1					input i															
R	R	PIN17						Pin		.0.														
			Low	0					input i	s low														
			High	1					input i															
S	R	PIN18	-					Pin																
			Low	0					input i	s low														
			High	1					input i															
Т	R	PIN19						Pin																



Bit n	umbe	er		31 30	2	9 28	27	7 26	25	24	23	3 22 2	1 2	20 1	9 :	18 1	17 :	16	15 :	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				f e	С	d c	b	а	Z	Υ	Χ	W١	/	U I	Г	S	R	Q	Р	0	N N	1 [. K	J	1	Н	G	F	ΕI	D C	В	Α
Rese	et 0x0	0000000		0 0	C	0	0	0	0	0	0	0 ()	0 ()	0	0	0	0	0	0 0	(0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	2						De	escrip	tio	n																		
			Low	0							Pir	n inpu	ıt i:	s lov	v																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
U	R	PIN20									Pir	n 20																				
			Low	0							Pir	n inpu	ıt i:	s lov	v																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
V	R	PIN21									Pir	n 21																				
			Low	0							Pir	n inpu	ıt i:	s lov	V																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
W	R	PIN22									Pir	n 22																				
			Low	0							Pir	n inpu	ıt i:	s lov	V																	
			High	1							Pir	n inpu	ıt i	s hig	gh																	
Χ	R	PIN23									Pir	n 23																				
			Low	0							Pir	n inpu	ıt i	s lov	V																	
			High	1							Pir	n inpu	ıt i	s hig	gh																	
Υ	R	PIN24									Pir	n 24																				
			Low	0							Pir	n inpu	ıt i	s lov	V																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
Z	R	PIN25									Pir	n 25																				
			Low	0							Pir	n inpu	ıt i	s lov	V																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
а	R	PIN26									Pir	n 26																				
			Low	0							Pir	n inpu	ıt i	s lov	V																	
			High	1							Pir	n inpu	ıt i:	s hig	gh																	
b	R	PIN27									Pir	n 27																				
			Low	0							Pir	n inpu	ıt i:	s lov	V																	
			High	1								n inpu	ıt i:	s hig	gh																	
С	R	PIN28										n 28																				
			Low	0							Pir	n inpu	ıt i	s lov	V																	
			High	1								n inpu	ıt i:	s hig	gh																	
d	R	PIN29										n 29																				
			Low	0								n inpu																				
			High	1								n inpu	ıt i:	s hig	gh																	
е	R	PIN30										n 30																				
			Low	0								n inpu																				
			High	1								n inpu	ıt i:	s hig	gh																	
f	R	PIN31										n 31																				
			Low	0								n inpu																				
			High	1							Pir	n inpu	ıt i	s hig	gh																	

20.3.5 DIR

Address offset: 0x514 Direction of GPIO pins

Bit	numbe	er		31 30 29 28 27 26 25 2									22	21	20	19	18	17	16	15	14	13	12	11 1	10 9	9	8 7	6	5	4	3	2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N	M	L	Κ.	J	I H	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	iptic	n																			
Α	RW	PIN0										Pir	n 0																					_
			Input	0								Pir	se	t as	inp	ut																		
			Output	1								Pir	se	t as	out	put	t																	
В	RW	PIN1										Pir	1																					
			Input	0								Pir	set	t as	inp	ut																		
			Output	1								Pin set as output																						
С	RW	PIN2											12																					



Bit r	umbe	er		31 30	29 2	28 2	7 26	25 24	4 2	3 22 21	1 20) 19 1	L8 17	' 16	15	14 1	3 12	11	10	9 8	3 7	6	5	4 3	3 2	1 (
Id				f e	d	c b	а	Z Y	/	x w v	/ U	Т	S R	Q	Р	1 0	۱ M	L	K	J	Н	G	F	E C) С	ВА
Rese	et 0x0	0000000		0 0	0	0 0	0	0 0) (0 0	0	0	0 0	0	0	0 (0	0	0	0 (0	0	0	0 0	0	0 (
Id	RW	Field	Value Id	Value	9				D	escript	ion															
			Input	0						in set a																
-	DVA	DINIA	Output	1						in set a	IS OI	utput														
D	KW	PIN3	lanut	0						in 3 in set a																
			Input Output	1						in set a																
E	RW	PIN4	Output	1						in 4	13 00	асрас														
			Input	0						in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
F	RW	PIN5							Р	in 5																
			Input	0					Р	in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
G	RW	PIN6							Р	in 6																
			Input	0					Р	in set a	ıs in	put														
			Output	1						in set a	IS OI	utput														
Н	RW	PIN7								in 7																
			Input	0						in set a																
1	D\A/	PIN8	Output	1						in set a in 8	IS OI	utput														
'	NVV	rino	Input	0						in set a	ıc in	nut														
			Output	1						in set a																
J	RW	PIN9	Catput	_						in 9		асрас														
			Input	0						in set a	ıs in	put														
			Output	1						in set a																
K	RW	PIN10							Р	in 10																
			Input	0					Р	in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
L	RW	PIN11							Р	in 11																
			Input	0						in set a																
	DIA	DINIA	Output	1						in set a	IS OI	utput														
M	KW	PIN12	lanut	0						in 12																
			Input Output	1						in set a in set a																
N	RW	PIN13	Output	_						in 13	13 00	асрас														
			Input	0						in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
0	RW	PIN14								in 14																
			Input	0					Р	in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
Р	RW	PIN15							Р	in 15																
			Input	0						in set a																
	P	DINIAG	Output	1						in set a	IS OI	utput														
Q	КW	PIN16	Innut	0						in 16	·c :	nı.+														
			Input	0						in set a																
R	RW/	PIN17	Output	1						in set a in 17	is Ul	atput														
	11.00		Input	0						in set a	ıs in	put														
			Output	1						in set a																
S	RW	PIN18								in 18																
			Input	0					Р	in set a	ıs in	put														
			Output	1					Р	in set a	ıs oı	utput														
Т	RW	PIN19							Р	in 19																
			Input	0					Р	in set a	ıs in	put														
			Output	1					Р	in set a	is ou	utput														
U	RW	PIN20								in 20																
			Input	0					Р	in set a	ıs in	put														



Bit	numbe	er		31 30	29 :	28 2	7 26	25 2	24 :	23 2	22 21	20	19	18 17	7 16	15	14 :	13 12	11	10	9	8 7	6	5	4	3 2	1	0
Id				f e	d	c I	b a	Ζ	Υ	ΧV	w v	U	Т	S R	Q	Р	0	N M	L	K	J	ΙН	G	i F	Ε	D C	В	Α
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0 (0 0	0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value					-	Des	cripti	on																
			Output	1					-	Pin s	set as	out	tput															
V	RW	PIN21							-	Pin 2	21																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
W	RW	PIN22							-	Pin 2	22																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
Χ	RW	PIN23							-	Pin 2	23																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
Υ	RW	PIN24							-	Pin 2	24																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
Z	RW	PIN25							-	Pin 2	25																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
а	RW	PIN26							-	Pin 2	26																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
b	RW	PIN27							-	Pin 2	27																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					- 1	Pin s	set as	out	tput															
С	RW	PIN28							-	Pin 2	28																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
d	RW	PIN29							-	Pin 2	29																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					- 1	Pin s	set as	out	tput															
е	RW	PIN30							-	Pin 3	30																	
			Input	0					1	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															
f	RW	PIN31							-	Pin 3	31																	
			Input	0					-	Pin s	set as	inp	ut															
			Output	1					-	Pin s	set as	out	tput															

20.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit r	umbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R	Q	Р	О	N	M	L	K	J	1	Н	G	F	Е	D	С	ВА	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																				ı
Α	RW	PIN0										Set	t as	out	put	t pi	n 0																		
			Input	0								Re	ad:	pin	set	as	inp	ut																	
			Output	1								Re	ad:	pin	set	as	out	put	:																
			Set	1								Wr	ite:	wr	itin	g a	'1'	sets	pi	n to	ou	tpu	t; w	/riti	ng a	a '0	' ha	s n	o e	ffe	t				
В	RW	PIN1										Set	t as	out	put	t pi	n 1																		
			Input	0								Re	ad:	pin	set	as	inp	ut																	
			Output	1								Re	ad:	pin	set	as	out	put	:																
			Set	1								Wr	ite:	wr	itin	g a	'1'	sets	pi	n to	ou	tpu	t; w	/riti	ng a	a '0	' ha	s n	o e	ffe	ct				
С	RW	PIN2										Set	t as	out	put	t pi	n 2																		



Bit n	umbe	er		31 30	29 28 :	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese		0000000			0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_	B111	2442	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
D	RW	PIN3						Set as output pin 3
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_	B111		Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
E	RW	PIN4						Set as output pin 4
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
-	DVA	DINE	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
F	RW	PIN5	lam.	0				Set as output pin 5
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_	DIA	DINIC	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
G	KVV	PIN6	land.	0				Set as output pin 6
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	DVA	DIAIZ	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
H	KVV	PIN7	land.	0				Set as output pin 7
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	D\A/	PIN8	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
	KVV	PIN8	Innut	0				Set as output pin 8
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
ı	D\A/	PIN9	Set	1				Set as output pin 9
,	11.00	FINS	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
K	D\A/	PIN10	Set	1				Set as output pin 10
IX.	11.00	FINIO	Innut	0				Read: pin set as input
			Input Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
L	R\M	PIN11	Jei	1				Set as output pin 11
_	IVV	LINTI	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
М	R\M/	PIN12	Set	1				Set as output pin 12
ıvı	11.00	1 11112	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
N	R\M	PIN13	361	_				Set as output pin 13
14	11.00	111113	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
0	RW/	PIN14		-				Set as output pin 14
_			Input	0				Read: pin set as input
			Output	1				Read: pin set as input
				1				
D	DIA	DINI15	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
*	K VV	PIN15	Innut	0				Set as output pin 15
			Input	0				Read: pin set as output
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFE	D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
Id	RW Field	Value Id	Value Description	
Q	RW PIN16		Set as output pin 16	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
_		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
R	RW PIN17		Set as output pin 17	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
_	DIA DINA	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
S	RW PIN18		Set as output pin 18	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
-	DIA DINA	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
1	RW PIN19		Set as output pin 19	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
U	RW PIN20		Set as output pin 20	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
	D	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
V	RW PIN21		Set as output pin 21	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
W	RW PIN22		Set as output pin 22	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
Χ	RW PIN23		Set as output pin 23	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
Υ	RW PIN24		Set as output pin 24	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
_		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
Z	RW PIN25		Set as output pin 25	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
	DIM DINI26	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
а	RW PIN26	lanc.	Set as output pin 26	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
	DIA DINIZZ	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
b	RW PIN27	lan t	Set as output pin 27	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
	DIA DIACC	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
С	RW PIN28		Set as output pin 28	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	
		Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect	
d	RW PIN29		Set as output pin 29	
		Input	0 Read: pin set as input	
		Output	1 Read: pin set as output	



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
e RW PIN30		Set as output pin 30
	Input	0 Read: pin set as input
	Output	1 Read: pin set as output
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
f RW PIN31		Set as output pin 31
	Input	0 Read: pin set as input
	Output	1 Read: pin set as output
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect

20.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

Bit r	number			31 30	29	28 2	7 20	6 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	c l	b a	ı Z	Υ	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	000000		0 0	0	0	0 0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	9					Description
Α	RW	PIN0								Set as input pin 0
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
В	RW I	PIN1								Set as input pin 1
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW	PIN2								Set as input pin 2
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW I	PIN3								Set as input pin 3
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
Ε	RW	PIN4								Set as input pin 4
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
F	RW	PIN5								Set as input pin 5
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
G	RW	PIN6								Set as input pin 6
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
Н	RW I	PIN7								Set as input pin 7
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1						Write: writing a '1' sets pin to input; writing a '0' has no effect
I	RW	PIN8								Set as input pin 8
			Input	0						Read: pin set as input



Bit r	numbe	er		31 30 29	28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d	c I	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0	0 (0 0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value				Description
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
J	RW	PIN9						Set as input pin 9
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
K	RW	PIN10						Set as input pin 10
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
L	RW	PIN11						Set as input pin 11
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
M	RW	PIN12						Set as input pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
N	RW	PIN13						Set as input pin 13
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	DIA	DINIA	Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
0	RW	PIN14	land.	0				Set as input pin 14
			Input	0				Read: pin set as input
			Output Clear	1				Read: pin set as output Write: writing a '1' sets pin to input; writing a '0' has no effect
D	D\A/	PIN15	Cledi	1				Write: writing a '1' sets pin to input; writing a '0' has no effect Set as input pin 15
r	IVVV	LIMID	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
Q	RW	PIN16	Ciccii.	-				Set as input pin 16
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
R	RW	PIN17						Set as input pin 17
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
S	RW	PIN18						Set as input pin 18
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
Т	RW	PIN19						Set as input pin 19
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
U	RW	PIN20						Set as input pin 20
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
V	RW	PIN21						Set as input pin 21
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Clear	1				Write: writing a '1' sets pin to input; writing a '0' has no effect
W	RW	PIN22						Set as input pin 22



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Χ	RW PIN23			Set as input pin 23
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Υ	RW PIN24			Set as input pin 24
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Z	RW PIN25			Set as input pin 25
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
а	RW PIN26			Set as input pin 26
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
b	RW PIN27			Set as input pin 27
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN28			Set as input pin 28
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
d	RW PIN29			Set as input pin 29
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
е	RW PIN30			Set as input pin 30
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
	DIM DINI24	Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Ť	RW PIN31		•	Set as input pin 31
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect

20.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

Bit	numbe	er		31	. 30	29	28	27	26	25	24 :	23 2	22 2	21 2	0 1	.9 1	8 1	7 16	15	14	13	12	11	LO !	9 :	8 7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	X	w '	Vι	J -	T S	F	R Q	P	0	Ν	M	L	Κ .	J	I H	G	F	Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue						- 1	Des	crip	tior	1																	
Α	RW	PIN0										Stat	us c	on w	/he	the	r PI	NO ł	nas	met	cri	teria	a se	t in	PIN	_CN	F0.9	SEN	SE			
											-	regi	ster	r. W	rite	e '1'	to (clea	r.													
			NotLatched	0							(Crit	eria	has	nc	ot be	een	me	t													
			Latched	1							(Crit	eria	has	be	een	me	t														
В	RW	PIN1										Stat	us c	on w	/he	the	r PI	N1 ł	nas	met	cri	teria	a se	t in	PIN	_CN	F1.5	SEN	SE			
											-	regi	ster	r. W	rite	e '1'	to (clea	r.													



Bit r	numbe	er		31 30	29 28	3 27 2	6 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								'XWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0	0 0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	9			Description
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
С	RW	PIN2						Status on whether PIN2 has met criteria set in PIN_CNF2.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
D	RW	PIN3						Status on whether PIN3 has met criteria set in PIN_CNF3.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
E	RW	PIN4						Status on whether PIN4 has met criteria set in PIN_CNF4.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
_			Latched	1				Criteria has been met
F	RW	PIN5						Status on whether PIN5 has met criteria set in PIN_CNF5.SENSE
			Not otok	0				register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
_	D\A/	DING	Latched	1				Criteria has been met
G	KVV	PIN6						Status on whether PIN6 has met criteria set in PIN_CNF6.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
Н	RW	PIN7	Editifica	-				Status on whether PIN7 has met criteria set in PIN_CNF7.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
ı	RW	PIN8						Status on whether PIN8 has met criteria set in PIN_CNF8.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
J	RW	PIN9						Status on whether PIN9 has met criteria set in PIN_CNF9.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
K	RW	PIN10						Status on whether PIN10 has met criteria set in
								PIN_CNF10.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
L	RW	PIN11						Status on whether PIN11 has met criteria set in
				_				PIN_CNF11.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
	DVA	DINIA	Latched	1				Criteria has been met
М	KVV	PIN12						Status on whether PIN12 has met criteria set in PIN CNE12 SENSE register. Write '1' to clear
			NotLatched	0				PIN_CNF12.SENSE register. Write '1' to clear. Criteria has not been met
			Latched	1				Criteria has been met
N	RW	PIN13		_				Status on whether PIN13 has met criteria set in
.,								PIN_CNF13.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
0	RW	PIN14		-				Status on whether PIN14 has met criteria set in
-								PIN_CNF14.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met



Bit	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			f e d c b a	Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Р	RW PIN15			Status on whether PIN15 has met criteria set in
				PIN_CNF15.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
	B.11 B.1116	Latched	1	Criteria has been met
Q	RW PIN16			Status on whether PIN16 has met criteria set in
		NotLatched	0	PIN_CNF16.SENSE register. Write '1' to clear. Criteria has not been met
		Latched	1	Criteria has been met
R	RW PIN17	2000.100	-	Status on whether PIN17 has met criteria set in
				PIN_CNF17.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
S	RW PIN18			Status on whether PIN18 has met criteria set in
				PIN_CNF18.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Т	RW PIN19			Status on whether PIN19 has met criteria set in
				PIN_CNF19.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
	DW DINIO	Latched	1	Criteria has been met
U	RW PIN20			Status on whether PIN20 has met criteria set in PIN_CNF20.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
V	RW PIN21			Status on whether PIN21 has met criteria set in
				PIN_CNF21.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
W	RW PIN22			Status on whether PIN22 has met criteria set in
				PIN_CNF22.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Х	RW PIN23			Status on whether PIN23 has met criteria set in
		Noted and and	0	PIN_CNF23.SENSE register. Write '1' to clear.
		NotLatched Latched	0 1	Criteria has not been met Criteria has been met
Υ	RW PIN24	Lattried	1	Status on whether PIN24 has met criteria set in
•	11124			PIN_CNF24.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Z	RW PIN25			Status on whether PIN25 has met criteria set in
				PIN_CNF25.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
а	RW PIN26			Status on whether PIN26 has met criteria set in
			_	PIN_CNF26.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
h	DW/ DIN 27	Latched	1	Criteria has been met
b	RW PIN27			Status on whether PIN27 has met criteria set in
		NotLatched	0	PIN_CNF27.SENSE register. Write '1' to clear. Criteria has not been met
		Latched	1	Criteria has been met
С	RW PIN28			Status on whether PIN28 has met criteria set in
				PIN_CNF28.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met



Bit r	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 2	3 2:	2 21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id				f	e	d	С	b	a i	Z '	Y X	(W	v v	U	Т	S	R	Q	Р	О	N I	ИΙ	_ K	J	1	Н	G	F	E C	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Val	lue						D	esc	ripti	on																		
			Latched	1							С	rite	ria h	as l	bee	n m	et															
d	RW	PIN29									St	tatu	ıs or	wł	neth	ner I	PIN	29 ł	nas	me	cri	teri	set	in								
											Р	IN_	CNF	29.9	SEN	SE r	egis	ster	. W	rite	'1'	to c	lear									
			NotLatched	0							С	rite	ria h	as ı	not	bee	n m	net														
			Latched	1							С	rite	ria h	as l	bee	n m	et															
е	RW	PIN30									St	tatu	ıs or	wh	neth	ier I	PIN:	30 ł	nas	me	cri	teri	a set	in								
											Р	IN_	CNF	30.9	SEN	SE r	egis	ster	. W	rite	'1'	to c	lear									
			NotLatched	0							С	rite	ria h	as ı	not	bee	n n	net														
			Latched	1							С	rite	ria h	as l	bee	n m	et															
f	RW	PIN31									St	tatu	ıs or	wh	neth	er I	PIN:	31 h	nas	me	cri	teri	a set	in								
											Р	IN_	CNF	31.9	SEN	SE r	egis	ster	. W	rite	'1'	to c	lear									
			NotLatched	0							С	rite	ria h	as ı	not	bee	n n	net														
			Latched	1							С	rite	ria h	as l	bee	n m	et															

20.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 18	8 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5 .	4 3	2	1	0
Id																																Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Α	RW	DETECTMODE										Sele	ect l	oetv	vee	n de	efau	lt D	ETE	CT s	igna	l be	havi	our	and	l LD	ETE	СТ				
												mo	de																			
			Default	0								DET	ΓECT	dir	ectl	ly co	onne	ecte	d to	PIN	I DE	TEC	T sig	nals	5							
			LDETECT	1								Use	the	e lat	che	d L[DET	ECT	beh	avio	ur											

20.3.10 PIN_CNF[0]

Address offset: 0x700

Bit r	numbe	er e		31	30	29 2	28.2	77 :	26.2	5 2	4 2	3 2:	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				01				- ' -		_		J					E			- '					D	D		Ŭ	Ŭ		С	<u>-</u>	ВА
	at NvC	0000002		0	0	0	0	n	0 0		0 0	٠ n	0	0	n	0	_	0	n	n	0	0	0	0	0	0	n	0	n	n			1 0
Id		Field	Value Id	_	lue	•		•		,	ח	0000	ripti	o on		•	Ü	•	•	Ü	Ü	Ū	Ü	Ü	Ü	Ü		•			•	•	
		DIR	value lu	va	iue								•		Co.		n h	vele	ما د				DII	2 = 0	-i-								
Α	KVV	DIK											irect							egi	ste	dS	ווט	N I E	gis	ler							
			Input	0									gure	•																			
			Output	1							С	onfi	gure	pir	n as	an	ou	tpu	pir	1													
В	RW	INPUT									С	onn	ect o	or d	isco	nn	ect	inp	ut k	uf	fer												
			Connect	0							С	onn	ect i	npu	ıt bı	uffe	er																
			Disconnect	1							D	isco	nne	ct ir	nput	b.	ıffe	r															
С	RW	PULL									Р	ull c	onfi	gura	atio	n																	
			Disabled	0							N	lo p	ull																				
			Pulldown	1							Р	ull c	lowr	on	pin																		
			Pullup	3							Р	ull u	ıp or	n pir	n																		
D	RW	DRIVE									D	rive	con	figu	ırati	on																	
			S0S1	0							St	tano	dard	'0',	staı	nda	ırd	'1'															
			H0S1	1							Н	ligh	drive	9 '0'	, sta	and	lard	1'1'															
			SOH1	2							St	tano	dard	'0',	higl	h d	rive	1'															
			H0H1	3							Н	ligh	drive	e '0'	, hi	gh '	dri	ve '	1''														
			DOS1	4							D	isco	nne	ct 'C)' st	and	dar	1'1	(nc	orm	all	y us	sed	for	wii	ed-	or						
											C	onn	ectic	ns)																			



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002		$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value Description
	D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
		connections)
	SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
		connections)
	H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
	Disabled	0 Disabled
	High	2 Sense for high level
	Low	3 Sense for low level

20.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

Bit nu	mbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Reset	0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld I	RW	Field	Value Id	Value	Description
A I	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В І	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
C I	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D I	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E I	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.12 PIN_CNF[2]

Address offset: 0x708



Bit r	umbe	er		3	1 30	29	28 2	27 26	5 25	24	23	22 2:	1 20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5 4	1 3	3 2	1	0
Id																Ε	Ε					D	D	D				(С	В	Α
Rese	et 0x0	0000002		0	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0) (0	1	0
Id	RW	Field	Value Id	٧	alue						Des	cript	ion																		
Α	RW	DIR									Pin	dired	ction	ո. Sa	me	phy	ysic	al r	egis	ter a	s D	IR r	egis	ter							
			Input	0							Con	nfigur	e pi	in as	an	inp	ut p	in													
			Output	1							Con	nfigur	e pi	in as	an	out	put	piı	1												
В	RW	INPUT									Con	nect	or	disco	nne	ect	inp	ut k	ouff	er											
			Connect	0							Con	nect	inp	ut b	uffe	r															
			Disconnect	1							Disc	conn	ect i	inpu	t bu	ıffe	r														
С	RW	PULL									Pull	conf	figuı	ratio	n																
			Disabled	0							No	pull																			
			Pulldown	1							Pull	l dow	n o	n pir	1																
			Pullup	3							Pull	l up c	n p	in																	
D	RW	DRIVE									Driv	ve co	nfig	urat	ion																
			S0S1	0							Stai	ndar	d '0'	, sta	nda	rd '	'1'														
			H0S1	1							Higl	h dri	ve 'C)', st	and	ard	'1'														
			S0H1	2							Star	ndar	'0' b	, hig	h dr	rive	'1'														
			H0H1	3							Higl	h dri	ve 'C)', hi	gh '	driv	/e '1	L'''													
			DOS1	4							Disc	conn	ect '	'0' st	and	lard	1'1'	(no	rm	ally i	use	d fo	r wi	red	or						
											con	nect	ions	5)																	
			D0H1	5								conn			igh	dri	ve '	1' (norı	mally	/ us	ed f	or v	wire	d-o	r					
			SOD1	6								necti ndar		′			+ 14	۱/۵		بالد		d fo		امما		۵					
			3001	U								nect			.011	nec	1	(11)	UIII	lally	use	uic)I VV	iieu	-a11	u					
			H0D1	7							Higl	h driv	ve 'C)', di	scoi	nne	ct '	1' (nori	mally	y us	ed f	or v	wire	d-aı	nd					
											con	nect	ions	5)																	
Е	RW	SENSE									Pin	sens	ing	mec	nan	ism															
			Disabled	0							Disa	abled	ı																		
			High	2							Sen	se fo	r hi	gh le	vel																
			Low	3							Sen	se fo	r lo	w le	/el																
			LOW	3							Jen	136 10	110	W IC	/61																

20.3.13 PIN_CNF[3]

Address offset: 0x70C Configuration of GPIO pins

Bit r	numb	er		31	30	29	28	27	26 2	25 :	24 :	23.2	22 2	1 2	0 1	19 1	8 1	7 1	6 1	15 1	4 1	3 1	2 1	1 10) 9	8	7	6	5	4	3	2	1)
Id																		E I) D	D					- C	- C	В.	΄
	et Oxí	00000002		0	0	0	0	0	0	n	0	0	0	0	n	0 (n (0	0	0 () (ם מ		0	0	0	n	0			1	
Id		Field	Value Id	_	lue	ŭ	•	•		•	۰	Des	crir	tio	2				•				,							•	•	•		ĺ
A		DIR	value lu	Vo	iue							Pin (Can	20.1	shve	cica	al ro	aic	tor	ac F	ND .	ogic	tor								
А	KVV	DIK		_														•			gis	ler	dS L	ואונ	egis	ier								
			Input	0								Con	_					•																
			Output	1							(Con	figu	ıre	pin	as a	n c	outp	out	pin														
В	RW	INPUT									(Con	nec	t or	di	scor	nne	ct i	npı	ıt b	uffe	er												
			Connect	0							(Con	nec	t in	put	but	ffer	-																
			Disconnect	1							[Disc	coni	nect	in	put	but	fer																
С	RW	PULL									F	Pull	100	nfig	ura	tion																		
			Disabled	0							1	No p	pull																					
			Pulldown	1							F	Pull	do	wn	on	pin																		
			Pullup	3							F	Pull	up	on	pin																			
D	RW	DRIVE									[Driv	e c	onfi	gui	atic	n																	
			S0S1	0							9	Stan	nda	rd '()', s	tan	dar	'd '1	l'															
			H0S1	1							ŀ	High	h dr	ive	'0',	staı	nda	ard	'1'															
			SOH1	2							9	Stan	nda	rd '()', ł	nigh	dri	ve	'1'															
			H0H1	3							ı	High	h dr	ive	'0',	hig	h 'c	lriv	e '1	0														
			DOS1	4							[Disc	coni	nect	'0'	sta	nda	ard	'1'	(no	rma	ally	use	d fc	r w	ired	-or							
											(coni	nec	tior	ıs)																			



Bit number	31 30	0 29 28 27 26 25 24 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E DDD CCBA
Reset 0x00000002	0 0	0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field Value	ue Id Value	e [Description
D0H	11 5	[Disconnect '0', high drive '1' (normally used for wired-or
		C	connections)
SOD	1 6	9	Standard '0'. disconnect '1' (normally used for wired-and
		C	connections)
HOD	7	ŀ	High drive '0', disconnect '1' (normally used for wired-and
		C	connections)
E RW SENSE		F	Pin sensing mechanism
Disa	abled 0	[Disabled
High	h 2	9	Sense for high level
Low	3	9	Sense for low level

20.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

Bit	numbe	er		31	30	29	28	27	26	25	24	23	3 2	22 21	20) 1:	9 18	3 1	7 16	6 1	5 1	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		Е	Е							D	D	D					С	С	В	Α
Res	et 0x0	0000002		0	0	0	0	0	0	0	0	0) (0 0	0	C	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Id	RW	Field	Value Id	Va	lue							De	esc	criptio	on																					
Α	RW	DIR										Piı	in c	direct	ior	n. S	Sam	e p	hys	ica	l re	gis	ter	as	DI	R re	egis	ter								
			Input	0								Cc	onf	figure	e pi	in a	as a	n ir	put	t pi	n															
			Output	1								Co	onf	figure	e pi	in a	as a	n o	utp	ut	pin															
В	RW	INPUT										Co	oni	nect o	or (dis	con	nec	t in	pu	t b	uff	er													
			Connect	0								Co	oni	nect i	np	ut	buf	fer																		
			Disconnect	1								Di	isc	conne	ct i	inp	ut l	ouf	fer																	
С	RW	PULL										Pu	ull	confi	gui	rat	ion																			
			Disabled	0								No	o p	pull																						
			Pulldown	1								Pu	ull	dowr	0	n p	in																			
			Pullup	3								Pu	ull	up or	n p	in																				
D	RW	DRIVE										Dr	riv	e con	fig	ura	atio	n																		
			S0S1	0								St	an	ndard	'0'	, st	tano	dar	d '1																	
			H0S1	1								Hi	igh	n drive	e 'C)', :	star	ıda	rd ':	1'																
			SOH1	2								St	an	ndard	'0'	, h	igh	driv	/e ':	1'																
			H0H1	3								Hi	igh	n drive	e 'C)',	high	'd	rive	'1																
			DOS1	4								Di	isc	conne	ct '	'0'	star	nda	rd '	1' (no	rm	ally	us	sed	foi	wi	ired	-or							
												со	onr	nectio	ons	5)																				
			D0H1	5										onne nectic			hig	h d	rive	e '1	' (r	ori	mal	lly	use	ed f	or	wire	d-o	r						
			SOD1	6										ndard			isco	nn	ect	'1'	(nc	nrm	all	v 11	SEI	l fo	r w	ired	l-an	hd						
			3001	Ü										nectic			1500			-	(,,,,,		, u			. ••			iu						
			H0D1	7								Hi	igh	n drive	e 'C)', (disc	oni	nect	t '1	' (r	or	ma	lly	use	ed f	or	wire	d-a	nd						
												со	onr	nectio	ons	5)																				
Е	RW	SENSE										Piı	n s	sensir	ng i	me	cha	nis	m																	
			Disabled	0								Di	isa	bled																						
			High	2								Se	ens	se for	hi	gh	lev	el																		
			Low	3								Se	ens	se for	lo	w l	eve	I																		

20.3.15 PIN_CNF[5]

Address offset: 0x714



Reset 0x00000002	Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 0 Connect input buffer 0 Connect input buffer C RW PULL Pull configuration Pull configuration D Pullup 3 Pull upon pin D Pullup 3 Pull upon pin D Sosi 0 Standard '0', standard '1' Sobi 0 Standard '0', standard '1' Sobi 2 Standard '0', high drive '0', high drive '1' Hohl 3 High drive '0', high drive '1' B FW DISCONNECT '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0'	Id					E E D D D C C B A
A RW DIR Input 0 Configure pin as an input pin Output 1 Connect or disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configure pin as an output pin Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pull up on pin Disconnect input buffer Sosi 0 Standard '0', standard '1' Hobi 1 1 High drive '0', standard '1' Hohi 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' istandard '1' (normally used for wired-or connections) SoD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High C Sense for high level	Res	et 0 x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect of input buffer Connect 1 Disconnect input buffer Connect 1 Disconnect input buffer Disconnect input buffer Pull configuration Pull on P	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Con	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Disconnect 1 Disconnect input buffer Pull configuration No pull Pull down 0 1 Pull down on pin Pull up on pin Disabled 0 Standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' high drive '1' DOS1 5 Disconnect '0', high drive '1' DOS1 6 Standard '0', disconnect '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Output	1	Configure pin as an output pin
Disconnect 1 Disconnect input buffer Pull configuration Pull down on pin Pullup 3 Pull up on pin Pull up on p	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pull up on pin Pull up on pin Drive configuration Drive configuration Sos1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) F RW SENSE Pinseled 0 Disabled High 0 Disabled High 0 Disabled High 0 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin D RW DRIVE SoS1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE SoS1				Pulldown	1	Pull down on pin
S0S1 0 Standard 'D', standard '1' H0S1 1 High drive 'O', standard '1' S0H1 2 Standard 'O', high drive '1' H0H1 3 High drive 'O', high drive '1' D0S1 4 Disconnect 'O' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect 'O', high drive '1' (normally used for wired-or connections) S0D1 6 Standard 'O'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive 'O', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
Connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
Low 3 Sense for low level				High	2	Sense for high level
				Low	3	Sense for low level

20.3.16 PIN_CNF[6]

Address offset: 0x718 Configuration of GPIO pins

Rit r	numbe	or		31	30	29	28	27	26 2	25 :	24 2	73 2	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8 .	7 1	6 1	5 4	. 3	2	1	0
ld.				-	-										, 15			E	10					D	D	D.				C	C	B	Δ
	et Ox0	0000002		0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	0	0	0	0	0			0 (0 (0 (0 0	0 (0	1	
Id		Field	Value Id	Va	lue							Desc	ript	ion																			
Α	RW	DIR									F	in d	lirec	tior	ո. Sa	ame	e ph	ıysi	cal r	egi	stei	r as	DIF	reو	gist	er							
			Input	0							(Conf	igur	e pi	in a	s ar	ı in	put	pin														
			Output	1							(Conf	igur	e pi	in a	s ar	า อน	ıtpu	t pi	n													
В	RW	INPUT									(Conr	nect	or o	disc	onr	nect	t inp	out l	ouf	fer												
			Connect	0							(Conr	nect	inp	ut k	ouff	er																
			Disconnect	1								Disco	onne	ect i	inpı	ıt b	uffe	er															
С	RW	PULL									F	Pull (conf	igur	rati	on																	
			Disabled	0							١	No p	ull																				
			Pulldown	1							F	Pull (dow	n oı	n pi	n																	
			Pullup	3							F	ull i	ир о	n pi	in																		
D	RW	DRIVE									[Drive	e coi	nfig	ura	tior	1																
			S0S1	0							S	tan	dard	1 '0'	, sta	and	ard	'1'															
			H0S1	1							H	ligh	driv	/e 'C)', s	tan	dar	d '1															
			S0H1	2							S	Stan	dard	1 '0'	, hi	gh c	driv	e '1															
			H0H1	3							H	ligh	driv	'e '0)', h	igh	'dr	ive	'1''														
			DOS1	4							[Disco	onne	ect '	'0' s	tan	dar	d '1	' (n	orn	all	y us	ed	for	wir	ed-c	r						
											C	conn	ecti	ons	()																		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E D D D C C B A
Reset 0x00000002	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

20.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

Bit r	umbe	er		3	1 30	29	28	27	26	25	24	23	3 22 2	1 2	0	19 1	8 1	7 1	6 :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																		E E	Ε						D	D	D					С	С	В	Α
Res	et OxO	0000002		0	0	0	0	0	0	0	0	0	0 (0 (0	0 () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Id	RW	Field	Value Id	٧	alue	•						De	escrip	tio	n																				
Α	RW	DIR										Pin	n dire	ctic	on.	San	ne p	hys	sica	al r	egis	ster	as	DI	R re	egis	ter								
			Input	0								Со	nfigu	re p	oin	as a	ın i	npu	t p	in															
			Output	1								Со	nfigu	re p	pin	as a	ın c	utp	out	pir	1														
В	RW	INPUT										Со	nnec	t or	di	scor	ne	ct ir	าрเ	ut b	uff	er													
			Connect	0								Со	nnec	t in	pu	t bu	ffer																		
			Disconnect	1								Dis	sconr	nect	in	put	but	fer																	
С	RW	PULL										Pu	ıll con	ıfigu	ura	tion																			
			Disabled	0								No	pull																						
			Pulldown	1								Pu	ıll dov	vn (on	pin																			
			Pullup	3								Pu	ıll up	on	pin	1																			
D	RW	DRIVE										Dri	ive co	onfi	gu	ratio	n																		
			S0S1	0								Sta	andar	d 'C)', :	stan	dar	d '1	<u>'</u>																
			H0S1	1								Hig	gh dri	ive	'0',	, sta	nda	ırd '	'1'																
			SOH1	2								Sta	andar	d 'C)',	high	dri	ve '	1'																
			H0H1	3								Hig	gh dri	ive	'0',	, hig	h 'c	lrive	e '1	."															
			DOS1	4								Dis	sconr	nect	: '0	' sta	nda	ard	'1'	(nc	rm	ally	us	sed	foi	wi	ired	-or							
												COI	nnec	tion	ıs)																				
			D0H1	5								Dis	sconr	nect	: '0	', hi	gh (drive	e ':	L' (ı	nor	ma	lly	use	ed f	or	wire	d-o	r						
													nnec																						
			SOD1	6								Sta	andar	d 'C)'.	disc	onr	ect	'1'	(n	orn	nall	y u	se	d fo	r w	ired	l-an	nd						
													nnec		′																				
			H0D1	7								Hig	gh dri	ive	'0',	, dis	con	nec	t ':	1' (1	nor	ma	lly	use	ed f	or	wire	d-a	nd						
												COI	nnec	tion	ıs)																				
E	RW	SENSE											n sens	_	g m	ech	ani	sm																	
			Disabled	0									sable																						
			High	2									nse f		-																				
			Low	3								Sei	nse f	or lo	ow	leve	١																		

20.3.18 PIN_CNF[8]

Address offset: 0x720 Configuration of GPIO pins



Reservion	Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin B RW INPUT Connect Connect or disconnect input buffer C Connect Disconnect Disconnect input buffer C RW PUL Pull configuration C RW Pullup 3 Pull down on pin Pullup 3 Pull up on pin D Pull Pullup 3 Pull up on pin B RW Pull Pullup 3 Pull up on pin B Pull Upon pin Disconnect "O", standard "1" Pull upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B <th>Id</th> <th></th> <th></th> <th></th> <th></th> <th>E E DDD CCBA</th>	Id					E E DDD CCBA
A RW DIR	Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input	Id	RW	Field	Value Id	Value	Description
B RV IPUT Connect Connect or disconnect input buffer Connect or Disconnect input buffer Disconnect inp	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Onnect of disconnect input buffer Connect Onnect Disconnect 1 Connect input buffer Disconnect 1 Disconnect input buffer CC RW PULL Pulloom Disabled ON Pulloom Disabled Pulloom Pulloom Disabled Pulloom Disabled Pulloom Pulloom Disabled Pulloom Disabled Pulloom Pull				Input	0	Configure pin as an input pin
CONNECT NOW PULL				Output	1	Configure pin as an output pin
C RW PULL Pulldown 1 Pull down on pin Pullup Disconnect input buffer Pull down on pin Pullup 3 Pull down on pin Pullup 1 Pullup	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pullup 3 Pull up on pin Drive configuration Pullup Drive Configuration Standard '0', standard '1' HOS1 1 HOS1 2 Standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Sandard '0', disconnect '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive Drive Configuration SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE PID Sense PID Standard 10 Disabled Disabled 0 Disabled High 2 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Standard '0'. disconnect '1' (normally used for wired-and connections) EVALUATE: HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and (1) (normally used	С	RW	PULL			Pull configuration
Pullup 3 Pull up on pin D RW DRIVE 5051 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Sono Standard '0', high drive '1' (normally used for wired-or connections) D0H1 6 Standard '0', high drive '1' (normally used for wired-or connections) E RW SENSE FOR SENSE FOR SENSE FOR Standard '0' Disabled High drive '0', disconnect '1' (normally used for wired-on Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE Drive configuration S051 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Pulldown	1	Pull down on pin
SOS1 0 Standard '1', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled O Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
HOH1 3 High drive '0', high 'drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOH1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HDD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
E RW SENSE Connections) Disabled Disabled Disabled Disabled Disabled Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
				High	2	Sense for high level
Low 3 Sense for low level				Low	3	Sense for low level

20.3.19 PIN_CNF[9]

Address offset: 0x724 Configuration of GPIO pins

Bit r	umbe	er		31	30	29	28	27	26 2	25 2	24 2	23 2	2 21	20	19	18	17	16	15	14	13	12	11 1	10 9	9 8	7	6	5	4	3	2	1 0
Id																	Ε	Ε						D [) [)				С	С	ВА
Res	et 0x0	0000002		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	1 0
Id	RW	Field	Value Id	Va	lue							Desc	ripti	on																		
Α	RW	DIR									F	Pin d	lirec	tion	ı. Sa	me	e ph	nysio	calı	egi	ster	as	DIR	regi	ste	r						
			Input	0							(Conf	igur	e pi	n a	s ar	in	put	pin													
			Output	1							(Conf	igur	e pi	n a	ar	า อน	itpu	t pi	n												
В	RW	INPUT									(Conr	nect	or c	disc	onr	nect	t inp	out	buf	er											
			Connect	0							(Conr	nect	inpı	ut b	uff	er															
			Disconnect	1							[Disco	onne	ct i	npı	ıt b	uffe	er														
С	RW	PULL									F	Pull o	conf	igur	ratio	on																
			Disabled	0							١	No p	ull																			
			Pulldown	1							F	Pull (dow	n or	n pi	n																
			Pullup	3							F	ull ı	ир о	n pi	in																	
D	RW	DRIVE									[Drive	100	nfigu	ura	tior	1															
			S0S1	0							S	Stan	dard	'0',	, sta	nd	ard	'1'														
			H0S1	1							H	ligh	driv	e '0)', si	an	dar	d '1														
			SOH1	2							S	Stan	dard	'0',	, hig	gh c	driv	e '1	'													
			H0H1	3							H	ligh	driv	e '0)', h	igh	'dr	ive	'1''													
			DOS1	4							[Disco	onne	ct '	0' s	tan	dar	d '1	' (n	orm	ally	us!	ed f	or w	ire	d-or						
											C	onn	ecti	ons)																	



Bit number		31 3	30 29	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Е	Ε					D	D	D				C	. c	В	Α
Reset 0x00000002		0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
Id RW Field	Value Id	Valu	ue						Des	scrip	otion	า																	
	D0H1	5							Disc	con	nect	'0'	, hig	h dı	ive	'1' (ı	norn	nally	use	d fo	r w	ired	-or						
									con	nec	tion	ıs)																	
	SOD1	6							Star	nda	rd 'C)'. d	lisco	nne	ct '	L' (n	orm	ally i	used	l for	wii	ed-	and	b					
									con	nec	tion	ıs)																	
	H0D1	7							High	h dr	ive	'0',	disc	onn	ect	'1' (norn	nally	use	d fo	r w	ired	-ar	nd					
									con	nec	tion	ıs)																	
E RW SENSE									Pin	sen	sing	me	echa	nisi	m														
	Disabled	0							Disa	able	ed																		
	High	2							Sen	ise f	or h	igh	lev	el															
	Low	3							Sen	nse f	or lo	ow	leve	el															

20.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

Bit n	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			SOH1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.21 PIN_CNF[11]

Address offset: 0x72C



Bit r	umbe	er		31	30 2	29 2	8 2	7 26	25	24	23	22 2	21 2	0 1	9 18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5 4	1 3	3 2	1	0
Id																Ε	Ε					D	D	D				(С	В	Α
Rese	et OxC	0000002		0	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	1	0
Id	RW	Field	Value Id	Va	lue						De	escrip	tior	n																	
Α	RW	DIR									Pir	n dire	ectic	on. S	Samo	e ph	iysid	al r	egis	ter	as D	IR re	egis	ter							
			Input	0							Со	nfigu	ıre p	oin a	as ar	n inp	out	pin													
			Output	1							Со	nfigu	ıre p	oin a	as ar	n ou	tpu	t pi	n												
В	RW	INPUT									Со	nnec	t or	dis	coni	nect	inp	ut	ouffe	er											
			Connect	0							Со	nnec	t in	put	buff	er															
			Disconnect	1							Dis	sconi	nect	inp	ut b	uffe	er														
С	RW	PULL									Pu	ıll cor	nfigu	urat	ion																
			Disabled	0							No	pull																			
			Pulldown	1							Pu	ıll do	wn (on p	in																
			Pullup	3							Pu	ıll up	on	pin																	
D	RW	DRIVE									Dri	ive c	onfi	gur	atior	1															
			S0S1	0							Sta	anda	rd 'C)', si	tand	ard	'1'														
			H0S1	1							Hig	gh dr	ive	'0',	stan	dar	d '1'														
			S0H1	2							Sta	anda	rd 'C)', h	igh (drive	e '1'														
			H0H1	3							Hig	gh dr	ive	'0',	high	'dri	ive '	1''													
			DOS1	4							Dis	sconi	nect	'0'	stan	dar	d '1	' (n	orma	ally	use	d fo	wi	red-	or						
											co	nnec	tion	ıs)																	
			D0H1	5							Dis	sconi	nect	: '0',	higl	h dr	ive	'1' (norr	nall	y us	ed f	or v	vire	o-b						
											co	nnec	tion	ıs)																	
			SOD1	6							Sta	anda	rd 'C)'. d	isco	nne	ct '1	L' (r	orm	ally	use	d fo	rw	ired	-and	t					
											CO	nnec	tion	ıs)																	
			H0D1	7							Hig	gh dr	ive	'0',	disc	onn	ect	'1' (norr	nall	y us	ed f	or v	vire	d-ar	nd					
											CO	nnec	tion	ıs)																	
E	RW	SENSE									Pir	n sen	sing	g me	cha	nisn	n														
			Disabled	0							Dis	sable	d																		
			High	2							Se	nse f	or h	igh	leve	el															
			Low	3							Se	nse f	or lo	ow l	evel																

20.3.22 PIN_CNF[12]

Address offset: 0x730 Configuration of GPIO pins

umb	er		31	30	29	28 2	27 :	26 2	25 2	24 2	3 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
																Ε	Е					D	D	D				С	С	В	Α
et OxC	00000002		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	1	0
RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
RW	DIR									Р	in d	irec	tion	ı. Sa	me	phy	/sic	al re	gist	er a	s DI	R re	gist	er							
		Input	0							C	onf	igur	e pi	n as	an	inp	ut p	in													
		Output	1							C	onf	igur	e pi	n as	an	out	put	pin													
RW	INPUT									C	onr	ect	or c	lisco	onn	ect	inp	ut b	uffe	r											
		Connect	0							C	onr	ect	inpı	ut b	uffe	er															
		Disconnect	1							D	isco	nne	ct i	npu	t bı	ıffe	r														
RW	PULL									Р	ull	conf	igur	atic	n																
		Disabled	0							Ν	lo p	ull																			
		Pulldown	1							Р	ull	wob	n or	niq r	1																
		Pullup	3							Р	ull ı	nb o	n pi	n																	
RW	DRIVE									D	rive	100	nfigu	urat	ion																
		S0S1	0							S	tan	dard	'0',	sta	nda	ırd '	1'														
		HOS1	1							Н	ligh	driv	e '0	', st	and	lard	'1'														
		S0H1	2							S	tan	dard	'0',	hig	h d	rive	'1'														
		H0H1	3							Н	ligh	driv	e '0	', hi	gh	driv	/e ':	L''													
		D0S1	4							D	isco	nne	ct '	0' st	and	darc	l '1'	(no	rma	lly u	sed	for	wir	ed-d	or						
										С	onn	ecti	ons)																	
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value I	RW Field Value Id Value I	RW Field Value Id Value Id Value Id RW DIR Input	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 DISCONNECT 1 SOH1 1 SOH1 1 SOH1 2 HOH1 3 FROM DRIVE RW DRIVE SORI 1 SOH1 1 SOH1 2 HOH1 3	RW Field Value Id Val	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup 3 RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 DOS1 4 RW INPUT 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value	RW Field Value Id Id Value Id Id Id Id Id Id Id I	RW Field Value Id Value Id Value Id Description Pin direction. Same physical response Pin direction. Pin	RW Field Value Id Value	No	No	No	No	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR register RW DIR Input Output 1	RW Field Value Id Value Id Pind incection. Same physical register as DIR regis	RW Field Value Id Val	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR r	RW Field Value Id Value I					



Bit number		31 3	30 29	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Е	Е					D	D	D				C	. c	В	Α
Reset 0x00000002		0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
Id RW Field	Value Id	Valu	ue						Des	scrip	otion	า																	
	D0H1	5							Disc	con	nect	'0'	, hig	h dı	ive	'1' (ı	norn	nally	use	d fo	r w	ired	-or						
									con	nec	tion	ıs)																	
	SOD1	6							Star	nda	rd 'C)'. d	lisco	nne	ct '	L' (n	orm	ally i	used	l for	wii	ed-	and	b					
									con	nec	tion	ıs)																	
	H0D1	7							High	h dr	ive	'0',	disc	onn	ect	'1' (norn	nally	use	d fo	r w	ired	-ar	nd					
									con	nec	tion	ıs)																	
E RW SENSE									Pin	sen	sing	me	echa	nisi	m														
	Disabled	0							Disa	able	ed																		
	High	2							Sen	ise f	or h	igh	lev	el															
	Low	3							Sen	nse f	or lo	ow	leve	el															

20.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
		00000002			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			SOH1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.24 PIN_CNF[14]

Address offset: 0x738



Reset 0x00000002	Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 0 Connect input buffer 0 Connect input buffer C RW PULL Pull configuration Pull configuration D Pullup 3 Pull upon pin D Pullup 3 Pull upon pin D Sosi 0 Standard '0', standard '1' Sobi 0 Standard '0', standard '1' Sobi 2 Standard '0', high drive '0', high drive '1' Hohl 3 High drive '0', high drive '1' B FW DISCONNECT '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0'	Id					E E D D D C C B A
A RW DIR Input 0 Configure pin as an input pin Output 1 Connect or disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configure pin as an output pin Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pull up on pin Disconnect input buffer Sosi 0 Standard '0', standard '1' Hobi 1 1 High drive '0', standard '1' Hohi 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' istandard '1' (normally used for wired-or connections) SoD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High C Sense for high level	Res	et 0 x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect of input buffer Connect 1 Disconnect input buffer Connect 1 Disconnect input buffer Disconnect input buffer Pull configuration Pull on P	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Con	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Disconnect 1 Disconnect input buffer Pull configuration No pull Pull down 0 1 Pull down on pin Pull up on pin Disabled 0 Standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' high drive '1' DOS1 5 Disconnect '0', high drive '1' DOS1 6 Standard '0', disconnect '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Output	1	Configure pin as an output pin
Disconnect 1 Disconnect input buffer Pull configuration Pull down on pin Pullup 3 Pull up on pin Pull up on p	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pull up on pin Pull up on pin Drive configuration Drive configuration Sos1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) F RW SENSE Pinseled 0 Disabled High 0 Disabled High 0 Disabled High 0 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin D RW DRIVE SoS1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE SoS1				Pulldown	1	Pull down on pin
S0S1 0 Standard 'D', standard '1' H0S1 1 High drive 'O', standard '1' S0H1 2 Standard 'O', high drive '1' H0H1 3 High drive 'O', high drive '1' D0S1 4 Disconnect 'O' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect 'O', high drive '1' (normally used for wired-or connections) S0D1 6 Standard 'O'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive 'O', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
Connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
Low 3 Sense for low level				High	2	Sense for high level
				Low	3	Sense for low level

20.3.25 PIN_CNF[15]

Address offset: 0x73C Configuration of GPIO pins

umb	er		31	30	29	28 2	27 :	26 2	25 2	24 2	3 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
																Ε	Е					D	D	D				С	С	В	Α
et OxC	00000002		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	1	0
RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
RW	DIR									Р	in d	irec	tion	ı. Sa	me	phy	/sic	al re	gist	er a	s DI	R re	gist	er							
		Input	0							C	onf	igur	e pi	n as	an	inp	ut p	in													
		Output	1							C	onf	igur	e pi	n as	an	out	put	pin													
RW	INPUT									C	onr	ect	or c	lisco	onn	ect	inp	ut b	uffe	r											
		Connect	0							C	onr	ect	inpı	ut b	uffe	er															
		Disconnect	1							D	isco	nne	ct i	npu	t bı	ıffe	r														
RW	PULL									Р	ull	conf	igur	atic	n																
		Disabled	0							Ν	lo p	ull																			
		Pulldown	1							Р	ull	wob	n or	niq r	ı																
		Pullup	3							Р	ull ı	nb o	n pi	n																	
RW	DRIVE									D	rive	100	nfigu	urat	ion																
		S0S1	0							S	tan	dard	'0',	sta	nda	rd '	1'														
		HOS1	1							Н	ligh	driv	e '0	', st	and	lard	'1'														
		S0H1	2							S	tan	dard	'0',	hig	h d	rive	'1'														
		H0H1	3							Н	ligh	driv	e '0	', hi	gh	driv	/e ':	L''													
		D0S1	4							D	isco	nne	ct '	0' st	and	darc	l '1'	(no	rma	lly u	sed	for	wir	ed-d	or						
										С	onn	ecti	ons)																	
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value I	RW Field Value Id Value I	RW Field Value Id Value Id Value Id RW DIR Input	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 DISCONNECT 1 SOH1 1 SOH1 1 SOH1 2 HOH1 3 FROM DRIVE RW DRIVE SORI 1 SOH1 1 SOH1 2 HOH1 3	RW Field Value Id Val	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup 3 RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 DOS1 4 RW INPUT 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value	RW Field Value Id Id Value Id Id Id Id Id Id Id I	RW Field Value Id Value Id Value Id Description Pin direction. Same physical response Pin direction. Pin	RW Field Value Id Value	No	No	No	No	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR register RW DIR Input Output 1	RW Field Value Id Value Id Pind incection. Same physical register as DIR regis	RW Field Value Id Val	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR r	RW Field Value Id Value I					



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E D D D C C B A
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

Bit num	ber			31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	3 12	2 1	1 1	0 9	9 8	7	6	5	4	3	2	1	0
Id																		Ε	Ε						[) [) [)				С	С	В	A
Reset 0	x00	000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	() (0	0	0	0	0	0	0	0	1	0
ld RV	W	Field	Value Id	Va	lue							De	scr	ipti	on																				
A RV	N	DIR										Pin	n di	rect	ion	ı. Sa	me	e pl	nysi	cal	reg	ist	er a	ıs D)IR ı	egi	ste	r							
			Input	0								Со	nfi	gure	e pi	n as	s ar	n in	put	pir	1														
			Output	1								Со	nfi	gure	e pi	n as	s ar	ι οι	ıtpı	ıt p	in														
B RV	N	INPUT										Со	nne	ect (or c	disc	onr	nec	t in	put	bu	ffe	r												
			Connect	0								Со	nne	ect i	np	ut b	uff	er																	
			Disconnect	1								Dis	sco	nne	ct i	npı	ıt b	uff	er																
C RV	N	PULL										Pu	II c	onfi	gur	ratio	on																		
			Disabled	0								No	pu	III																					
			Pulldown	1								Pu	ll d	owr	no r	n pi	n																		
			Pullup	3								Pu	ll u	no q	n pi	in																			
D RV	W	DRIVE										Dri	ive	con	fig	ura	tior	า																	
			S0S1	0								Sta	and	ard	'0',	, sta	nd	ard	'1'																
			H0S1	1								Hig	gh d	driv	e '0)', s1	an	dar	d '1	.'															
			SOH1	2								Sta	and	ard	'0',	, hig	gh c	driv	e '1	.'															
			H0H1	3								Hig	gh d	driv	e '0)', h	igh	'dr	ive	'1''															
			DOS1	4								Dis	sco	nne	ct '	0' s	tan	daı	'd '1	L' (r	nori	ma	lly ι	ıse	d fo	r w	ire	d-or							
												COI	nne	ectio	ons)																			
			D0H1	5								Dis	sco	nne	ct '	0', I	nigl	h dı	ive	'1'	(nc	rm	ally	/ us	sed	for	wir	ed-	or						
												COI	nne	ectio	ons)																			
			SOD1	6								Sta	and	ard	'0'	. dis	co	nne	ct '	1' (nor	ma	lly	use	ed f	or v	vire	d-a	nd						
												COI	nne	ectio	ons)																			
			H0D1	7								Hig	gh d	driv	e '0)', d	isco	onn	ect	'1'	(nc	rm	ally	/ us	sed	for	wir	ed-a	and						
												COI	nne	ectio	ons)																			
E RV	W S	SENSE										Pin	ı se	nsir	ng r	med	ha	nisı	n																
			Disabled	0								Dis	sab	led																					
			High	2								Sei	nse	for	hig	gh l	eve	ŀ																	
			Low	3								Sei	nse	for	lov	w le	vel																		

20.3.27 PIN_CNF[17]

Address offset: 0x744



Bit r	umbe	er		31	30 2	29 2	8 2	7 26	25	24	23	22 2	21 2	0 1	9 18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5 4	1 3	3 2	1	0
Id																Ε	Ε					D	D	D				(С	В	Α
Rese	et OxC	0000002		0	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	1	0
Id	RW	Field	Value Id	Va	lue						De	escrip	tior	n																	
Α	RW	DIR									Pir	n dire	ectic	on. S	Samo	e ph	iysid	al r	egis	ter	as D	IR re	egis	ter							
			Input	0							Со	nfigu	ıre p	oin a	as ar	n inp	out	pin													
			Output	1							Со	nfigu	ıre p	oin a	as ar	n ou	tpu	t pi	n												
В	RW	INPUT									Со	nnec	t or	dis	coni	nect	inp	ut	ouffe	er											
			Connect	0							Со	nnec	t in	put	buff	er															
			Disconnect	1							Dis	sconi	nect	inp	ut b	uffe	er														
С	RW	PULL									Pu	ıll cor	nfigu	urat	ion																
			Disabled	0							No	pull																			
			Pulldown	1							Pu	ıll do	wn (on p	in																
			Pullup	3							Pu	ıll up	on	pin																	
D	RW	DRIVE									Dri	ive c	onfi	gur	atior	1															
			S0S1	0							Sta	anda	rd 'C)', si	tand	ard	'1'														
			H0S1	1							Hig	gh dr	ive	'0',	stan	dar	d '1'														
			S0H1	2							Sta	anda	rd 'C)', h	igh (drive	e '1'														
			H0H1	3							Hig	gh dr	ive	'0',	high	'dri	ive '	1''													
			DOS1	4							Dis	sconi	nect	'0'	stan	dar	d '1	' (n	orma	ally	use	d fo	wi	red-	or						
											co	nnec	tion	ıs)																	
			D0H1	5							Dis	sconi	nect	: '0',	higl	h dr	ive	'1' (norr	nall	y us	ed f	or v	vire	o-b						
											co	nnec	tion	ıs)																	
			SOD1	6							Sta	anda	rd 'C)'. d	isco	nne	ct '1	L' (r	orm	ally	use	d fo	rw	ired	-and	t					
											CO	nnec	tion	ıs)																	
			H0D1	7							Hig	gh dr	ive	'0',	disc	onn	ect	'1' (norr	nall	y us	ed f	or v	vire	d-ar	nd					
											CO	nnec	tion	ıs)																	
E	RW	SENSE									Pir	n sen	sing	g me	cha	nisn	n														
			Disabled	0							Dis	sable	d																		
			High	2							Se	nse f	or h	igh	leve	el															
			Low	3							Se	nse f	or lo	ow l	evel																

20.3.28 PIN_CNF[18]

Address offset: 0x748 Configuration of GPIO pins

		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
		E E DDD CCB/
x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V Field	Value Id	Value Description
V DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
V INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
V PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
V DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	SOH1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1''
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
V PULL	Connect Disconnect Disabled Pulldown Pullup SOS1 HOS1 SOH1 HOH1	Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin Drive configuration Standard '0', standard '1' High drive '0', standard '1' Standard '0', high drive '1' High drive '0', high 'drive '1'' Disconnect '0' standard '1' (normally used for wired-or



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E DDD C C B A
Reset 0x00000002	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

20.3.29 PIN_CNF[19]

Address offset: 0x74C Configuration of GPIO pins

Bit n	umbe	er		31 3	30 2	9 28	27	26 2	25 2	4 23	3 22	21	20	19 3	18 :	17	16	15 1	L4 1	3 1	2 1	1 10	9	8	7	6	5 .	4 3	2	1	0
Id																E	E					D	D	D				C	С	В	Α
Rese	et 0x0	0000002		0	0 (0 0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Valu	ıe					De	escr	iptio	n																		
Α	RW	DIR								Pir	n di	recti	on.	. Sar	ne	phy	sic	al re	gis	ter a	is D	IR r	egis	ter							
			Input	0						Co	onfi	gure	pir	n as	an i	inpı	ut p	in													
			Output	1						Co	onfi	gure	pir	n as	an (out	put	pin													
В	RW	INPUT								Co	onne	ect o	r d	isco	nne	ect i	inp	ut b	uffe	er											
			Connect	0						Co	onne	ect ir	npu	ıt bu	ffe	r															
			Disconnect	1						Dis	sco	nnec	t ir	nput	bu	ffer	-														
С	RW	PULL								Pu	ıll c	onfig	gura	atior	1																
			Disabled	0						No	o pu	III																			
			Pulldown	1						Pu	ıll d	own	on	pin																	
			Pullup	3						Pu	ıll u	p on	pir	n																	
D	RW	DRIVE								Dr	rive	conf	igu	ırati	on																
			S0S1	0						Sta	and	ard '	0',	star	ıda	rd '	1'														
			H0S1	1						Hi	gh (drive	'0'	, sta	nd	ard	'1'														
			SOH1	2						Sta	and	ard '	0',	high	dr	ive	'1'														
			H0H1	3						Hig	gh (drive	'0'	, hig	h 'd	driv	e '1	L''													
			DOS1	4						Dis	sco	nnec	t 'C)' sta	nd	ard	'1'	(no	rma	ally	use	d fo	r wi	ired	or						
										со	nne	ctio	ns)																		
			D0H1	5						Dis	sco	nnec	t '0)', hi	gh	driv	/e '	1' (r	orr	nally	y us	ed f	or	wire	d-o	r					
										со	nne	ctio	ns)																		
			SOD1	6						Sta	and	ard '	0'.	disc	oni	nec	t '1	' (no	orm	ally	use	ed fo	r w	irec	-an	d					
										со	nne	ctio	ns)																		
			H0D1	7						Hi	gh (drive	'0'	, dis	cor	nne	ct '	1' (r	orr	nall	y us	ed f	or v	wire	d-aı	nd					
										со	nne	ctio	ns)																		
E	RW	SENSE								Pir	n se	nsin	g n	nech	ani	ism															
			Disabled	0						Dis	sab	led																			
			High	2						Se	nse	for	hig	h le	/el																
			Low	3						Se	nse	for	lοw	lev lev	el																

20.3.30 PIN_CNF[20]

Address offset: 0x750 Configuration of GPIO pins



Reservion	Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin B RW INPUT Connect Connect or disconnect input buffer C Connect Disconnect Disconnect input buffer C RW PUL Pull configuration C RW Pullup 3 Pull down on pin Pullup 3 Pull up on pin D Pull Pullup 3 Pull up on pin B RW Pull Pullup 3 Pull up on pin B Pull Upon pin Disconnect "O", standard "1" Pull upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B Pull Upon pin Pull Upon pin Pull Upon pin B <th>Id</th> <th></th> <th></th> <th></th> <th></th> <th>E E DDD CCBA</th>	Id					E E DDD CCBA
A RW DIR	Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input	Id	RW	Field	Value Id	Value	Description
B RV IPUT Connect Connect or disconnect input buffer Connect or Disconnect input buffer Disconnect inp	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Onnect of disconnect input buffer Connect Onnect Disconnect 1 Connect input buffer Disconnect 1 Disconnect input buffer CC RW PULL Pulloom Disabled ON Pulloom Disabled Pulloom Pulloom Disabled Pulloom Disabled Pulloom Pulloom Disabled Pulloom Disabled Pulloom Pull				Input	0	Configure pin as an input pin
CONNECT NOW PULL				Output	1	Configure pin as an output pin
C RW PULL Pulldown 1 Pull down on pin Pullup Disconnect input buffer Pull down on pin Pullup 3 Pull down on pin Pullup 1 Pullup	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pullup 3 Pull up on pin Drive configuration Pullup Drive Configuration Standard '0', standard '1' HOS1 1 HOS1 2 Standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Sandard '0', disconnect '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive Drive Configuration SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE PID Sense PID Standard 10 Disabled Disabled 0 Disabled High 2 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Standard '0'. disconnect '1' (normally used for wired-and connections) EVALUATE: HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and connections) EVALUATE: Province Total Experiment (1) (normally used for wired-and (1) (normally used	С	RW	PULL			Pull configuration
Pullup 3 Pull up on pin D RW DRIVE 5051 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Sono Standard '0', high drive '1' (normally used for wired-or connections) D0H1 6 Standard '0', high drive '1' (normally used for wired-or connections) E RW SENSE FOR SENSE FOR SENSE FOR Standard '0' Disabled High drive '0', disconnect '1' (normally used for wired-on Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE Drive configuration S051 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Pulldown	1	Pull down on pin
SOS1 0 Standard '1', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled O Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
HOH1 3 High drive '0', high 'drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOH1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HDD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
E RW SENSE Connections) Disabled Disabled Disabled Disabled Disabled Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
				High	2	Sense for high level
Low 3 Sense for low level				Low	3	Sense for low level

20.3.31 PIN_CNF[21]

Address offset: 0x754 Configuration of GPIO pins

		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
		E E DDD CCB/
x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V Field	Value Id	Value Description
V DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
V INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
V PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
V DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	SOH1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1''
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
V PULL	Connect Disconnect Disabled Pulldown Pullup SOS1 HOS1 SOH1 HOH1	Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin Drive configuration Standard '0', standard '1' High drive '0', standard '1' Standard '0', high drive '1' High drive '0', high 'drive '1'' Disconnect '0' standard '1' (normally used for wired-or



Bit number		31 3	30 29	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Е	Е					D	D	D				C	. c	В	Α
Reset 0x00000002		0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
Id RW Field	Value Id	Valu	ue						Des	scrip	otion	า																	
	D0H1	5							Disc	con	nect	'0'	, hig	h dı	ive	'1' (ı	norn	nally	use	d fo	r w	ired	-or						
									con	nec	tion	ıs)																	
	SOD1	6							Star	nda	rd 'C)'. d	lisco	nne	ct '	L' (n	orm	ally i	used	l for	wii	ed-	and	b					
									con	nec	tion	ıs)																	
	H0D1	7							High	h dr	ive	'0',	disc	onn	ect	'1' (norn	nally	use	d fo	r w	ired	-ar	nd					
									con	nec	tion	ıs)																	
E RW SENSE									Pin	sen	sing	me	echa	nisi	m														
	Disabled	0							Disa	able	ed																		
	High	2							Sen	ise f	or h	igh	lev	el															
	Low	3							Sen	nse f	or lo	ow	leve	el															

20.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

Bit nu	umbe	er		31 30 29 28	27 26 2	25 24	23 2	22 21 2	20 1	19 18	3 17	16	15 1	4 1	3 12	11	10 9	8	7	6	5 4	1 3	2	1
Id											Ε	Ε					D [D				С	С	В
Rese	t 0x0	0000002		0 0 0 0	0 0	0 0	0 (0 0	0	0 0	0	0	0 (0 0	0	0	0 0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Value			Desc	criptio	n															
Α	RW	DIR					Pin c	directi	on.	Sam	e ph	ysic	al re	gist	er as	DIR	regi	ster						
			Input	0			Conf	figure	pin	as a	n inp	out	pin											
			Output	1			Conf	figure	pin	as a	n ou	tpu	t pin											
В	RW	INPUT					Coni	nect o	r di	scon	nect	inp	ut b	uffe	r									
			Connect	0			Coni	nect in	nput	t buf	fer													
			Disconnect	1			Disc	onnec	t in	put b	ouffe	er												
С	RW	PULL					Pull	config	gura	tion														
			Disabled	0			No p	oull																
			Pulldown	1			Pull	down	on	pin														
			Pullup	3			Pull	up on	pin															
D	RW	DRIVE					Drive	e conf	igu	ratio	n													
			S0S1	0			Stan	dard '	0', s	stand	lard	'1'												
			H0S1	1			High	drive	'0',	stan	dar	d '1'												
			S0H1	2			Stan	dard '	'0', l	high	drive	e '1'												
			H0H1	3			High	drive	'0',	high	dri'	ve '	1''											
			DOS1	4			Disc	onnec	t '0	' star	ndar	d '1	' (no	rma	lly us	ed t	for w	/ired	-or					
							conr	nectio	ns)															
			D0H1	5			Disc	onnec	t '0	', hig	h dr	ive '	'1' (n	orm	ally	use	d for	wire	d-o	r				
							conr	nectio	ns)															
			SOD1	6			Stan	dard '	'0'. d	disco	nne	ct '1	L' (no	rma	ally u	sed	for v	vired	l-an	d				
							conr	nectio	ns)															
			H0D1	7			High	drive	'0',	disc	onne	ect '	'1' (n	orm	ally	use	d for	wire	d-a	nd				
							conr	nectio	ns)															
E	RW	SENSE					Pin s	sensin	g m	echa	nisn	n												
			Disabled	0			Disa	bled																
			High	2			Sens	se for I	high	ı leve	el													
			Low	3			Sens	se for I	low	leve	I													

20.3.33 PIN_CNF[23]

Address offset: 0x75C Configuration of GPIO pins



Reset 0x00000002	Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 0 Connect input buffer 0 Connect input buffer C RW PULL Pull configuration Pull configuration D Pullup 3 Pull upon pin D Pullup 3 Pull upon pin D Sosi 0 Standard '0', standard '1' Sobi 0 Standard '0', standard '1' Sobi 2 Standard '0', high drive '0', high drive '1' Hohl 3 High drive '0', high drive '1' B FW DISCONNECT '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0'	Id					E E D D D C C B A
A RW DIR Input 0 Configure pin as an input pin Output 1 Connect or disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configure pin as an output pin Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pull up on pin Disconnect input buffer Sosi 0 Standard '0', standard '1' Hobi 1 1 High drive '0', standard '1' Hohi 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' istandard '1' (normally used for wired-or connections) SoD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High C Sense for high level	Res	et 0 x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect of input buffer Connect 1 Disconnect input buffer Connect 1 Disconnect input buffer Disconnect input buffer Pull configuration Pull on P	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Con	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Disconnect 1 Disconnect input buffer Pull configuration No pull Pull down 0 1 Pull down on pin Pull up on pin Disabled 0 Standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' high drive '1' DOS1 5 Disconnect '0', high drive '1' DOS1 6 Standard '0', disconnect '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Output	1	Configure pin as an output pin
Disconnect 1 Disconnect input buffer Pull configuration Pull down on pin Pullup 3 Pull up on pin Pull up on p	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pull up on pin Pull up on pin Drive configuration Drive configuration Sos1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) F RW SENSE Pinseled 0 Disabled High 0 Disabled High 0 Disabled High 0 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin D RW DRIVE SoS1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE SoS1				Pulldown	1	Pull down on pin
S0S1 0 Standard 'D', standard '1' H0S1 1 High drive 'O', standard '1' S0H1 2 Standard 'O', high drive '1' H0H1 3 High drive 'O', high drive '1' D0S1 4 Disconnect 'O' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect 'O', high drive '1' (normally used for wired-or connections) S0D1 6 Standard 'O'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive 'O', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
Connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
Low 3 Sense for low level				High	2	Sense for high level
				Low	3	Sense for low level

20.3.34 PIN_CNF[24]

Address offset: 0x760 Configuration of GPIO pins

		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
		E E DDD CCB/
x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V Field	Value Id	Value Description
V DIR		Pin direction. Same physical register as DIR register
	Input	0 Configure pin as an input pin
	Output	1 Configure pin as an output pin
V INPUT		Connect or disconnect input buffer
	Connect	0 Connect input buffer
	Disconnect	1 Disconnect input buffer
V PULL		Pull configuration
	Disabled	0 No pull
	Pulldown	1 Pull down on pin
	Pullup	3 Pull up on pin
V DRIVE		Drive configuration
	S0S1	0 Standard '0', standard '1'
	H0S1	1 High drive '0', standard '1'
	SOH1	2 Standard '0', high drive '1'
	H0H1	3 High drive '0', high 'drive '1''
	DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
		connections)
V PULL	Connect Disconnect Disabled Pulldown Pullup SOS1 HOS1 SOH1 HOH1	Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin Drive configuration Standard '0', standard '1' High drive '0', standard '1' Standard '0', high drive '1' High drive '0', high 'drive '1'' Disconnect '0' standard '1' (normally used for wired-or



Bit number		31 30 29 28 27 26 25 24	⁴ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E DDD CCBA
Reset 0x00000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
			connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
			connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
			connections)
E RW SENSE			Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

Bit n	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			SOH1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.36 PIN_CNF[26]

Address offset: 0x768



Reset 0x00000002	Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 0 Connect input buffer 0 Connect input buffer C RW PULL Pull configuration Pull configuration D Pullup 3 Pull upon pin D Pullup 3 Pull upon pin D Sosi 0 Standard '0', standard '1' Sobi 0 Standard '0', standard '1' Sobi 2 Standard '0', high drive '0', high drive '1' Hohl 3 High drive '0', high drive '1' B FW DISCONNECT '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0'	Id					E E D D D C C B A
A RW DIR Input 0 Configure pin as an input pin Output 1 Connect or disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configure pin as an output pin Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pull up on pin Disconnect input buffer Sosi 0 Standard '0', standard '1' Hobi 1 1 High drive '0', standard '1' Hohi 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' istandard '1' (normally used for wired-or connections) SoD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High C Sense for high level	Res	et 0 x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect of input buffer Connect 1 Disconnect input buffer Connect 1 Disconnect input buffer Disconnect input buffer Pull configuration Pull on P	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Con	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Disconnect 1 Disconnect input buffer Pull configuration No pull Pull down 0 1 Pull down on pin Pull up on pin Disabled 0 Standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' high drive '1' DOS1 5 Disconnect '0', high drive '1' DOS1 6 Standard '0', disconnect '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Output	1	Configure pin as an output pin
Disconnect 1 Disconnect input buffer Pull configuration Pull down on pin Pullup 3 Pull up on pin Pull up on p	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pull up on pin Pull up on pin Drive configuration Drive configuration Sos1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) F RW SENSE Pinseled 0 Disabled High 0 Disabled High 0 Disabled High 0 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin D RW DRIVE SoS1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE SoS1				Pulldown	1	Pull down on pin
S0S1 0 Standard 'D', standard '1' H0S1 1 High drive 'O', standard '1' S0H1 2 Standard 'O', high drive '1' H0H1 3 High drive 'O', high drive '1' D0S1 4 Disconnect 'O' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect 'O', high drive '1' (normally used for wired-or connections) S0D1 6 Standard 'O'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive 'O', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
Connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
Low 3 Sense for low level				High	2	Sense for high level
				Low	3	Sense for low level

20.3.37 PIN_CNF[27]

Address offset: 0x76C Configuration of GPIO pins

umb	er		31	30	29	28 2	27 :	26 2	25 2	24 2	3 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
																Ε	Е					D	D	D				С	С	В	Α
et OxC	00000002		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	1	0
RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
RW	DIR									Р	in d	irec	tion	ı. Sa	me	phy	/sic	al re	gist	er a	s DI	R re	gist	er							
		Input	0							C	onf	igur	e pi	n as	an	inp	ut p	in													
		Output	1							C	onf	igur	e pi	n as	an	out	put	pin													
RW	INPUT									C	onr	ect	or c	lisco	onn	ect	inp	ut b	uffe	r											
		Connect	0							C	onr	ect	inpı	ut b	uffe	er															
		Disconnect	1							D	isco	nne	ct i	npu	t bı	ıffe	r														
RW	PULL									Р	ull	conf	igur	atic	n																
		Disabled	0							Ν	lo p	ull																			
		Pulldown	1							Р	ull	wob	n or	niq r	1																
		Pullup	3							Р	ull ı	nb o	n pi	n																	
RW	DRIVE									D	rive	100	nfigu	urat	ion																
		S0S1	0							S	tan	dard	'0',	sta	nda	rd '	1'														
		HOS1	1							Н	ligh	driv	e '0	', st	and	lard	'1'														
		S0H1	2							S	tan	dard	'0',	hig	h d	rive	'1'														
		H0H1	3							Н	ligh	driv	e '0	', hi	gh	driv	/e ':	L''													
		D0S1	4							D	isco	nne	ct '	0' st	and	darc	l '1'	(no	rma	lly u	sed	for	wir	ed-d	or						
										С	onn	ecti	ons)																	
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value I	RW Field Value Id Value I	RW Field Value Id Value Id Value Id RW DIR Input	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 DISCONNECT 1 SOH1 1 SOH1 1 SOH1 2 HOH1 3 FROM DRIVE RW DRIVE SORI 1 SOH1 1 SOH1 2 HOH1 3	RW Field Value Id Val	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup 3 RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 DOS1 4 RW INPUT 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value	RW Field Value Id Id Value Id Id Value Id Id Id Id Id Id Id I	RW Field Value Id Value Id Value Id Description Pin direction. Same physical response Pin direction. Pin	RW Field Value Id Value	No	No	No	No	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR register RW DIR Input Output 1	RW Field Value Id Value Id Pind incection. Same physical register as DIR regis	RW Field Value Id Val	RW Field Value Id Value I	RW Field Value Id Value I					



Bit number		31 3	30 29	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Е	Е					D	D	D				C	. c	В	Α
Reset 0x00000002		0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
Id RW Field	Value Id	Valu	ue						Des	scrip	otion	า																	
	D0H1	5							Disc	con	nect	'0'	, hig	h dı	ive	'1' (ı	norn	nally	use	d fo	r w	ired	-or						
									con	nec	tion	ıs)																	
	SOD1	6							Star	nda	rd 'C)'. d	lisco	nne	ct '	L' (n	orm	ally i	used	l for	wii	ed-	and	b					
									con	nec	tion	ıs)																	
	H0D1	7							High	h dr	ive	'0',	disc	onn	ect	'1' (norn	nally	use	d fo	r w	ired	-ar	nd					
									con	nec	tion	ıs)																	
E RW SENSE									Pin	sen	sing	me	echa	nisı	m														
	Disabled	0							Disa	able	ed																		
	High	2							Sen	ise f	or h	igh	lev	el															
	Low	3							Sen	nse f	or lo	ow	leve	el															

20.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

Bit n	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			SOH1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.39 PIN_CNF[29]

Address offset: 0x774



Reset 0x00000002	Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 0 Connect input buffer 0 Connect input buffer C RW PULL Pull configuration Pull configuration D Pullup 3 Pull upon pin D Pullup 3 Pull upon pin D Sosi 0 Standard '0', standard '1' Sobi 0 Standard '0', standard '1' Sobi 2 Standard '0', high drive '0', high drive '1' Hohl 3 High drive '0', high drive '1' B FW DISCONNECT '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0', high drive '1' B FW Sobi Standard '0'	Id					E E D D D C C B A
A RW DIR Input 0 Configure pin as an input pin Output 1 Connect or disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configure pin as an output pin Connect or disconnect input buffer Connect input buffer Disconnect input buffer Pull configuration No pull Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pull up on pin Disconnect input buffer Sosi 0 Standard '0', standard '1' Hobi 1 1 High drive '0', standard '1' Hohi 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' istandard '1' (normally used for wired-or connections) SoD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High C Sense for high level	Res	et 0 x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect of input buffer Connect 1 Disconnect input buffer Connect 1 Disconnect input buffer Disconnect input buffer Pull configuration Pull on P	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Con	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Disconnect 1 Disconnect input buffer Pull configuration No pull Pull down 0 1 Pull down on pin Pull up on pin Disabled 0 Standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' high drive '1' DOS1 5 Disconnect '0', high drive '1' DOS1 6 Standard '0', disconnect '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Output	1	Configure pin as an output pin
Disconnect 1 Disconnect input buffer Pull configuration Pull down on pin Pullup 3 Pull up on pin Pull up on p	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pull up on pin Pull up on pin Drive configuration Drive configuration Sos1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) F RW SENSE Pinseled 0 Disabled High 0 Disabled High 0 Disabled High 0 Sense for high level				Disconnect	1	Disconnect input buffer
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled High 2 Sense for high level	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin D RW DRIVE SoS1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				Disabled	0	No pull
D RW DRIVE SoS1				Pulldown	1	Pull down on pin
S0S1 0 Standard 'D', standard '1' H0S1 1 High drive 'O', standard '1' S0H1 2 Standard 'O', high drive '1' H0H1 3 High drive 'O', high drive '1' D0S1 4 Disconnect 'O' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect 'O', high drive '1' (normally used for wired-or connections) S0D1 6 Standard 'O'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive 'O', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				S0S1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
Connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level						connections)
High 2 Sense for high level	Е	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
Low 3 Sense for low level				High	2	Sense for high level
				Low	3	Sense for low level

20.3.40 PIN_CNF[30]

Address offset: 0x778 Configuration of GPIO pins

umb	er		31	30	29	28 2	27 :	26 2	25 2	24 2	3 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
																Ε	Е					D	D	D				С	С	В	Α
et OxC	00000002		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	1	0
RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
RW	DIR									Р	in d	irec	tion	ı. Sa	me	phy	/sic	al re	gist	er a	s DI	R re	gist	er							
		Input	0							C	onf	igur	e pi	n as	an	inp	ut p	in													
		Output	1							C	onf	igur	e pi	n as	an	out	put	pin													
RW	INPUT									C	onr	ect	or c	lisco	onn	ect	inp	ut b	uffe	r											
		Connect	0							C	onr	ect	inpı	ut b	uffe	er															
		Disconnect	1							D	isco	nne	ct i	npu	t bı	ıffe	r														
RW	PULL									Р	ull	conf	igur	atic	n																
		Disabled	0							N	lo p	ull																			
		Pulldown	1							Р	ull	wob	n or	niq r	ı																
		Pullup	3							Р	ull ı	nb o	n pi	n																	
RW	DRIVE									D	rive	100	nfigu	urat	ion																
		S0S1	0							S	tan	dard	'0',	sta	nda	rd '	1'														
		HOS1	1							Н	ligh	driv	e '0	', st	and	lard	'1'														
		S0H1	2							S	tan	dard	'0',	hig	h d	rive	'1'														
		H0H1	3							Н	ligh	driv	e '0	', hi	gh	driv	/e ':	L''													
		D0S1	4							D	isco	nne	ct '	0' st	and	darc	l '1'	(no	rma	lly u	sed	for	wir	ed-d	or						
										С	onn	ecti	ons)																	
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value I	RW Field Value Id Value I	RW Field Value Id Value Id Value Id RW DIR Input	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 DISCONNECT 1 SOH1 1 SOH1 1 SOH1 2 HOH1 3 FROM DRIVE RW DRIVE SORI 1 SOH1 1 SOH1 2 HOH1 3	RW Field Value Id Val	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup 3 RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 DOS1 4 RW INPUT 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value	RW Field Value Id Id Value Id Id Value Id Id Id Id Id Id Id I	RW Field Value Id Value Id Value Id Description Pin direction. Same physical response Pin direction. Pin	RW Field Value Id Value	No	No	No	No	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value Id Value Id Pin direction. Same physical register as DIR register RW DIR Input Output 1	RW Field Value Id Value Id Pind incection. Same physical register as DIR regis	RW Field Value Id Val	RW Field Value Id Value I	RW Field Value Id Value I					



Bit number		31 3	30 29	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	16	15	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Е	Ε					D	D	D				C	. c	В	Α
Reset 0x00000002		0	0 0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
Id RW Field	Value Id	Valu	ue						Des	scrip	otion	า																	
	D0H1	5							Disc	con	nect	'0'	, hig	h dı	ive	'1' (ı	norn	nally	use	d fo	r w	ired	-or						
									con	nec	tion	ıs)																	
	SOD1	6							Star	nda	rd 'C)'. d	lisco	nne	ct '	L' (n	orm	ally i	used	l for	wii	ed-	and	b					
									con	nec	tion	ıs)																	
	H0D1	7							High	h dr	ive	'0',	disc	onn	ect	'1' (norn	nally	use	d fo	r w	ired	-ar	nd					
									con	nec	tion	ıs)																	
E RW SENSE									Pin	sen	sing	me	echa	nisı	m														
	Disabled	0							Disa	able	ed																		
	High	2							Sen	ise f	or h	igh	lev	el															
	Low	3							Sen	nse f	or lo	ow	leve	el															

20.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

3it n	umbe	er		31 30 29 28 27	26 25	24 23	22 21 2	20 1	9 18	3 17	16	15 1	14 1	L3 1	2 1	1 10	9	8	7	6	5	4 3	2	1	C
d										Ε	Е					D	D	D				C	С	В	A
Rese	t 0x0	0000002		0 0 0 0 0	0 0	0 0	0 0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	1	(
d	RW	Field	Value Id	Value		De	scriptio	n																	
4	RW	DIR				Pir	n directi	on.	Sam	e ph	iysid	al re	egis	ter a	is D	IR re	egis	ter							
			Input	0		Co	nfigure	pin	as a	n inp	out	pin													
			Output	1		Co	nfigure	pin	as a	n ou	tpu	t pin	1												
3	RW	INPUT				Co	nnect o	r dis	con	nect	inp	ut b	uffe	er											
			Connect	0		Co	nnect in	put	buf	fer															
			Disconnect	1		Di	sconnec	t inp	out k	ouffe	er														
2	RW	PULL				Pu	II config	urat	ion																
			Disabled	0		No	pull																		
			Pulldown	1		Pu	ll down	on p	oin																
			Pullup	3		Pu	ll up on	pin																	
)	RW	DRIVE				Dr	ive conf	igur	atio	n															
			S0S1	0		Sta	andard '	0', s	tano	dard	'1'														
			H0S1	1		Hi	gh drive	'0',	star	dar	d '1'	'													
			S0H1	2		Sta	andard '	0', h	igh	driv	e '1'														
			H0H1	3		Hi	gh drive	'0',	high	'dri	ive '	1''													
			DOS1	4		Di	sconnec	t '0'	star	ndar	d '1	' (no	rm	ally i	use	d fo	wi	red-	or						
						со	nnectio	ns)																	
			D0H1	5			sconnec nnectio		, hig	h dr	ive	'1' (r	norr	mally	y us	ed f	or v	vire	d-o	r					
			SOD1	6			andard '		lisco	nne	ct '1	L' (no	orm	ally	use	d fo	rw	ired	-an	d					
			H0D1	7			gh drive nnectio		disc	onn	ect	'1' (r	norr	nally	y us	ed f	or v	vire	d-a	nd					
	D\A/	SENSE					n sensin	•	acha	nicn	n														
	11.00	51,151	Disabled	0			sabled	ь	-6116	11131															
			High	2			nse for l	high	leva	اد															
			Low	3		26		-	leve																

20.4 Electrical specification

20.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
V _{IH}	Input high voltage	0.7 x VD	D	VDD	V



Symbol	Description	Min.	Тур.	Max.	Units
V _{IL}	Input low voltage	VSS		0.3 x VDI	V
V _{OH,SD}	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4	1	VDD	V
V _{OH,HDH}	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4	1	VDD	V
V _{OH,HDL}	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4	1	VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
V _{OL,HDH}	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
V _{OL,HDL}	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I _{OL,SD}	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
I _{OL,HDH}	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
I _{OL,HDL}	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
I _{OH,SD}	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
I _{OH,HDH}	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
I _{OH,HDL}	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
t _{RF,15pF}	Rise/fall time, standard drive mode, 10-90%, 15 pF load ¹		9		ns
t _{RF,25pF}	Rise/fall time, standard drive mode, 10-90%, 25 pF load ¹		13		ns
t _{RF,50pF}	Rise/fall time, standard drive mode, 10-90%, 50 pF load ¹		25		ns
t _{HRF,15pF}	Rise/Fall time, high drive mode, 10-90%, 15 pF load ¹		4		ns
t _{HRF,25pF}	Rise/Fall time, high drive mode, 10-90%, 25 pF load ¹		5		ns
t _{HRF,50pF}	Rise/Fall time, high drive mode, 10-90%, 50 pF load ¹		8		ns
R _{PU}	Pull-up resistance	11	13	16	kΩ
R _{PD}	Pull-down resistance	11	13	16	kΩ
C _{PAD}	Pad capacitance		3		pF

The current drawn from the battery when GPIO is active as an output is calculated as follows:

 I_{GPIO} = V_{DD} C_{load} f

 C_{load} being the load capacitance and "f" is the switching frequency.

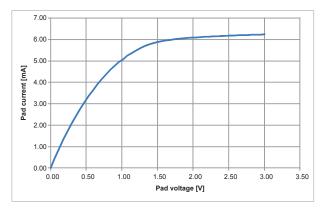


Figure 23: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

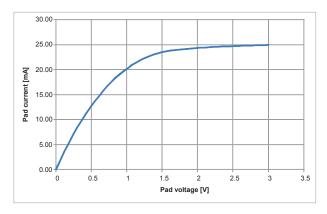


Figure 24: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

¹ Rise and fall times based on simulations



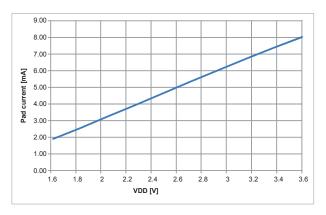


Figure 25: Max sink current vs Voltage, standard drive

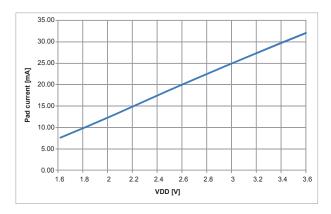


Figure 26: Max sink current vs Voltage, high drive

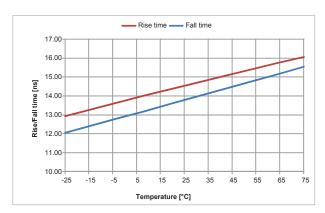


Figure 27: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V



21 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

Table 28: GPIOTE properties

Instance	Number of GPIOTE channels
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- · Rising edge
- Falling edge
- · Any change

21.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY, and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 29: Task priorities* on page 142.

Table 29: Task priorities

Priority	Task
1	OUT
2	CLR
3	SET



When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

21.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* — *General purpose input/output* on page 96 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 96.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

21.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

21.4 Registers

Table 30: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40006000	GPIOTE	GPIOTE	GPIO tasks and events		

Table 31: Register Overview

Register	Offset	Description	
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in	
		CONFIG[0].POLARITY.	
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in	
		CONFIG[1].POLARITY.	



Register	Offset	Description
TASKS_OUT[2]	0x008	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in
0 . [=]		CONFIG[2].POLARITY.
TASKS_OUT[3]	0x00C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in
		CONFIG[3].POLARITY.
TASKS_OUT[4]	0x010	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is configured in
		CONFIG[4].POLARITY.
TASKS_OUT[5]	0x014	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is configured in
,		CONFIG[5].POLARITY.
TASKS_OUT[6]	0x018	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is configured in
		CONFIG[6].POLARITY.
TASKS_OUT[7]	0x01C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is configured in
_		CONFIG[7].POLARITY.
TASKS_SET[0]	0x030	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it high.
TASKS_SET[1]	0x034	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it high.
TASKS_SET[2]	0x038	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high.
TASKS_SET[3]	0x03C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high.
TASKS_SET[4]	0x040	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high.
TASKS_SET[5]	0x044	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high.
TASKS_SET[6]	0x048	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_SET[7]	0x04C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high.
TASKS_CLR[0]	0x060	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[1]	0x064	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[1]	0x104	Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[5]	0x114	Event generated from pin specified in CONFIG[5].PSEL
EVENTS_IN[6]	0x118	Event generated from pin specified in CONFIG[6].PSEL
EVENTS_IN[7]	0x11C	Event generated from pin specified in CONFIG[7].PSEL
EVENTS_PORT	0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG[0]	0x510	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[1]	0x514	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[2]	0x518	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[3]	0x51C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[4]	0x520	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[5]	0x524	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[6]	0x528	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7]	0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

21.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	1	HGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
		and the late of th

A RW INO Write '1' to Enable interrupt for IN[0] event



Bit r	numbe	r		31 30 2	29 2	28 27	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				1					H G F E D C B A
		0000000	Value Id		0	0 0	0 (0	
Id	KVV	Field	Value Id	Value					Description See EVENTS_IN[0]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
В	RW	IN1							Write '1' to Enable interrupt for IN[1] event
									See EVENTS_IN[1]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
С	RW	IN2							Write '1' to Enable interrupt for IN[2] event
									See EVENTS_IN[2]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
D	RW	IN3							Write '1' to Enable interrupt for IN[3] event
									See EVENTS_IN[3]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
E	RW	IN4							Write '1' to Enable interrupt for IN[4] event
									See EVENTS_IN[4]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
F	RW	IN5							Write '1' to Enable interrupt for IN[5] event
									See EVENTS_IN[5]
			Set	1					Enable
			Disabled	0					Read: Disabled
G	RW	IN6	Enabled	1					Read: Enabled Write '1' to Enable interrupt for IN[6] event
			Cat	1					See EVENTS_IN[6]
			Set Disabled	1					Enable Read: Disabled
			Enabled	1					Read: Enabled
Н	RW	IN7	Enabled	-					Write '1' to Enable interrupt for IN[7] event
									See EVENTS_IN[7]
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
I	RW	PORT							Write '1' to Enable interrupt for PORT event
									See EVENTS_PORT
			Set	1					Enable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled

21.4.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				1	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	INO			Write '1' to Disable interrupt for IN[0] event
					See EVENTS_IN[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	IN1			Write '1' to Disable interrupt for IN[1] event
					See EVENTS_IN[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	IN2			Write '1' to Disable interrupt for IN[2] event
					See EVENTS_IN[2]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	IN3			Write '1' to Disable interrupt for IN[3] event
					See EVENTS_IN[3]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	IN4			Write '1' to Disable interrupt for IN[4] event
					See EVENTS_IN[4]
			Clear	1	Disable
			Disabled	0	Read: Disabled
-	DIM	INIE	Enabled	1	Read: Enabled
F	KW	IN5			Write '1' to Disable interrupt for IN[5] event
					See EVENTS_IN[5]
			Clear	1	Disable
			Disabled	0	Read: Disabled
_	DVA	INC	Enabled	1	Read: Enabled
G	KVV	IN6			Write '1' to Disable interrupt for IN[6] event
					See EVENTS_IN[6]
			Clear	1	Disable
			Disabled	0	Read: Disabled
	DVA	INIZ	Enabled	1	Read: Enabled
Н	KVV	IN7			Write '1' to Disable interrupt for IN[7] event
					See EVENTS_IN[7]
			Clear	1	Disable
			Disabled	0	Read: Disabled
	Ditt	DODT	Enabled	1	Read: Enabled
ı	кW	PORT			Write '1' to Disable interrupt for PORT event
					See EVENTS_PORT
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

21.4.3 CONFIG[0]

Address offset: 0x510



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	. 0
Id	E DD BBBBB	А
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id RW Field Value Id	Value Description	
A RW MODE	Mode	
Disabled	O Disabled. Pin specified by PSEL will not be acquired by the	
	GPIOTE module.	
Event	1 Event mode	
	The pin specified by PSEL will be configured as an input and the	
	IN[n] event will be generated if operation specified in POLARITY	
	occurs on the pin.	
Task	3 Task mode	
	The GPIO specified by PSEL will be configured as an output and	
	triggering the SET[n], CLR[n] or OUT[n] task will perform the	
	operation specified by POLARITY on the pin. When enabled as a	
	task the GPIOTE module will acquire the pin and the pin can no	
	longer be written as a regular output pin from the GPIO module.	
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks	
	and IN[n] event	
D RW POLARITY	When In task mode: Operation to be performed on output	
	when OUT[n] task is triggered. When In event mode: Operation	
	on input that shall trigger IN[n] event.	
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no	
	IN[n] event generated on pin activity.	
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate	
	IN[n] event when rising edge on pin.	
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate	
	IN[n] event when falling edge on pin.	
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate	
	IN[n] when any change on pin.	
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE	
	channel is configured. When in event mode: No effect.	
Low	0 Task mode: Initial value of pin before task triggering is low	
High	1 Task mode: Initial value of pin before task triggering is high	

21.4.4 CONFIG[1]

Address offset: 0x514

	_	_		-	-						-	-																						
Bit r	umbe	er		31	30	29	28 2	27 :	26 2	5 2	4 2	23 2	22 2	21 2	20 1	19 :	18	17	16	15	14	13	12	11	10	9	8 7	7	6 5	4	3	2	1	0
Id															Ε			D	D				В	В	В	В	В						Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)	0 0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	crip	otio	n																			
Α	RW	MODE									١	Mod	le																					
			Disabled	0							[Disal	ble	d. P	in :	spe	cifi	ed	by	PSE	Lw	/ill r	not	be a	cqu	uire	d by	th	ie					
											(GPIC	OTE	mo	odu	le.																		
			Event	1							Е	ven	nt r	nod	le																			
											1	Γhe i	pir	n spe	ecif	ied	bv	PS	EL۱	will	be	cor	nfigi	ured	d as	an	inpu	ıt a	and t	the				
																							-				d in							
											(occu	ırs	on t	the	pir	٦.																	
			Task	3							1	Γask	m	ode																				
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Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E DD BBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
D RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.5 CONFIG[2]

Address offset: 0x518

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E DD BBBB AA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	MODE		Mode
			Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
				GPIOTE module.
			Event	1 Event mode
				The pin specified by PSEL will be configured as an input and the
				IN[n] event will be generated if operation specified in POLARITY
				occurs on the pin.
			Task	3 Task mode
				The GPIO specified by PSEL will be configured as an output and
				triggering the SET[n], CLR[n] or OUT[n] task will perform the
				operation specified by POLARITY on the pin. When enabled as a
				task the GPIOTE module will acquire the pin and the pin can no
				longer be written as a regular output pin from the GPIO module.
В	RW	PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
				and IN[n] event
D	RW	POLARITY		When In task mode: Operation to be performed on output
				when OUT[n] task is triggered. When In event mode: Operation
				on input that shall trigger IN[n] event.
			None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
				IN[n] event generated on pin activity.
			LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
				IN[n] event when rising edge on pin.
			HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
				IN[n] event when falling edge on pin.
			Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
				IN[n] when any change on pin.



nur	nbei	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
															Ε			D	D				В	В	В	В	В						Α	Α
set (0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
R	w	Field	Value Id	Va	lue							De	scri	iptio	on																			
R	W	OUTINIT										Wł	nen	in t	tas	k m	ode	e: Ir	nitia	al va	alue	of	the	out	put	wh	en	the	GP	IOT	E			
												cha	ann	el is	s co	onfi	gur	ed.	Wł	nen	in	eve	nt n	nod	e: N	lo e	ffe	t.						
			Low	0								Tas	sk n	nod	le:	Initi	ial v	valu	ie o	f pi	n b	efo	re ta	ask	trig	ger	ng	s Ic	w					
			High	1								Tas	sk n	nod	le:	Initi	ial v	valu	ie o	f pi	n b	efo	re ta	ask 1	trig	ger	ng	s h	gh					
	set (set 0x00		set 0x00000000 RW Field Value Id RW OUTINIT Low	set 0x00000000 0 RW Field Value Id Value Id RW OUTINIT Low 0	set 0x00000000 0 0 0 RW Field Value Id Value RW OUTINIT Low 0	RW Field Value Id Value RW OUTINIT Low 0	RW Field Value Id Value RW OUTINIT Low 0	set 0x00000000 0	set 0x000000000 0 0 0 0 0 0 0 0 RW Field Value Id RW OUTINIT Low 0	RW Field Value Id Value Value	set 0x000000000 0	RW Field Value Id Value Set Value Id Value Set Value Id Value Set Va	RW Field Value Id Value Section Value Section	RW Field Value Id Value Id Value Id Description of the property of	Set 0x00000000	E set 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	E set 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RW Field Value Id Value Value Description RW OUTINIT When in task mode: In task mo	RW Field Value Id Value State Over the control of the	E TO D D set 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	E D D set 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	E D D Set 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	E D D B set 0x000000000 0 <t< td=""><td>RW Field Value Id Value Set UNIFICATION OF THE NAME OF TH</td><td>RW Field Value Id Value Value Value Id Description RW OUTINIT When in task mode: Initial value of the output channel is configured. When in event mode: Note that the properties of the configured in the configured in the configured in the configured in the configuration of the configur</td><td>RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when the event mode: No each of the count of the count</td><td>RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when channel is configured. When in event mode: No effective like in the control of the country o</td><td>set 0x00000000000000000000000000000000000</td><th>RW Field Value Id Value Val</th><th> Set 0x000000000</th><td>RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0</td></t<> <td>The section of the content of the co</td> <td>RW OUTINIT Low 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>	RW Field Value Id Value Set UNIFICATION OF THE NAME OF TH	RW Field Value Id Value Value Value Id Description RW OUTINIT When in task mode: Initial value of the output channel is configured. When in event mode: Note that the properties of the configured in the configured in the configured in the configured in the configuration of the configur	RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when the event mode: No each of the count	RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when channel is configured. When in event mode: No effective like in the control of the country o	set 0x00000000000000000000000000000000000	RW Field Value Id Value Val	Set 0x000000000	RW Field Value Id Value Id Description RW OUTINIT When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect. Low 0	The section of the content of the co	RW OUTINIT Low 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

21.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit	num	ber			33	1 30	29	28	27	26	25	24	23	3 2	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Id																Ε			D	D				В	В	В	В	В							Α
Res	et 0	х О О	000000		0	0	0	0	0	0	0	0	0	(0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	R۱	N	Field	Value Id	V	alue							De	esc	cripti	on																			
Α	R۱	Ν	MODE										M	od	de																				
				Disabled	0							1	Di	sal	bled.	Pir	spe	cif	ied	by	PSE	Lν	/ill	not	be	acc	uir	ed l	y t	he					
													GF	PIC	OTE n	nod	lule.																		
				Event	1							-	Ev	/en	nt mo	de																			
													Th	ne	pin s	pec	ified	l by	/ PS	EL	will	be	СО	nfig	gure	ed a	s ar	n in	out	and	d th	e			
													IN	l[n]	eve]	nt ۱	will l	oe g	gen	era	ted	if	ре	rati	ion	spe	cifi	ed i	n P	OL/	ARIT	Υ			
													ос	cu	ırs or	th	e pi	۱.																	
				Task	3								Та	sk	mod	le																			
													Th	ne i	GPIO	sp	ecifi	ed	by I	PSE	Lw	rill b	oe o	conf	figu	ired	as	an	out	put	and	d			
												1	tri	igg	gering	th	e SE	T[n	i], C	LR	[n]	or (רטכ	[[n]	tas	sk w	/ill p	erf	orn	th	e				
													ор	oer	ratior	n sp	ecif	ied	by	РО	LAF	RITY	or or	th.	ер	in. ۱	Νhe	en e	nal	oled	l as	а			
												1	tas	sk	the 0	3PI	ОТЕ	mc	du	e v	vill	acq	uir	e th	ne p	in a	nd	the	pir	са	n no	0			
												-	lol	ng	er be	wr	itte	n a	s a ı	eg	ula	r oı	ıtpı	ut p	in f	ron	n th	ie G	PIO	mo	odu	le.			
В	R۷	Ν	PSEL		[0	31	.]					(GF	PIC) nun	nbe	er as	soc	iate	ed v	with	n SE	T[r	n], C	CLR	[n] a	and	OU	T[n] ta	sks				
													an	nd	IN[n]	ev	ent																		
D	R۱	Ν	POLARITY									,	W	he	en In 1	tasl	k mo	de	: O _I	oer	atio	n t	o b	e p	erf	orm	ed	on (out	out					
												,	wł	he	n OU	T[n] ta	k is	s tri	gge	ere	d. V	Vhe	n lı	n e	ven	t m	ode	: 0	oera	atio	n			
												•	on	ı ir	nput	tha	t sh	all t	rigg	ger	IN[n] e	eve	nt.											
				None	0								Та	sk	mod	le: I	No e	ffe	ct c	n p	oin 1	froi	n C	UT	[n]	tas	k. E	ven	t m	ode	e: no	0			
												-	IN	I[n]] eve	nt g	gene	rat	ed	on	pin	act	ivit	y.											
				LoToHi	1										mod										eve	nt n	nod	le: 0	en	era	te				
														-] eve				•		-														
				HiToLo	2										mod							-	-		E\	/en	m	ode	: Ge	ene	rate	à			
														-] eve					-	_		•					_							
				Toggle	3										mod		-						[[n]	. E\	/en	t m	ode	:: G	ene	rate	9				
_	Di	.,	OUTINIT											-] whe				-		•									-	210				
E	K۱	/V	OUTINIT												en in 1											•				e Gl	10	ΙĖ			
				Laur	0										nnel i		_																		
				Low	0										mod						•							_							
				High	1								ıa	ISK	mod	ie: I	mitia	ii V	alu	5 0	рп	וו מ	eto	re t	ask	tri	gei	ring	ıs r	iigh					

21.4.7 CONFIG[4]

Address offset: 0x520



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id	E DD BBBBB A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW MODE	Mode
Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
	GPIOTE module.
Event	1 Event mode
	The pin specified by PSEL will be configured as an input and the
	IN[n] event will be generated if operation specified in POLARITY
	occurs on the pin.
Task	3 Task mode
	The GPIO specified by PSEL will be configured as an output and
	triggering the SET[n], CLR[n] or OUT[n] task will perform the
	operation specified by POLARITY on the pin. When enabled as a
	task the GPIOTE module will acquire the pin and the pin can no
	longer be written as a regular output pin from the GPIO module.
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
D RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.8 CONFIG[5]

Address offset: 0x524

	_	_		-	-						-	-																						
Bit r	umbe	er		31	30	29	28 2	27 :	26 2	5 2	4 2	23 2	22 2	21 2	20 1	19 :	18	17	16	15	14	13	12	11	10	9	8 7	7	6 5	4	3	2	1	0
Id															Ε			D	D				В	В	В	В	В						Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)	0 0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	crip	otio	n																			
Α	RW	MODE									١	Mod	le																					
			Disabled	0							[Disal	ble	d. P	in :	spe	cifi	ed	by	PSE	Lw	/ill r	not	be a	cqu	uire	d by	th	ie					
											(GPIC	OTE	mo	odu	le.																		
			Event	1							Е	ven	nt r	nod	le																			
											1	Γhe i	pir	n spe	ecif	ied	bv	PS	EL۱	will	be	cor	nfigi	ured	d as	an	inpu	ut a	and t	the				
																							-				d in							
											(occu	ırs	on t	the	pir	٦.																	
			Task	3							1	Γask	m	ode																				
											,	Γhρ (GP	ه ۱۱	ne	cifi	ad I	av I	OSE	l 147	ill h	na r	onf	igur	ha:	20.2	ın oı	ıtn	ut a	nd				
																								-			erfoi							
														_			-		-	-							n en							
																		•						•			he p							
																								•			GPI							
												Uligi	CI	ne i	vv 1 11	LCI	ı as	al	cgi	ııal	ou	ιμα	ı Pi	11 11	UIII	cit	. Gr	U	11100	iuie				



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E DD BBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
D RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.9 CONFIG[6]

Address offset: 0x528

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E DD BBBB AA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	MODE		Mode
			Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
				GPIOTE module.
			Event	1 Event mode
				The pin specified by PSEL will be configured as an input and the
				IN[n] event will be generated if operation specified in POLARITY
				occurs on the pin.
			Task	3 Task mode
				The GPIO specified by PSEL will be configured as an output and
				triggering the SET[n], CLR[n] or OUT[n] task will perform the
				operation specified by POLARITY on the pin. When enabled as a
				task the GPIOTE module will acquire the pin and the pin can no
				longer be written as a regular output pin from the GPIO module.
В	RW	PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
				and IN[n] event
D	RW	POLARITY		When In task mode: Operation to be performed on output
				when OUT[n] task is triggered. When In event mode: Operation
				on input that shall trigger IN[n] event.
			None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
				IN[n] event generated on pin activity.
			LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
				IN[n] event when rising edge on pin.
			HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
				IN[n] event when falling edge on pin.
			Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
				IN[n] when any change on pin.



Bit number		31	. 30	29	28	27	26	25	24	23	3 22	2 2	1 2	0 1	9 1	8 1	7 1	L6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id													E			[)	D				В	В	В	В	В							Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0) () (0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id RW Field	Value Id	Va	lue							De	esci	ript	ior	1																				
E RW OUTINIT										W	hei	n in	ta	sk r	noc	le:	Init	tial	va	lue	of t	he	out	put	wl	nen	the	e GF	019	ГΕ				
										ch	anı	nel	is c	on	figu	ired	l. V	Vh	en i	in e	ver	nt m	nod	e: N	lo e	effe	ct.							
	Low	0								Та	sk	mo	de:	Ini	tial	va	lue	of	pir	n be	for	e ta	sk	trig	ger	ing	is l	ow						
	High	1								Та	sk	mo	de:	Ini	tial	va	lue	of	pir	n be	for	e ta	sk	trig	ger	ing	is h	igh						

21.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit	numbe	er		31	30	29 28	3 27	26 2	5 24	1 23	3 22 2	1 20	19	18 :	17 1	6 15	14	13	12 :	11 1	0 9	8	7	6	5	4	3 2	1	0
Id												Е			D C)			В	ВЕ	3 B	В						Α	Α
Res	et 0x0	0000000		0	0	0 0	0	0 (0 0	0	0 (0 0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	lue					D	escrip	tion																	
Α	RW	MODE								M	lode																		
			Disabled	0						Di	isable	d. Pi	n spe	cifi	ed b	y PS	EL v	vill n	ot l	oe ad	cqui	red	by t	he					
										GI	PIOTE	mo	dule.																
			Event	1						Εv	ent m	node	<u> </u>																
										Th	ne pin	spe	cified	l by	PSE	L wil	l be	con	figu	ired	as a	n in	put	and	d th	e			
										IN	I[n] ev	/ent	will b	oe g	ener	ate	d if o	per	atic	n sp	ecif	ied	in P	OLA	ARIT	Υ			
										00	ccurs o	on th	ne pir	١.															
			Task	3						Ta	ask mo	ode																	
										Th	ne GPI	IO sp	ecifi	ed b	oy PS	SEL v	vill l	oe co	nfi	gure	d as	s an	out	put	and	t			
										tri	iggeriı	ng th	ne SE	T[n]], CLI	R[n]	or ()TUC	n] t	ask	will	per	forn	n th	е				
										op	peratio	on s	pecif	ied	by P	OLA	RITY	on '	the	pin.	Wh	en e	enal	oled	d as	a			
										ta	sk the	GP	IOTE	mo	dule	will	acq	uire	the	pin	and	the	e pir	ca	n no)			
										lo	nger b	oe w	rittei	n as	a re	gula	ır oı	ıtpu	t pi	n fro	m t	he G	PIC	mo	odul	le.			
В	RW	PSEL		[0	.31]					GI	PIO nu	umb	er as	soci	iated	l wit	h SE	T[n]	, Cl	.R[n]] and	d Ol	JT[n] ta	isks				
										ar	nd IN[ı	n] ev	/ent																
D	RW	POLARITY								W	/hen Ir	n tas	k mo	de:	Оре	erati	on t	o be	pe	rforı	med	l on	out	put					
										W	hen O	UT[i	n] tas	k is	trig	gere	d. V	Vher	ı In	eve	nt m	node	e: O	oera	atio	n			
										or	n inpu	t tha	at sha	all tr	rigge	r IN	[n] e	even	t.										
			None	0						Ta	ask mo	ode:	No e	ffec	ct on	pin	froi	n Ol	JT[i	n] ta	sk. I	Ever	nt m	ode	e: no)			
										IN	I[n] ev	/ent	gene	rate	ed o	n pir	n act	tivity	٠.										
			LoToHi	1						Ta	ask mo	ode:	Set p	oin f	from	OU	T[n]	task	. Ev	/ent	mo	de: (Gen	era	te				
										IN	I[n] ev	/ent	whe	n ris	sing (edge	on	pin.											
			HiToLo	2						Ta	ask mo	ode:	Clea	r piı	n fro	m O	UT[n] ta	sk.	Evei	nt m	ode	:: Ge	enei	rate				
										IN	I[n] ev	/ent	whe	n fa	lling	edg	e or	n pin											
			Toggle	3							ask mo		-					Γ[n].	Eve	ent n	nod	e: G	ene	rate	9				
										IN	I[n] w	hen	any c	har	nge o	n p	in.												
Е	RW	OUTINIT								W	/hen ir	n tas	k mo	de:	Initi	al v	alue	of t	he (outp	ut v	vher	the	e GF	PIOT	ГЕ			
										ch	nannel	l is c	onfig	ure	d. W	/hen	in e	even	t m	ode:	: No	effe	ect.						
			Low	0						Ta	ask mo	ode:	Initia	al va	alue	of p	in be	efore	e ta	sk tr	igge	ering	g is I	ow					
			High	1						Ta	ask mo	ode:	Initia	al va	alue	of p	in be	efore	e ta	sk tr	igge	ering	g is h	nigh	1				

21.5 Electrical specification

21.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{GPIOTE,IN}	Run current with 1 or more GPIOTE active channels in Input				μΑ
	mode, System On Idle				



Symbol	Description	Min.	Тур.	Max.	Units
I _{GPIOTE,OUT}	Run current with 1 or more GPIOTE active channels in Output				μΑ
	mode, System On Idle				
I _{GPIOTE,IDLE}	Run current when all channels in Idle mode.				μΑ



22 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

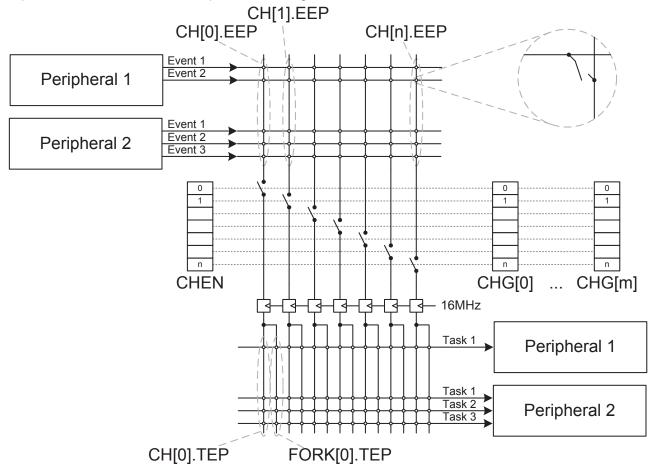


Figure 28: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 32: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.



Note that shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks.
 Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

22.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

Table 33: Pre-programmed channels

Channel	EEP	TEP
20	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMERO->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMERO->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMERO->TASKS_CAPTURE[2]
28	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_CLEAR
31	RTC0->EVENTS_COMPARE[0]	TIMERO->TASKS_START

22.2 Registers

Table 34: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	Programmable peripheral interconnect	

Table 35: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4



Register	Offset	Description
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 task end-point
CH[12].EEP	0x570	Channel 12 event end-point
CH[12].TEP	0x574	Channel 12 task end-point
CH[13].EEP	0x578	Channel 13 event end-point
CH[13].TEP	0x57C	Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x584	Channel 14 task end-point
CH[15].EEP	0x588	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x594	Channel 16 task end-point
CH[17].EEP	0x598	Channel 17 event end-point
CH[17].TEP	0x59C	Channel 17 task end-point
CH[18].EEP	0x5A0	Channel 18 event end-point
CH[18].TEP	0x5A4	Channel 18 task end-point
CH[19].EEP	0x5A8	Channel 19 event end-point
CH[19].TEP	0x5AC	Channel 19 task end-point
CHG[0]	0x800	Channel group 0
CHG[1]	0x804	Channel group 1
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 3
CHG[4]	0x810	Channel group 4
CHG[5]	0x814	Channel group 5
FORK[0].TEP	0x910	Channel 0 task end-point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point



Register	Offset	Description	
FORK[6].TEP	0x928	Channel 6 task end-point	
FORK[7].TEP	0x92C	Channel 7 task end-point	
FORK[8].TEP	0x930	Channel 8 task end-point	
FORK[9].TEP	0x934	Channel 9 task end-point	
FORK[10].TEP	0x938	Channel 10 task end-point	
FORK[11].TEP	0x93C	Channel 11 task end-point	
FORK[12].TEP	0x940	Channel 12 task end-point	
FORK[13].TEP	0x944	Channel 13 task end-point	
FORK[14].TEP	0x948	Channel 14 task end-point	
FORK[15].TEP	0x94C	Channel 15 task end-point	
FORK[16].TEP	0x950	Channel 16 task end-point	
FORK[17].TEP	0x954	Channel 17 task end-point	
FORK[18].TEP	0x958	Channel 18 task end-point	
FORK[19].TEP	0x95C	Channel 19 task end-point	
FORK[20].TEP	0x960	Channel 20 task end-point	
FORK[21].TEP	0x964	Channel 21 task end-point	
FORK[22].TEP	0x968	Channel 22 task end-point	
FORK[23].TEP	0x96C	Channel 23 task end-point	
FORK[24].TEP	0x970	Channel 24 task end-point	
FORK[25].TEP	0x974	Channel 25 task end-point	
FORK[26].TEP	0x978	Channel 26 task end-point	
FORK[27].TEP	0x97C	Channel 27 task end-point	
FORK[28].TEP	0x980	Channel 28 task end-point	
FORK[29].TEP	0x984	Channel 29 task end-point	
FORK[30].TEP	0x988	Channel 30 task end-point	
FORK[31].TEP	0x98C	Channel 31 task end-point	

22.2.1 CHEN

Address offset: 0x500 Channel enable register

																										_						
	numb	er					28																			7	6	5		3 2	! 1	. 0
Id				f	е	d	С	b	a :	Z۱	/ X	W	/ V	' U	ΙT	S	R	Q	Р	0	N	M	LI	K J	- 1	Н	G	F	Ε	D (: B	3 A
Res	et 0x(00000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	٧	alue	!					D	escr	ript	ion																		
Α	RW	CH0									Er	nabl	le o	r d	isab	le i	har	nne	0 ا													
			Disabled	0							D	isab	le c	cha	nne	1																
			Enabled	1							Eı	nabl	le c	har	nnel																	
В	RW	CH1									Er	nabl	le o	r d	isab	le i	har	nne	1													
			Disabled	0							D	isab	le c	cha	nne	I																
			Enabled	1							Er	nabl	le c	har	nnel																	
С	RW	CH2									Er	nabl	le o	r d	isab	le	har	nne	12													
			Disabled	0							D	isab	le c	cha	nne	1																
			Enabled	1							Eı	nabl	le c	har	nnel																	
D	RW	CH3									Er	nabl	le o	r d	isab	le i	har	nne	13													
			Disabled	0							D	isab	le c	cha	nne	1																
			Enabled	1							Er	nabl	le c	har	nnel																	
Ε	RW	CH4									Er	nabl	le o	r d	isab	le i	har	nne	14													
			Disabled	0							D	isab	le c	cha	nne	1																
			Enabled	1							Er	nabl	le c	har	nnel																	
F	RW	CH5									Er	nabl	le o	r d	isab	le i	har	nne	15													
			Disabled	0							D	isab	le c	cha	nne	I																
			Enabled	1							Er	nabl	le c	har	nnel																	
G	RW	CH6									Er	nabl	le o	r d	isab	le	har	nne	16													
			Disabled	0							D	isab	le c	cha	nne	1																
			Enabled	1							Er	nabl	le c	har	nnel																	
Н	RW	CH7									Eı	nabl	le o	r d	isab	le i	har	nne	17													



Bit r	numbe	er		31 30	29 28	3 27 :	26 25	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Υ	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et OxC	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Disabled	0					Disable channel
			Enabled	1					Enable channel
I	RW	CH8							Enable or disable channel 8
			Disabled	0					Disable channel
			Enabled	1					Enable channel
J	RW	CH9							Enable or disable channel 9
			Disabled	0					Disable channel
			Enabled	1					Enable channel
K	RW	CH10							Enable or disable channel 10
			Disabled	0					Disable channel
			Enabled	1					Enable channel
L	RW	CH11							Enable or disable channel 11
			Disabled	0					Disable channel
			Enabled	1					Enable channel
М	RW	CH12							Enable or disable channel 12
			Disabled	0					Disable channel
			Enabled	1					Enable channel
N	RW	CH13							Enable or disable channel 13
			Disabled	0					Disable channel
			Enabled	1					Enable channel
0	RW	CH14							Enable or disable channel 14
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Р	RW	CH15							Enable or disable channel 15
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Q	RW	CH16							Enable or disable channel 16
			Disabled	0					Disable channel
			Enabled	1					Enable channel
R	RW	CH17							Enable or disable channel 17
			Disabled	0					Disable channel
			Enabled	1					Enable channel
S	RW	CH18							Enable or disable channel 18
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Т	RW	CH19							Enable or disable channel 19
			Disabled	0					Disable channel
			Enabled	1					Enable channel
U	RW	CH20							Enable or disable channel 20
			Disabled	0					Disable channel
			Enabled	1					Enable channel
V	RW	CH21							Enable or disable channel 21
			Disabled	0					Disable channel
			Enabled	1					Enable channel
W	RW	CH22							Enable or disable channel 22
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Χ	RW	CH23							Enable or disable channel 23
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Υ	RW	CH24							Enable or disable channel 24
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Z	RW	CH25							Enable or disable channel 25
			Disabled	0					Disable channel



Bit	numbe	er		3	1 30	29	28	27 2	26 2	25 2	4 2	3 22	21	20	19	18	17 :	16 1	l5 1	.4 13	3 12	11	10	9 :	8 7	6	5	4	3 2	2 1	1 0
Id				f	е	d	С	b	а	ΖY	′ X	W	٧	U	Т	S	R	Q	Р (N C	М	L	K	J	ΙН	G	F	Ε	D (С Е	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0 0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	V	alue	•					D	escri	ipti	on																	
			Enabled	1							Eı	nable	e ch	nann	nel																
а	RW	CH26									E	nable	e or	r dis	able	e ch	anr	el 2	26												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							E	nable	e ch	nann	nel																
b	RW	CH27									E	nable	e or	r dis	able	e ch	anr	iel 2	27												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							E	nable	e ch	nann	nel																
С	RW	CH28									E	nable	e or	r dis	able	e ch	anr	el 2	28												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							E	nable	e ch	nann	nel																
d	RW	CH29									Eı	nable	e or	r dis	able	e ch	anr	el 2	29												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							Ei	nable	e ch	nann	nel																
е	RW	CH30									Ei	nable	e or	r dis	able	e ch	anr	el 3	30												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							Ei	nable	e ch	nann	nel																
f	RW	CH31									Eı	nable	e or	r dis	able	e ch	anr	iel 3	31												
			Disabled	0							D	isabl	e cl	hanı	nel																
			Enabled	1							E	nable	e ch	nann	nel																

22.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Bit r	umbe	er		3	1 30	29	9 28	3 2	7 26	5 2	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10 9	9 8	3 7	6	5	4	3	2 1	1 0
Id				f	e	d	l c	b	а	Z	Y.	Χ	W	V	U	Т	S	R	Q	Р	О	Ν	М	L	Κ.	J	Н	G	F	Ε	D	C E	3 A
Rese	et 0x0	0000000		0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 (0
Id	RW	Field	Value Id	٧	alue	9						De	escri	ptic	on																		
Α	RW	CH0										Ch	ann	el C	en (abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sal	oled	ı														
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															
В	RW	CH1										Ch	nann	el 1	en	abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sal	oled	ı														
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															
С	RW	CH2										Ch	ann	el 2	en!	abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sal	oled	I														
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															
D	RW	CH3										Ch	ann	el 3	en.	abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sak	oled	ı														
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															
E	RW	CH4										Ch	nann	el 4	l en	abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sak	oled	I														
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															
F	RW	CH5										Ch	ann	el 5	en	abl	e se	et r	egis	ter	. W	riti	ng ')' h	as no	o ef	fect						
			Disabled	0								Re	ead:	cha	nne	el di	sak	oled															
			Enabled	1								Re	ead:	cha	nne	el ei	nab	led															
			Set	1								W	rite:	En	able	e ch	anı	nel															



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value Description
G	RW CH6	Disabled	Channel 6 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled 1 Read: channel enabled
		Enabled	
Н	RW CH7	Set	
П	KW CH/	Disabled	Channel 7 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
	RW CH8	300	Channel 8 enable set register. Writing '0' has no effect
	NW CHO	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
1	RW CH9	361	Channel 9 enable set register. Writing '0' has no effect
•	55	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
K	RW CH10	500	Channel 10 enable set register. Writing '0' has no effect
	620	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
L	RW CH11		Channel 11 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
М	RW CH12		Channel 12 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
N	RW CH13		Channel 13 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
0	RW CH14		Channel 14 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Р	RW CH15		Channel 15 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Q	RW CH16		Channel 16 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
R	RW CH17		Channel 17 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
S	RW CH18		Channel 18 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Т	RW CH19		Channel 19 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDO	СВА
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id	RW Field	Value Id	Value Description	
		Set	1 Write: Enable channel	
U	RW CH20		Channel 20 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
V	RW CH21		Channel 21 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
W	RW CH22		Channel 22 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Х	RW CH23		Channel 23 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Υ	RW CH24		Channel 24 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
Z	RW CH25		Channel 25 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
а	RW CH26		Channel 26 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
b	RW CH27		Channel 27 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
С	RW CH28		Channel 28 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
d	RW CH29		Channel 29 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
e	RW CH30		Channel 30 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	
f	RW CH31		Channel 31 enable set register. Writing '0' has no effect	
		Disabled	0 Read: channel disabled	
		Enabled	1 Read: channel enabled	
		Set	1 Write: Enable channel	

22.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register



Read: reads value of CH{i} field in CHEN register.

Bit r	numbe	er		31 30 2	9 28 2	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Α	RW	CH0						Channel 0 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
В	RW	CH1						Channel 1 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
С	RW	CH2						Channel 2 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
D	RW	CH3						Channel 3 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
E	R\M/	CH4	Cicai	-				Channel 4 enable clear register. Writing '0' has no effect
_	11.00	CH	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
				1				Write: disable channel
_	DIA	CHE	Clear	1				
F	KVV	CH5	Disabled	0				Channel 5 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
G	RW	CH6		_				Channel 6 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Н	RW	CH7						Channel 7 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
I	RW	CH8						Channel 8 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
J	RW	CH9						Channel 9 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
K	RW	CH10						Channel 10 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
L	RW	CH11						Channel 11 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
М	B/v/	CH12	J.Cui					Channel 12 enable clear register. Writing '0' has no effect
141	11.44	C.112	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
N:	Divi	CUIA	Clear	1				Write: disable channel
N	RW	CH13						Channel 13 enable clear register. Writing '0' has no effect



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
0	RW CH14		Channel 14 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Р	RW CH15		Channel 15 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Q	RW CH16		Channel 16 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
-	D 0.115	Clear	1 Write: disable channel
R	RW CH17	S. 11.1	Channel 17 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
_	DW CHIA	Clear	1 Write: disable channel
S	RW CH18	Disabled	Channel 18 enable clear register. Writing '0' has no effect O Read: channel disabled
		Disabled Enabled	0 Read: channel disabled 1 Read: channel enabled
		Clear	Read: Channel enabled Write: disable channel
т	RW CH19	Cicai	Channel 19 enable clear register. Writing '0' has no effect
	KW CIII3	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
U	RW CH20	olea.	Channel 20 enable clear register. Writing '0' has no effect
	6.1.20	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
V	RW CH21		Channel 21 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
W	RW CH22		Channel 22 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Χ	RW CH23		Channel 23 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Υ	RW CH24		Channel 24 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Z	RW CH25		Channel 25 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
а	RW CH26		Channel 26 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel



Bit number		3:	1 30	29	28	27 2	26 2	25 2	24 2	23	22 :	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4 3	3 2	1	0
Id		f	е	d	С	b	а	Ζ	Υ	Х	W	٧	U	Т	S	R	Q	Р	О	Ν	М	L	K	J	1	Н	G	F	E [) C	В	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	V	alue							Des	scrip	ptic	on																			
b RW CH27									(Cha	anne	el 2	27 e	enal	ble	cle	ar r	egi	ster	. W	ritin	g '0)' ha	ıs n	o e	ffe	ct					
	Disabled	0							F	Rea	ad: d	cha	nne	el d	lisa	ble	d															
	Enabled	1							F	Rea	ad: d	cha	nne	el e	na	ble	t															
	Clear	1							١	Wri	ite:	dis	abl	le c	haı	nne	ı															
c RW CH28									(Cha	anne	el 2	28 e	enal	ble	cle	ar r	egi	ster	. W	ritin	g '0)' ha	ıs n	o e	ffe	ct					
	Disabled	0							F	Rea	ad: d	cha	nne	el d	lisa	ble	d															
	Enabled	1							F	Rea	ad: d	cha	nne	el e	na	ble	t															
	Clear	1							١	Wri	ite:	dis	sabl	le c	haı	nne	I															
d RW CH29									(Cha	anne	el 2	29 e	enal	ble	cle	ar r	egi	ster	. W	ritin	g '0)' ha	is n	o e	ffe	ct					
	Disabled	0							F	Rea	ad: d	cha	nn	el d	lisa	ble	d															
	Enabled	1							F	Rea	ad: d	cha	nn	el e	na	ble	t															
	Clear	1							١	Wri	ite:	dis	sabl	le c	haı	nne	ı															
e RW CH30									(Cha	anne	el 3	30 e	enal	ble	cle	ar r	egi	ster	. W	ritin	g '0)' ha	is n	o e	ffe	ct					
	Disabled	0							F	Rea	ad: d	cha	nn	el d	lisa	ble	d															
	Enabled	1							F	Rea	ad: d	cha	nne	el e	na	ble	t															
	Clear	1							١	Wri	ite:	dis	abl	le c	haı	nne	ı															
f RW CH31									(Cha	anne	el 3	31 e	enal	ble	cle	ar r	egi	ster	. W	ritin	g '0)' ha	ıs n	o e	ffe	ct					
	Disabled	0							F	Rea	ad: d	cha	nne	el d	lisa	ble	d															
	Enabled	1							F	Rea	ad: d	cha	nne	el e	na	ble	t															
	Clear	1							١	Wri	ite:	dis	sabl	le c	haı	nne																

22.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 :	11 1	10 !	9 8	3 7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Α Α	A	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α.	Α	A	À.
Re	set 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	EEP										Poi	nter	to	eve	nt r	egis	ter.	Acc	ept	s or	ıly a	ıddı	ess	es t	o re	gist	ers					

from the Event group.

22.2.5 CH[0].TEP

Address offset: 0x514 Channel 0 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 1	.7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ ,	A A	A /	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α
Res	et 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Val	lue							Des	crip	tio	n																		
Α	RW	TEP										Poi	ntei	to	tas	k re	gist	er.	Acc	ept	s or	ıly a	ddr	esse	es to	o re	gist	ters					

from the Task group.

22.2.6 CH[1].EEP

Address offset: 0x518

Channel 1 event end-point



Bit r	numbe	er		31	30	29	28 :	27	26	25	24	23	22	21 :	20 :	19 1	18 1	L7 1	16 :	15 1	L4 :	13 :	12 :	11 1	.0 !	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α .	Α	Α.	Α	Α	Α	Α.	Δ,	Δ.	A	Α	Α	Α	A ,	λ Α	A A	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	n																			
Α	RW	EEP										Poi	nte	r to	eve	ent	regi	iste	r. A	Acce	pts	on	ly a	ddr	ess	es 1	to r	egi	ste	rs				

from the Event group.

from the Task group.

22.2.7 CH[1].TEP

Address offset: 0x51C Channel 1 task end-point

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21 :	20	19 1	18 1	17 1	16 :	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A	Α	A	Δ ,	Δ Α	Α Α	A A	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gis	ter.	Ac	cep	ts o	nly	ado	res	es 1	to r	egis	ters	5				

22.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α ,	Α Α	A	Α	Α	Α	Α	Α	Α	Α ,	Δ /	АА
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	า																	
Α	RW	EEP										Poir	nter	to	even	it re	gist	er.	Acc	epts	on	y ac	ldre	sse	s to	reg	iste	rs				
																	_															

22.2.9 CH[2].TEP

Address offset: 0x524 Channel 2 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	9 1	8 17	7 16	15	14	13	12 :	11 1	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	A	Δ ,	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0 0
Id												Des	crip	otio	n																	
Α	RW	TEP										Poi	ntei	r to	tasl	c re	giste	er. A	ссе	pts	only	ad	dres	ses	to r	egis	ters	S				

22.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 1	18 1	17 1	16 :	15 :	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑД		A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	EEP										Poi	ntei	r to	eve	ent	reg	iste	r. A	Acce	epts	or	ıly a	add	res	ses	toı	reg	iste	rs				

from the Event group.

from the Task group.

22.2.11 CH[3].TEP

Address offset: 0x52C Channel 3 task end-point



Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 :	15 1	.4 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	A	Δ,	A A	Α Α	A	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	gis	ter.	Ac	cep	ts o	nly	add	lress	es 1	o re	egis	ters	5				

from the Task group.

22.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bit r	umb	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	A	Α	Α	Α	A	A A	A	Α	Α	Α	Α	Α	Α	A A	Δ Δ	А
Res	et Ox	00000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																	
Α	RW	EEP										Poi	nte	r to	evei	nt re	egist	er.	Acc	ept	s on	ly a	ddre	sse	s to	reg	iste	rs				
												fro	m tł	ne E	vent	gro	oup.															

22.2.13 CH[4].TEP

Address offset: 0x534

Channel 4 task end-point

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	17 :	16 1	.5 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ.	Α Α	A A	. Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Acc	сер	ts o	nly	add	res	ses	to r	egis	ter	s					_
												fro	m th	he 1	Fask	gr	nun																	

22.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	l8 1	.7 1	16 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	A A	Δ <i>A</i>	A A	. 4	Α Α	A	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0) (0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	EEP										Poi	nter	to	eve	ent	regi	ste	r. A	cce	pts	onl	y ac	ddre	sse	s to	reg	iste	rs				

from the Event group.

22.2.15 CH[5].TEP

Address offset: 0x53C Channel 5 task end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	.5 1	4 1	3 1:	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	Δ ,	Α Α	Δ Δ	. A	A	Α	Α	Α	Α	Α	Α	A	Α.	А А
Res	et 0 x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter.	Acc	ept	s o	nly	add	ress	es 1	o re	egis	ter	5				

Pointer to task register. Accepts only addresses to registers from the Task group.

22.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point



Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	14 1	l3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	A A	Α Α	A A	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	r. A	Acce	pts	onl	y a	ddre	sses	to	reg	iste	rs				

from the Event group.

22.2.17 CH[6].TEP

Address offset: 0x544 Channel 6 task end-point

Bit r	umb	er		31	30	29	28	27	26	25	24	23	22	21	20 1	9 1	8 17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A	Α	Α	Α	Α	Α	Α	Α.	Α	A	Α	A	Α.	A A	A	Α	Α
Res	et Ox	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	inte	r to	tasl	c re	giste	r. A	ссе	pts	onl	y ac	dre	sse	s to	re	gist	ers					
												fro	m tl	he 1	ask	gro	up.																

22.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

Bit r	umbe	er		31	. 30	29	28	27	' 26	25	24	23	22	21	20	19	18 1	17 :	16 1	15 1	.4 1	3 12	2 11	. 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α Α	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	t OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue							De	scri	ptic	on																		
Α	RW	EEP										Ро	inte	r tc	ev	ent	reg	iste	r. A	cce	pts	only	/ ad	dre	sses	s to	reg	iste	ers				
												fro	m t	he I	Eve	nt g	rou	p.															

22.2.19 CH[7].TEP

Address offset: 0x54C Channel 7 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α Α	Δ Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	to	tas	k re	gist	er.	Acc	epts	on	ly a	ddr	ess	es t	o re	egis	ters	5				

from the Task group.

22.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 1	l8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	EEP										Poi	ntei	to	eve	ent i	regi	ster	. Ac	сер	ts o	nly	add	Ires	ses	to r	egi	iste	rs				

Pointer to event register. Accepts only addresses to registers from the Event group.

22.2.21 CH[8].TEP

Address offset: 0x554 Channel 8 task end-point



Bit	num	nbe	r		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Α
Res	et 0)x00	000000	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	
Id	R۱	W	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	R۱	W	TEP										Poi	nte	r to	tasl	k re	gist	er. /	Ассе	epts	onl	y a	ddre	esse	s to	o re	gist	ters					

from the Task group.

from the Event group.

22.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	L3 1	12 :	11 1	0 9) ;	8 7	7 (5 5	4	3	2	1 (
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A ,	A /	۱ ۸	Δ	\ <i>A</i>	Δ Δ	A	Α	Α	Α /	Ĺ
Res	et OxO	0x00000000 RW Field Value Id				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 0) (0	0	0	0	0 (
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			I
Α	RW	EEP										Poi	nte	r to	ev	ent	reg	iste	r. A	Ассе	pts	on	ly a	ddr	ess	es t	o re	gis	ters	5				

22.2.23 CH[9].TEP

Address offset: 0x55C Channel 9 task end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13	12 :	11 1	.0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	A A	A A	Α	Α	Α	Α	Α	Α.	Δ ,	A /	A	Α	Α	Α	Α	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otio	n																	
Α	RW	TEP										Poi	nte	r to	tasl	re	giste	r. A	cce	pts	onl	/ ad	dre	sses	to	regi	ster	S				
				Pointer to task register. Accepts only addresses to registers from the Task group.																												

22.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit n	umbe	er		31	30	29	28	27	7 26	5 25	24	23	22	21 2	20 1	19 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α.	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	4 А	Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	RW	EEP										Ро	inte	r to	eve	nt r	egis	ter	Ac	cept	s o	nly	add	res	ses	to i	egi	stei	s				
												fro	m t	he E	ver	nt gr	oun	١.															

22.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit r	umbe	r		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	9 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	. 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	Α Α	Δ /	4 Α	A /	Α Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	Д А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	r to	tasl	c re	gist	er.	Acc	ept	S 01	ıly a	dd	ress	es t	o re	egis	ter	5				

from the Task group.

22.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

from the Task group.

22.2.27 CH[11].TEP

Address offset: 0x56C Channel 11 task end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	.8 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 4	A /	A /	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 (
Id	Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0														n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er.	Acc	ept	s on	ly a	ddr	esse	es t	o re	gis	ters	5				

22.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 :	16 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1	C
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ
Res	Reset 0x00000000								0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	D	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	EEP										Poi	nte	r to	eve	ent	reg	iste	r. A	cce	pts	only	ad	dre	sses	s to	reg	giste	ers					_
												fro	m th	he F	Vei	nt σ	rou	n																

22.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α Α	Δ Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A ,	А А		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	to	tas	k re	gist	er.	Acc	epts	on	ly a	ddr	ess	es t	o re	egis	ters	5				

from the Task group.

22.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id	A A A A A A A A A A A A A A A A A A A	Α
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id RW Field Value Id	Value Description	
A RW EEP	Pointer to event register. Accepts only addresses to registers	

from the Event group.

22.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point



Bit	num	nbe	r		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	A A	Α
Res	et 0)x00	000000	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	
Id	R۱	W	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	R۱	W	TEP										Poi	nte	r to	tasl	k re	gist	er. /	Ассе	epts	onl	y a	ddre	esse	s to	o re	gist	ters					

from the Task group.

22.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bit r	umb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. 4	A
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	tio	n																		
Α	RW	EEP										Poi	nter	to	evei	nt r	egist	ter.	Acc	ept	s or	nly a	dd	res	ses	to	regi	iste	rs				
												fro	m th	ne E	vent	gr	oup.																

22.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 19	9 18	3 17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ΑД	A	Α	Α	Α	Α	Α	Α.	Δ Α	, Δ	A	A	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue							Des	crip	otio	n																	
Α	RW	TEP										Poi	ntei	r to	task	reg	iste	r. A	ccep	ots	only	ad	dres	ses	to	regi	ster	s				
												froi	m th	ne T	askı	rnı	ın															

22.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20	19 :	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	EEP										Poi	nter	to	eve	ent	reg	iste	r. A	Acce	pts	s or	ıly a	add	res	ses	to	reg	iste	ers				

22.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bit r	umbe	r		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	9 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	. 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	Α Α	Δ /	4 Α	A /	Α Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	Д А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	r to	tasl	c re	gist	er.	Acc	ept	S 01	ıly a	dd	ress	es t	o re	egis	ter	5				

from the Task group.

from the Event group.

22.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point



Bit	nur	mbe	r		31	30 2	9 2	28 2	27 2	26 2	25	24	23 2	22 2	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id					Α	Α	Д	Α	Α ,	Α	Α	Α	Α	Α	Α.	A A	A /	A	A	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α.	A A	A A	Α.	Α
Res	et	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	R	RW	Field	Value Id	Val	lue							Des	crip	otio	n																		
Α	R	RW	EEP										Poir	nter	to	eve	nt r	egis	ter	. Ac	cep	ts o	nly a	add	ress	ses	to r	regi	ste	rs				

from the Event group.

22.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	15 1	L4 1	13 1	L2 1	.1 :	10 9	9 8	3 7	· 6	5	4	3	2	1	C
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	A	Α.	A ,	Δ.	A A	Δ ,	Δ Α		A	. A	Α	Α	Α	Δ
Res	t OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	D
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Ро	inte	r to	tas	k re	gis	ter.	Ac	сер	ts c	nly	ad	dre	sses	to	reg	iste	rs					
												fro	m t	he ⁻	Γask	gro	oup																	

22.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 1	9 1	.8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	ДД	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																		
Α	RW	EEP										Poi	ntei	r to	eve	nt i	regis	ter	. Ac	cept	s o	nly a	add	ress	ses	to	reg	iste	rs				
												fro	m th	ne F	ven	t ør	ากเมา																

22.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit r	umbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	TEP		Pointer to task register. Accepts only addresses to registers

from the Task group.

22.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	A /	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	EEP										Poi	nter	to	eve	ent i	regi	ster	. Ac	cep	ts c	nly	ado	Ires	ses	to	egi	iste	rs				

from the Event group.

22.2.41 CH[18].TEP

Address offset: 0x5A4

Channel 18 task end-point



Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	18 1	17 1	16 1	15 1	L4 1	13 1	.2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	Α,	Α.	Α.	A A	Δ,	Δ Δ	. A	Α	Α	Α	Α	Α	Α	A	А А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	ntei	r to	tas	k re	gist	ter.	Ac	сер	ts c	nly	ad	dres	ses	to r	egis	ter	s				

from the Task group.

22.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 :	17 1	16 :	15 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	Δ ,	A /	. 4	A	Α	Α	Α	Α	Α	Α	A A	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	EEP										Poi	nte	r to	eve	ent	reg	iste	r. A	Acce	pts	onl	y ac	ddre	sses	to	reg	iste	rs				

Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.43 CH[19].TEP

Address offset: 0x5AC Channel 19 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 1	.9 :	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Д	A A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	А А
Re	set 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	TEP										Poi	inte	r to	tas	k re	gist	er.	Acce	epts	on	ly a	ddr	ess	es t	o re	egis	ters	5				

from the Task group.

22.2.44 CHG[0]

Address offset: 0x800 Channel group 0

Bit	numbe	er		31	30 2	29 2	8 2	7 26	6 25	5 24	4 23	3 22	2 21	1 20	0 19	18	3 17	16	15	14	13	12 1	.1 10	9	8	7	6 5	5 4	. 3	2	1 0
Id				f	е	d (c b	a	Z	. Y	X	(W	V V	U	ΙT	S	R	Q	Р	О	N	М	L K	J	1	Н	G I	- E	D	С	ВА
Res	et 0x0	0000000		0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						D	esci	ript	ion	1																
Α	RW	CH0									In	ıclu	de c	or e	exclu	ıde	cha	ann	el 0												
			Excluded	0							E>	xclu	ıde																		
			Included	1							In	ıclu	de																		
В	RW	CH1									In	ıclu	de c	or e	exclu	ude	cha	ann	el 1												
			Excluded	0							E>	xclu	ıde																		
			Included	1							In	ıclu	de																		
С	RW	CH2									In	ıclu	de c	or e	exclu	ıde	cha	ann	el 2												
			Excluded	0							E>	xclu	ıde																		
			Included	1							In	ıclu	de																		
D	RW	CH3									In	ıclu	de c	or e	exclu	ude	cha	ann	el 3												
			Excluded	0							E>	xclu	ıde																		
			Included	1							In	ıclu	de																		
Е	RW	CH4									In	ıclu	de c	or e	exclu	ıde	cha	ann	el 4												
			Excluded	0							E>	xclu	ıde																		
			Included	1							In	ıclu	de																		
F	RW	CH5									In	ıclu	de c	or e	exclu	ude	cha	ann	el 5												
			Excluded	0							Ex	xclu	ide																		
			Included	1							In	ıclu	de																		
G	RW	CH6									In	clu	de c	or e	exclu	ıde	cha	ann	el 6												



Bit r	umb	er		31 30	29 2	28 27	7 26 2	25 24	1 23	22 21 3	20 19 :	18 17	7 16	15	14 13	3 12 1	.1 10	9	8 7	7 (5 5	4	3 2	1 (
Id				f e	d	c b	а	Z Y	Χ	w v	U T	S R	Q	Р	O N	М	L K	J	T F	1 (3 F	Ε	D C	B A
Res	et OxC	0000000		0 0	0	0 0	0	0 0	0	0 0	0 0	0 0	0	0	0 0	0	0 0	0	0 () (0	0	0 0	0 0
Id	RW	Field	Value Id	Value	•				De	scriptio	n													
			Excluded	0					Exc	clude														
			Included	1						lude														
Н	RW	CH7								lude or	exclud	le cha	ann	el 7										
			Excluded	0						clude														
	DIA	CHO	Included	1						lude lude or				-10										
I	KVV	CH8	Excluded	0						clude or	exclud	ie cha	ann	ei 8										
			Included	1						lude														
J	RW	CH9	o.uucu	_						lude or	exclud	le cha	ann	el 9										
			Excluded	0					Exc	clude														
			Included	1					Inc	lude														
K	RW	CH10							Inc	lude or	exclud	le cha	ann	el 10	1									
			Excluded	0					Exc	clude														
			Included	1					Inc	lude														
L	RW	CH11							Inc	lude or	exclud	le cha	ann	el 11										
			Excluded	0					Exc	clude														
			Included	1						lude														
M	RW	CH12								lude or	exclud	le cha	ann	el 12										
			Excluded	0						clude														
	DIA	01143	Included	1						lude				140										
N	RW	CH13	Evaludad	0						lude or	exclud	le cha	ann	el 13										
			Excluded Included	1						clude clude														
0	RW/	CH14	included	1						lude or	excluc	le cha	ann	el 14										
		0.11	Excluded	0						clude	CACIGO													
			Included	1						lude														
Р	RW	CH15							Inc	lude or	exclud	le cha	ann	el 15										
			Excluded	0					Exc	clude														
			Included	1					Inc	lude														
Q	RW	CH16							Inc	lude or	exclud	le cha	ann	el 16										
			Excluded	0					Exc	clude														
			Included	1						lude														
R	RW	CH17								lude or	exclud	le cha	ann	el 17	'									
			Excluded	0						clude														
_	D\A/	CU10	Included	1						lude lude or	ovelue	ام ماء		al 10	,									
S	KVV	CH18	Excluded	0						clude or	exclud	ie ch	amn	61 10	'									
			Included	1						lude														
Т	RW	CH19		_						lude or	exclud	le cha	ann	el 19	1									
			Excluded	0					Exc	clude														
			Included	1					Inc	lude														
U	RW	CH20							Inc	lude or	exclud	le cha	ann	el 20										
			Excluded	0					Exc	clude														
			Included	1					Inc	lude														
V	RW	CH21							Inc	lude or	exclud	le cha	ann	el 21										
			Excluded	0						clude														
			Included	1						lude														
W	RW	CH22	5 1 1 1	0						lude or	exclud	le cha	ann	el 22										
			Excluded	0						clude														
V	D\A/	CH33	Included	1						lude or	ovel	ام داء	an-	ol 22										
X	KVV	CH23	Excluded	0						lude or clude	excluc	ie cna	ariri	ei Ză										
			Included	1						lude														
Υ	RW	CH24		•						lude or	exclud	le cha	ann	el 24										
•			Excluded	0						clude		110		- -1										
				-																				



Bit	numbe	er		31 30	29	28	27 26	25 2	4 23	3 22	21	20 19	9 18	3 17	16	15 :	14 1	3 12	2 11	10	9	8 7	6	5	4	3 2	1	0
Id				f e	d	С	b a	Z '	ΥX	w	٧	U T	S	R	Q	Р	0 N	I M	l L	K	J	ΙН	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0 (0 0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	е				D	escri	iptic	on																
			Included	1					ln	clud	e																	
Z	RW	CH25							In	clud	e or	excl	ude	cha	nne	1 25												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
а	RW	CH26							In	clud	e or	excl	ude	cha	nne	1 26												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
b	RW	CH27							In	clud	e or	excl	ude	cha	nne	1 27												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
С	RW	CH28							In	clud	e or	excl	ude	cha	nne	1 28												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
d	RW	CH29							In	clud	e or	excl	ude	cha	nne	1 29												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
е	RW	CH30							In	clud	e or	excl	ude	cha	nne	1 30												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
f	RW	CH31							In	clud	e or	excl	ude	cha	nne	131												
			Excluded	0					Ex	kclud	le																	
			Included	1					In	clud	e																	
1	KVV	CH31							Ex	kclud	le	exci	uue	CIId	nne	:1 31												

22.2.45 CHG[1]

Address offset: 0x804

Channel group 1

Bit r	numbe	er		31	1 30	29	28	27 2	26 2	25 2	4 2	23 2	22 21	1 2	0 19	18	3 17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4 3	2	1	0
Id													w v																			
	et 0x0	0000000											0 0																			
Id	RW	Field	Value Id	Va	alue						D	es	cript	ior	1																	
Α	RW	CH0									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 0													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
В	RW	CH1									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 1													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
С	RW	CH2									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 2													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
D	RW	CH3									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 3													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
Е	RW	CH4									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 4													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
F	RW	CH5									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 5													
			Excluded	0							Ε	xcl	lude																			
			Included	1							Ir	ncl	ude																			
G	RW	CH6									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 6													
			Excluded	0							Е	xcl	lude																			
			Included	1							Ir	ncl	ude																			
Н	RW	CH7									Ir	ncl	ude d	or e	exclu	ıde	cha	nn	el 7													
			Excluded	0							Е	xcl	lude																			



Bit r	umb	er		31 30	29	28 2	7 26	25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 C
Id				f e	d	c l	о а	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et OxC	0000000		0 0	0	0 (0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	9				Description
			Included	1					Include
I	RW	CH8							Include or exclude channel 8
			Excluded	0					Exclude
			Included	1					Include
J	RW	CH9							Include or exclude channel 9
			Excluded	0					Exclude
			Included	1					Include
K	RW	CH10							Include or exclude channel 10
			Excluded	0					Exclude
			Included	1					Include
L	RW	CH11							Include or exclude channel 11
			Excluded	0					Exclude
			Included	1					Include
М	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
			Included	1					Include
Р	RW	CH15							Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16							Include or exclude channel 16
			Excluded	0					Exclude
			Included	1					Include
R	RW	CH17							Include or exclude channel 17
			Excluded	0					Exclude
			Included	1					Include
S	RW	CH18							Include or exclude channel 18
			Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19							Include or exclude channel 19
			Excluded	0					Exclude
		0.100	Included	1					Include
U	RW	CH20		•					Include or exclude channel 20
			Excluded	0					Exclude
.,	Dia	CU24	Included	1					Include
V	KW	CH21	Fuelude d	0					Include or exclude channel 21
			Excluded	0					Exclude
147	Divi	CU22	Included	1					Include
W	кW	CH22	Evaludad	0					Include or exclude channel 22
			Excluded	0					Exclude
V	DIA	CH33	Included	1					Include
Χ	KW	CH23	Evaludad	0					Include or exclude channel 23
			Excluded	0					Exclude
V	Divi	CU24	Included	1					Include
Υ	ĸW	CH24	Evaludad	0					Include or exclude channel 24
			Excluded	0					Exclude
,	D: 1	CURE	Included	1					Include
Z	RW	CH25	5 1 1 1	0					Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
a RW CH26		Include or exclude channel 26
	Excluded	0 Exclude
	Included	1 Include
b RW CH27		Include or exclude channel 27
	Excluded	0 Exclude
	Included	1 Include
c RW CH28		Include or exclude channel 28
	Excluded	0 Exclude
	Included	1 Include
d RW CH29		Include or exclude channel 29
	Excluded	0 Exclude
	Included	1 Include
e RW CH30		Include or exclude channel 30
	Excluded	0 Exclude
	Included	1 Include
f RW CH31		Include or exclude channel 31
	Excluded	0 Exclude
	Included	1 Include

22.2.46 CHG[2]

Address offset: 0x808 Channel group 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW CHO	10000	Include or exclude channel 0
	Excluded	0 Exclude
	Included	1 Include
B RW CH1		Include or exclude channel 1
	Excluded	0 Exclude
	Included	1 Include
C RW CH2		Include or exclude channel 2
	Excluded	0 Exclude
	Included	1 Include
D RW CH3		Include or exclude channel 3
	Excluded	0 Exclude
	Included	1 Include
E RW CH4		Include or exclude channel 4
	Excluded	0 Exclude
	Included	1 Include
F RW CH5		Include or exclude channel 5
	Excluded	0 Exclude
	Included	1 Include
G RW CH6		Include or exclude channel 6
	Excluded	0 Exclude
	Included	1 Include
H RW CH7		Include or exclude channel 7
	Excluded	0 Exclude
	Included	1 Include
I RW CH8		Include or exclude channel 8
	Excluded	0 Exclude
	Included	1 Include



Bit r	numbe	er		31 30	29 28	27 26	25 24	
Id				f e	d c	b a	ΖY	Y X W V U T S R Q P O N M L K J I H G F E D C B /
Res	et 0 x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
J	RW	CH9						Include or exclude channel 9
			Excluded	0				Exclude
			Included	1				Include
K	RW	CH10						Include or exclude channel 10
			Excluded	0				Exclude
			Included	1				Include
L	RW	CH11						Include or exclude channel 11
			Excluded	0				Exclude
		2112	Included	1				Include
M	RW	CH12	5 1 1 1					Include or exclude channel 12
			Excluded	0				Exclude
N.	DIA	CUA2	Included	1				Include
N	KVV	CH13	Evaludad	0				Include or exclude channel 13
			Excluded Included					Exclude Include
0	D\A/	CH14	iliciadea	1				Include or exclude channel 14
U	NVV	CH14	Excluded	0				Exclude
			Included	1				Include
Р	R\M	CH15	included	1				Include or exclude channel 15
	11.00	CITIS	Excluded	0				Exclude
			Included	1				Include
Q	RW	CH16	moladed	-				Include or exclude channel 16
			Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
			Included	1				Include
S	RW	CH18						Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
			Included	1				Include
U	RW	CH20						Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
V	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Х	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
V	DIA	CH34	Included	1				Include
Υ	KW	CH24	Evaludad	0				Include or exclude channel 24
			Excluded	0				Exclude Include
Z	D\A/	CH25	Included	1				Include Include or exclude channel 25
_	KVV	CI123	Excluded	0				Exclude
			Included	1				Include
a	R\M	CH26	melaucu	1				Include or exclude channel 26
u		5.120	Excluded	0				Exclude
			Included	1				Include
b	RW	CH27		_				Include or exclude channel 27



Bit	numb	er		31	30	29	28 2	27 2	26 2	25 2	24 2	3 22	2 21	20	19	18	17	16	15	14 :	13 1	2 11	10	9	8	7	6	5 4	1 3	2	1	0
Id				f	е	d	С	b	a :	Ζ	Y X	(W	/ V	U	Т	S	R	Q	Р	О	N N	1 L	K	J	1	Н	G	F I	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
			Excluded	0							E	xclu	de																			
			Included	1							In	ıclu	de																			
С	RW	CH28									In	ıclu	de o	r ex	clu	de c	hai	nne	1 28	3												
			Excluded	0							E	xclu	de																			
			Included	1							In	ıclu	de																			
d	RW	CH29									In	ıclu	de o	r ex	clu	de c	chai	nne	1 29)												
			Excluded	0							E	xclu	de																			
			Included	1							In	ıclu	de																			
е	RW	CH30									In	ıclu	de o	r ex	clu	de c	hai	nne	130)												
			Excluded	0							E	xclu	de																			
			Included	1							In	ıclu	de																			
f	RW	CH31									In	ıclu	de o	r ex	clu	de c	chai	nne	l 31													
			Excluded	0							E	xclu	de																			
			Included	1							In	ıclu	de																			

22.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
ld	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	
ld RW Field Value Id	Value Description
A RW CHO	Include or exclude channel 0
Excluded	0 Exclude
Included	1 Include
B RW CH1	Include or exclude channel 1
Excluded	0 Exclude
Included	1 Include
C RW CH2	Include or exclude channel 2
Excluded	0 Exclude
Included	1 Include
D RW CH3	Include or exclude channel 3
Excluded	0 Exclude
Included	1 Include
E RW CH4	Include or exclude channel 4
Excluded	0 Exclude
Included	1 Include
F RW CH5	Include or exclude channel 5
Excluded	0 Exclude
Included	1 Include
G RW CH6	Include or exclude channel 6
Excluded	0 Exclude
Included	1 Include
H RW CH7	Include or exclude channel 7
Excluded	0 Exclude
Included	1 Include
I RW CH8	Include or exclude channel 8
Excluded	0 Exclude
Included	1 Include
J RW CH9	Include or exclude channel 9
Excluded	0 Exclude
Included	1 Include
K RW CH10	Include or exclude channel 10



Excluded 0 Exclude Included 1 Include Y RW CH24 Include or exclude channel 24 Excluded 0 Exclude Include Include	Bit n	umbe	er		31 30	29 28	27 26	25 24	23 22 21	20 19	18 17	16	15 14	13 1	2 11	10	9 8	7	6 5	5 4	3 2	1 0
	Id				f e	d c	b a	ΖY	x w v	U T	S R	Q	РО	N N	1 L	K	JI	Н	G I	E	D C	ВА
	Rese	t 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0	0 0	0 0	0	0 0	0 (0	0	0 0	0	0 (0	0 0	0 0
	Id	RW	Field	Value Id	Value				Descripti	on												
L RW CH112 Excluded 0 Excluded M RW CH12 Included 1 Included M RW CH12 Evaluated 0 Excluded N BW CH13 Included 1 Included N BW CH13 Included 0 Excluded O RW CH14 Included 1 Included O RW CH15 Included 1 Included P RW CH15 Included 1 Included Q RW CH16 Excluded 0 Excluded Q RW CH16 Excluded 0 Excluded Q RW CH17 Excluded 0 Excluded Q RW CH18 Included 1 Included S RW CH19 Included 1 Included Y RW CH19				Excluded	0				Exclude													
				Included	1				Include													
	L	RW	CH11						Include o	r exclud	de cha	nne	11									
M RW CH12 Excluded 0 Excluded N Included 1 included 1 recluded N RW CH3 Excluded 0 Excluded 0 Excluded N RW CH14 Included 1 included 2 included				Excluded	0				Exclude													
				Included	1				Include													
No.	M	RW	CH12						Include o	r exclud	de cha	nne	12									
No. RWL PL3 Excluded 0 Exclude controlled channel 13 0 No. RWL CH14 1 Included 0 No. RWL CH14 1 Included 0 No. RWL CH15 Excluded 0 Exclude or exclude channel 15 0 No. RWL CH15 Included 1 Include or exclude channel 15 0 No. RWL CH16 1 Include or exclude channel 16 0 No. RWL CH17 Included 0 Exclude 0 No. RWL CH18 Included 0 Exclude Or exclude channel 17 0 No. RWL CH19 Included 0 Exclude Or exclude channel 18 0 No. RWL CH19 Included 0 Exclude Or exclude channel 19 0 No. RWL CH29 Included 0 Exclude Or exclude channel 20																						
Part				Included	1																	
	N	RW	CH13							r exclud	de cha	anne	13									
O RW RV L144 Excluded (included) 1 concluded (included) 2 concluded (included) 3 concluded (incl																						
P	0	D\A/	CH14	included	1					r ovelu	do cha	nno	111									
	U	NVV	CH14	Evoluded	0					i exciuc	ue ciio	iiiie	1 14									
P RW R																						
	Р	RW	CH15	meladea	_					r exclud	de cha	nne	l 15									
				Excluded	0					CACIO	0110											
Q RW File Framework Framew																						
	Q	RW	CH16							r exclud	de cha	nne	16									
R RW Land Excluded (included) 0 Exclude (included) S RW Land Ch18 (included) 1 Include or exclude channel 18 S RW Land Excluded (included) 0 Excluded T Land Excluded (included) 1 Include or exclude channel 19 T Land Excluded (included) 1 Include or exclude channel 19 Land Excluded (included) 1 Included or exclude channel 20 Land Excluded (included) 1 Included or exclude channel 20 Land Excluded (included) 1 Included or exclude channel 21 Land Excluded (included) 2 Excluded (channel 22) Land Excluded (included) 2 Excluded (channel 23) Land Excluded (included) 2 Excluded (included) 2 Land Excluded (included) 3 Included (included) 3 Land Excluded (included) 3 Included (included) 4 Land Excluded (included) 3 Included (included)				Excluded	0				Exclude													
				Included	1				Include													
	R	RW	CH17						Include o	r exclud	de cha	anne	17									
S RW Label Excluded (ncluded) 1 (nclude or exclude channel 18) T RW Label Excluded (ncluded) 1 (nclude or exclude channel 19) T RW Label Excluded (ncluded) 0 (nclude or exclude channel 19) T RW Label Excluded (nclude or exclude channel 20) RW Label Excluded (nclude or exclude channel 20) RW Label Excluded (nclude or exclude channel 20) RW Label Excluded (nclude or exclude channel 21) RW Label Excluded (nclude or exclude channel 21) RW Label Excluded (nclude or exclude channel 22) RW Label Excluded (nclude or exclude channel 22) RW Label Excluded (nclude or exclude channel 23) RW Label Excluded (nclude or exclude channel 23) RW Label Excluded (nclude or exclude channel 24) RW Label Excluded (nclude or exclude channel 24) RW Label Excluded (nclude or exclude channel 25) RW Label Excluded (nclude or exclude channel 26) RW Label Excluded (nclude or exclude channel 26) RW Label Excluded (nclude or exclude channel 26) RW Label <t< td=""><td></td><td></td><td></td><td>Excluded</td><td>0</td><td></td><td></td><td></td><td>Exclude</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>				Excluded	0				Exclude													
				Included	1				Include													
RW	S	RW	CH18						Include o	r exclud	de cha	anne	18									
T RW CH19 Excluded 0 Exclude U RW CH20 Excluded 1 Include or exclude channel 20 U RW CH20 Excluded 0 Exclude Included 1 Include Include V RW CH21 Excluded 0 Exclude Included 1 Include Include Included 1 Include Included 1 Include Included 1 Include or exclude channel 22 Excluded 0 Exclude Included 1 Include or exclude channel 23 Excluded 0 Exclude Included 1 Include Include 1 Include Include 1 Include Excluded 0 Exclude Include 1 Include Include 1 Include Include 2 Exclude <td></td> <td></td> <td></td> <td>Excluded</td> <td>0</td> <td></td> <td></td> <td></td> <td>Exclude</td> <td></td>				Excluded	0				Exclude													
				Included	1																	
Name	Т	RW	CH19							r exclud	de cha	anne	19									
Nation N																						
RW PW		DIA	CU20	Included	1								120									
No.	U	KVV	CH2U	Evaludad	0					rexciud	ue cna	mne	1 20									
Note																						
RW PW	V	RW	CH21		_					r exclud	de cha	anne	21									
No. May No.				Excluded	0																	
X EXUMENT EXCLUDE EXCLUDE EXCLUDE Include or exclude channel 23 Include or exclude channel 24 Include or exclude channel 25 Include or exclude channel 25 Include or exclude channel 25 Include or exclude channel 26 Include or exclude channel 27 Include or exclude channel 28 Include or exclude chann																						
X RW CH23 Excluded 0 Exclude Y RW CH24 Excluded 0 Exclude Y RW CH24 Included or exclude channel 24 Y Excluded 0 Exclude Include or exclude channel 24 Include or exclude channel 24 Included 1 Include or exclude channel 25 Included or exclude channel 25 Excluded 0 Include or exclude channel 26 Excluded Include or exclude channel 26 Excluded Include or exclude channel 27 Include or exclude channel 27 Include or exclude channel 27 Excluded Include or exclude channel 28 Include or exclude channel 27 Included 1 Include or exclude channel 27 Include or exclude channel 27 Include or exclude channel 28	W	RW	CH22						Include o	r exclud	de cha	nne	122									
X RW LH23 Excluded Included 0 Exclude Exclu				Excluded	0				Exclude													
Excluded 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				Included	1				Include													
Y RW PART PART PART PART PART PART PART PART	Χ	RW	CH23						Include o	r exclud	de cha	anne	123									
Y RW CH24 Excluded 0 Exclude Z RW CH25 Included 1 Include or exclude channel 25 Z Excluded 0 Excluded Included 1 Include Include or exclude channel 25 Include Include or exclude channel 26 Excluded Include or exclude channel 26 Excluded Include or exclude channel 27 Excluded Include or exclude channel 28				Excluded	0				Exclude													
Excluded 0 Exclude Include Inc				Included	1				Include													
RW CH25	Υ	RW	CH24							r exclud	de cha	anne	124									
Z RW CH25 Excluded 0 Exclude a RW CH26 Included 1 Include a RW CH26 Excluded 0 Exclude b Excluded 0 Exclude b Include 1 Include c Excluded 0 Exclude b Include Exclude Include or exclude channel 27 Excluded 0 Exclude include Include Include c RW CH28 Include or exclude channel 28																						
RW CH27 Excluded 0 Exclude BW CH27 Excluded 0 Exclude BW CH27 Included 1 Include BW CH27 Included 1 Include or exclude channel 27 BW CH27 Excluded 0 Exclude BR Included 1 Include BR CH28 Included Include	_			Included	1																	
a RW LP26 Excluded Sciuded Sc	Z	RW	CH25	5 1 1 1	0					r exclud	de cha	anne	1 25									
a RW LP26 Excluded Excluded Included 0 Exclude Excluded Included Excluded Included Excluded Included Include or exclude channel 27 Include or exclude channel 27 Excluded Included Excluded Included Include or exclude channel 27 Include or exclude channel 28 Include or exclude channel 28 Include or exclude channel 28																						
Excluded O Exclude Included 1 Include Include or exclude channel 27 Include or exclude channel 27 Excluded 0 Exclude Include Include Include Include	2	B/V	CH26	included	1					r oveling	do cha	nno	126									
b RW CH27 Fxcluded 1 Include or exclude channel 27 Excluded Excluded 0 Exclude Included 1 Include c RW CH28 Include or exclude channel 28	a	11.00	CHZU	Fycluded	0					- EXCIU	ue Ulia	anne	20									
b RW CH27 Excluded 0 Exclude Excluded Included 1 Include c RW CH28 Include or exclude channel 28																						
Excluded 0 Exclude Included 1 Include Include Include or exclude channel 28	b	RW	CH27		-					r exclud	de cha	anne	127									
c RW CH28 Included 1 Include c RW CH28 Include or exclude channel 28				Excluded	0						5.10											
c RW CH28 Include or exclude channel 28																						
Excluded 0 Exclude	С	RW	CH28						Include o	r exclud	de cha	nne	128									
				Excluded	0				Exclude													



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Included	1 Include
d RW CH29		Include or exclude channel 29
	Excluded	0 Exclude
	Included	1 Include
e RW CH30		Include or exclude channel 30
	Excluded	0 Exclude
	Included	1 Include
f RW CH31		Include or exclude channel 31
	Excluded	0 Exclude
	Included	1 Include

22.2.48 CHG[4]

Address offset: 0x810 Channel group 4

	uiil	iei group -																												
Bit	numb	er		31	30	29 2	28 2	27 2	6 2	25 2	4 2	23 22 21	20 1	19 1	8 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5 4	3	2	1	0
Id				f	е	d	С	b a	a i	Z Y	′ :	X W V	U	T 9	R	Q	Р	0	Ν	M I	. K	J	1	Н	G	F E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0 (0 (0 0) (0 0 0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Val	ue						0	Description	on																	
Α	RW	CH0									li	nclude o	r exc	lude	ch	ann	el 0													
			Excluded	0							Е	Exclude																		
			Included	1							li	nclude																		
В	RW	CH1									li	nclude o	r exc	lude	ch	ann	el 1													
			Excluded	0							Е	Exclude																		
			Included	1							li	nclude																		
С	RW	CH2									li	nclude o	r exc	lude	ch:	ann	el 2													
			Excluded	0							Е	Exclude																		
			Included	1							I	nclude																		
D	RW	CH3									li	nclude o	r exc	lude	ch:	ann	el 3													
			Excluded	0							Е	Exclude																		
			Included	1							li	nclude																		
Е	RW	CH4									li	nclude o	r exc	lude	ch	ann	el 4													
			Excluded	0							Е	Exclude																		
			Included	1							li	nclude																		
F	RW	CH5									li	nclude o	r exc	lude	ch	ann	el 5													
			Excluded	0							Е	Exclude																		
			Included	1							li	nclude																		
G	RW	CH6									li	nclude o	r exc	lude	ch	ann	el 6													
			Excluded	0								Exclude																		
			Included	1								nclude																		
Н	RW	CH7										nclude o	r exc	lude	ch	ann	el 7													
			Excluded	0								Exclude																		
			Included	1								nclude																		
I	RW	CH8										nclude o	r exc	lude	ch:	ann	el 8													
			Excluded	0								Exclude																		
			Included	1								nclude																		
J	RW	CH9										nclude o	r exc	lude	ch:	ann	el 9													
			Excluded	0								Exclude																		
			Included	1								nclude		. ,																
K	КW	CH10	5 1 1 1	•								nclude o	r exc	iude	ch	ann	ei 1	U												
			Excluded	0								Exclude																		
	Dicc	CUIA	Included	1								nclude					. 1.0													
L	RW	CH11	5 1 1 1	•								nclude o	r exc	iude	ch	ann	ei 1	1												
			Excluded	0							E	Exclude																		



	umbe	er		31 30	29 2	8 27	26 2	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res		0000000				0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Included	1					Include
М	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
			Included	1					Include
Р	RW	CH15							Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16							Include or exclude channel 16
			Excluded	0					Exclude
			Included	1					Include
R	RW	CH17							Include or exclude channel 17
			Excluded	0					Exclude
			Included	1					Include
S	RW	CH18	moradea	-					Include or exclude channel 18
,		C1110	Excluded	0					Exclude
			Included	1					Include
Т	D\A/	CH19	melaucu	_					Include or exclude channel 19
	11.00	CITIS	Excluded	0					Exclude
			Included	1					Include
U	D\A/	CH20	iliciadea	1					Include or exclude channel 20
U	NVV	CH20	Evaluded	0					Exclude
			Excluded						Include
.,	DVA	CU24	Included	1					
V	KVV	CH21	Fueluded	0					Include or exclude channel 21
			Excluded	0					Exclude
		01100	Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Χ	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
а	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27							Include or exclude channel 27
			Excluded	0					Exclude
			Included	1					Include
С	RW	CH28							Include or exclude channel 28
			Excluded	0					Exclude
			Included	1					Include
d	RW	CH29							Include or exclude channel 29
			Excluded	0					Exclude
			Included	1					Include



Bit	numbe	er		31	30 2	29	28	27	26 2	5 2	24 2	3 2	2 21	. 20	19	18	17	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id				f	е	d	С	b	a Z	Z	Υ)	< V	V V	U	Т	S	R	Q	Р (1 C	N N	l L	K	J	1	Н	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	ion																		
е	RW	CH30									Ir	nclu	de c	r ex	clu	de	chai	nne	130													
			Excluded	0							Е	xclu	ıde																			
			Included	1							Ir	nclu	de																			
f	RW	CH31									Ir	nclu	de c	r ex	kclu	de	chai	nne	l 31													
			Excluded	0							Е	xclu	ıde																			
			Included	1							Ir	nclu	de																			

22.2.49 CHG[5]

Address offset: 0x814
Channel group 5

Cn	ann	nel group 5																											
Bit	numb	er		31	30 2	9 28	27 2	26 2	5 24	1 23	3 22 2:	1 20	19	18	17	16	15	14 1	L3 1	2 11	l 10	9	8	7 (5 5	4	3	2	1 0
Id				f	e (d c	b	a Z	ΖY	X	wv	/ U	Т	S	R	Q	Р	0	N N	ЛL	K	J	1 1	1 (3 F	Ε	D	С	ВА
Res	et 0x0	00000000		0	0 (0 0	0	0 (0 0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue					De	escript	ion																	
Α	RW	CH0								In	clude	or e	xclu	de (char	nne	10												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
В	RW	CH1								In	clude	or e	xclu	de (char	nne	11												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
С	RW	CH2								In	clude	or e	xclu	de (char	nne	12												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
D	RW	CH3								In	clude	or e	xclu	de (char	nne	13												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
Е	RW	CH4								In	clude (or e	xclu	de (char	nne	14												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
F	RW	CH5								In	ıclude	or e	xclu	de (char	nne	15												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
G	RW	CH6								In	clude	or e	xclu	de (char	nne	16												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
Н	RW	CH7								In	clude	or e	xclu	de (char	nne	17												
			Excluded	0						Ex	kclude																		
			Included	1						In	clude																		
I	RW	CH8								In	clude	or e	xclu	de (char	nne	18												
			Excluded	0						Ex	kclude																		
			Included	1							clude																		
J	RW	CH9								In	ıclude	or e	xclu	de (char	nne	19												
			Excluded	0						Ex	kclude																		
			Included	1							clude																		
K	RW	CH10								In	ıclude	or e	xclu	de (char	nne	110												
			Excluded	0						Ex	kclude																		
			Included	1							clude																		
L	RW	CH11									clude	or e	xclu	de (char	nne	l 11												
			Excluded	0							kclude																		
			Included	1							clude																		
M	RW	CH12									clude	or e	xclu	de (char	nne	l 12												
			Excluded	0							kclude																		
			Included	1						In	clude																		



Bit r	numbe	er		31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id				f e	d c	b a	Z Y	'X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
N	RW	CH13						Include or exclude channel 13
			Excluded	0				Exclude
			Included	1				Include
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
			Included	1				Include
Р	RW	CH15						Include or exclude channel 15
			Excluded	0				Exclude
0	DIA	CU16	Included	1				Include Include or exclude channel 16
Q	KVV	CH16	Excluded	0				Exclude
			Included	1				Include
R	R\M	CH17	included	1				Include or exclude channel 17
11	11.00	CIII	Excluded	0				Exclude
			Included	1				Include
S	RW	CH18	meladea	-				Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
			Included	1				Include
U	RW	CH20						Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
V	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Х	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
			Included	1				Include
Υ	RW	CH24						Include or exclude channel 24
			Excluded	0				Exclude
-	DIA	CURE	Included	1				Include
Z	KVV	CH25	Evaludad	0				Include or exclude channel 25 Exclude
			Excluded Included	1				Include
2	R\M	CH26	iliciadea	1				Include or exclude channel 26
а	11.44	0.120	Excluded	0				Exclude
			Included	1				Include
b	RW	CH27		_				Include or exclude channel 27
			Excluded	0				Exclude
			Included	1				Include
С	RW	CH28						Include or exclude channel 28
			Excluded	0				Exclude
			Included	1				Include
d	RW	CH29						Include or exclude channel 29
			Excluded	0				Exclude
			Included	1				Include
е	RW	CH30						Include or exclude channel 30
			Excluded	0				Exclude
			Included	1				Include
f	RW	CH31						Include or exclude channel 31



Bit numb	per		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	0
Id			f	е	d	С	b	а	Z	Υ	Х	W	V	U 1	Γ 5	S R	Q	P	О	Ν	М	L	K	J	1	Н	G	F	Ε	D	СВ	Α
Reset 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0
ld RW	/ Field	Value Id	Va	lue							Des	crip	otio	n																		
Id RW	/ Field	Value Id Excluded	Va 0	lue								s crip lude		n																		

22.2.50 FORK[0].TEP

Address offset: 0x910 Channel 0 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.51 FORK[1].TEP

Address offset: 0x914 Channel 1 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.52 FORK[2].TEP

Address offset: 0x918 Channel 2 task end-point

Bit r	numbe	er		31	30	29 :	28 2	27 2	6 2	5 24	1 23	22	21	20 1	.9 1	.8 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id				А	Α	Α	Α	A A	Α Α	4 A	. A	Α	Α	A	A A	А А	Α	Α	Α	A	Δ ,	4 A	Α	Α	Α	Α	Α	Α	A	Α Α	А А
Res	et 0x0	0000000		0	0	0	0	0 (0	0 0	0	0	0	0	0 (0 0	0	0	0	0) (0 0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																	
Α	RW	TEP									Ро	nte	r to	tasl	k re	giste	r														

22.2.53 FORK[3].TEP

Address offset: 0x91C Channel 3 task end-point

Bit number		31 30 29 28 27 2	$25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id		AAAAA	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description

A RW TEP Pointer to task register

22.2.54 FORK[4].TEP

Address offset: 0x920 Channel 4 task end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.55 FORK[5].TEP

Address offset: 0x924 Channel 5 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	1 2	20 1	9 1	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Δ	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	TEP										Poi	nter	to	task	re	giste	r															

22.2.56 FORK[6].TEP

Address offset: 0x928 Channel 6 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	l8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er															

22.2.57 FORK[7].TEP

Address offset: 0x92C Channel 7 task end-point

Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22	21	20 1	19 1	18 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α Α	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A A
Res	et 0x	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue							Des	cri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er															

22.2.58 FORK[8].TEP

Address offset: 0x930 Channel 8 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.59 FORK[9].TEP

Address offset: 0x934 Channel 9 task end-point

Bit number	31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A	A A A A A A A A A A	A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description	

A RW TEP Pointer to task register



22.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	.8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Α Α	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	A	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	r to	tasl	k re	gist	er															

22.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

В	Bit n	umb	er			31	30	29	28	27	26	25	24	23	22	21	20 2	19 1	18 1	.7 1	.6 1	.5 1	4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
le	d					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Δ,	Δ,	Δ ,	Δ,	4 Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	A	А А
R	Rese	t Ox	00000	0000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0 (0 0) (0	0	0	0	0	0	0	0	0	0 0
10	d	RW	Fiel	d	Value Id	Va	lue							De	scri	ptic	n																		
Δ	4	RW	TEP											Poi	nte	r to	tas	k re	gist	er															

22.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

В	it nı	umb	er		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	l8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Ic	ł				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A /	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Α	А А
R	ese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Ic	i	RW	Field	Value Id	Va	lue							Des	scri	otio	n																		
Α		RW	TEP										Poi	nte	r to	tas	k re	gist	er															

22.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit number		31 30 29 28	27 26 2	5 24 23	22 21	20 19	18 17	' 16 1	5 14	13 12	11 1	.0 9	8	7	6	5	4 3	3 2	1 0	
Id		A A A A	A A A	A A A	АА	A A	A A	Α /	4 А	A A	Α /	4 Α	Α	Α	Α	Α	A A	A A	АА	
Reset 0x0000	000	0 0 0 0	0 0 0	0 0	0 0	0 0	0 0	0 (0 0	0 0	0 (0 0	0	0	0	0	0 0	0	0 0	
Id RW Fie	d Value Id	Value		Do	escripti	on														
A RW TE				Po	inter t	o task i	egiste	er												

22.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	to	tas	k re	gist	er															

22.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit number		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id RW Field	Value Id	Va	alue							De	scri	ptic	on																				
A RW TEP										Ро	inte	er to	ta	sk r	egis	ster																	_

22.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number		31 3	30 2	9 28	27	26	25	24	23 2	22 2	21 2	0 19	9 18	3 17	16	15	14	13 :	12 1	.1 10	9	8	7	6	5	4	3 2	2 1	0
Id	,	Α.	A A	A	Α	Α	Α	Α	Α	Α.	A A	4 Α	A	Α	Α	Α	Α	Α	A	А А	Α	Α	Α	Α	Α	Α	A A	A А	Α
Reset 0x00000000	(0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0
Id RW Field Va	alue Id	Valu	ıe						Des	crip	tior	n																	

A RW TEP Pointer to task register



22.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	L4 1	13 1	.2 1	1 10) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	A ,	Δ Δ	Α	Α	Α	Α	Α	Α	Α.	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter															

22.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

В	it nı	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
lo	ł				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ą
R	ese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
le	ł	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α		RW	TEP										Poi	inte	er to	tas	sk re	egis	ter																	-

22.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TFP		Pointer to task register

22.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 1	11 10) 9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A /	A	Α	Α	Α	Α	Α	А А	Α	Α	Α	Α	Α	Α	Α.	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	TEP										Poi	nter	to	task	re	giste	r														

22.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	TEP		Pointer to task register

22.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16	15 1	L4 1	13 1	.2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α ,	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	А А
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0
d RW Field Value Id			lue							De	scri	ptic	on																		

A RW TEP Pointer to task register





23 RADIO — 2.4 GHz Radio

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps *Bluetooth*[®] low energy mode.

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 29: RADIO block diagram* on page 191 for details.

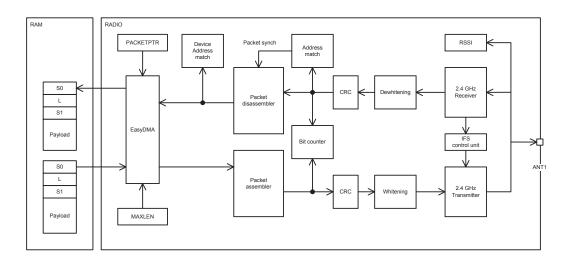


Figure 29: RADIO block diagram

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

23.1 EasyDMA

The RADIO peripheral uses EasyDMA for reading of data packets from and writing to RAM, without CPU involvement.

As illustrated in *Figure 29: RADIO block diagram* on page 191, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. This pointer should be reconfigured by the CPU each time before RADIO is started by the START task. If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The DISABLED event indicates that the EasyDMA has finished accessing the RAM.

The structure of a radio packet is described in detail in *Packet configuration* on page 192. The data that is stored in Data RAM and transported by EasyDMA consists of the following fields:

- S0
- LENGTH
- S1
- PAYLOAD

In addition, a static add-on is sent immediately after the payload.



The size of each of the above fields in the frame is configurable, and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen. For the field sizes defined in bits, the occupation in RAM will always be rounded up to the next full byte size (for instance 3 bit length will allocate 1 byte in RAM, 9 bit length will allocate 2 bytes, etc.).

The sizes of the fields S0, LENGTH and S1 can be individually configured by the S0LEN, LFLEN and S1LEN fields of the PCNF0 register respectively. The size of the payload is configured through the value in RAM corresponding to the LENGTH field. The size of the static add-on to the payload is configured through the STATLEN field in PCNF1 register.

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by the PCNF1.STATLEN and the LENGTH field in the packet specify a packet larger than MAXLEN, the payload will be truncated at MAXLEN. The packet's LENGTH field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

Important: Note that MAXLEN includes the size of the payload and the add-on, but excludes the size occupied by the fields S0, LENGTH and S1. This has to be taken into account when allocating RAM.

23.2 Packet configuration

RADIO packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

The content of a RADIO packet is illustrated in *Figure 30: On-air packet layout* on page 192. The RADIO sends the different fields in the packet in the order they are illustrated below, from left to right:



Figure 30: On-air packet layout

PREAMBLE is sent with least significant bit first on-air. For all modes that can be specified in the MODE register, the PREAMBLE is one byte long. If the first bit of the ADDRESS is 0, the PREAMBLE is set to 0xAA. Otherwise the PREAMBLE is set to 0x55.

Not shown in the figure above is the static payload add-on (the length of which is defined in PCNF1.STATLEN, and which is 0 bytes long in a standard BLE packet). The static payload add-on is sent between the PAYLOAD and CRC fields.

The RADIO packets are stored in memory, inside instances of a radio packet data structure as illustrated in *Figure 31: In-RAM representation of radio packet - S0, LENGTH and S1 are optional* on page 192. The PREAMBLE, ADDRESS and CRC fields are omitted in this data structure.

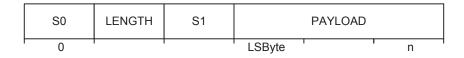


Figure 31: In-RAM representation of radio packet - S0, LENGTH and S1 are optional

The byte ordering on the air is always:



- Least significant byte first for the fields ADDRESS and PAYLOAD. The ADDRESS fields are also always transmitted and received least significant bit first on-air.
- Most significant byte first for the CRC field. The CRC field is also always transmitted and received most significant bit first.

The bit endianness, i.e. the order in which the bits are sent and received, is configured in PCNF1.ENDIAN for the fields S0, LENGTH, S1 and PAYLOAD.

The sizes of the fields S0, LENGTH and S1 can be individually configured in the S0LEN, LFLEN and S1LEN fields of the PCNF0 register respectively. If any of these fields are configured to be less than 8 bit long, the least significant bits of the fields are used, as seen from the RAM representation.

If S0, LENGTH or S1 are specified with zero length, their fields will be omitted in memory. Otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

23.3 Maximum packet length

Independent of the configuration of MAXLEN, the combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes.

23.4 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 36: Definition of logical addresses* on page 193.

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 36: Definition of logical addresses* on page 193.

Table 36: Definition of logical addresses

Logical address	Base address	Prefix byte	
0	BASE0	PREFIXO.APO	
1	BASE1	PREFIXO.AP1	
2	BASE1	PREFIXO.AP2	
3	BASE1	PREFIXO.AP3	
4	BASE1	PREFIX1.AP4	
5	BASE1	PREFIX1.AP5	
6	BASE1	PREFIX1.AP6	
7	BASE1	PREFIX1.AP7	

23.5 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.



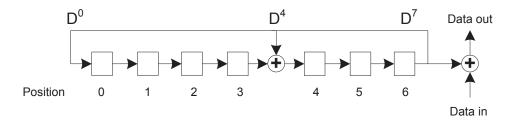


Figure 32: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 32: Data whitening and de-whitening* on page 194 can be initialised via the DATAWHITEIV register.

23.6 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 33: CRC generation of an n bit CRC* on page 194 where bit 0 in the CRCPOLY register corresponds to X^0 and bit 1 corresponds to X^1 etc. See CRCPOLY for more information.

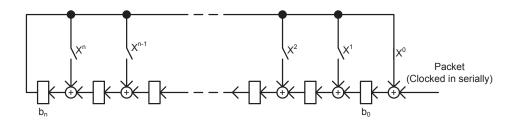


Figure 33: CRC generation of an n bit CRC

As illustrated in *Figure 33: CRC generation of an n bit CRC* on page 194, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.



The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

23.7 Radio states

The RADIO can enter a number of states.

The RADIO can enter the states described the table below. An overview state diagram for the RADIO is illustrated in *Figure 34: Radio states* on page 195. This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 34: Radio states* on page 195, the PAYLOAD event is always generated even if the payload is zero.

Table 37: RADIO state diagram

C	
State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISABLE	The radio is disabling the transmitter

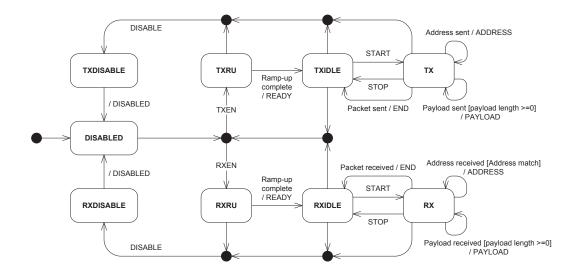


Figure 34: Radio states

23.8 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 34: Radio states* on page 195 and *Figure 35: Transmit sequence* on page 196. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 195 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

Figure 35: Transmit sequence on page 196 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in Figure 35: Transmit sequence on page 196



the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

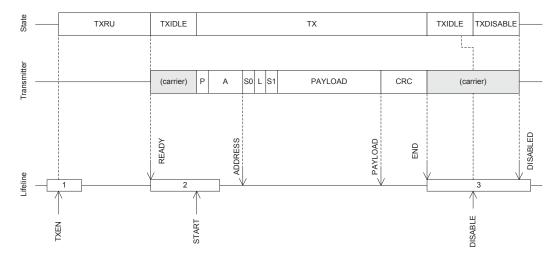


Figure 35: Transmit sequence

A slightly modified version of the transmit sequence from *Figure 35: Transmit sequence* on page 196 is illustrated in *Figure 36: Transmit sequence using shortcuts to avoid delays* on page 196 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

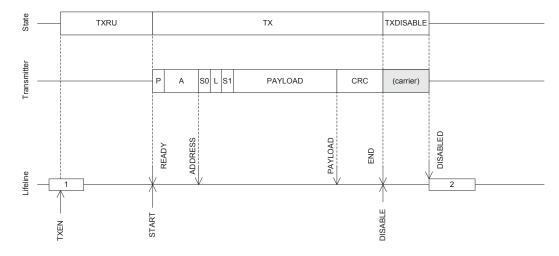


Figure 36: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 37: Transmission of multiple packets* on page 197.



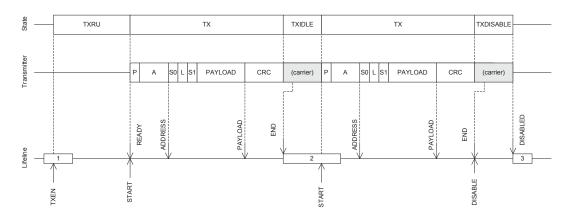


Figure 37: Transmission of multiple packets

23.9 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in *Figure 34: Radio states* on page 195 and *Figure 38: Receive sequence* on page 197. An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 195 the START task can, first be triggered after the RADIO has entered into the RXIDLE state.

Figure 38: Receive sequence on page 197 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated Figure 38: Receive sequence on page 197 the RADIO will be listening and possibly receiving undefined data, illustrated with an 'X', from START and until a packet with valid preamble (P) is received.

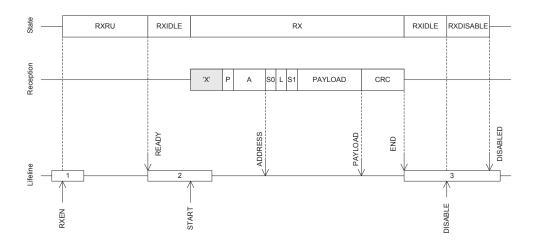


Figure 38: Receive sequence

A slightly modified version of the receive sequence from *Figure 38: Receive sequence* on page 197 is illustrated in *Figure 39: Receive sequence using shortcuts to avoid delays* on page 198 where the the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.



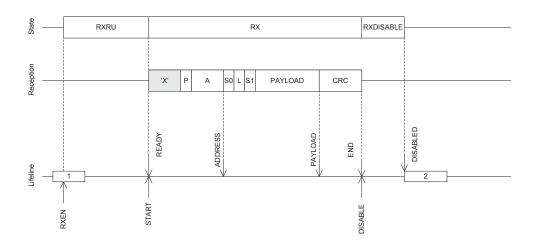


Figure 39: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated *Figure 40: Reception of multiple packets* on page 198.

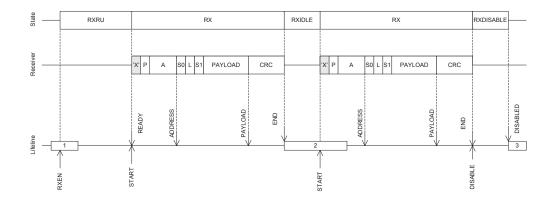


Figure 40: Reception of multiple packets

23.10 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by RSSI_{PERIOD}, see the device product specification for details. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

23.11 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this



interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turnaround time, i.e. the time needed to switch off the receiver, and switch back on the transmitter.

TIFS is only enforced if END_DISABLE and DISABLED_TXEN or END_DISABLE and DISABLED_RXEN shortcuts are enabled. TIFS is only qualified for use in BLE_1MBIT mode, and default ramp-up mode.

23.12 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

23.13 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.



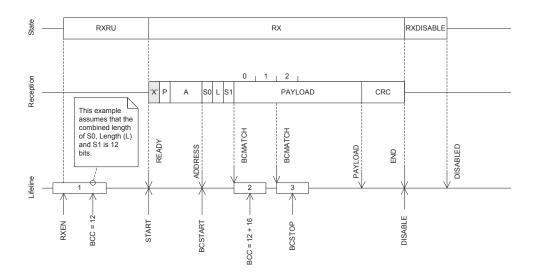


Figure 41: Bit counter example

23.14 Registers

Table 38: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40001000	RADIO	RADIO	2.4 GHz radio		

Table 39: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS_RXEN	0x004	Enable RADIO in RX mode
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete.
EVENTS_BCMATCH	0x128	Bit counter reached bit count value.
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
RXCRC	0x40C	CRC field of previously received packet



Register	Offset	Description	
DAI	0x410	Device address match index	
PACKETPTR	0x504	Packet pointer	
FREQUENCY	0x508	Frequency	
TXPOWER	0x50C	Output power	
MODE	0x510	Data rate and modulation	
PCNF0	0x514	Packet configuration register 0	
PCNF1	0x518	Packet configuration register 1	
BASE0	0x51C	Base address 0	
BASE1	0x520	Base address 1	
PREFIXO	0x524	Prefixes bytes for logical addresses 0-3	
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7	
TXADDRESS	0x52C	Transmit address select	
RXADDRESSES	0x530	Receive address select	
CRCCNF	0x534	CRC configuration	
CRCPOLY	0x538	CRC polynomial	
CRCINIT	0x53C	CRC initial value	
	0x540		Reserved
TIFS	0x544	Inter Frame Spacing in us	
RSSISAMPLE	0x548	RSSI sample	
STATE	0x550	Current radio state	
DATAWHITEIV	0x554	Data whitening initial value	
BCC	0x560	Bit counter compare	
DAB[0]	0x600	Device address base segment 0	
DAB[1]	0x604	Device address base segment 1	
DAB[2]	0x608	Device address base segment 2	
DAB[3]	0x60C	Device address base segment 3	
DAB[4]	0x610	Device address base segment 4	
DAB[5]	0x614	Device address base segment 5	
DAB[6]	0x618	Device address base segment 6	
DAB[7]	0x61C	Device address base segment 7	
DAP[0]	0x620	Device address prefix 0	
DAP[1]	0x624	Device address prefix 1	
DAP[2]	0x628	Device address prefix 2	
DAP[3]	0x62C	Device address prefix 3	
DAP[4]	0x630	Device address prefix 4	
DAP[5]	0x634	Device address prefix 5	
DAP[6]	0x638	Device address prefix 6	
DAP[7]	0x63C	Device address prefix 7	
DACNF	0x640	Device address match configuration	
MODECNF0	0x650	Radio mode configuration register 0	
POWER	0xFFC	Peripheral power control	

23.14.1 SHORTS

Address offset: 0x200

Shortcut register

Bit r	numbe	er		31	1 30	29	28	3 27	26	5 25	24	1 23	3 22	2 2 1	20	19	18	17	16	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Н		G	F	Ε	D (2	ВА
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Id	RW	Field	Value Id	Va	alue							De	escr	ripti	on																		
Α	RW	READY_START										Sh	ort	cut	betv	wee	n R	EAI	PΥ	ver	ıt aı	nd S	TAF	RT ta	isk								
												Se	e E	VEN	TS_	RE/	DY	an	d TA	\SK!	<u>_</u> S	ΓAR	Т										
			Disabled	0								Di	sab	le sl	nort	cut																	
			Enabled	1								En	nabl	e sh	orto	cut																	
В	RW	END_DISABLE										Sh	ort	cut	betv	wee	n E	ND	eve	nt a	and	DIS	ABL	E ta	sk								
												Se	e E	VEN	TS_	ENL) ar	nd 7	ASI	(S_I	DIS/	ABLE	Ε										



Bit r	numbe	er		31	30 2	29 2	8 27	7 26	25	24	23	3 22	21 2	20 19	18	17	16	15 1	4 13	3 12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																								Н		G	F	E C) C	В	Α
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	ptio	n																	
			Disabled	0							Dis	sabl	e sho	ortcu	ıt																
			Enabled	1							En	nable	sho	rtcu	t																
С	RW	DISABLED_TXEN									Sh	orto	ut be	etwe	en	DISA	BLE	D e	vent	and	KT b	ŒN	tasl	k							
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			Disabled	0										ortcu																	
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Ε	RW	ADDRESS_RSSISTART									Sh	orto	ut be	etwe	en	ADD	RES	s e	/ent	and	RS	SIST	AR	I ta	sk						
											Se	e EV	ENT.	S_AL	DDR	ESS	and	TA.	SKS_	RSS	IST	4RT									
			Disabled	0							Dis	sabl	e sho	ortcu	it																
			Enabled	1							En	nable	sho	rtcu	t																
F	RW	END_START									Sh	orto	ut be	etwe	en	END	eve	ent a	and S	STAI	RT t	ask									
											Se	e EV	ENT.	S_EI	VD a	and 1	TAS	KS_	STAR	?T											
			Disabled	0							Dis	sabl	e sho	ortcu	ıt																
			Enabled	1							En	nable	sho	rtcu	t																
G	RW	ADDRESS_BCSTART									Sh	orto	ut be	etwe	en .	ADD	RES	S e	/ent	and	ВС	STA	RT 1	task							
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			Disabled	0										ortcu																	
			Enabled	1							En	iable	sho	rtcu	τ																

23.14.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
A RW READY			Write '1' to Enable interrupt for READY event
			See EVENTS_READY
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ADDRESS			Write '1' to Enable interrupt for ADDRESS event
			See EVENTS_ADDRESS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW PAYLOAD			Write '1' to Enable interrupt for PAYLOAD event
			See EVENTS_PAYLOAD
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW END			Write '1' to Enable interrupt for END event



Bit number		31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	000000000000000000000000000000000000000
Id RW Field	Value Id	Value	Description
			See EVENTS_END
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW DISABLED			Write '1' to Enable interrupt for DISABLED event
			See EVENTS_DISABLED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW DEVMATCH			Write '1' to Enable interrupt for DEVMATCH event
			See EVENTS_DEVMATCH
	Set	1	Enable
	Disabled Enabled	0	Read: Disabled
G RW DEVMISS	Enabled	1	Read: Enabled Write '1' to Enable interrupt for DEVMISS event
G KW DEVIVIISS			write 1 to chable interrupt for Devivings event
			See EVENTS_DEVMISS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
H RW RSSIEND			Write '1' to Enable interrupt for RSSIEND event
			See EVENTS_RSSIEND
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
I RW BCMATCH			Write '1' to Enable interrupt for BCMATCH event
			See EVENTS_BCMATCH
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
J RW CRCOK			Write '1' to Enable interrupt for CRCOK event
			See EVENTS CRCOK
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
K RW CRCERROR			Write '1' to Enable interrupt for CRCERROR event
	Sot	1	See EVENTS_CRCERROR Enable
	Set Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

23.14.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22 2	1 2	0 1	9 1	8 17	7 16	5 15	14	13	12	11 1	0 9	8 6	7	6	5	4	3	2	1 ()
Id																					K	J				Н	G	F	Ε	D	С	ВА	A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																		
Α	RW	READY										Wri	te '1	' to	Dis	abl	e in	teri	rupt	for	REA	ADY	eve	nt									_
												See	EVE	NT.	S_R	EAL	DΥ																
			Clear	1								Disa	ble																				



Bit r	iumbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					K J I H G F E D C B A
Rese	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ADDRESS			Write '1' to Disable interrupt for ADDRESS event
					See EVENTS_ADDRESS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	PAYLOAD			Write '1' to Disable interrupt for PAYLOAD event
					See EVENTS_PAYLOAD
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled		Read: Enabled
D	D\A/	END	Enabled	1	
D	KVV	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Е	RW	DISABLED			Write '1' to Disable interrupt for DISABLED event
					See EVENTS_DISABLED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	DEVMATCH			Write '1' to Disable interrupt for DEVMATCH event
					See EVENTS_DEVMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	DEVMISS			Write '1' to Disable interrupt for DEVMISS event
					See EVENTS_DEVMISS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	RSSIEND			Write '1' to Disable interrupt for RSSIEND event
					See EVENTS_RSSIEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
	RW	BCMATCH		-	Write '1' to Disable interrupt for BCMATCH event
-		eren er er *			
					See EVENTS_BCMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW	CRCOK			Write '1' to Disable interrupt for CRCOK event
					See EVENTS_CRCOK
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CRCERROR			Write '1' to Disable interrupt for CRCERROR event
			Class	1	See EVENTS_CRCERROR
			Clear	1	Disable Dead: Disable
			Disabled	0	Read: Disabled



Id			Field	Value Id		lue		Ĭ		_	•		Des				•	_	Ť	Ĭ	Ŭ	•	Ĭ	Ť	Ĭ	Ĭ	Ŭ	•	_	Ť	•				
Res	set	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														0
Id																							K	J		į.			Н	G	F	F I	D (. B	Α
Bit	nui	mb	er		31	30	29	28	27 2	26 2	25 2	24 :	23 2	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0

23.14.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit	numbe	er		31 3	0 29	28	27	26	25	24	23 2	22 2	1 20) 19	18	17	16	15	14	13 1	l2 1	.1 10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	e						Des	crip	tion	ı																	
Α	R	CRCSTATUS									CRC	sta	tus (of pa	acke	et re	ecei	ved													
			CRCError	0							Pac	ket ı	ece	ivec	l wi	th C	RC	erro	or												
			CRCOk	1							Pac	ket ı	ece	ivec	l wi	th C	RC	ok													

23.14.5 RXMATCH

Address offset: 0x408 Received address

Bit	numb	er		31	30	29	28 :	27 2	26 2	25 2	24 :	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																														Δ	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	า																	
Α	R	RXMATCH										Rec	eive	d a	ddr	ess																

Logical address of which previous packet was received

23.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20 1	.9 1	8 17	16	15	14	13 1	2 1:	1 10	9	8	7	6	5	4	3	2 :	1 0
Id												Α	Α	Α	Α ,	Α ,	Α Α	Α	Α	Α	A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α ,	Δ Α	А А
Res	et 0 x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 0
Id	RW	Field	Value Id	Va	alue							Des	scri	ptic	n																	
Α	R	RXCRC										CRO	C fie	eld (of pr	evi	ousl	y re	ceiv	ed p	ack	et										

23.14.7 DAI

Address offset: 0x410

Device address match index

Bit	numb	er		31	1 30	29	28 2	27 26	5 2	25 2	24 2	23 2	22 2	21 :	20	19	18	17	16	15	14	13	12	11 1	10	9	8	7	6	5	4	3	2	1	0
Id																																	Α	Α	Α
Res	et Ox(0000000		0	0	0	0	0 0	(0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue						ı	Des	crip	tio	n																				
Α	R	DAI									[Dev	ice	ado	dre	ss r	nat	ch i	nde	ex															_
												n de	av (1	م۱.	۴ ۹			ماما				- A F	r1		D.4	חוי	.1 +	hai	٠	+ -					

Index (n) of device address, see DAB[n] and DAP[n], that got an address match.

23.14.8 PACKETPTR

Address offset: 0x504



Packet pointer

Bit	numbe	er		31	L 30	29	28	27	26	25 :	24 2	23 2	2 2	1 20	19	18	17	16	15 1	14 1	3 12	2 11	10	9	8	7 (6 5	5 4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Δ	4 A	Α	Α	Α	Α	Α .	A A	A	Α.	Α	Α	Α	۱ ۸	4 Α	Α Α	A	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0 0	0	0	0	0	0) (0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						0	Desc	ript	tion																	
Α	RW	PACKETPTR									P	ack	et p	ooin	ter																
														addr on. V													this				
											а	ddr	ess	will	be t	trar	ısmi	tte	d an	d w	hen	rec	eivir	ıg, t	he r	ece	ive	d			
											p	ack	et v	will b	oe w	/ritt	en t	o tl	his a	ddre	ess.	This	ado	dres	s is	a b	yte				
											а	align	ed i	ram	ado	dres	s.														

23.14.9 FREQUENCY

Address offset: 0x508

Frequency

Bit number		31 3	0 29	28 2	7 26	25 2	24 23	22 2	1 20	19 1	.8 1	7 16	15 1	4 13	12 1	1 10	9	8	7 6	5	4	3 2	. 1	0
Id																		В	Д	. A	Α	A A	Α	Α
Reset 0x00000002		0 0	0 0	0 (0 0	0	0 0	0 0	0	0	0 0	0	0 (0 0	0 (0	0	0 (0	0	0	0 0	1	0
Id RW Field	Value Id	Valu	е				De	script	tion															
A RW FREQUE	ICY	[010	00]				Ra	dio ch	nann	el fre	que	ncy												
							Fre	quen	ncy =	2400) + F	REQ	UEN	CY (M	IHz).									
B RW MAP							Ch	annel	l map	o sele	ectio	n.												
	Default	0					Ch	annel	l map	bet	wee	n 24	00 N	HZ	2500	МН	Z							
							Fre	quen	ncy =	2400) + F	REQ	UEN	CY (M	IHz)									
	Low	1					Ch	annel	l map	bet	wee	n 23	60 N	HZ	2460	MH	Z							
							Fre	quen	ncy =	2360) + F	REQ	UEN	CY (M	IHz)									

23.14.10 TXPOWER

Address offset: 0x50C

Output power

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id	A A A A	A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id RW Field Value Id	Value Description	
A RW TXPOWER	RADIO output power.	
	Output power in number of dBm, i.e. if the value -20 is specified	
	the output power will be set to -20dBm.	
Pos4dBm	0x04 +4 dBm	
Pos3dBm	0x03 +3 dBm	
0dBm	0x00 0 dBm	
Neg4dBm	0xFC -4 dBm	
Neg8dBm	0xF8 -8 dBm	
Neg12dBm	0xF4 -12 dBm	
Neg16dBm	0xF0 -16 dBm	
Neg20dBm	0xEC -20 dBm	
Neg30dBm	0xD8 -40 dBm De	eprecated
Neg40dBm	0xD8 -40 dBm	

23.14.11 MODE

Address offset: 0x510

Data rate and modulation



Bit r	numbe	er		31	1 30	29	28	8 27	7 2	6 25	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6 5	5 4	4 3	2	1	0
Id																															Д	A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	C	0 0	C	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	ripti	on																			
Α	RW	MODE										R	adio	dat	ta r	ate	and	d m	odu	ılat	ion	set	ting	. Th	ie ra	adio	su _l	эрс	rts					
												F	equ	uenc	cy-s	hift	: Ke	yin	g (F	SK)	mo	dul	atio	n.										
			Nrf_1Mbit	0								1	Mb	it/s	Noi	rdic	pr	opr	ieta	ry i	radi	o n	ode	9										
			Nrf_2Mbit	1								2	Mb	it/s	Noi	rdic	pr	opr	ieta	ry i	radi	o n	ode	9										
			Ble_1Mbit	3								1	Mb	it/s	Blu	eto	oth	Lo	w E	ner	gy													
			Ble_2Mbit	4								2	Mb	it/s	Blu	eto	oth	Lo	w E	ner	gy													

23.14.12 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit r	numbe	er		31 30 29 28 27 26 25 24											19	18	17	16 :	15 :	14 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1	0
Id										(ĵ.			F	Ε	Ε	Е	Е							С				Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 ()	0 (0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	n																		
Α	RW	LFLEN									Le	engtl	h on	air	of	LEN	IGT	H fi	eld	in n	umb	er c	f bi	ts.								_
С	RW	SOLEN									Le	engtl	h on	air	of	S0 1	field	d in	nur	nbe	r of	byte	s.									
Е	RW	S1LEN									Le	engt	h on	air	of	S1 1	field	d in	nur	nbe	r of	bits										
F	RW	S1INCL									Ir	clud	le or	ex	cluc	de S	51 fi	eld	in F	RAM												
			Automatic	0							Ir	clud	le S1	fie	ld i	n R	AM	onl	y if	S1L	EN >	0 •										
			Include	1							Α	lway	s inc	luc	le S	1 fi	eld	in F	RAN	1 inc	depe	nde	nt o	f S1	LEN							
G	RW	PLEN									Le	engt	h of	pre	am	ble	on	air.	De	cisic	n p	oint	TA	SKS_	_STA	RT	tas	k				
			8bit	0							8	-bit p	orea	mb	le																	
			16bit	1							1	6-bit	pre	am	ble																	

23.14.13 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit r	numbe	er		31	30 2	29 2	8 27	26	25	24	23 2	22 21	1 20	19	18	17	16	15 1	14 1	L3 1:	2 11	10	9	8	7	6	5 4	4 3	2	1	0
Id									Ε	D					С	С	С	В	В	ВВ	3 B	В	В	В	Α	Α	Α /	4 A	Α	Α	Α
Res	et 0x0	0000000		0	0 (0 (0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	ue						Des	cript	ion																		
Α	RW	MAXLEN		[0.	255]]					Max	imu	m le	engt	h o	f pa	cke	t pa	ylo	ad. I	f the	e pa	cket	pa	yloa	ad is	;				
											large	er th	an I	MΑ	KLEI	N, tł	ne r	adio	o wi	ll tru	ınca	te tl	he p	ayl	oad	l to					
											MAX	KLEN	١.																		
В	RW	STATLEN		[0.	255]]					Stati	ic lei	ngth	in i	nun	nbe	r of	byt	es												
											The	stati	ic le	ngtl	h pa	aran	nete	er is	ado	ded 1	to tl	ne to	otal	len	gth	of t	he				
											payl	oad	whe	en s	end	ling	and	l red	ceiv	ing p	oack	ets,	e.g	. if t	he	stat	ic				
											leng	th is	set	to I	N th	ne ra	adic	wil	l re	ceive	e or	sen	d N	byt	es r	nor	e				
											than	n wh	at is	det	fine	d in	the	e LE	NG	ΓΗ fi	eld	of th	ne p	ack	et.						
С	RW	BALEN		[2.	4]						Base	e ado	dres	s le	ngtl	h in	nur	nbe	r of	byt	es										
											The	add	ress	fiel	d is	cor	npc	sed	of	the I	base	e ado	dres	s ar	nd t	he o	one				
											byte	lon	g ad	ldre	ss p	refi	х, е	.g. s	set I	BALE	N=2	2 to	get	a to	tal	ado	lres	S			
											of 3	byte	es.										_								
D	RW	ENDIAN									On a	air ei	ndia	inne	ess c	of pa	acke	et, t	his	appl	ies 1	to th	ne Si	o, Li	ENG	STH,	, S1				
											and	the	PAY	LOA	AD f	ield	s.														
			Little	0							Leas	t Sig	nifi	cant	t bit	on	air	first	t												
			Big	1							Mos	t sig	nific	cant	t bit	on	air	first													
Е	RW	WHITEEN									Enal	ble o	r di	sabl	le p	acke	et w	/hite	enir	ıg											
			Disabled	0							Disa	ble																			
			Enabled	1							Enal	ble																			



23.14.14 BASE0

Address offset: 0x51C

Base address 0

Bit	num	nbei	r		31	30	29	28	27	26	25	24	23	22 2	21 2	20 19	9 18	8 17	16	15	14	13	12 1	.1 10) 9	8	7	6	5	4	3	2	1	C
Id					А	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A .	A A	. Д	A	Α	Α	Α	Α	Α.	4 Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ
Re	set 0)x00	000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	D
Id	R۱	W	Field	Value Id	Va	lue							Des	scrip	tio	n																		
Α	R۱	W	BASE0										Bas	e ac	ldre	ess 0																		

Radio base address 0.

23.14.15 BASE1

Address offset: 0x520

Base address 1

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	18 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	A A	A /	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ДД	Α	Α	Α
Re	et 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	BASE1										Bas	e ad	ddr	ess	1																	

Radio base address 1.

23.14.16 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21	20	19	18	17 :	16	15 :	L4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 :	1 0			
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	ВЕ	В	В	В	В	В	Α	Α	Α	Α	A	Δ Α	А А			
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 () (0 0			
Id	RW	Field	Value Id	Va	lue							Des	scrip	otic	n																					
Α	RW	AP0										Add	dres	s p	refi	x 0.	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																			
В	RW	AP1	D D D D D D D D D D D D D D D D D D D																																	
С	RW	AP2										Add	dres	s p	refi	x 2.								B B B A A A A A A A												
D	RW	AP3										Add	dres	s p	refi	x 3.																				

23.14.17 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bit n	umbe	er		31	. 30	29	28	27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Α	Α	Α	Α	A A	4 Α	4 A
Rese	t 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (
Id	RW	Field	Value Id	Va	llue	2						De	scri	ptic	on																			
Α	RW	AP4	Value Id Value Description Address prefix 4.																															
В	RW	AP5										Ad	dre	ss p	ref	ix 5																		
С	RW	AP6										Ad	dre	ss p	ref	ix 6																		
D	RW	AP7										Ad	dres	ss p	ref	ix 7																		

23.14.18 TXADDRESS

Address offset: 0x52C
Transmit address select



Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	1 2	0 1	9 18	8 17	7 16	5 15	14	13	12 1	.1 10) 9	8	7	6	5	4	3	2	1 0
Id																															A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	TXADDRESS										Tra	nsm	it a	ddr	ess :	sele	ct														

Logical address to be used when transmitting a packet.

23.14.19 RXADDRESSES

Address offset: 0x530 Receive address select

	umbe	er		31 30 29 28 27 26 25 24	+ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	ADDR0			Enable or disable reception on logical address 0.
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	ADDR1			Enable or disable reception on logical address 1.
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	ADDR2			Enable or disable reception on logical address 2.
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	ADDR3			Enable or disable reception on logical address 3.
			Disabled	0	Disable
			Enabled	1	Enable
Е	RW	ADDR4			Enable or disable reception on logical address 4.
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	ADDR5			Enable or disable reception on logical address 5.
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	ADDR6			Enable or disable reception on logical address 6.
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ADDR7			Enable or disable reception on logical address 7.
			Disabled	0	Disable
			Enabled	1	Enable

23.14.20 CRCCNF

Address offset: 0x534 CRC configuration

Bit	numbe	er		31	1 30	29	28 2	27 :	26 2	25 2	24 2	23 23	2 2:	1 20	19	18	17	16	15	14	13 :	12 :	11 1	.0 9	9 8	7	6	5	4	3	2 :	1 0
Id																									В						,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue							Desc	ript	ion																		
Α	RW	LEN		[1	3]						(CRC I	leng	gth i	in nı	uml	ber	of b	yte	s.												
			Disabled	0							(CRC I	leng	gth i	s ze	ro a	and	CR	Сса	lcul	atic	n is	dis	abl	ed							
			One	1							(CRC I	leng	gth i	s or	ne b	yte	and	d CI	RC c	alcı	ılat	on i	is eı	nabl	ed						
			Two	2							(CRC I	leng	gth i	is tw	o b	yte	s ar	nd C	RC	calc	ula	tion	is e	nak	led						
			Three	3							(CRC I	leng	gth i	is th	ree	by	es	and	CR	Сса	lcu	atic	n is	en	able	d					
В	RW	SKIPADDR									- 1	nclu	de d	or e	xclu	de	pac	ket	ado	dres	s fie	eld	out	of C	RC	calc	ulat	tion				
			Include	0							(CRC	calc	ulat	tion	inc	lud	es a	ddr	ess	fiel	d										
			Skip	1							(CRC	calc	ulat	tion	do	es n	ot i	ncli	ıde	ado	dres	s fie	eld.	The	CR	2					
											C	alcu	ılati	on v	will	staı	rt at	the	e fir	st b	yte	aft	er th	ne a	ddr	ess.						



23.14.21 CRCPOLY

Address offset: 0x538

CRC polynomial

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	l8 1	7 1	6 15	5 14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	АА
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptio	n																	
Α	RW	CRCPOLY										CRO	Срс	lyn	omi	ial																
												reg	iste	r w	hich	n ind	dex	corı	resp	ond	al is i ds to l-wir	the	teri	n's (expo	one	nt.					
												nur	nbe	er O	of t	he i	regi	ster	cor	iten	nt is	igno	red	by t	he h	narc	lwa	re.				
												The	e fol	llow	ing	exa	mp	le is	for	an	8 bi	t CR	Сро	lync	mia	al: x	8 +	x7 -	+			
												х3 -	+ x2	+ 1	. = 1	l 10	00 :	110:	1.													

23.14.22 CRCINIT

Address offset: 0x53C

CRC initial value

Bit	numbe	er		31	30 2	9 2	28	27	26	25	24	1 23	22	2 2 1	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id												Α	А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Val	ue							De	esc	ipt	on																				ı
Α	RW	CRCINIT										CF	lC i	niti	al v	alue	è																		

Initial value for CRC calculation.

23.14.23 TIFS

Address offset: 0x544

Inter Frame Spacing in us

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																											A	Δ.	Α.	Α.	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	llue							De	scri	ipti	on																				
Α	RW	TIFS										Int	er F	rar	ne	Spa	cin	g ir	า us																
																											o co				9				
												end	d of	f th	e la	ist k	oit (of t	he į	ore	viou	ıs p	ack	et t	o th	e st	art o	of t	he	firs	t				
												bit	of	the	sul	bse	que	ent	pac	ket															

23.14.24 RSSISAMPLE

Address offset: 0x548

RSSI sample

Bit	numbe	r		31 3	0 29	28	27	26	25 2	24 2	23 2	22	21	20	19 :	18	17	16	15	14 :	13 :	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																											Α	Α	Α	A	Α	А А
Res	et 0x0	0000000		0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	е					ı	Des	cri	ptic	n																		
Α	R	RSSISAMPLE		[01	27]					F	RSSI	l sa	mp	le																		
										\	valu	ie v	whil Act	e tł ual	ne a rec	ctu eive	ial r	ece	eive al s	d si trei	gna ngtl	al st	reng	gth i	s a ı	neg	a po ative	е	ive			



23.14.25 STATE

Address offset: 0x550 Current radio state

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A R STATE		Current radio state
	Disabled	O RADIO is in the Disabled state
	RxRu	1 RADIO is in the RXRU state
	RxIdle	2 RADIO is in the RXIDLE state
	Rx	3 RADIO is in the RX state
	RxDisable	4 RADIO is in the RXDISABLED state
	TxRu	9 RADIO is in the TXRU state
	TxIdle	10 RADIO is in the TXIDLE state
	Tx	11 RADIO is in the TX state
	TxDisable	12 RADIO is in the TXDISABLED state

23.14.26 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit	umbe	r		31	1 30	29	28	27	26	25	24	23	22	21	. 20	19	18	3 1	7 16	5 1	5 14	1 13	3 12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	ion																				
Α	RW	DATAWHITEIV										Da	ta v	whi	ten	ing	ini	tial	l val	ue.	Bit	6 is	s ha	rd-v	wire	d to) ' 1'	, w	ritir	ng '(0'				
												to	it h	ıas ı	no (effe	ect,	an	d it	wi	ll al	way	s be	e re	ad l	oacl	c an	d u	sed	by					
												the	e de	evic	e a	s '1	٠.																		
												Bit		corr	resp	on	ds 1	to f	Posi	tio	n 6	of t	he I	LSFI	R, B	it 1	to F	osi	tior	ı 5,					

23.14.27 BCC

Address offset: 0x560 Bit counter compare

Bit nu	ımbe	r		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	18 1	17 1	6 1	.5 1	4 1	L3 1	2 1	1 1	.0 9) ;	3	7 (6	5 4	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α ,	Α ,	Δ ,	Δ.	A A	Δ ,	Δ ,	A A	۱ ۸	Δ ,	Δ,	Α.	Α /	Δ,	4 A	Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 (0 () (0 () () (0 (0	0 (0 (0 0	0	0
Id	RW	Field	Value Id	0 0 0 0 0 Value									cri	ptio	n																			
Α	RW	BCC										Bit	cou	inte	r cc	amo	are																	

Bit counter compare register

23.14.28 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW DAB	Device address base segment 0

Device address base segment 0



23.14.29 DAB[1]

Address offset: 0x604

Device address base segment 1

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 :	15 1	14	13 :	12 1	11 1	0 9	9 8	7	6	5	4	3	2	1 (0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	A	Д
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	DAB										Dev	/ice	ad	dre	ss b	ase	se	gme	ent	1													-

23.14.30 DAB[2]

Address offset: 0x608

Device address base segment 2

В	t nı	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
R	ese	t Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Ic	ı	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α		RW	DAB										De	vice	ad	dre	ss b	ase	se	gm	ent	2													

23.14.31 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	17 1	6 1	.5 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α ,	A A	Δ ,	Δ Α	A /	Α	А	Α	Α	Α	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0) (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	RW	DAB										De	vice	ad	dre	ss b	ase	seg	gme	nt 3	3												

23.14.32 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW DAB		Device address base segment 4

23.14.33 DAB[5]

Address offset: 0x614

Device address base segment 5

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	15 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	Α /	A A	Δ Α	A /	A A	Α	Α	Α	Α	Α	Α	A A	Α Α	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0 (0	0
Id RW Field	Value Id	Va	lue							Des	cri	ptic	n																		

A RW DAB Device address base segment 5

23.14.34 DAB[6]

Address offset: 0x618

Device address base segment 6



Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	L8 1	L7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																			
Α	RW	DAB										Dev	/ice	ad	dre	ss b	ase	seg	gme	ent	6													

23.14.35 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit	numb	er			31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	15 1	14 1	L3 1	12	11 1	.0 9	9 :	8 7	7 (6 !	5	4	3 2	2 1	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α ,	A ,	A.	Α.	Α	A	Δ ,	Δ,	Δ Α	Α,	Δ,	Α	Α	A A	Δ Α	A A
Res	et 0x	000	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0 (0	0	0 (0 (0 (
Id	RW	/ F	ield	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																														
Α	RW	/ [DAB										De	vice	ad	dre	ss b	ase	seg	gme	ent '	7													

23.14.36 DAP[0]

Address offset: 0x620 Device address prefix 0

Bit	numbe	er		31	. 30	29	28	27	26 2	25 2	24 :	23 2	22 2	1 2	0 1	9 1	8 17	16	15	14	13	12 :	11 1	.0 9	9 8	3 7	6	5	4	3	2	1 ()
Id																			Α	Α	Α	Α	A ,	Δ /	Α Α	A		A A	Α	Α	Α	A A	À.
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0)	0 (0	0	0	0	0	0	0	0	0 () (0	C	0	0	0	0	0 (,
Id	RW	Field	Value Id	Va	lue						- 1	Des	crip	tio	n																		
Α	RW	DAP									- 1	Dev	ice	add	lres	s pr	efix	0															

23.14.37 DAP[1]

Address offset: 0x624

Device address prefix 1

Bit r	number	31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Res	set 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW DAP		Device address prefix 1

23.14.38 DAP[2]

Address offset: 0x628

Device address prefix 2

В	Bit n	umb	er			31	. 30	29	28	27 2	26 2	25 2	24 2	3 2	2 2	1 2	0 19	18	3 17	16	15	14	13	12	11 1	.0 9	9 8	3 7	' 6	5 5	4	3	2	1	0
lo	d																				Α	Α	Α	Α	Α.	Δ /	A /	A A		, Δ	A	Α	Α	Α	Α
R	lese	t Ox(000000	00		0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 () (0) (0	0	0	0	0	0
10	d	RW	Field		Value Id	Va	lue						0	eso	crip	tion	1																		
Δ	١	RW	DAP										0)evi	ce a	ıddı	ress	pre	efix	2															_

23.14.39 DAP[3]

Address offset: 0x62C Device address prefix 3

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19	18 17 16 15 14	13 12 11 10 9	8 7 6 5	5 4 3 2 1 0
Id				A A	AAAAA	. A A A A	AAAAAA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value	Description				
				f: 0			

A RW DAP Device address prefix 3



23.14.40 DAP[4]

Address offset: 0x630

Device address prefix 4

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16	6 15 14 13 12 11 10 9	9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A A A
iu					
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0000000	0000000000
Id RW Field	Value Id	Value	Description		
A RW DAP	·	·	Device address prefix 4		

23.14.41 DAP[5]

Address offset: 0x634

Device address prefix 5

Bit	nun	nbe	r		31	30 2	9 2	28 27	26	25	24	23 2	2 2:	1 20	19	18	17 :	L6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																		A	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 Δ	А	Α
Re	set 0)x0	000000		0	0 (0	0 0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	R	w	Field	Value Id	Va	lue						Desc	ript	ion																		
Α	R'	W	DAP									Devi	ce a	ddr	ess i	oref	ix 5															

23.14.42 DAP[6]

Address offset: 0x638

Device address prefix 6

В	it nı	ımbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Ic	t																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Ĺ
R	ese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Ic	t	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α		RW	DAP										De	vice	ad	dre	SS	pre	fix (5																Ī

23.14.43 DAP[7]

Address offset: 0x63C Device address prefix 7

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	2 1 0
Id		A A A A A A A A A A A A A A A A A A A	A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field	Value Id	Value Description	
A RW DAP		Device address prefix 7	

23.14.44 DACNF

Address offset: 0x640

Device address match configuration

Bit	numbe	er		31	L 30	29	28	8 27	7 2	6 25	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8 7	7 (6 5	5 4	1 3	2	1	0
Id																				Р	О	N	M	L	K	J	I F	1 (G F	= 1	E D	С	В	Α
Res	et 0 x0	0000000		0	0	0	0	0	(0 0	(0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esci	riptio	on																			
Α	RW	ENA0										Ei	nabl	le or	dis	abl	e d	evio	e a	ddr	ess	ma	tch	ing	usir	ng c	levio	e a	addr	ess				
												0																						
			Disabled	0								D	isab	led																				
			Enabled	1								E	nabl	led																				
В	RW	ENA1										E	nabl	le or	dis	abl	e d	evi	e a	ddr	ess	ma	tch	ing	usir	ng c	levio	e a	addr	ess	;			
												1																						
			Disabled	0								D	isab	led																				



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			PONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Enabled	1 Enabled
С	RW ENA2		Enable or disable device address matching using device address
			2
		Disabled	0 Disabled
		Enabled	1 Enabled
D	RW ENA3		Enable or disable device address matching using device address
			3
		Disabled	0 Disabled
		Enabled	1 Enabled
Ε	RW ENA4		Enable or disable device address matching using device address
			4
		Disabled	0 Disabled
		Enabled	1 Enabled
F	RW ENA5		Enable or disable device address matching using device address
			5
		Disabled	0 Disabled
		Enabled	1 Enabled
G	RW ENA6		Enable or disable device address matching using device address
			6
		Disabled	0 Disabled
		Enabled	1 Enabled
Н	RW ENA7		Enable or disable device address matching using device address
			7
		Disabled	0 Disabled
		Enabled	1 Enabled
I	RW TXADD0		TxAdd for device address 0
J	RW TXADD1		TxAdd for device address 1
K	RW TXADD2		TxAdd for device address 2
L	RW TXADD3		TxAdd for device address 3
M	RW TXADD4		TxAdd for device address 4
N	RW TXADD5		TxAdd for device address 5
0	RW TXADD6		TxAdd for device address 6
Р	RW TXADD7		TxAdd for device address 7

23.14.45 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit r	umbe	er		31	30 2	9 2	28 27	7 2	6 25	24	23 22	2 21 2	20	19 1	L8 1	17 1	6 1	5 14	13	12	11 1		8		6	5	4	3 2	2 1	0 A
	et OxO	0000200		0	0 () (0 0) (0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 1	. 0	0	0	0	0	0 0	0	
Id	RW	Field	Value Id	Va	lue						Desci	riptio	n																	
Α	RW	RU									Radio	o ram	ıp-u	ıp tiı	me															_
			Default	0							Defa	ult rai	mp	-up	tim	e (tl	RXE	N),	com	pati	ble	with	fir	nwa	ire					
											writt	en fo	r nl	RF51	L															
			Fast	1							Fast r	ramp-	-up	(tR	XEN	I,FA	ST),	see	ele	ctric	al s	peci	fica	tion	for	mo	re			
											infor	matio	on																	
С	RW	DTX									Defa	ult TX	(va	lue																
											Speci	ifies v	wha	t th	e R	ADIO) w	ill tr	ans	mit	whe	n it i	is n	ot si	arte	ed, i	.e.			
											betw	een:																		
											RADI	O EVI	FNIT	rs R	FΔ	DV 2	nd	RΔΓ	NΟ.	ΤΔςμ	′S S	TΔR	т							
														_							_									
											RADI	O.EVE	ENT	ΓS_E	ND	and	I RA	DIC	AT.	SKS_	STA	ART								



Bit number		31	30 2	29 2	28 2	7 2	6 25	5 24	4 23	3 22	21	20	19	18	17	16	15 1	L4 1	3 12	2 11	10	9	8	7 (5 5	4	3	2	1 ()
Id																						С	С						A	
Reset 0x00000200		0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	1	0	0 (0	0	0	0	0 ()
Id RW Field	Value Id	Va	lue						D	escr	ipti	on																		ı
									RA	ADIC	D.EV	/EN	TS_	END) ar	nd R	ADI	O.E	/EN	TS_	DISA	BLE	D							
	B1	0							Tr	ans	mit	'1'																		
	B0	1							Tr	ans	mit	'0'																		
	Center	2							Tr	ans	mit	cer	iter	fre	que	ncy														
									W	/hen	tur	ning	g the	e cr	ysta	al fo	r ce	ntre	fre	que	ncy,	the	RA	DIO	mι	ıst				
									be	e set	t in	DT>	< = C	Cent	ter	mod	de t	o be	abl	e to	ach	ieve	e the	e ex	pec	ted				
									ac	cur	асу.																			

23.14.46 POWER

Address offset: 0xFFC
Peripheral power control

Bit	numbe	r		31	1 30	29	2	8 2	7 2	26	25	24	1 2	3 2	2 2	21	20	19	18	3 1	.7 :	L6	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																						Α
Res	et 0x0	0000001		0	0	0	C) ()	0	0	0	0) ()	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	alue								D	esc	rip	otic	n																					
Α	RW	POWER											P	erip	ohe	era	Ιp	wc	er	COI	ntr	ol.	Th	ер	erip	he	ral	and	lits	re	gist	ers	wil	l be				
													re	se	t to	o it	s ir	nitia	al s	ta	te l	by :	swi	tch	ing	th	ер	erip	her	al d	off a	and	the	en				
													b	ack	10	n a	gai	n.																				
			Disabled	0									P	erip	ohe	era	l is	ро	we	ere	d c	ff																
			Enabled	1									P	erip	ohe	era	l is	ро	we	ere	d c	n																

23.15 Electrical specification

23.15.1 General Radio Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
f _{OP}	Operating frequencies	2360		2500	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
f _{PLL,CH,SP}	PLL channel spacing		1		MHz
f _{DELTA,1M}	Frequency deviation @ 1 Msps		±170		kHz
f _{DELTA,BLE,1M}	Frequency deviation @ BLE 1Msps		±250		kHz
f _{DELTA,2M}	Frequency deviation @ 2 Msps		±320		kHz
fsksps	On-the-air data rate	1		2	Msps

23.15.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,PLUS4dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+4 dBm		7.0		mA
I _{TX,PLUS4dBM}	TX only run current P _{RF} = +4 dBm		15.4		mA
I _{TX,OdBM,DCDC}	TX only run current (DCDC, 3V)P _{RF} = 0dBm		4.6		mA
I _{TX,0dBM}	TX only run current P _{RF} = 0dBm		10.1		mA
I _{TX,MINUS4dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -4dBm		3.6		mA
I _{TX,MINUS4dBM}	TX only run current P _{RF} = -4 dBm		7.8		mA
I _{TX,MINUS8dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -8 dBm		3.2		mA
I _{TX,MINUS8dBM}	TX only run current P _{RF} = -8 dBm		6.8		mA
I _{TX,MINUS12dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -12 dBm		2.9		mA
I _{TX,MINUS12dBM}	TX only run current P _{RF} = -12 dBm		6.2		mA
I _{TX,MINUS16dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -16 dBm		2.7		mA
I _{TX,MINUS16dBM}	TX only run current P _{RF} = -16 dBm		5.7		mA
I _{TX,MINUS20dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -20 dBm		2.5		mA
I _{TX,MINUS20dBM}	TX only run current P _{RF} = -20 dBm		5.4		mA
I _{TX,MINUS40dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -40 dBm		2.1		mA



Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,MINUS40dBM}	TX only run current P _{RF} = -40 dBm		4.3		mA
I _{START,TX,DCDC}	TX start-up current DCDC, 3V, P _{RF} = 4 dBm		TBD		mA
I _{START,TX}	TX start-up current, P _{RF} = 4 dBm		TBD		mA

23.15.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Тур.	Max.	Units
I _{RX,1M,DCDC}	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		4.6		mA
I _{RX,1M}	RX only run current 1Msps / 1Msps BLE		10.0		mA
I _{RX,2M,DCDC}	RX only run current (DCDC, 3V) 2Msps		5.8		mA
I _{RX,2M}	RX only run current 2Msps		11.2		mA
I _{START,RX,1M,DCDC}	N,DCDC RX start-up current (DCDC 3V) 1Msps / 1Msps BLE				mA
I _{START,RX,1M}	RX start-up current 1Msps / 1Msps BLE		7.5		mA

23.15.4 Transmitter specification

Symbol	Description	Min.	Тур.	Max.	Units
P _{RF}	Maximum output power			4	dBm
P _{RFC}	RF power control range		24		dB
P _{RFCR}	RF power accuracy			±4	dB
P _{RF1,1}	1st Adjacent Channel Transmit Power 1 MHz (1 Msps)		-25		dBc
P _{RF2,1}	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps)		-50		dBc
P _{RF1,2}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps)		-25		dBc
P _{RF2,2}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps)		-50		dBc

23.15.5 Receiver operation

Symbol	Description	Min.	Тур.	Max.	Units
P _{RX,MAX}	Maximum received signal strength at < 0.1% BER		0		dBm
P _{SENS,IT,1M}	Sensitivity, 1Msps nRF mode ¹⁵		-93		dBm
P _{SENS,IT,SP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3 ¹⁶		-96		dBm
P _{SENS,IT,LP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4 -95			dBm	
PCENIC IT 2M	Sensitivity, 2Msps nRF mode ¹⁸		-89		dBm

23.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal¹⁹

Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1M,co-channel}	1Msps mode, Co-Channel interference		9		dB
C/I _{1M,-1MHz}	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1M,+1MHz}	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
C/I _{1M,-2MHz}	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
C/I _{1M,+2MHz}	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
C/I _{1M,-3MHz}	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
C/I _{1M,+3MHz}	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
C/I _{1M,±6MHz}	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I _{1MBLE,co-channel}	1 Msps BLE mode, Co-Channel interference		6		dB

Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

Equivalent BER limit < 10E-04

Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented



Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1MBLE,-1MHz}	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1MBLE,+1MHz}	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
C/I _{1MBLE,-2MHz}	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
C/I _{1MBLE,+2MHz}	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
C/I _{1MBLE,>3MHz}	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
C/I _{1MBLE,image}	Image frequency Interference		-22		dB
C/I _{1MBLE,image,1MHz}	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
C/I _{2M,co-channel}	2Msps mode, Co-Channel interference		10		dB
C/I _{2M,-2MHz}	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
C/I _{2M,+2MHz}	2 Msps mode, Adjacent (+2 MHz) interference		-14		dB
C/I _{2M,-4MHz}	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
C/I _{2M,+4MHz}	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
C/I _{2M,-6MHz}	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
C/I _{2M,+6MHz}	2 Msps mode, Adjacent (+6 MHz) interference -47			dB	
C/I _{2M,≥12MHz}	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB

23.15.7 RX intermodulation

RX intermodulation²⁰

Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,1M}	IMD performance, 1 Msps, 3rd, 4th, and 5th offset channel		-33		dBm
P _{IMD,1M,BLE}	IMD performance, BLE 1 Msps, 3rd, 4th, and 5th offset channel		-30		dBm
P _{IMD,2M}	IMD performance, 2 Msps, 3rd, 4th, and 5th offset channel		-33		dBm

23.15.8 Radio timing

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXEN}	Time between TXEN task and READY event after channel		140		us
	FREQUENCY configured				
t _{TXEN,FAST}	Time between TXEN task and READY event after channel		40		us
	FREQUENCY configured (Fast Mode)				
t _{TXDISABLE}	Time between DISABLE task and DISABLED event when the		6		us
	radio was in TX and mode is set to 1Msps				
t _{TXDISABLE,2M}	Time between DISABLE task and DISABLED event when the		4		us
	radio was in TX and mode is set to 2Msps				
t _{RXEN}	Time between the RXEN task and READY event after channel		140		us
	FREQUENCY configured in default mode				
t _{RXEN,FAST}	Time between the RXEN task and READY event after channel		40		us
	FREQUENCY configured in fast mode				
t _{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX		20		us
	(channel FREQUENCY unchanged)				
t _{RXDISABLE}	Time between DISABLE task and DISABLED event when the		0		us
	radio was in RX				
t _{TXCHAIN}	TX chain delay		0.6		us
t _{RXCHAIN}	RX chain delay		9.4		us
t _{RXCHAIN,2M}	RX chain delay in 2Msps mode		5		us

23.15.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{ACC}	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
RSSI _{RESOLUTION}	RSSI resolution		1		dB
RSSI _{PERIOD}	Sample period		0.25		us

Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.



23.15.10 Jitter

Symbol	Description Min. Typ. Max. Uni					
t _{DISABLEDJITTER}	itter on DISABLED event relative to END event when shortcut 0.25				us	
	between END and DISABLE is enabled.					
t _{READYJITTER}	Jitter on READY event relative to TXEN and RXEN task.	ter on READY event relative to TXEN and RXEN task. 0.25				

23.15.11 Delay when disabling the RADIO

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXDISABLE,1M}	Disable delay from TX.		6		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit				
t _{RXDISABLE,1M}	Disable delay from RX.		0		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit				



24 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

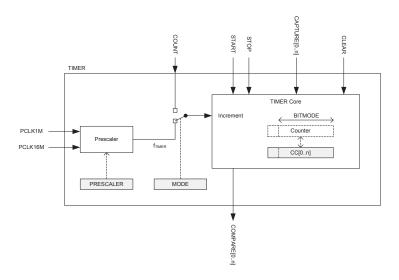


Figure 42: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 220. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

```
f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})
```

When $f_{TIMER} \le 1$ MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 225 register.

PRESCALER on page 225 and the *BITMODE* on page 225 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.



When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 220.

24.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

24.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE on page 225 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

24.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

24.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

24.5 Registers

Table 40: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers
				(CC[03])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
				(CC[03])
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
				(CC[03])

Table 41: Register Overview

Register	Offset	Description	
TASKS_START	0x000	Start Timer	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated



Register	Offset	Description
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MODE	0x504	Timer mode selection
BITMODE	0x508	Configure the number of bits used by the TIMER
PRESCALER	0x510	Timer prescaler register
CC[0]	0x540	Capture/Compare register 0
CC[1]	0x544	Capture/Compare register 1
CC[2]	0x548	Capture/Compare register 2
CC[3]	0x54C	Capture/Compare register 3
CC[4]	0x550	Capture/Compare register 4
CC[5]	0x554	Capture/Compare register 5

24.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L K J I H G F E D C B A
Res	et 0 x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	COMPAREO_CLEAR			Shortcut between COMPARE[0] event and CLEAR task
					See EVENTS_COMPARE[0] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW	COMPARE1_CLEAR			Shortcut between COMPARE[1] event and CLEAR task
					See EVENTS COMPARE[1] and TASKS CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW	COMPARE2_CLEAR			Shortcut between COMPARE[2] event and CLEAR task
					See EVENTS COMPARE[2] and TASKS CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	COMPARE3_CLEAR			Shortcut between COMPARE[3] event and CLEAR task
					See EVENTS COMPARE[3] and TASKS CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
Ε	RW	COMPARE4_CLEAR			Shortcut between COMPARE[4] event and CLEAR task
					See EVENTS COMPARE[4] and TASKS CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
F	RW	COMPARE5 CLEAR			Shortcut between COMPARE[5] event and CLEAR task
		_			
					See EVENTS_COMPARE[5] and TASKS_CLEAR



Bit	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW COMPAREO_STOP			Shortcut between COMPARE[0] event and STOP task
				See EVENTS_COMPARE[0] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Н	RW COMPARE1_STOP			Shortcut between COMPARE[1] event and STOP task
				See EVENTS COMPARE[1] and TASKS STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
ı	RW COMPARE2_STOP			Shortcut between COMPARE[2] event and STOP task
				See EVENTS COMPARE[2] and TASKS STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
J	RW COMPARE3_STOP			Shortcut between COMPARE[3] event and STOP task
				See EVENTS COMPARE[3] and TASKS STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
K	RW COMPARE4_STOP	Lilabica	-	Shortcut between COMPARE[4] event and STOP task
				See EVENTS_COMPARE[4] and TASKS_STOP
		Disabled	0	Disable shortcut
	DW COMPARES STOR	Enabled	1	Enable shortcut
L	RW COMPARE5_STOP			Shortcut between COMPARE[5] event and STOP task
				See EVENTS_COMPARE[5] and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

24.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umber		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW COMPARE	0		Write '1' to Enable interrupt for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW COMPARE	1		Write '1' to Enable interrupt for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW COMPARE	2		Write '1' to Enable interrupt for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW COMPARE	3		Write '1' to Enable interrupt for COMPARE[3] event



Bit r	numbe	r		31 3	30 29	28	27 2	26 25	24	23 2	22 2	1 20	19	18	17	16 :	15 1	L4 1	3 12	11	10	9 8	7	6	5	4	3 2	1	0
Id											F	F E	D	С	В	Α													
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0 (0 0	0 0	0	0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Valu	ıe					Desc	cript	tion																	
										See	EVE	NTS_	_cc	ОМР	ARE	[3]													
			Set	1						Enab	ble																		
			Disabled	0						Read	d: Di	isabl	ed																
			Enabled	1						Read	ıd: Er	nable	ed																
Ε	RW	COMPARE4								Writ	te '1	' to E	Ena	ble	inte	rrup	ot fo	or CO	OMP	ARE	[4] 6	ven	t						
										See	EVE	NTS_	_cc	ОМР	ARE	[4]													
			Set	1						Enak	ble																		
			Disabled	0						Read	d: Di	isabl	ed																
			Enabled	1						Read	ıd: Er	nable	ed																
F	RW	COMPARE5								Writ	te '1	' to E	Ena	ble	inte	rrup	ot fo	or CO	OMP	ARE	[5] 6	ven	t						
										See	EVE	NTS_	_cc	ОМР	ARE	[5]													
			Set	1						Enak	ble																		
			Disabled	0						Read	d: Di	isabl	ed																
			Enabled	1						Read	d: Er	nable	ed																

24.5.3 INTENCLR

Address offset: 0x308 Disable interrupt

		o intorrupt																																
Bit	numb	er		31	30	29	28 2	7 2	26 2	5 2	4 2	23 2	22 21	21	0 19	9 18	3 17	7 16	5 1	5 14	4 1	3 1	2 1	.1 1	0 9	9	8	7	6	5	4 3	2	1	0
Id													F	E	D) C	В	Α																
Res	et 0x0	0000000		0	0	0	0	0 (0 0) ()	0	0 0	0	0	0	0	0	0	0	0	()	0 () (0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0	Des	scripti	ion	1																			
Α	RW	COMPARE0									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[0] 6	eve	nt							
											S	See	EVEN	VTS		ом	PAF	RE[C)]															
			Clear	1								Disa	able																					
			Disabled	0							F	Rea	ad: Dis	sab	led																			
			Enabled	1							F	Rea	ad: En	ab	led																			
В	RW	COMPARE1									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[1] 6	eve	nt							
											S	See	EVEN	VTS		ЭМ	PAF	RE[1	!]															
			Clear	1								Disa	able																					
			Disabled	0							F	Rea	ad: Dis	sab	led																			
			Enabled	1							F	Rea	ad: En	ab	led																			
С	RW	COMPARE2									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[2] 6	eve	nt							
											S	See	EVEN	VTS	c C	ЭМ	PAF	RE[2	21															
			Clear	1									able		_																			
			Disabled	0							F	Rea	ad: Dis	sab	led																			
			Enabled	1							F	Rea	ad: En	ab	led																			
D	RW	COMPARE3									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[3] 6	eve	nt							
											5	See	EVEN	VTS	5 C	ЭМ	PAF	RE[:	31															
			Clear	1									able						,															
			Disabled	0							F	Rea	ad: Dis	sab	led																			
			Enabled	1							F	Rea	ad: En	ab	led																			
Ε	RW	COMPARE4									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[4] 6	eve	nt							
											,	See	EVEN	VT	5 C	ЭΜ	ΡΔΙ	RF[4	11															
			Clear	1									able	•					,															
			Disabled	0									ad: Dis	sab	led																			
			Enabled	1							F	Rea	ad: En	ab	led																			
F	RW	COMPARE5									١	Wri	ite '1'	to	Dis	abl	e in	ter	rup	t fo	r C	ON	1P <i>A</i>	RE[5] 6	eve	nt							
											,	See	EVEN	VT	5 C	ЭM	РДІ	RF[4	57															
			Clear	1									able	.,.	_==	2111	. , .,		1															
			2.20.	-							-																							



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			FEDCBA
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled		Read: Enabled

24.5.4 MODE

Address offset: 0x504 Timer mode selection

Bit	numb	er		3	1 30	0 29	9 2	8 2	7 2	6 2	5 2	24 2	23 2	2 2	1 2	0 1	.9 1	.8 1	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et 0x	0000000		0	0	0	0	0) (0 () (0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alu	е							Des	rip	tio	า																				
Α	RW	MODE										1	Time	er m	nod	e																				
			Timer	0								9	Sele	ct T	ime	er n	nod	le																		
			Counter	1								9	Sele	ct C	oui	nte	r m	ode	9														De	ore	cate	b
			LowPowerCounter	2								9	Sele	ct L	ow.	Po	wei	r Cc	un	ter	m	ode	!													

24.5.5 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit	number	31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A
Res	set 0x00000000	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW BITMODE		Timer bit width
	16Bit	0	16 bit timer bit width
	08Bit	1	8 bit timer bit width
	24Bit	2	24 bit timer bit width
	32Bit	3	32 bit timer bit width

24.5.6 PRESCALER

Address offset: 0x510
Timer prescaler register

Bit	numbe	r		31	30	29	28 2	7 26	5 25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14 1	3 12	2 11	10	9	8	7	6	5	4 3	2	1	0
Id																												A	A	Α	Α
Res	et 0x00	000004		0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	1	0	0
Id	RW	Field	Value Id	Va	lue	0 0 0 0 0 0 ue					Des	crip	tior	1																	
Α	RW	PRESCALER		[09]							Pre	scal	er v	alue																	

24.5.7 CC[0]

Address offset: 0x540

Capture/Compare register 0

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 2	17 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	CC										Cap	tur	e/C	om	par	e va	alue	9															

Only the number of bits indicated by BITMODE will be used by the TIMER.



24.5.8 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit	num	ber	r		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 1	7 16	15	14	13	12	11	10	9	8	7 6	5 5	5 4	1 3	2	1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 Α	Α Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	Α Α	A A	Α Α	Α.	Α	Α
Re	et 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0
Id	R۱	W	Field	Value Id	Va	lue							De	scri	ptio	n																		
Α	R۱	N	СС										Ca	otur	e/C	omp	oare	va	lue															
														ly th		uml	ber	of b	its i	ndi	cate	d b	y BI	TM	ODE	Wi	ll be	e us	ed	by				

24.5.9 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14	13	12	11 1	10 !	9 8	8 7	7 6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	4 Α	A	A	Α	Α	Α .	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	scrip	tior	1																	
Α	RW	CC										Cap	otur	e/Co	mp	are	val	ue														
												On	ly th	e nı	ımb	er c	of bi	its i	ndic	ate	d by	v BI	TMO	DDE	wi	ll be	use	ed b	V			
												the	TIN	1ER.								,							•			

24.5.10 CC[3]

Address offset: 0x54C

Capture/Compare register 3

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 18	3 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A	. A	Α	Α	Α	A A	4 A	Α	Α	Α	Α	Α	Α	A	4 Α	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	ptio	n																	
Α	RW	CC										Cap	otur	e/C	omp	are	val	ue														
												On	ly th	ne n	uml	oer (of b	its i	ndic	ate	d by	BIT	MO	DE v	vill k	oe u	ısec	d by	,			
												the	TIN	ИER																		

24.5.11 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bit	umbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ	A	A	Α	Α	Α	A	4 <i>A</i>	A	. A	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																	
Α	RW	CC										Cap	otur	e/C	om	oare	val	ue														
												Οn	lv th	n a	uml	her	of h	itc i	ndir	-ata	d hv	BIT	MO	DE :	will	he i	ICAI	d hv	,			
												OII	iy cii	10 11	uiiii	JCI	01 10	113 1	iuic	acc	u Dy	DII	IVIO	DL	vviii	DC I	usci	и Бу	y			
												the	TIN	1ER																		

24.5.12 CC[5]

Address offset: 0x554

Capture/Compare register 5



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW CC		Canture/Compare value

Only the number of bits indicated by BITMODE will be used by the TIMER.

24.6 Electrical specification

24.6.1 Timers Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{TIMER_1M}	Run current with 1 MHz clock input (PCLK1M)	3	5	8	μΑ
I _{TIMER_16M}	Run current with 16 MHz clock input (PCLK16M)	50	70	120	μΑ
t _{TIMER,START}	Time from START task is given until timer starts counting		0.25		μs



25 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

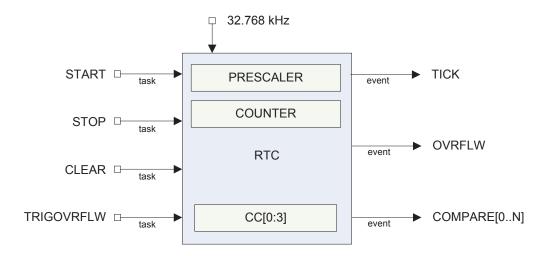


Figure 43: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

25.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be $30.517 \mu s$. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See CLOCK — Clock control on page 87 for more information about clock sources.

25.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

```
f_{RTC} [kHz] = 32.768 / (PRESCALER + 1 )
```

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

$$f_{RTC} = 99.9 \text{ Hz}$$



10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round(32.768 kHz / 8 Hz) - 1 = 4095

 $f_{RTC} = 8 Hz$

125 ms counter period

Table 42: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 μs	512 seconds
28-1	7812.5 μs	131072 seconds
2 ¹² -1	125 ms	582.542 hours

25.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

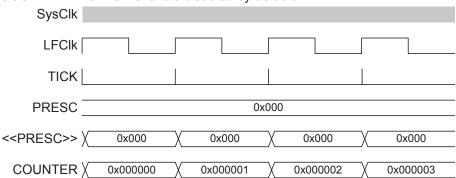


Figure 44: Timing diagram - COUNTER_PRESCALER_0

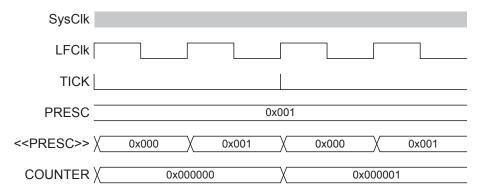


Figure 45: Timing diagram - COUNTER_PRESCALER_1

25.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

Important: The OVRFLW event is disabled by default.

25.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.



Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

25.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Peripheral interface* on page 58. The RTC task and event system is illustrated in *Figure 46: Tasks, events and interrupts in the RTC* on page 230.

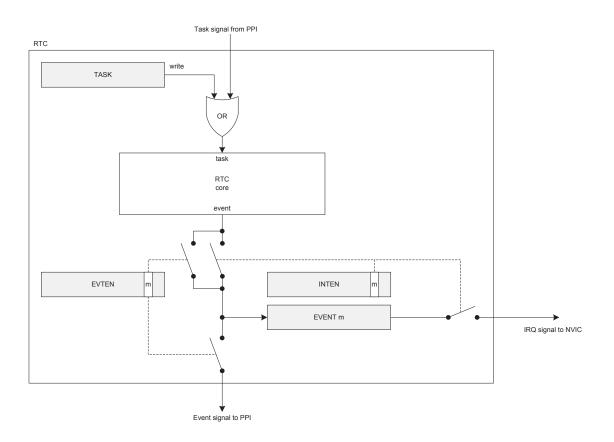


Figure 46: Tasks, events and interrupts in the RTC

25.7 Compare feature

There are a number of Compare registers.

For more information, see *Registers* on page 234.

When setting a compare register, the following behavior of the RTC compare event should be noted:

• If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.



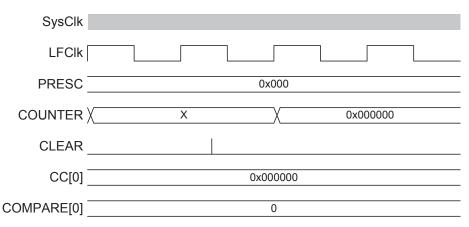


Figure 47: Timing diagram - COMPARE_CLEAR

 If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

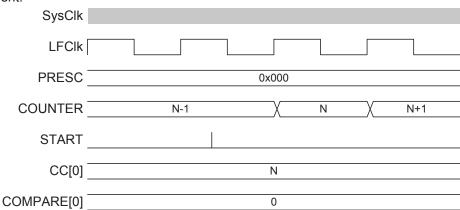


Figure 48: Timing diagram - COMPARE_START

• COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

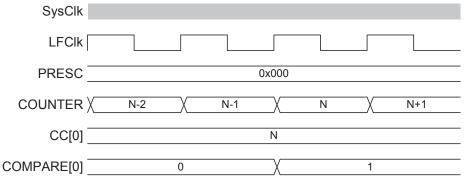


Figure 49: Timing diagram - COMPARE

• If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.



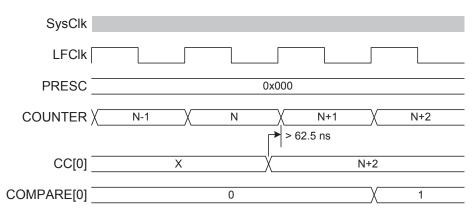


Figure 50: Timing diagram - COMPARE_N+2

• If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

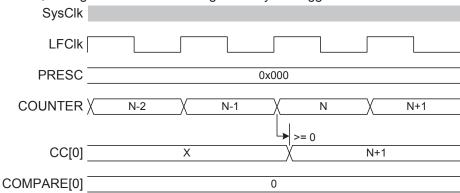


Figure 51: Timing diagram - COMPARE_N+1

• If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

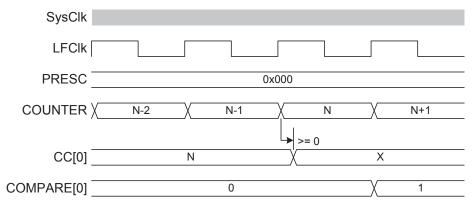


Figure 52: Timing diagram - COMPARE_N-1

25.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.



Table 43: RTC jitter magnitudes on tasks

 Task
 Delay

 CLEAR, STOP, START, TRIGOVRFLOW
 +15 to 46 μs

Table 44: RTC jitter magnitudes on events

Operation/Function	Jitter
START to COUNTER increment	+/- 15 μs
COMPARE to COMPARE 21	+/- 62.5 ns

1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 μ s and 45.7755 μ s – rounded to 15 μ s and 46 μ s for the remainder of the section.

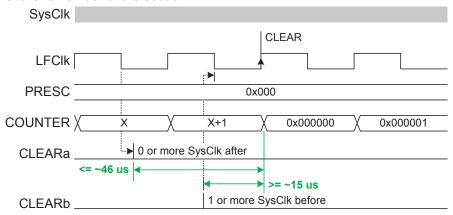


Figure 53: Timing diagram - DELAY_CLEAR

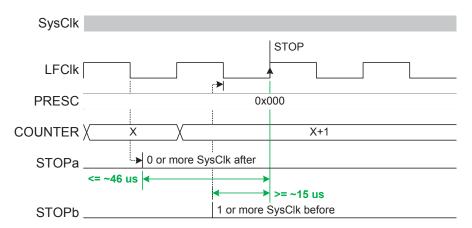


Figure 54: Timing diagram - DELAY_STOP

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 μs +/-15 μs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 μs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 μs jitter on the first COUNTER increment.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

Assumes RTC runs continuously between these events.



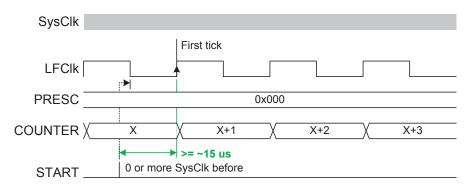


Figure 55: Timing diagram - JITTER_START-

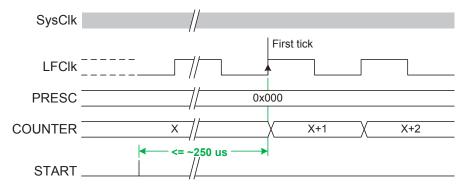


Figure 56: Timing diagram - JITTER_START+

25.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

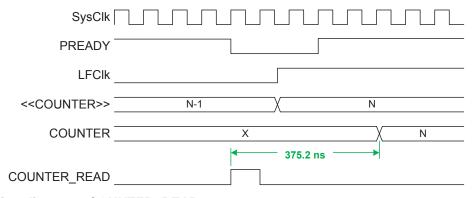


Figure 57: Timing diagram - COUNTER_READ

25.10 Registers

Table 45: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[02] implemented, CC[3] not
				implemented
0x40011000	RTC	RTC1	Real-time counter 1	CC[03] implemented



Table 46: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is
		stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

25.10.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TICK			Write '1' to Enable interrupt for TICK event
			See EVENTS_TICK
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW OVRFLW			Write '1' to Enable interrupt for OVRFLW event
			See EVENTS_OVRFLW
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW COMPAREO			Write '1' to Enable interrupt for COMPARE[0] event
			See EVENTS_COMPARE[0]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
			See EVENTS_COMPARE[1]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW COMPARE2			Write '1' to Enable interrupt for COMPARE[2] event

See EVENTS_COMPARE[2]



Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARE3			Write '1' to Enable interrupt for COMPARE[3] event
			See EVENTS_COMPARE[3]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

25.10.2 INTENCLR

Address offset: 0x308

Disable interrupt

		c interrupt																															
Bit	numbe	er		31	. 30	29 2	28 2	7 2	6 25	5 24	2:	3 2	22 21	20	19	18	17	16	15	14	13	12	1	1 10	9	8	7	6	5	4	3 2	2 1	L O
Id															F	Ε	D	С														E	3 A
Res	et 0x0	0000000		0	0	0	0 (0	0	0	0)	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	alue						D)es	scriptio	n																			
Α	RW	TICK									W	Vri	ite '1' t	о [Disal	ole	int	err	upt	fo	r TIO	CK (eve	nt									
											Se	ee	e EVEN	TS_	TIC	K																	
			Clear	1							D)isa	able																				
			Disabled	0							R	ea	ad: Disa	able	ed																		
			Enabled	1							R	ea	ad: Ena	ble	ed																		
В	RW	OVRFLW									W	Vri	ite '1' t	о [Disal	ole	int	err	upt	fo	٥١	/RF	LW	ev/	ent								
											Se	ee	e EVENT	TS	OV	RFL	w																
			Clear	1									able																				
			Disabled	0							R	lea	ad: Disa	able	ed																		
			Enabled	1							R	lea	ad: Ena	ble	ed																		
С	RW	COMPARE0									W	Vri	ite '1' t	о [Disal	ole	int	err	upt	fo	· CC	M	PAI	RE[C)] ev	ent							
											Se	66	e EVEN	TS	col	MР	ARI	-[0	1														
			Clear	1									able	_	.00.			. [°.	,														
			Disabled	0									ad: Disa	able	ed																		
			Enabled	1							R	ea	ad: Ena	ble	ed																		
D	RW	COMPARE1									W	Vri	ite '1' t	о [Disal	ole	int	err	upt	fo	CC	M	PAI	RE[1	.] ev	ent							
											Se	ee	e EVENT	TS	coi	MР	ARI	-[1	1														
			Clear	1									able	_	.00.			-1	,														
			Disabled	0									ad: Disa	able	ed																		
			Enabled	1							R	ea	ad: Ena	ble	ed																		
Е	RW	COMPARE2									W	Vri	ite '1' t	о [Disal	ole	int	err	upt	fo	· CC	M	PAI	RE[2	!] e\	ent							
											Si	66	e EVENT	TS	col	MР	ΔRI	-[2	1														
			Clear	1									able	,	_00,	****	, 1, 1,	-L	1														
			Disabled	0									ad: Disa	able	ed																		
			Enabled	1									ad: Ena																				
F	RW	COMPARE3											ite '1' t			ole	int	err	upt	fo	· CC	M	PAI	RE[3	s] ev	ent							
			Clear	1									e <i>EVEN</i> able	13_	.001	VIP.	ANI	.[3	I														
			Disabled	0									ad: Disa	able	ьd																		
			Enabled	1									ad: Ena																				
			2.103100	-								cu	.a. Lila	٠.٠																			

25.10.3 EVTEN

Address offset: 0x340



Enable or disable event routing

Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW TICK			Enable or disable event routing for TICK event
				See EVENTS_TICK
		Disabled	0	Disable
		Enabled	1	Enable
В	RW OVRFLW			Enable or disable event routing for OVRFLW event
				See EVENTS_OVRFLW
		Disabled	0	Disable
		Enabled	1	Enable
С	RW COMPAREO			Enable or disable event routing for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Disabled	0	Disable
		Enabled	1	Enable
D	RW COMPARE1			Enable or disable event routing for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Disabled	0	Disable
		Enabled	1	Enable
Ε	RW COMPARE2			Enable or disable event routing for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Disabled	0	Disable
		Enabled	1	Enable
F	RW COMPARE3			Enable or disable event routing for COMPARE[3] event
				See EVENTS_COMPARE[3]
		Disabled	0	Disable
		Enabled	1	Enable

25.10.4 EVTENSET

Address offset: 0x344 Enable event routing

Bit	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	RW	TICK			Write '1' to Enable event routing for TICK event
					See EVENTS_TICK
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	OVRFLW			Write '1' to Enable event routing for OVRFLW event
					See EVENTS_OVRFLW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPAREO			Write '1' to Enable event routing for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable event routing for COMPARE[1] event
0	11.00	COIVII AILLI			Write I to Eliable event routing for colvil ARE[1] event



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14	4 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		F E D C	В А
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description	
		See EVENTS_COMPARE[1]	
	Set	1 Enable	
	Disabled	0 Read: Disabled	
	Enabled	1 Read: Enabled	
E RW COMPARE2		Write '1' to Enable event routin	ng for COMPARE[2] event
		See EVENTS_COMPARE[2]	
	Set	1 Enable	
	Disabled	0 Read: Disabled	
	Enabled	1 Read: Enabled	
F RW COMPARE3		Write '1' to Enable event routin	ng for COMPARE[3] event
		See EVENTS_COMPARE[3]	
	Set	1 Enable	
	Disabled	0 Read: Disabled	
	Enabled	1 Read: Enabled	

25.10.5 EVTENCLR

Address offset: 0x348

Disable event routing

Bit	numbe	er .		31	30.7	29 2	8 27	7 26	25	24.2	23	22 21	20	19	18	17	16	15	14	13	12	11 -	10	9	8	7	6	5	4	3 2	1	. 0
Id		-		01	50.											D									Ŭ		Ŭ	J		-	В	
	et OxO	0000000		0	0	0 (0 0	0	0	0 (0	0 0	0					0	0	0	0	0	0	0	0	0	0	0	0	0 0		0
Id		Field	Value Id		lue			Ť				scription			_	_	_	_	Ť	_	•		•	_	•	•	•	_				
Α	RW	TICK								٧	Wri	ite '1'	to [Disal	ble	eve	nt	rou	tin	g fo	r TI	CK e	ever	nt								
										S	See	e <i>EVEN</i>	ITS	TIC	K																	
			Clear	1								able																				
			Disabled	0								ad: Dis	sable	ed																		
			Enabled	1						F	Rea	ad: Ena	able	ed																		
В	RW	OVRFLW								٧	Wri	ite '1' 1	to [Disal	ble	eve	nt	rou	tin	g fo	r O'	VRF	LW	eve	ent							
										ç	مم۶	e EVEN	ITS	OV	RFI	147																
			Clear	1								able	113_	_001																		
			Disabled	0								ad: Dis	sable	ed																		
			Enabled	1								ad: Ena																				
С	RW	COMPARE0								٧	Wri	ite '1'	to [Disal	ble	eve	nt	rou	tin	g fo	r C(OMF	PAR	E[0)] e	/en	t					
										ς	See	e <i>EVEN</i>	ITS	coi	MР	ΔRF	ะเกา															
			Clear	1								able	.,,_	_001	•	, ,,,,	.[0]															
			Disabled	0								ad: Dis	sable	ed																		
			Enabled	1						F	Rea	ad: Ena	able	ed																		
D	RW	COMPARE1								٧	Wri	ite '1' 1	to [Disal	ble	eve	nt	rou	tin	g fo	r C(OME	PAR	E[1	.] e	/en	t					
										ç	مم۶	e EVEN	ITS	COL	NΔD	ΔRF	[1]	,														
			Clear	1								able	113_	_001	VIII	ANL	.[±]															
			Disabled	0								ad: Dis	sable	ed																		
			Enabled	1								ad: Ena																				
E	RW	COMPARE2								٧	Wri	ite '1'	to [Disal	ole	eve	nt	rou	tin	g fo	r C(OMF	PAR	E[2	!] e	/en	t					
										ς	See	e EVEN	ıts	coi	MP	ΔRF	[2]															
			Clear	1								able	113_	_001	VIII	ANL.	.[4]															
			Disabled	0								ad: Dis	sable	ed																		
			Enabled	1								ad: Ena																				
F	RW	COMPARE3								٧	Wri	ite '1'	to E	Disal	ble	eve	nt	rou	tin	g fo	r C(OMF	PAR	E[3	s] ev	/en	t					
										c	Sac	e EVEN	ITS	COL	MP	ΔRE	[2]															
			Clear	1								able	113_	_001	VII	ANE	رد].															
			0.00.	_							-136	a Dic																				



Bit number		31 30 29 28 3	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			F E D C
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

25.10.6 COUNTER

Address offset: 0x504 Current COUNTER value

Bit	numbe	er		31 30 29 28 27	7 26 25 24	23 22	21 2	0 19	18 17	16	15 1	4 13	12	11 10	9	8	7	6	5	4 3	2	1	0
Id						А А	A A	A A	A A	Α	A	A А	Α	А А	Α	Α	Α	Α	Α	ΑА	. A	Α	Α
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0	0 0	0	0 0	0	0 (0	0	0 0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value	I	Descri	otion	1															
Α	R	COUNTER				Counte	er val	lue															

25.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18	3 17 16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Id					A A A A A	A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW PRESCAL	ER		Prescaler value			

25.10.8 CC[0]

Address offset: 0x540 Compare register 0

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	6 1	5 14	13	12	11	10	9 8	3 7	7 6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	A	4 Δ	A	Α	Α	Α	A	A A	A A	A	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																	
Α	RW	COMPARE		0 0 0 0 0 0 0 0 0 0 Descr												ıe																

25.10.9 CC[1]

Address offset: 0x544 Compare register 1

Bit	numbe	er		31	30	29	28	27 :	26 2	25 2	24	23 :	22	21	20	19	18	17	16	15 :	14 :	L3 1	.2 1	111	0 9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	Α.	A A	. 4	A	Α	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	COMPARE		Value Descripti Compare												ıe																	

25.10.10 CC[2]

Address offset: 0x548 Compare register 2



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	COMPARE										Cor	npa	re v	valu	ıe																		

25.10.11 CC[3]

Address offset: 0x54C Compare register 3

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (ĺ
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	
Res	et Ox0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ipti	on																				ı
Α	RW	COMPARE										Со	mp	are	val	ue																			1

25.11 Electrical specification

25.11.1 RTC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
Into	Run current Real Time Counter (LECLK source)		0.1		пА



26 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

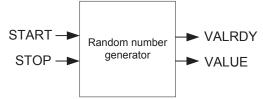


Figure 58: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

26.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

26.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

26.3 Registers

Table 47: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random number generator	

Table 48: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

26.3.1 SHORTS

Address offset: 0x200 Shortcut register



Bi	t nu	mbe	r		31	L 30	29	28	27	⁷ 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	3	7 (5 5	5 4	4 3	2	1	0
Id																																			Α
R	eset	0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () () (0 (0	0	0
Id	- 1	RW	Field	Value Id	Va	alue							De	scri	iptic	n																			
Α	-	RW	VALRDY_STOP										Sh	orto	cut b	etv	wee	n V	ALF	RDY	ev ev	ent	an	d S	ГОР	tas	k								
													See	e <i>EV</i>	/EN	TS_	VAL	.RD	Y aı	nd	TAS	SKS_	ST	OP											
				Disabled	0								Dis	abl	e sh	ort	cut																		
				Enabled	1								En	able	e sh	orto	cut																		

26.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	1 30	29	2	8 2	7	26	25	24	23	22	21	L 20	19	9 1	8 1	17 1	L6	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	() (0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	esci	ipti	ion																					
Α	RW	VALRDY											W	rite	'1'	to	Ena	able	e ir	nter	ru	pt 1	for	VA	LRE	ΟY e	ever	nt									
													Se	e E	VEI	VTS.	_ <i>V</i>	ALF	RDY	/																	
			Set	1									En	abl	e																						
			Disabled	0									Re	ad	Dis	sab	led																				
			Enabled	1									Re	ad	En	abl	ed																				

26.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	umbe	er		31 3	30 2	9 2	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id																																		Α
Res	t 0x0	0000000		0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Valu	ue							De	scri	pti	on																			
Α	RW	VALRDY										Wı	ite	'1'	to [Disa	ble	int	err	upt	for	VΑ	LRE	Υe	ver	it								
												Se	e <i>E</i> \	/EN	ITS_	VA	LRL	ΟY																
			Clear	1								Dis	abl	e																				
			Disabled	0								Re	ad:	Dis	abl	ed																		
			Enabled	1								Re	ad:	Ena	able	ed																		

26.3.4 CONFIG

Address offset: 0x504 Configuration register

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	1 2	20 1	9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	alue	•						Des	crip	tio	n																		
Α	RW	DERCEN										Bia	s coi	rec	ctio	n																	
			Disabled	0								Dis	able	d																			
			Enabled	1								Ena	bled	t																			

26.3.5 VALUE

Address offset: 0x508

Output random number



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id		A A A A A	A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value Description	
A R VALUE		[0255] Generated random number	

26.4 Electrical specification

26.4.1 RNG Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{RNG}	Run current, CPU sleeping.		500		μΑ
t _{RNG,START}	Time from setting the START task to generation begins. This is		128		μs
	a one-time delay on START signal and does not apply between				
	samples.				
t _{RNG,RAW}	Run time per byte without bias correction. Uniform distribution		30		μs
	of 0 and 1 is not guaranteed.				
t _{RNG,BC}	Run time per byte with bias correction. Uniform distribution		120		μs
	of 0 and 1 is guaranteed. Time to generate a byte cannot be				
	guaranteed.				



27 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- · Temperature range is greater than or equal to operating temperature of the device
- · Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK* — *Clock control* on page 87 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

27.1 Registers

Table 49: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature sensor	

Table 50: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of 1st piece wise linear function
A1	0x524	Slope of 2nd piece wise linear function
A2	0x528	Slope of 3rd piece wise linear function
A3	0x52C	Slope of 4th piece wise linear function
A4	0x530	Slope of 5th piece wise linear function
A5	0x534	Slope of 6th piece wise linear function
ВО	0x540	y-intercept of 1st piece wise linear function
B1	0x544	y-intercept of 2nd piece wise linear function
B2	0x548	y-intercept of 3rd piece wise linear function
В3	0x54C	y-intercept of 4th piece wise linear function
B4	0x550	y-intercept of 5th piece wise linear function
B5	0x554	y-intercept of 6th piece wise linear function
TO	0x560	End point of 1st piece wise linear function
T1	0x564	End point of 2nd piece wise linear function
T2	0x568	End point of 3rd piece wise linear function
T3	0x56C	End point of 4th piece wise linear function
T4	0x570	End point of 5th piece wise linear function



27.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	1 30	29	28	8 2	7 2	6 2	5 2	24 2	23 2	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	t 0x0	0000000		0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						ı	Des	crip	otic	n																			
Α	RW	DATARDY										١	Wri	te '	1' t	o E	nak	le i	inte	erru	pt	for	DA [·]	ΓAR	DY	eve	nt								
												9	See	EV	EN	TS_	DA	TAI	RDY	,															
			Set	1								E	Ena	ble																					
			Disabled	0								F	Rea	d: [Disa	ble	ed																		
			Enabled	1								F	Rea	d: E	Ena	ble	d																		

27.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	r		31	. 30	29	28	8 2	7 2	16 2	25	24	23	22	21	20	19	18	3 17	7 1	6 1	5 1	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	•							Des	scri	ptio	on																					
Α	RW	DATARDY											Wr	ite	'1' 1	to [Disa	able	e in	ter	rup	ot f	or	DA	TAI	RD۱	۷ e۱	ent	t								
													See	EV	⁄EN	TS_	DA	\TA	RD	Υ																	
			Clear	1									Dis	able	е																						
			Disabled	0									Rea	ad:	Dis	abl	ed																				
			Enabled	1									Rea	ad:	Ena	able	ed																				

27.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit	numbe	er		31	30	29	28	27	26	25 2	24 :	23 2	22 2	1 2	0 1	9 1	8 1	7 16	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ /	4 Α	Δ Α	A A	A	A	A	Α	Α	Α .	Δ Δ	A	Α	Α	Α	Α	Α	Α.	A A
Res	et 0 x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						- 1	Des	crip	tio	n																	
Α	R	TEMP										Tem	nper	atu	ıre i	n °(0) 3	.25°	ste	eps)												
													ult c									nt. D	ie te	mp	erat	ure	in °	°C, 2	2's			
												Dec	isioi	n po	oint	: D/	AΤΑ	RD۱	1													

27.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id			A A	. A A A A A A A A A
Reset 0x00000326		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 1 0 0 1 1 0
Id RW Field	Value Id	Value	Description	
A RW A0			Slope of 1st piece wise linear function	

27.1.5 A1

Address offset: 0x524



Slope of 2nd piece wise linear function

E	3it nı	umb	er			31	30	29	28	27	26	25 2	24 :	23 2	2 2:	1 20) 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
1	d																								Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	l
F	Rese	t Ox	00	000348		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0 (
1	d	RW	/	Field	Value Id	Va	lue						- 1	Desc	ript	ion	ı																			
7	Δ	RW	,	Δ1										Slon	e of	2n	d ni	ece	wis	e lii	nea	r fu	ncti	ion												1

27.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

Bit r	numbe	er		31 30 29 28 27 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id					A A A A A A A A A A A A A A A A A A A	A A
Rese	et 0x0	00003AA		0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	1 0
Id	RW	Field	Value Id	Value	Description	
Α	RW	A2			Slope of 3rd piece wise linear function	

27.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

Bit	numb	er		31	30	29	28 2	7 26	6 25	5 24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 1	9	8	7	6	5	4	3	2 1	0
Id																						,	Δ Δ	Α	Α	Α	Α	Α	Α	A	Δ Α	АА
Res	et 0x(000040E		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () 1	0	0	0	0	0	0	1	1 1	L O
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	on																		
Α	RW	A3									Slo	pe	of 4	lth i	niec	e w	/ise	lin	ear	fun	ctic	n										

27.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

F	Rit n	umb	or		31	30	29	28 .	77 2	6 2)5 -	2/1	73 -)) ·	21	20	19	12	17	16	15	1/1	13	12	11	10	q	Q	7	6	5	1	3	2	1	\cap
		uiiib	CI		31	. 50	23	20 .	_ / _	-0 2		۷,	25,		۷.	20.	15.	10	Ι/.	10	13	17	13							Ť				_	_	-
1	d																								Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
F	Rese	t Ox	000004BD		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	1
1	d	RW	Field	Value Id	Va	lue						- 1	Des	crip	otic	n																				
-	Α	RW	A4										Slop	oe c	of 5	th p	iec	e w	/ise	lin	ear	fur	ncti	on												_

27.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	/ 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2	1 0
1.1						
Id				AAA	. A A A A A A	A A
Reset 0x000005A3		0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0	1 1 0 1 0 0 0	1 1
Reset 0x000003A3		0 0 0 0	0 0 0 0 0 0 0 0 0	0000010	110100	, 1 1
Id RW Field	Value Id	Value	Description			
	74.40.14	74.40	2000			
A RW A5			Slope of 6th piece wis	e linear function		

27.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function



Bit r	umbe	r		31 30 29 28 27	26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 11 10 9	8 7 6 5	5 4 3 2	1 0
Id						AAAAA	AAAA	AAAA	АА
Res	et 0x0	0003FEF		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1	1 1 1 :	1011	1 1
Id	RW	Field	Value Id	Value	Description				
Α	RW	В0			y-intercept of 1st p	iece wise linear function			

27.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

Bit numb	er		31	30 2	9 2	8 27	26	25 2	24 2	3 2	2 21	20	19	18 1	17 1	6 15	14	13	12	11	10	9	8 7	7	6 5	5 4	3	2	1 0
Id																		Α	Α	Α	Α.	Д	A A	Α.	Δ ,	Δ Δ	Α	Α	A A
Reset 0x	00003FBE		0	0 0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	1	1	1	1	1	1 :	ı	0 1	1 1	1	1	1 0
Id RW	Field	Value Id	Val	lue					0	esc	ripti	on																	
A RW	B1								У	-int	erce	pt o	f 2n	d pi	ece	wise	e lin	ear	fun	ctio	n								

27.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 :	17 :	16 1	.5 1	4 1	3 1	2 1	1 10) 9	8	7	6	5	4	3	2 :	1 0
Id																					,	Α Α	A /	A	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et 0x0	0003FBE		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 :	1	L 1	. 1	1	1	1	0	1	1	1	1 :	1 0
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
Α	RW	B2										y-ir	nter	сер	t of	3rd	iq b	ece	wis	e li	nea	r fu	nct	ion									

27.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Reset 0x00000012		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW B3			y-intercept of 4th piece wise linear function

27.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	L9 1	L8 1	L7 :	16 :	15 :	L4 :	13 :	12 :	11 1	.0	9	8	7	6	5	4	3	2	1 0	
Id																						Α	Α	Α	Δ,	Д	Α	Α	Α	Α	Α	Α	Α.	А А	
Res	et 0x0	0000124		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0 0	
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																				ı
Α	RW	B4										y-in	ter	cep	t of	5th	n pie	ece	wi	se l	inea	ar f	unc	tior											•

27.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

Bit	numb	oer			31	30	29	28 2	27 2	6 2	5 2	4 2	3 22	21	20	19	18	17 :	16 1	L5 1	4 1	3 1	2 11	10	9	8	7	6	5	4	3	2 :	1 0
Id																					A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Res	et 0x	(00	00027C	0	0	0	0	0 (0) (0 (0	0	0	0	0	0	0	0 (0 (0	0	0	1	0	0	1	1	1	1	1 (0 0	
Id	Reset 0x0000027C 0 0 0 Id RW Field Value Id Value												esci	iptio	on																		
Α	RW	/	B5									y.	inte	rce	ot o	f 6t	h pi	ece	wis	se li	nea	r fu	ncti	on									

y-intercept of 6th piece wise linear function



27.1.16 TO

Address offset: 0x560

End point of 1st piece wise linear function

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	⁷ 16	15	14	13 1	L2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																										Α	Α	Α	Α	A A	4 Α	А
Res	et 0x0	00000E2		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	1	1	1	0	0 () 1	. 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	T0										Enc	l poi	int d	of 1	st p	iece	wis	e li	near	fur	ctio	n									

27.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

Bit n	umbe	er		31	30	29	28 2	27 2	26 2	5 2	24 2	3 2	2 2:	1 20) 19	18	17	16	15 1	L4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																										Α	A	A A	A A	Α	Α	Α
Rese	et OxO	0000000		0	0	0	0	0	0 (0	0 (0 (0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
Α	RW	T1									Е	nd	poir	nt of	f 2n	d pi	ece	wis	e lir	near	fun	ctio	n									

27.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																										Α	Α	Α	Α	A A	Α Α	A A
Res	et OxO	0000019		0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	1	1 (0	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	T2											l poi	nt o	of 3	rd p	iec	e wi	se li	nea	r fu	nctio	n									

27.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

Bit	numbe	er		31 30 29 28 2	27 26 25 24	23 22 21 20	19 18 1	7 16 1	5 14 1	.3 12 1	1 10	9	8 7	6	5 4	3	2	1 0
Id													Α	Α	A A	A	Α	A A
Res	et 0x0	000003C		0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 (0 0	0	0 0	0 0	0	0 0	0	1 1	. 1	1	0 0
Id	RW	Field	Value Id	Value		Description												
Α	RW	T3				End point of	4th piec	e wise	linear	functi	on							

27.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A
Reset 0x00000050	0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
A RW T4		End point of 5th piece wise linear function



27.2 Electrical specification

27.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{TEMP}	Time required for temperature measurement		36		μs
T _{TEMP,RANGE}	Temperature sensor range	-40		85	°C
T _{TEMP,ACC}	Temperature sensor accuracy	-5		5	°C
T _{TEMP,RES}	Temperature sensor resolution		0.25		°C
T _{TEMP,STB}	Sample to sample stability at constant device temperature		+/-0.25		°C
T _{TEMP,OFFST}	Sample offset at 25°C	-2.5		2.5	°C



28 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- · Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

28.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

28.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

28.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 51: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block



28.4 Registers

Table 52: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000E000	ECB	ECB	AES Electronic Codebook (ECB) mode blo	ck
			encryption	

Table 53: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

28.4.1 INTENSET

Address offset: 0x304

Enable interrupt

	numbe	r		31	30	29 2	28 2	27 2	26 2	5 24	4 23	3 22	21	20	19	18	17	16	15	14	13	12 :	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																																В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	iptic	on																			
Α	RW	ENDECB									W	/rite	'1' t	o E	nab	le i	nte	rru	pt f	or E	NC	ECE	3 ev	/ent	t								
											Se	ee <i>E</i> \	/EN	TS_	ENL	DEC	В																
			Set	1							Er	nable	е																				
			Disabled	0							Re	ead:	Disa	able	ed																		
			Enabled	1							Re	ead:	Ena	ble	d																		
В	RW	ERRORECB									W	/rite	'1' t	o E	nab	le i	nte	rru	pt f	or E	RR	ORE	CE	eve	ent								
											Se	ee <i>E</i> \	/EN	TS_	ERF	ROR	RECE	3															
			Set	1							Er	nable	9																				
			Disabled	0							Re	ead:	Disa	able	ed																		
			Enabled	1							Re	ead:	Ena	ble	d																		

28.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
Id			B A				
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
Id RW Field	Value Id	Value	Description				
A RW ENDECB		Write '1' to Disable interrupt for ENDECB event					
			See EVENTS_ENDECB				
	Clear	1	Disable				
	Disabled	0	Read: Disabled				
	Enabled	1	Read: Enabled				
B RW ERRORECB			Write '1' to Disable interrupt for ERRORECB event				
			See EVENTS_ERRORECB				
	Clear	1	Disable				
	Disabled	0	Read: Disabled				

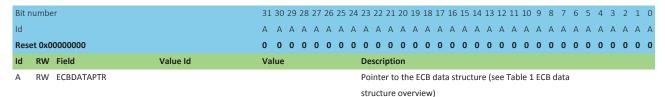


Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 :	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					ВА
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Read: Enabled		

28.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers



28.5 Electrical specification

28.5.1 ECB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{ECB}	Run time per 16 byte block in all modes		6		μs



29 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in *Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification. ²²

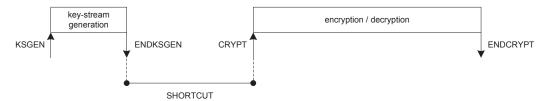


Figure 59: Key-stream generation followed by encryption or decryption. The shortcut is optional.

29.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

29.2 Key-steam generation

A new key-stream needs to be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task and an ENDKSGEN event will be generated when the key-stream has been generated.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by *CNFPTR* on page 261. It is necessary to configure this pointer and its underlying data structure, and the *MODE* on page 260 register before the KSGEN task is triggered.

Bluetooth AES CCM 128 bit block encryption, see Bluetooth Core specification Version 4.0.



The key-stream will be stored in the AES CCM's temporary memory area, specified by the *SCRATCHPTR* on page 261, where it will be used in subsequent encryption and decryption operations.

For default length packets, that is when MODE.LENGTH is set to Default, the size of the generated key-stream is 27 bytes. When using extended length packets, that is when MODE.LENGTH is set to Extended, The *MAXPACKETSIZE* on page 261 register specifies the length of the key-stream to be generated. The length of the generated key-stream must be greater or equal to the length of the subsequent packet payload to be encrypted or decrypted. The maximum length of the key-stream in extended mode is 251 bytes, which means that the maximum packet payload size is 251.

If a shortcut is used between ENDKSGEN event and CRYPT task, the *INPTR* on page 261 pointer and the *OUTPTR* on page 261 pointers must also be configured before the KSGEN task is triggered.

29.3 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

Encryption is started by triggering the CRYPT task with the *MODE* on page 260 register set to ENCRYPTION. An ENDCRYPT event will be generated when packet encryption is completed

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the *OUTPTR* on page 261 pointer, see *Figure 60: Encryption* on page 254.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

The CCM supports different widths of the LENGTH field in the data structure for encrypted packets. This is configured in the *MODE* on page 260 register.

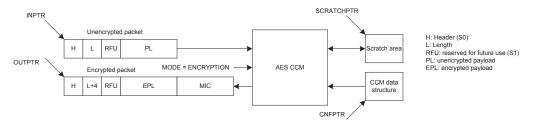


Figure 60: Encryption

29.4 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

Decryption is started by triggering the CRYPT task with the *MODE* on page 260 register set to DECRYPTION. An ENDCRYPT event will be generated when packet decryption is completed

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 61: Decryption* on page 255.

The CCM is only able to decrypt packet payloads that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.



The CCM supports different widths of the LENGTH field in the data structure for decrypted packets. This is configured in the *MODE* on page 260 register.

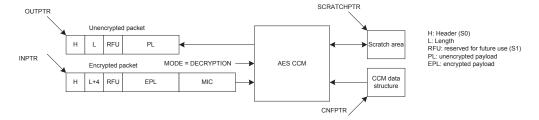


Figure 61: Decryption

29.5 AES CCM and RADIO concurrent operation

The CCM module is able to encrypt/decrypt data synchronously to data being transmitted or received on the radio.

In order for the CCM module to run synchronously with the radio, the data rate setting in the *MODE* on page 260 register needs to match the radio data rate. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered.

The data rate setting of the *MODE* on page 260 register can also be overridden on-the-fly during an ongoing encrypt/decrypt operation by the contents of the *RATEOVERRIDE* on page 262 register. The data rate setting in this register applies whenever the RATEOVERRIDE task is triggered. This feature can be useful in cases where the radio data rate is changed during an ongoing packet transaction.

29.6 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the radio is transmitting it, the radio must read the encrypted packet from the same memory location as the AES CCM is writing to.

The *OUTPTR* on page 261 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the radio, see *Figure 62: Configuration of on-the-fly encryption* on page 255.

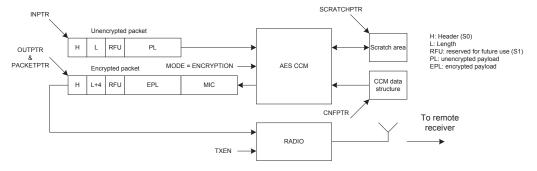


Figure 62: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the encryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 63: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection* on page 256 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the TXEN task in the RADIO is triggered.



Important: Refer to *Timing specification* on page 262 for information about the time needed for generating a key-stream.

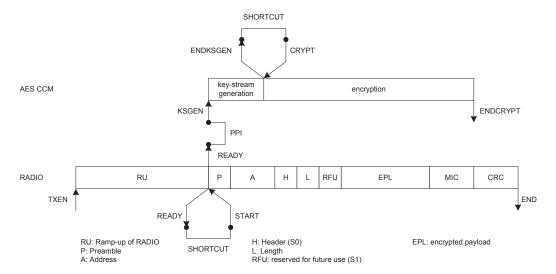


Figure 63: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection

29.7 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The *INPTR* on page 261 pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 64: Configuration of on-the-fly decryption* on page 256.

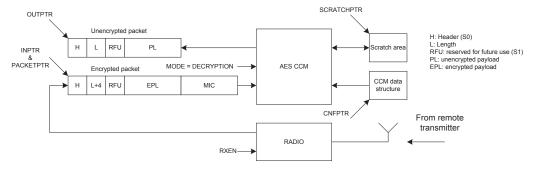


Figure 64: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the decryption of the packet shall start.

For short packets, that is when MODE.LENGTH = Default, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 65: On-the-fly decryption of short packets (MODE.LENGTH = Default)* using a PPI connection on page 257 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.

For long packets, that is when MODE.LENGTH = Extended, the key-stream generation will need to be started even earlier, for example at the time when the RXEN task in the RADIO is triggered.



Important: Refer to *Timing specification* on page 262 for information about the time needed for generating a key-stream.

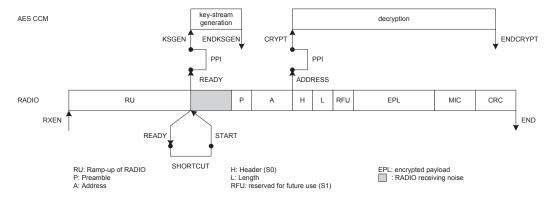


Figure 65: On-the-fly decryption of short packets (MODE.LENGTH = Default) using a PPI connection

29.8 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 54: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant
		bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV,, Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 54: CCM data structure overview* on page 257.

Table 55: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 56: Data structure for encrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in encrypted payload including length of MIC
		Important: LENGTH will be 0 for empty packets since the MIC is not added to empty
		packets
RFU	2	Reserved Future Use



Property	Address offset	Description
PAYLOAD	3	Encrypted payload
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC

Important: MIC is not added to empty packets

29.9 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In cases where the CPU and other EasyDMA enabled peripherals are accessing the same RAM block at the same time, a high level of bus collisions may cause too slow operation for correct on the fly encryption. In this case the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

29.10 Registers

Table 57: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4000F000	CCM	CCM	AES CCM mode encryption		

Table 58: Register Overview

Register	Offset	Description	
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.	
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.	
TASKS_STOP	0x008	Stop encryption/decryption	
TASKS_RATEOVERRIDE	0x00C	Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for	
		any ongoing encryption/decryption	
EVENTS_ENDKSGEN	0x100	Key-stream generation complete	
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete	
EVENTS_ERROR	0x108	CCM error event	Deprecated
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
MICSTATUS	0x400	MIC check result	
ENABLE	0x500	Enable	
MODE	0x504	Operation mode	
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector	
INPTR	0x50C	Input pointer	
OUTPTR	0x510	Output pointer	
SCRATCHPTR	0x514	Pointer to data area used for temporary storage	
MAXPACKETSIZE	0x518	Length of key-stream generated when MODE.LENGTH = Extended.	
RATEOVERRIDE	0x51C	Data rate override setting.	

29.10.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	l8 1	.7 1	6 15	5 14	13	12	11 1	0 9	9 8	7	6	5	4	3	2	1 0
Id																																Α
Re	set 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	scrip	otio	n																	
Α	RW	ENDKSGEN_CRYPT										Sho	ortcı	ut b	etw	vee	n EN	NDK:	SGE	N e	ven	and	d CR	YPT	tas	k						
												See	e EV	EN1	TS_I	END	KSC	GEN	and	t TA	SKS _.	_CR	YPT									
			Disabled	0								Dis	able	sh	orto	cut																
			Enabled	1								Ena	able	sho	ortc	ut																

29.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	30	29	28 2	27 2	6 25	5 24	23 2	2 2	1 20	19	18	17	16	15	14 :	13 1	2 1:	l 10	9	8	7 (5 5	4	3	2	1 0
Id																													С	ВА
Res	et 0x0	0000000		0	0	0	0 (0 (0 0	0	0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0) (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	crip	tion																	
Α	RW	ENDKSGEN									Writ	e '1	' to	Enal	ble	inte	rru	pt f	or E	NDI	(SGI	N e	vent	t						
											See	EVE	NTS	_EN	DKS	GEI	V													
			Set	1							Enab	ole																		
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: Ei	nabl	ed																
В	RW	ENDCRYPT									Writ	e '1	l' to	Enal	ble	inte	rru	pt f	or E	NDO	CRYF	T ev	ent							
											See	EVE	NTS	_EN	DCI	RYPT	г													
			Set	1							Enab	ole																		
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: Ei	nabl	ed																
С	RW	ERROR									Writ	e '1	' to	Enal	ble	inte	rru	pt f	or E	RRC)R e	vent								
											See	EVE	NTS	_ER	ROF	?														
			Set	1							Enak	ole																		
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: Ei	nabl	ed																

29.10.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW ENDKSGEN			Write '1' to Disable interrupt for ENDKSGEN event
				See EVENTS_ENDKSGEN
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDCRYPT			Write '1' to Disable interrupt for ENDCRYPT event
				See EVENTS_ENDCRYPT
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ERROR			Write '1' to Disable interrupt for ERROR event
				See EVENTS_ERROR
		Clear	1	Disable
		Disabled	0	Read: Disabled



Bit number		31 30 29 28 27 2	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id			C B A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	1	Read: Enabled

29.10.4 MICSTATUS

Address offset: 0x400 MIC check result

it nı	umbe	r		31	. 30	29	28	27	26	25	24	23	22 :	21 :	20	19 :	18 1	17 1	16 :	15 1	.4 1	.3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1	0
ł																																		Α
ese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
ł	RW	Field	Value Id	Va	llue							Des	scrip	ptio	n																			
	R	MICSTATUS										The	res	sult	of	the	MI	C ch	ecl	к ре	rfo	rme	ed c	lurir	g tl	ne p	rev	ious	S					
												ded	ryp	tior	n op	oera	tioi	า																
			CheckFailed	0								MI	C ch	eck	fai	led																		
			CheckPassed	1								MI	C ch	eck	ра	sse	d																	
	d	eset 0x0	d RW Field	deset 0x00000000 d RW Field Value Id A R MICSTATUS CheckFailed					Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000	Reset 0x000000000	Reset 0x0000000000000000000000000000000000	Reset 0x000000000	Reset 0x00000000000000000000000000000000000											

29.10.5 ENABLE

Address offset: 0x500

Enable

Bit	numb	ber			3	1 3	0 29	9 2	8 2	7 2	26 2	25 2	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																				А А
Res	et 0x	(00	000000		0	0	0	0) () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	V F	Field	Value Id	٧	alu	е						- 1	Des	cri	ptio	on																			
Α	RW	V E	ENABLE											Ena	ble	or	dis	abl	e C	CM																
				Disabled	0									Disa	able	9																				
				Enabled	2									Ena	ble																					

29.10.6 MODE

Address offset: 0x504 Operation mode

Bit	numbe	er		31	. 30	29	28 2	27 2	26 2	5 2	4 23	22	21 2	20 :	19 1	8 1	7 16	15	14	13 1	.2 1	1 10	9	8	7	6	5 4	1 3	2	1	0
Id										(0					E	3 B														Α
Res	et 0x0	0000001		0	0	0	0	0	0 0) (0 0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	1
Id	RW	Field	Value Id	Va	lue						De	escri	ptio	n																	
Α	RW	MODE									Th	e m	ode	of	ope	ratio	on to	be	use	d. T	he s	ettin	gs i	n th	is re	egis	ter				Τ
											apı	ply	whe	nev	ver e	eithe	er th	e K	SGE	V or	CRY	PT t	asks	are	trig	ggei	red.				
			Encryption	0							ΑE	S CC	CM p	pacl	ket e	encr	ypti	on i	nod	e											
			Decryption	1							ΑE	S CC	CM p	pacl	ket (decr	ypti	on i	nod	e											
В	RW	DATARATE									Ra	dio	data	a ra	te th	nat 1	the (CCIV	1 sha	ıll ru	ın sy	nchi	onc	ous v	with	1					
			1Mbit	0							1 N	Mbp	S																		
			2Mbit	1							2 N	Mbp	S																		
			125Kbps	2							12	5 Kb	ps																		
			500Kbps	3							50	0 Kb	ps																		
С	RW	LENGTH									Pa	cket	len	gth	cor	nfigu	ırati	on													
			Default	0							De	efaul	t ler	ngtl	h. Ef	fect	ive	leng	th c	f LE	NGT	H fie	ld ii	n en	cry	pte	d/				
											de	cryp	ted	pa	cket	is 5	bits	s. A	key-	stre	am 1	or p	ack	et p	aylo	oads	s up				
											to	27 k	yte	s w	ill b	e ge	nera	atec	l.												
			Extended	1							Ext	tenc	ded l	len	gth.	Effe	ectiv	e le	ngth	of	LENG	HT	field	d in	enc	rypt	ted/	,			
											de	cryp	ted	pa	cket	is 8	bits	s. A	key-	stre	am i	or p	ack	et p	aylo	oads	s up				
											to	MA	XPA	CKE	ETSI	ZE b	ytes	wil	l be	gen	erat	ed.									



29.10.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bit r	umbe	er		31	. 30	29	9 2	8 2	27 2	26 2	25	24	23	22	21	20	19	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	. A	Δ /	Α .	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	t OxO	0000000		0	0	0	() (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	•							Des	scri	ptic	on																				
Α	RW	CNFPTR											Poi	nte	r to	the	e da	ita s	tru	ctu	re l	nol	din	g th	e A	ES	key	an	d th	ne C	CCN	/				_
															E ve																					

29.10.8 INPTR

Address offset: 0x50C

Input pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW INPTR	<u> </u>	Input pointer

29.10.9 OUTPTR

Address offset: 0x510

Output pointer

Bit n	umbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id				A A A A A A A A A A A A A A A A A A A	Α
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id	RW	Field	Value Id	Value Description	
Α	RW	OUTPTR		Output pointer	

29.10.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW SCRATCHPTR		Pointer to a scratch data area used for temporary storage
		during key-stream generation, MIC generation and encryption/
		decryption.
		The scratch area is used for temporary storage of data during
		The scratch area is used for temporary storage of data during
		key-stream generation and encryption.
		When MODE.LENGTH = Default, a space of 43 bytes is required
		for this temporary storage. MODE.LENGTH = Extended (16 +
		MAXPACKETSIZE) bytes of storage is required.

29.10.11 MAXPACKETSIZE

Address offset: 0x518

Length of key-stream generated when MODE.LENGTH = Extended.



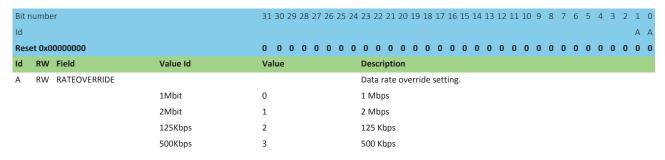
Bit r	umbe	r		31 30	29 2	8 27	26	25 2	24 2	23 2	2 21	. 20	19	18 17	7 16	15	14	13 1	2 11	. 10	9	8	7 6	5	4	3	2	1 0
Id																						A	Α Α	A A	Α	Α	A	А А
Res	et 0x0	00000FB		0 0	0 (0 0	0	0	0	0 (0	0	0	0 0	0	0	0	0 (0 0	0	0	0 :	L 1	1	1	1	0	1 1
Id	RW	Field	Value Id	Value					0	esc	ripti	ion																
Α	RW	MAXPACKETSIZE		[0x001	LBO	x00F	B]		L	.eng	th o	f ke	y-str	eam	ger	era	ted v	whe	n M	DDE.	LEN	GTH	ł					
									=	Ext	end	ed. ⁻	This	valu	e m	ust l	oe g	reat	er or	equ	al t	o th	e					
									S	ubs	eque	ent p	oack	et pa	aylo	ad t	o be	enc	rypt	ed/d	lecr	ypte	d.					

29.10.12 RATEOVERRIDE

Address offset: 0x51C

Data rate override setting.

Override value to be used instead of the setting of MODE.DATARATE. This override value applies when the RATEOVERRIDE task is triggered.



29.11 Electrical specification

29.11.1 Timing specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{kgen}	Time needed for key-stream generation (given priority access to				μs
	destination RAM block).				



30 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

30.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

30.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

30.3 Resolving a resolvable address

As per Bluetooth specification, a private resolvable address is composed of six bytes.

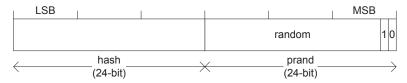


Figure 66: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification²³. The time it takes to resolve an address may vary depending on where in the list the

Bluetooth Specification Version 4.0 [Vol 3] chapter 10.8.2.3.



resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

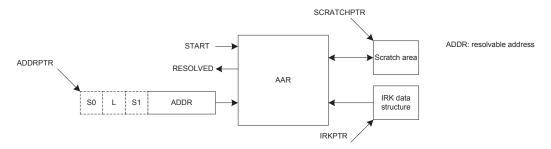


Figure 67: Address resolution with packet preloaded into RAM

30.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

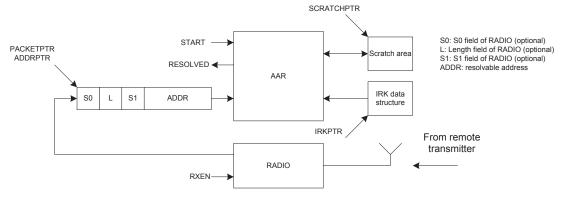


Figure 68: Address resolution with packet loaded into RAM by the RADIO

30.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 59: IRK data structure overview

Property	Address offset	Description
IRKO	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
IRK15	240	IRK number 15 (16 - byte)



30.6 Registers

Table 60: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Accelerated address resolver	

Table 61: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

30.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW RESOLVED			Write '1' to Enable interrupt for RESOLVED event
				See EVENTS_RESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW NOTRESOLVED			Write '1' to Enable interrupt for NOTRESOLVED event
				See EVENTS_NOTRESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

30.6.2 INTENCLR

Address offset: 0x308 Disable interrupt



Di+ ı	numbe	ar.		21	20	20	20.	77 -	26 21	E 2/	1 23 2	77 1	21 21	n 10	10	17	16	10	11	10 1	1 2 1	1 10	0	8	7	6	5 4	. 3	2	1 0
	lullibe	:1		31	30	25	20 1	21 2	20 2.	3 24	+ 23 .	ZZ 2	21 21	0 13	7 10) 1/	10	13	14	15.	12 1	1 10	9	0	/	O	<i>3</i> 4	. 5	2	1 0
Id																													С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	crip	otion	1																
Α	RW	END									Wri	te '	1' to	Dis	able	int	err	upt	for	END	eve	ent								
											See	EVI	ENTS	S_ <i>EI</i>	VD															
			Clear	1							Disa	able																		
			Disabled	0							Rea	ıd: E	Disab	led																
			Enabled	1							Rea	ıd: E	nab	led																
В	RW	RESOLVED									Wri	te '	1' to	Dis	able	e int	err	upt	for	RES	OLV	ED e	ven	t						
											See	EVI	ENTS	S_RE	SO	LVE	D													
			Clear	1							Disa	able																		
			Disabled	0							Rea	ıd: [Disab	oled																
			Enabled	1							Rea	ıd: E	nab	led																
С	RW	NOTRESOLVED									Wri	te '	1' to	Dis	able	int	err	upt	for	NO	TRES	OLV	ED 6	ever	nt					
											See	EVI	ENTS	5_ <i>N</i> (OTR	ESC	DLVI	ED												
			Clear	1							Disa	able																		
			Disabled	0							Rea	ıd: [Disab	led																
			Enabled	1							Rea	ıd: E	nab	led																

30.6.3 STATUS

Resolution status

Address offset: 0x400

Bit	numbe	er		31	30	29 2	28 2	7 26	25	24	23 2	22 2	1 2	0 19	18	17	16	15 1	4 13	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id																												Δ	А	Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 () (0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Val	lue						Des	crip	tior	1																	
Α	R	STATUS		[0	15]						The	IRK	tha	it wa	ıs u	sed	last	tim	e an	add	res	s wa	s re	esol	vec	i					

30.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit	numb	er		31 3	0 29	28	27	26	25	24	23	22	21 2	20 1	19 1	.8 1	.7 1	6 1	L5 1	L4 1	L3 1	.2 1	11 1	0 9	9 8	3 7	6	5	4	3	2	1 0
Id																																А А
Res	et 0x	00000000		0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0) (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	e						De	scri	otio	n																		
Α	RW	ENABLE									Ena	ble	or	disa	ble	ΑА	R															
			Disabled	0							Dis	able	2																			
			Enabled	3							Ena	able																				

30.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Reset 0x00000001		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW NIRK		[116]	Number of Identity root keys available in the IRK data structure

30.6.6 IRKPTR

Address offset: 0x508



Pointer to IRK data structure

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 :	16 1	L5 1	14 1	.3 1	.2 1	1 1) 9	8	7	6	5	4	3	2	1	O
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	A .	Δ,	Δ,	Δ Δ		A	A	Α	Α	Α	Α	Α	A	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	O
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	IRKPTR										Poi	nte	r to	the	e IR	K da	ata	stru	ıctu	re													_

30.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW ADDRPTR		Pointer to the resolvable address (6-bytes)

30.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numl	ber	r		33	1 30	29	28	27	⁷ 26	25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14 :	L3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A A	A	Α	Α	Α	Α	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	ΑА	Α Δ	АА
Res	et 0	x00	0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RV	N	Field	Value Id	Value Description																												
Α	RV	٧	SCRATCHPTR										Poi	nter	to a	scr	atc	h da	ata a	area	use	d fo	r te	emp	orar	y st	ora	ge					
													dur	ing r	eso	luti	on.	A sp	ace	of r	nini	mur	n 3	byte	s m	ust	be						
													resi	erve	Н																		

30.7 Electrical specification

30.7.1 AAR Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{AAR}	Address resolution time per IRK. Total time for several IRKs				μs
	is given as (1 μ s + n * t_AAR), where n is the number of IRKs.				
	(Given priority to the actual destination RAM block).				
t _{AAR,8}	Time for address resolution of 8 IRKs. (Given priority to the		48		μs
	actual destination RAM block).				



31 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Listed here are the main features for the SPIM

- SPI mode 0-3
- · EasyDMA direct transfer to/from RAM for both SPI Slave and SPI Master
- · Individual selection of IO pin for each SPI signal

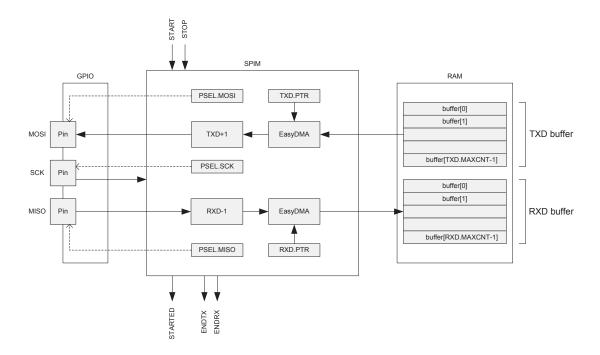


Figure 69: SPIM — SPI master with EasyDMA

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPIM supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 62: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA	
SPI_MOI	DEI 0 (Active High)	0 (Leading)	
SPI_MOI	DE 0 (Active High)	1 (Trailing)	
SPI_MOI	DE: 1 (Active Low)	0 (Leading)	
SPI MOI	DE: 1 (Active Low)	1 (Trailing)	

31.1 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.



Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

31.2 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 69: SPIM* — *SPI master with EasyDMA* on page 268. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

31.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

· Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];
```



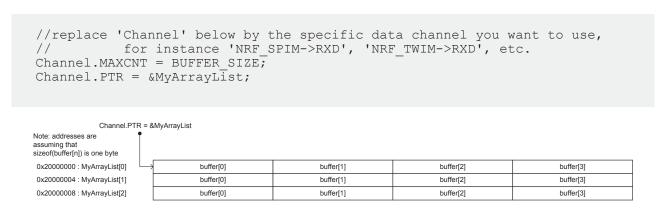


Figure 70: EasyDMA array list

31.3 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of events, and finally the STOP task.

An SPI master transaction is started by triggering the START task. The ENDTX event will be generated when the transmitter has transmitted all bytes in the TXD buffer as specified in the TXD.MAXCNT register. The ENDRX event will be generated when the receiver has filled the RXD buffer, i.e. received the last possible byte as specified in the RXD.MAXCNT register.

Following a START task, the SPI master will generate an END event when both ENDRX and ENDTX have been generated.

The SPI master is stopped by triggering the STOP task. A STOPPED event is generated when the SPI master has stopped.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDRX event explicitly even though the RX buffer is not full.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 71: SPI master transaction* on page 271.



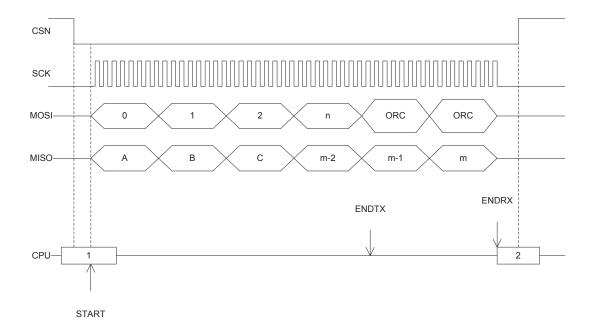


Figure 71: SPI master transaction

31.4 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

31.5 Master mode pin configuration

The SCK, MOSI, and MISO signals associated with the SPI master are mapped to physical pins according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively.

The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 63: GPIO configuration* on page 271 prior to enabling the SPI. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 63: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL	
MOSI	As specified in PSEL.MOSI	Output	0	
MISO	As specified in PSEL.MISO	Input	Not applicable	



31.6 Registers

Table 64: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40004000	SPIM	SPIM0	SPI master	

Table 65: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Over-read character. Character clocked out in case and over-read of the TXD buffer.

31.6.1 SHORTS

Address offset: 0x200

Shortcut register

Bi	t nur	mbe	r		31	. 30	29	28	27	26	25	24	23	22	2 2 1	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																			Α																
Re	eset (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	R	RW	END_START										Sho	ort	cut	bet	we	en	ENI) ev	ent	an	d S	ΓAR	T ta	sk									
													See	e <i>E</i>	VEN	ITS_	_EN	ID a	and	TAS	SKS_	ST	ART	-											
				Disabled	0								Dis	ab	le sl	nor	tcu	t																	
				Enabled	1								Ena	abl	le sh	ort	tcut																		

31.6.2 INTENSET

Address offset: 0x304

Enable interrupt



Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW STOPPED			Write '1' to Enable interrupt for STOPPED event
			See EVENTS_STOPPED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ENDRX			Write '1' to Enable interrupt for ENDRX event
			See EVENTS_ENDRX
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Enable interrupt for END event
			See EVENTS_END
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW ENDTX			Write '1' to Enable interrupt for ENDTX event
			See EVENTS_ENDTX
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW STARTED			Write '1' to Enable interrupt for STARTED event
			See EVENTS_STARTED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

31.6.3 INTENCLR

Address offset: 0x308 Disable interrupt

Rit	numbe	er .		31 30 29 28 27 26 25 2/	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iuiiibe	=1		31 30 29 28 27 20 23 24	
Res		0000000		0 0 0 0 0 0 0 0	
Id	RW	Field	Value Id	Value	Description
Α	RW	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ENDRX			Write '1' to Disable interrupt for ENDRX event
					See EVENTS_ENDRX
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	ENDTX			Write '1' to Disable interrupt for ENDTX event
					See EVENTS_ENDTX



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW STARTED			Write '1' to Disable interrupt for STARTED event
			See EVENTS_STARTED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

31.6.4 ENABLE

Address offset: 0x500

Enable SPIM

Bi	nu	mbe	r		31	. 30	29	28	27	26	6 25	5 24	4 2	3 2	2 2	1 2	0 1	9 1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α	Α	Α
Re	set	0x0	0000000		0 0 0 0 0 0 0 0 Value						0) (0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Id		RW	Field	Value Id	Va	alue	9						D	esc	rip	tio	1																				
Α		RW	ENABLE										Ε	nab	le d	or c	lisa	ble	SP	IM																	
				Disabled	0								D	isal	ble	SPI	M																				
				Enabled	7								Ε	nab	le S	SPII	VI																				
				Enabled	7								Е	nab	le S	SPII	VI																				

31.6.5 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	11111111111111111111111111111
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.6 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal

Bit	numbe	er		31 30 29 28 27 26	25 24	4 23	22 2	21 2	0 19	18 3	17 16	5 15	14 13	3 12	11 10	9	8	7	6	5 4	3	2	1 0
Id				С																Δ	Α	Α	А А
Res	et 0xF	FFFFFF		1 1 1 1 1 1	1 1	۱ 1	1	1 1	l 1	1	1 1	1	1 1	1	1 1	1	1	1	1	1 1	1	1	1 1
Id	RW	Field	Value Id	Value		De	scrip	tion	1														
Α	RW	PIN		[031]		Pin	nun	nbei	r														
С	RW	CONNECT				Coi	nnec	tion	1														
			Disconnected	1		Dis	conr	nect															
			Connected	0		Coi	nnec	:t															

31.6.7 PSEL.MISO

Address offset: 0x510
Pin select for MISO signal



Bit	numbe	er		31	. 30	29	28	27	26 2	25	24	23 2	22 2	1 2	0 1	.9 1	.8 1	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	. 1	0
Id				С																									Α	А А	A	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	1	1 :	1 1	. 1	1	1	1 :	L 1	. 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	PIN		[0	31]							Pin	nun	nbe	r																	
С	RW	CONNECT										Con	nec	tior	ı																	
			Disconnected	1								Disc	onr	nect																		
			Connected	0								Con	nec	t																		

31.6.8 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

Bit	numbe	er		31	30 2	9 2	8 27	26	25	24	23 22	2 21	20	19	18	17 1	L6 1	15 1	.4 13	3 12	11	10	9	8	7	6 !	5 4	3	2	1 0
Id				А	Α ,	Δ Δ	A A	Α	Α	Α	A A	Α.	Α	Α	Α	A	Α.	A	A A	Α	Α	Α	Α	Α .	Δ.	Α ,	A A	Α	Α	A A
Res	et 0x0	400000		0	0 (0	0	1	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desci	riptio	on																	
Α	RW	FREQUENCY								:	SPI m	aste	r da	ata i	rate	è														
			K125	0x	0200	000	0				125 k	bps																		
			K250	0x	0400	000	0			:	250 k	bps																		
			K500	0x	0800	000	0				500 k	bps																		
			M1	0x	1000	000	0				1 Mb	ps																		
			M2	0x	2000	000	0			:	2 Mb	ps																		
			M4	0x	4000	000	0				4 Mb	ps																		
			M8	0x	8000	000	0			:	8 Mb	ps																		

31.6.9 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

31.6.10 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW MAXCNT			Maximum number of bytes in receive buffer

31.6.11 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	umbe	er		31	30	29	28 2	7 2	6 25	5 24	4 23	3 22	21	20	19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2	1)
Id																										Α	Α	Α	Α	Α	Α.	A	4
Res	et OxO	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	R	AMOUNT									N	uml	oer o	of b	ytes	tra	ansf	err	ed	n t	he I	ast 1	tran	sact	ion								



31.6.12 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit r	nur	nbe	•		3	1 30	29	28	8 2	7 2	6 2	5 24	4 2	3 2	2 2:	1 20	19	9 18	3 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α	А А
Res	et (0x00	000000		0	0	0	0	0	0) (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R	RW	Field	Value Id	٧	alu	е						D)esc	ript	ion																			
Α	R	RW	LIST										L	ist t	ype	:																			
				Disabled	0								D	isak	ole I	Eas	yDΝ	ЛΑ	list																
				ArrayList	1								U	Jse a	arra	y li	st																		

31.6.13 TXD.PTR

Address offset: 0x544

Data pointer

Bi	it nı	umb	er			31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	L7 1	6 1	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2 2	1 0
Id						А	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A /	Δ Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
R	ese	t Ox	00000	000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	1	RW	Field	l	Value Id	Va	lue	9						De	scri	ptic	n																		
Α		RW	PTR											Dat	ta p	oin	ter																		

31.6.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6 5	4 3 2 1 0
Id					A A A	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum number o	f bytes in transmit buffer		

31.6.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number		21 20 20 20 27 20	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit number		31 30 29 28 27 26	25 24 25 22 21 20 19 18 1/ 10 15 14 15 12 11 10 9 8 / 6 5 4 5 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A R AMOUNT			Number of bytes transferred in the last transaction

31.6.16 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit	numl	bei	r		3:	1 30	29	28	3 27	7 2	6 2	5 2	4 2	3 2	2 21	. 20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 1	L O
Id																																	,	A A	A A
Re	set 0	x00	000000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	V	alu	9						D	esc	ript	ion																			
Α	RV	٧	LIST										Li	ist t	ype																				
				Disabled	0								D	isab	ole E	asy	DM	A li	st																
				ArrayList	1								U	Jse a	arra	y lis	t																		



31.6.17 CONFIG

Address offset: 0x554 Configuration register

Bit r	numbe	er		31	30 2	9 2	28 2	7 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0 ()	0 () (0 () (0 (0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	on																		
Α	RW	ORDER									В	it or	der																			
			MsbFirst	0							Ν	1ost	sign	ific	ant	bit	shi	ftec	d ou	ıt fii	st											
			LsbFirst	1							L	east	sign	ific	ant	bit	shi	fted	d ou	ıt fii	st											
В	RW	СРНА									S	eria	clo	ck (SCK) pł	nase	9														
			Leading	0							S	amp	le o	n le	adi	ng (edg	e of	fclo	ck,	shif	t se	ial c	lata	on	trai	iling	5				
											е	dge																				
			Trailing	1							S	amp	le o	n tr	ailir	ng e	edg	e of	clc	ck,	shift	ser	ial d	lata	on l	ea	ding	5				
											е	dge																				
С	RW	CPOL									S	eria	clo	ck (SCK) po	olar	ity														
			ActiveHigh	0							Α	ctiv	e hig	gh																		
			ActiveLow	1							Α	ctiv	e lov	v																		

31.6.18 ORC

Address offset: 0x5C0

Over-read character. Character clocked out in case and over-read of the TXD buffer.

Bit	numbe	r		33	1 30	29	28	27 2	6 2	25 24	4 23	3 2:	2 21	1 20	0 19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																										Α	Α	Α	Α	А А	. Д	Α
Res	et 0x0	0000000		0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue						D	esc	ript	ion	1																	
Α	RW	ORC									0	ver	-rea	ad c	har	act	er. C	Chai	act	er c	lock	ced	out i	n ca	ise a	and	ove	er-				
											re	ead	of t	he	TXE	bu	ffer															

31.7 Electrical specification

31.7.1 SPIM master interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIM}	Bit rates for SPIM ²⁴			8 ²⁵	Mbps
I _{SPIM,2Mbps}	Run current for SPIM, 2 Mbps		50		μΑ
I _{SPIM,8Mbps}	Run current for SPIM, 8 Mbps		50		μΑ
I _{SPIM,IDLE}	Idle current for SPIM (STARTed, no CSN activity)		1		μΑ
t _{SPIM,START}	Time from START task to transmission started				μs

31.7.2 Serial Peripheral Interface Master (SPIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM,CSCK}	SCK period				ns
t _{SPIM,RSCK,LD}	SCK rise time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,FSCK,LD}	SCK fall time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,WHSCK}	SCK high time ^a	(0.5*t _{CSC}	ck)		
		- t _{RSCK}			

High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO pin capacitance, see GPIO spec.



Symbol	Description	٨	Vlin.	Тур.	Max.	Units
t _{SPIM,WLSCK}	SCK low time ^a	(1	0.5*t _{CSC}	ĸ)		
		-	t _{FSCK}			
t _{SPIM,SUMI}	MISO to CLK edge setup time	1	19			ns
t _{SPIM,HMI}	CLK edge to MISO hold time	1	18			ns
t _{SPIM,VMO}	CLK edge to MOSI valid				59	ns
t _{SPIM.HMO}	MOSI hold time after CLK edge	2	20			ns

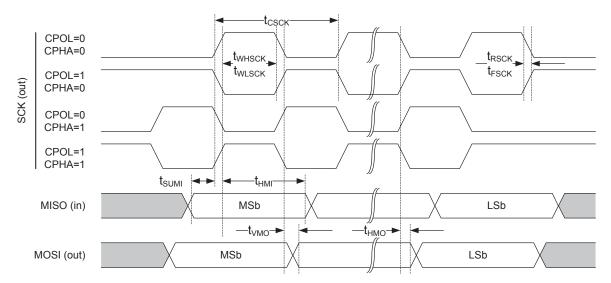


Figure 72: SPIM timing diagram



32 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

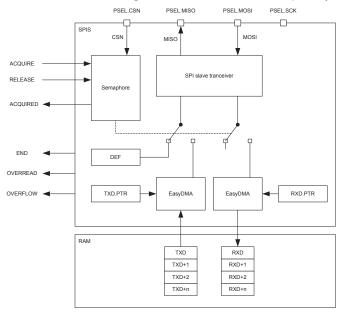


Figure 73: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 66: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE0	0 (Leading)	0 (Active High)
SPI_MODE1	0 (Leading)	1 (Active Low)
SPI_MODE2	1 (Trailing)	0 (Active High)
SPI_MODE3	1 (Trailing)	1 (Active Low)

32.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the SPI slave.

32.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.



If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

32.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled on page 281.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 281. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 281, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.



The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

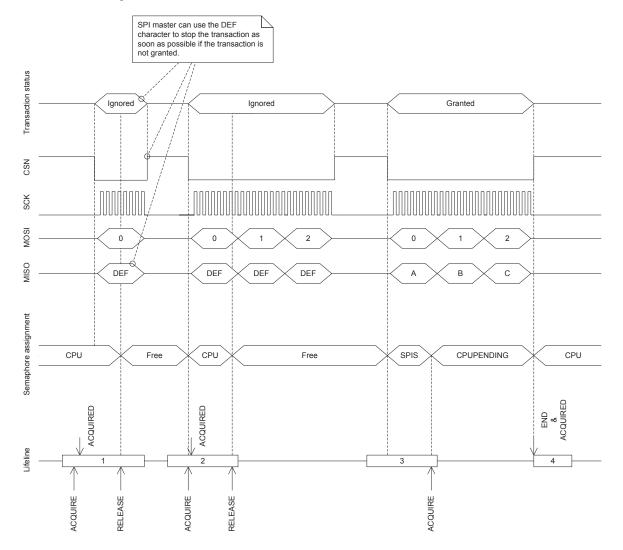


Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled

32.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see POWER - Power supply on page 67 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 67: GPIO configuration before enabling peripheral* on page 282 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI



slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 67: GPIO configuration before enabling peripheral

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

32.5 Registers

Table 68: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40004000	SPIS	SPIS0	SPI slave		

Table 69: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ENDRX	0x110	End of RXD buffer reached	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.	
		Over-read character	



32.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit	numbe	er		31	L 30	29	28	27 2	26 2	25 2	24	23 2	22 2	21 2	20 1	19 1	18 1	17 1	16	15	14	13	12	11 :	10 9	9 8	3 7	' 6	5	4	3	2	1	0
Id																																Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue						- 1	Des	crip	otio	n																			
Α	RW	END_ACQUIRE									:	Sho	rtcı	ut b	etw	/eei	n El	ND	eve	nt	and	A b	cqu	JIRE	tas	k								
											:	See	EVI	ENT	'S_1	END	an	ıd T	ASI	KS	AC	QUI	IRE											
			Disabled	0							-	Disa	ble	sho	orto	cut																		
			Enabled	1							-	Ena	ble	sho	rtc	ut																		

32.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	30 2	29 28	3 27	26 2	25 2	24 23	22 2	21 20	19	18	17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4 3	3 2	1 0
Id																					С						В		Α
Rese	et OxO	0000000		0	0	0 0	0	0	0	0 0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Val	lue					De	scrip	otion																	
Α	RW	END								Wr	rite '	1' to	Ena	ble i	inte	rru	pt f	or E	ND	eve	nt								
										See	e <i>EV</i>	ENTS	_EN	D															
			Set	1						Ena	able																		
			Disabled	0						Rea	ad: [Disab	led																
			Enabled	1						Rea	ad: E	Enabl	ed																
В	RW	ENDRX								Wr	rite '	1' to	Ena	ble i	inte	rru	pt f	or E	ND	RX e	ven	t							
										See	e <i>EV</i>	ENTS	_EN	DR)	K														
			Set	1						Ena	able																		
			Disabled	0						Rea	ad: [Disab	led																
			Enabled	1						Rea	ad: E	Enabl	ed																
С	RW	ACQUIRED								Wr	rite '	1' to	Ena	ole i	inte	rru	pt f	or A	ACQ	UIR	ED e	ven	t						
										See	e <i>EV</i>	ENTS	_AC	QUI	IREL)													
			Set	1						Ena	able																		
			Disabled	0						Rea	ad: [Disab	led																
			Enabled	1						Rea	ad: E	Enabl	ed																

32.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	umbe	r		31	. 30 :	29	28 2	7 2	26 2	25 2	24 2	3 22	2 21	. 20	19	18	17	16	15 :	14 1	3 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id																							С					В			Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	ion																	
Α	RW	END									٧	Vrite	e '1'	to [Disa	ble	inte	erru	pt f	or E	ND	eve	nt								
											S	ee E	VEN	VTS_	_EN	ID															
			Clear	1							D	isab	ole																		
			Disabled	0							R	ead	: Dis	sabl	ed																
			Enabled	1							R	ead	: En	able	ed																
В	RW	ENDRX									٧	Vrite	e '1'	to [Disa	ble	inte	erru	pt f	or E	NDI	RX e	vent	t							
											S	ee E	VEN	NTS_	_EN	DR.	X														
			Clear	1							D	isab	ole																		
			Disabled	0							R	ead	: Dis	sabl	ed																



Bit	numbe	er		31	30	29	28 2	27 :	26 2	25 2	24 2	23	22	21	20	19	18	17	16 1	15 1	.4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id																								С						В		ļ	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	scri	ptic	n																		
			Enabled	1							F	Rea	ad:	Ena	ble	d																	
С	RW	ACQUIRED									١	Wri	ite	'1' t	o D	isal	ole	inte	rru	pt f	or A	ACQ	UIR	ED e	ven	t							
											9	See	E۷	/EN	rs	AC	วบเ	REL)														
			Clear	1							[Disa	abl	е																			
			Disabled	0							F	Rea	ad:	Disa	ble	ed																	
			Enabled	1							F	Rea	ad:	Ena	ble	d																	

32.5.4 SEMSTAT

Address offset: 0x400

Semaphore status register

Bit r	umbe	er		31	1 30	29	28	27	26	5 25	5 2	4 2	3 22	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	C	0 (0) (0 (כ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	alue							D	esc	rip	tior	ı																				
Α	R	SEMSTAT										S	ema	aph	ore	st	atu	S																		
			Free	0								S	ema	aph	ore	is	fre	e																		
			CPU	1								S	ema	aph	ore	is	ass	igr	ed	to	CP	J														
			SPIS	2								S	ema	aph	ore	is	ass	igr	ed	to	SPI	sla	ve													
			CPUPending	3								S	ema	aph	ore	is	ass	igr	ed	to	SPI	bu	t a	har	ndo	ver	to 1	the	CPI	U is						
												р	end	ling	3																					

32.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ВА
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW OVERREAD			TX buffer over-read detected, and prevented
	NotPresent	0	Read: error not present
	Present	1	Read: error present
	Clear	1	Write: clear error on writing '1'
B RW OVERFLOW			RX buffer overflow detected, and prevented
	NotPresent	0	Read: error not present
	Present	1	Read: error present
	Clear	1	Write: clear error on writing '1'

32.5.6 ENABLE

Address offset: 0x500 Enable SPI slave



32.5.7 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bit r	umb	er		31	L 30	29	28	27	26	25	24	23	22	21	20 1	19 1	.8 1	7 16	5 15	14	13	12	11 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	ДД	A	Α	Α	Α	Α	ΑА	. A	Α	Α	Α	Α	Α .	4 А	Α	Α
Res	et OxF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																	
Α	RW	PSELSCK		[0	31]						Pin	nuı	mbe	er co	onfi	gura	itio	n fo	r SP	I SC	K si	gnal									
			Disconnected	0х	FFF	FFF	FF					Dis	con	nec	t																	

32.5.8 PSELMISO (Deprecated)

Address offset: 0x50C Pin select for MISO

Bit	nu	mbe	er		31	. 30	29	28	27	⁷ 26	25	24	23	22	21	20	19	18 :	17 :	16	15	14	13 :	12 :	11 1	.0	9	3 7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	Δ,	Δ Δ	A	Α	Α	Α	Α	АА
Res	et	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1	1 1	. 1	1	1	1	1	1 1
Id	-	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	-	RW	PSELMISO		[0	31	.]						Pir	nu	mb	er c	onf	igur	rati	on i	for	SPI	MIS	SO :	ign	al								
				Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																		

32.5.9 PSELMOSI (Deprecated)

Address offset: 0x510 Pin select for MOSI

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4 3	2	1 0
Id				A A A A A A A A A A A A A A A A A A A	Α	Α	Α .	А А	. A	A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1	1	1 1	1	1 1
Id	RW	Field	Value Id	Value Description						
Α	RW	PSELMOSI		[031] Pin number configuration for SPI MOSI signal						
			Disconnected	0xFFFFFFF Disconnect						

32.5.10 PSELCSN (Deprecated)

Address offset: 0x514 Pin select for CSN

Bit	numbe	er		3:	1 30	29	9 28	8 2	7 2	6 2	5 2	24 2	3 2	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12 :	11 1	0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	. Δ	. Δ	A /	A A	Δ,	A ,	Δ,	A A	Α Α	A A	. A	Α	Α	Α	Α	Α	Α	A A	A 4	Α Α	A	Α	Α	Α	Α ,	A ,	А А
Res	et OxF	FFFFFF		1	1	1	. 1	. 1	۱ 1	L 1	1	1	1	1 1	L 1	۱ 1	1	1	1	1	1	1	1	1 :	L 1	L 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	2						0)es	crip	tior	1																	
Α	RW	PSELCSN		[0)31	.]						P	in ı	num	ıbe	r co	nfig	ura	ion	for	SPI	CSI	V si	gnal									
			Disconnected	0	xFFF	FFI	FFF						isc	onn	ect																		

32.5.11 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 1	14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id		С			A A A A A
Reset OxFFFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description		
	Connected	0	Connect		

32.5.12 PSEL.MISO

Address offset: 0x50C Pin select for MISO signal

Bit	numbe	er		31	30 2	9 2	28 2	7 2	6 25	5 24	1 23	22	21	20	19 1	18 1	.7 16	5 15	14	13 1	2 1:	1 10	9	8	7	6	5	4 3	3 2	1	0
Id				С																								A A	АА	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1 1	L 1	. 1	. 1	1	1	1	1	1	1	1 1	1	1	1	l 1	. 1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue						De	escri	iptic	on																	
Α	RW	PIN		[0.	.31]						Pi	n nu	ımb	er																	
С	RW	CONNECT									Co	nne	ectic	n																	
			Disconnected	1							Di	1002	nnec	t																	
			Connected	0							Co	nne	ect																		

32.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit r	numbe	r		31 3	30 29	9 28	27	26	25	24	23 2	22 2	1 2	0 19	9 18	3 17	16	15	14 1	L3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				С																								Α	A A	. Δ	Δ
Res	et OxF	FFFFFF		1	1 1	. 1	1	1	1	1	1	1 :	1 1	1 1	. 1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Valu	ıe						Des	crip	tior	1																	
Α	RW	PIN		[03	31]						Pin ı	nun	nbei	r																	
С	RW	CONNECT								(Con	nec	tion	1																	
			Disconnected	1							Disc	onn	nect																		
			Connected	0						(Con	nec	t																		

32.5.15 RXDPTR (Deprecated)

Address offset: 0x534 RXD data pointer

Bit r	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0	9	8	7	6	5	4	3 2	. 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α.	Α	Α	Α	Α	Д Д	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	RXDPTR										RX	D d	ata	poi	nte	r																	



32.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit	numb	er		31	30 2	9 2	28 27	7 26	25	24	23 2	22 2	1 2	0 19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																									Α	Α	Α	Α	Α	Α /	А А
Res	et 0x0	0000000		0	0 (0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	ue					- 1	Des	crip	tion	1																	
Δ	RW/	MAXRX									Max	rimu	m r	าเเท	her	of I	hvte	s ir	rei	reiv	e hi	ıffeı	r								

32.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1	0
Id					A A A A A A	Α
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000000	0000000	0
Id RW Field	Value Id	Value	Description			
A R AMOUNTRX			Number of bytes rec	eived in the last granted trans	action	

32.5.18 RXD.PTR

Address offset: 0x534 RXD data pointer

Bit	nur	nbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	À
Re	set (0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	R	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	R	RW	PTR										RX	D d	ata	poi	nte	r																		

32.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	1 30 29 28 27	26 25 2	24 23	22 21	20 19	9 18	17 16	5 15 1	4 13	12 11	. 10	9 8	7	6	5 4	3	2 :	1 0
Id														Α	Α .	4 А	Α	A A	А А
Reset 0x00000000	0	0 0 0 0	0 0	0 0	0 0	0 0	0	0 0	0	0 0	0 0	0	0 0	0	0	0 0	0	0 (O O
Id RW Field V	alue Id Va	alue		Des	criptio	on													
A RW MAXCNT				Ma	ximum	num	ber	of byt	es in	recei	ve buf	fer							

32.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit r	umbe	r		31 3	0 29	28	27 2	26 2	5 24	1 23	22	21	20 1	19 1	8 1	7 16	15	14 :	13 1	2 11	10	9	8	7	6 5	4	3	2	1 0
Id																							,	Δ.	A A	A	Α	Α	A A
Res	et 0x0	0000000		0 0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 (0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	e					De	scri	ptio	n																
Α	R	AMOUNT								Nι	mb	er o	f by	tes	rece	eive	d in	the l	ast g	ran	ted t	tran	sact	ior	ı				

32.5.21 TXDPTR (Deprecated)

Address offset: 0x544
TXD data pointer



Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	TXDPTR										TXI) da	ata	ioc	nter																		

32.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit	umbe	er		31	30 2	29 :	28 2	7 26	25	24	23	22	21 2	20 2	19 1	.8 1	17 1	16 1	.5 1	.4 1	3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	Α.	А А
Res	et OxO	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																		
Α	RW	MAXTX									Ma	xim	ıum	nuı	mbe	er o	f by	/tes	in	trar	ısmi	t bı	ıffer									

32.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit	numbe	er		31	30	29 :	28 2	27 20	6 2!	5 24	1 23	22	21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	Α /	4 A
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	escri	ptic	on																		
Α	R	AMOUNTTX									Νι	ımb	er c	of b	ytes	tra	nsr	nit	ted	in la	ast g	gran	ted	tran	ısac	tio	n					

32.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

Bit r	numbe	er		31	30	29	28 2	27 2	6 2	5 24	4 23	22	21	20	19	18 1	17 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	A A	Δ	4 Α	A	Α	Α	Α	Α	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A /	А А
Res	et 0x0	0000000		0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						De	scr	iptio	on																		
Α	RW	PTR									TX	D d	lata	poi	ntei	r																

32.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit n	umber		31 30 29 28 27 26	25 24	23 22	21 20	19 1	.8 17	16 1	.5 14	13 1	2 11	10 9	8	7	6	5	4 3	3 2	1 0
Id															Α	Α	Α	A A	A	A A
Rese	t 0x000000	0	0 0 0 0 0 0	0 0	0 0	0 0	0	0 0	0 (0 0	0 (0 (0 0	0	0	0	0	0 0	0	0 0
Id	RW Field	Value Id	Value		Descri	ption														
Α	RW MAX	NT			Maxin	num n	umbe	er of b	ytes	in tr	ansm	it bu	fer							

32.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Id RW Field Value Id Value Description	
Neset 0X00000000	
Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Id	A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 1	3 12 11 10 9 8 7 6 5 4 3 2 1 0

R AMOUNT Number of bytes transmitted in last granted transaction



32.5.27 CONFIG

Address offset: 0x554 Configuration register

Bit r	umbe	er		31	30 2	9 2	28 2	7 2	6 25	5 24	4 2	3 22	21	20	19	18	17	16	15	14	13	12	11 1	.0 !	9	8 7	' 6	5	4	3	2	1 0
Id																															С	ВА
Rese	et 0x0	0000000		0	0 ()	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esci	iptio	on																		
Α	RW	ORDER									В	it or	der																			
			MsbFirst	0							N	1ost	sign	ific	ant	bit	shi	fte	o b	ıt fi	rst											
			LsbFirst	1							Le	east	sign	ific	ant	bit	shi	fte	o b	ut fi	rst											
В	RW	СРНА									Se	erial	cloc	k (SCK) pł	nas	е														
			Leading	0							Sa	amp	le o	n le	adiı	ng e	edg	e o	f clo	ock,	shi	ft s	erial	da	ta	on ti	aili	ng				
											e	dge																				
			Trailing	1							Sa	amp	le o	n tr	ailir	ng e	edg	e of	clo	ck,	shi	t se	erial	dat	ta d	on le	adi	ng				
											e	dge																				
С	RW	CPOL									Se	erial	cloc	k (SCK) pc	olar	ity														
			ActiveHigh	0							Α	ctiv	e hig	h																		
			ActiveLow	1							Α	ctiv	e lov	V																		

32.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit	numbe	r		31	. 30	29	28	27 2	26 2	25 2	24 2	23 2	2 2	1 20) 19	18	17	16	15	14 :	13 1	2 1:	L 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	A	Δ ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	cript	ion																		
Α	RW	DEF									[Defa	ault	cha	ract	er. (Cha	ract	er c	loc	ced	out	in c	ase	of a	an ig	gno	red				
												ran	cact	ion																		

32.5.29 ORC

Address offset: 0x5C0 Over-read character

Bit r	umber			31	30	29	28 :	27 2	6 2	5 24	1 23	3 22	21	20 1	19 1	8 17	7 16	15	14	13 :	12 1	1 10	9	8	7	6	5 4	4 3	2	1	0
Id																									Α	Α	A	4 Α	Α	Α	Α
Res	et 0x000	000000		0	0	0	0	0 () (0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0
Id	RW F	ield	Value Id	Va	lue						D	escri	ptic	n																	
Α	RW 0	ORC									0	ver-ı	ead	l cha	rac	ter.	Cha	ract	er c	lock	ed c	ut a	fter	an	ove	er-re	ead				
											of	the	trar	nsm	it bı	uffer															

32.6 Electrical specification

32.6.1 SPIS slave interface electrical specifications

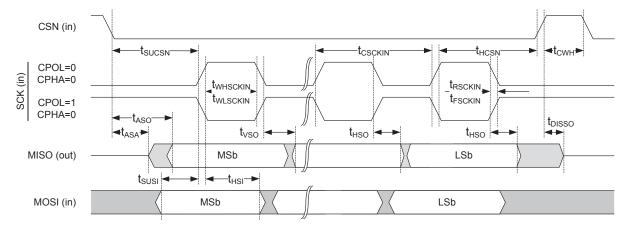
Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIS}	Bit rates for SPIS ²⁶			8 ²⁷	Mbps
I _{SPIS,2Mbps}	Run current for SPIS, 2 Mbps		45		μΑ
I _{SPIS,8Mbps}	Run current for SPIS, 8 Mbps		45		μΑ
I _{SPIS,IDLE}	Idle current for SPIS (STARTed, no CSN activity)		1		μΑ
t _{SPIS,START}	Time from RELEASE task to receive/transmit (CSN active)				μs

High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
 The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.



32.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIS,CSCKIN}	SCK input period				ns
t _{SPIS,RFSCKIN}	SCK input rise/fall time			30	ns
t _{SPIS,WHSCKIN}	SCK input high time	30			ns
t _{SPIS,WLSCKIN}	SCK input low time	30			ns
t _{SPIS,SUCSN}	CSN to CLK setup time				ns
t _{SPIS,HCSN}	CLK to CSN hold time	2000			ns
t _{SPIS,ASA}	CSN to MISO driven				ns
t _{SPIS,ASO}	CSN to MISO valid ^a			1000	ns
t _{SPIS,DISSO}	CSN to MISO disabled ^a			68	ns
t _{SPIS,CWH}	CSN inactive time	300			ns
t _{SPIS,VSO}	CLK edge to MISO valid			19	ns
t _{SPIS,HSO}	MISO hold time after CLK edge	18 ²⁸			ns
t _{SPIS,SUSI}	MOSI to CLK edge setup time	59			ns
t _{SPIS,HSI}	CLK edge to MOSI hold time	20			ns



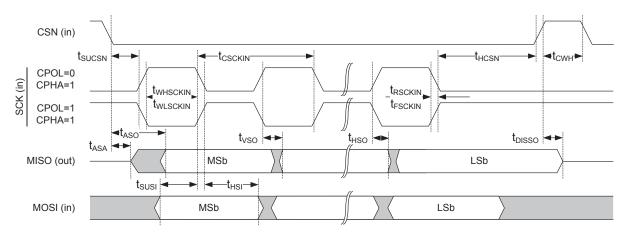


Figure 75: SPIS timing diagram

^a At 25pF load, including GPIO capacitance, see GPIO spec.

This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output



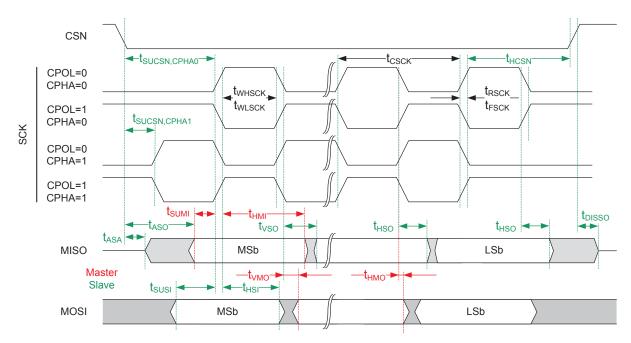


Figure 76: Common SPIM and SPIS timing diagram



33 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- Support for clock stretching (non I²C compliant)
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

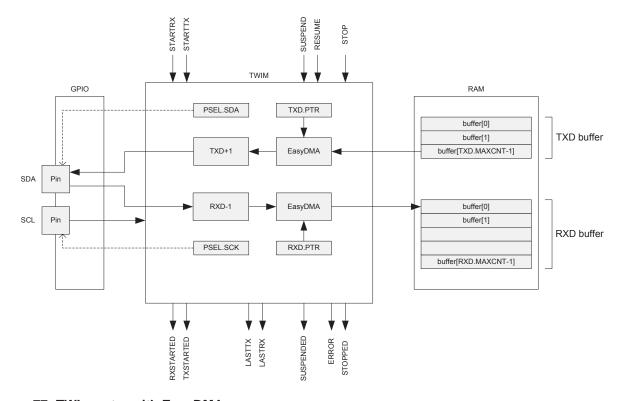


Figure 77: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 78: A typical TWI setup comprising one master and three slaves* on page 293. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.



Figure 78: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. Note that the SCK pulse following a stretched clock cycle may be shorter than specified by the I2C specification.

The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task. The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

33.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the TWI.

33.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

33.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.



A typical TWI master write sequence is illustrated in *Figure 79: TWI master writing data to a slave* on page 294. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

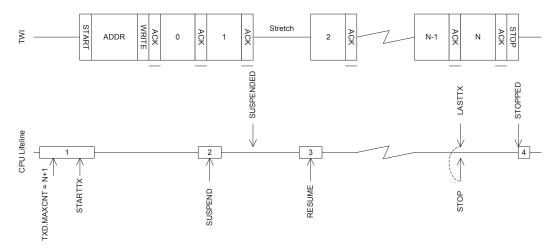


Figure 79: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 79: TWI master writing data to a slave* on page 294

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

33.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 80: The TWI master reading data from a slave* on page 295. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 80: The TWI master reading data from a slave* on page 295. If RXD.MAXCNT > 1 the LASTRX



event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

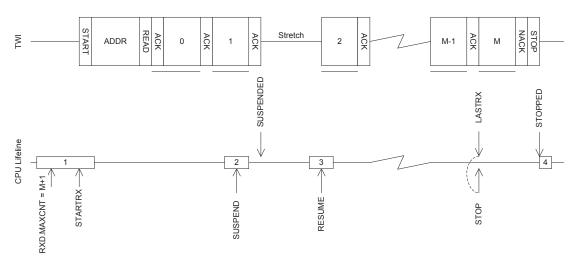


Figure 80: The TWI master reading data from a slave

33.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure Figure 81: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave on page 295 illustrates this:

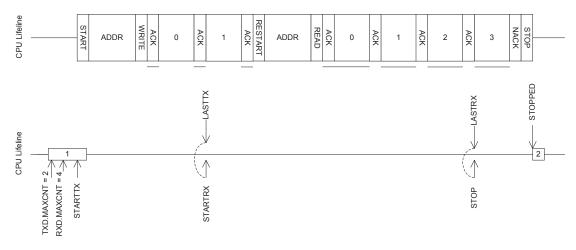


Figure 81: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave



If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. This is illustrated in *Figure 82: A double repeated start* sequence using the SUSPEND task to secure safe operation in low priority interrupts on page 296.

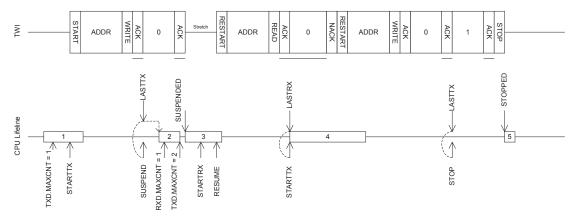


Figure 82: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

33.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

33.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 70: GPIO configuration before enabling peripheral* on page 296.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 70: GPIO configuration before enabling peripheral

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1

33.8 Registers

Table 71: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIM	TWIM0	Two-wire interface master	



Table 72: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_SUSPENDED	0x148	Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS	0x588	Address used in the TWI transfer

33.8.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F D C B A
Res	et 0x00000000		0 0 0 0 0	$f{0}$ $f{0$
Id	RW Field	Value Id	Value	Description
Α	RW LASTTX_STARTRX			Shortcut between LASTTX event and STARTRX task
				See EVENTS_LASTTX and TASKS_STARTRX
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
В	RW LASTTX_SUSPEND			Shortcut between LASTTX event and SUSPEND task
				See EVENTS_LASTTX and TASKS_SUSPEND
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW LASTTX_STOP			Shortcut between LASTTX event and STOP task
				See EVENTS_LASTTX and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW LASTRX_STARTTX			Shortcut between LASTRX event and STARTTX task
				See EVENTS_LASTRX and TASKS_STARTTX
		Disabled	0	Disable shortcut



Bit r	umbe	r		3:	1 30	29	28	8 27	7 26	6 25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO :	9	8	7	6 5	5	4 3	2	2 1	0
Id																							F		D	С	В	4						
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 ()	0 (0	0	0
Id	RW	Field	Value Id	V	alue							D	escr	ipti	on																			
			Enabled	1								Er	abl	e sh	ort	cut	t																	
F	RW	LASTRX_STOP										Sh	ort	cut	bet	we	en	LAS	TR)	(ev	ent	an	d ST	OP	task									
												Se	e E	VΕN	ITS_	_LA	STF	RX a	and	TAS	KS_	ST	ЭP											
			Disabled	0								Di	sab	le sl	hor	tcu	t																	
			Enabled	1								Er	abl	e sh	ort	cut	t																	

33.8.2 INTEN

Address offset: 0x300 Enable or disable interrupt

		or disable interre	- 1										_											_			_	_				
	numb	er		31 30	29 2	28 27	7 26									17 1	16	15	14	13 :	12 :	11			8	7	6 .	5 4	1 3	2		
Id																	_							D							A	
		0000000	Value Id	0 0	U	0 0	U	U						U	U	U	U	U	U	U	U	U	U	U	U	U	U	0 () (0	U	U
ld ^		Field STOPPED	value id	Value							script able c			ماماد	in			fo	. CT	ODI	200		ont									
Α	NVV	STOPPED															up	. 10	31	OPI	- []) e	rent									
									S	See	e EVE	NT.	S	STO	PP	ED																
			Disabled	0							able																					
			Enabled	1					E	na	able																					
D	RW	ERROR							E	na	able c	or d	disa	able	in	terr	up	fo	r EF	RRO	R e	ver	nt									
									S	See	EVE	NT.	·s_	ERR	OR																	
			Disabled	0						Disa	able																					
			Enabled	1					Е	Ena	able																					
F	RW	SUSPENDED							E	na	able c	or d	disa	able	in	terr	up	fo	٠S١	JSPI	ΝC	DEC	eve	ent								
									S	See	e EVE	NT.	s :	SUS	PE	NDE	D															
			Disabled	0							able		_																			
			Enabled	1					Е	na	able																					
G	RW	RXSTARTED							Е	Ena	able c	or d	disa	able	in	terr	up	fo	r R)	(ST/	١RT	ED	eve	nt								
									c	200	EVE	NIT	c	DVC	TΛ	DTE	D															
			Disabled	0							able	. I V I .	J_1	NAS	IA	NIL.	_															
			Enabled	1							able																					
Н	RW	TXSTARTED	Litablea	-							able c	or d	lisa	able	in	terr	นถ	fo	r T)	(ST/	RT	ED	eve	nt								
				_							EVE	NT.	<u>s_</u>	TXS	TAI	RTE	D															
			Disabled	0							able																					
	D\A/	LACTOV	Enabled	1							able		1:	-1-1-				£_		CTI	· · ·											
1	RW	LASTRX							E	na	able c	or c	IIS	abie	ın	terr	up	то	r LA	SIF	кхе	eve	nt									
									S	See	EVE	NT.	S_	LAS	TR	(
			Disabled	0					0	Disa	able																					
			Enabled	1							able																					
J	RW	LASTTX							E	na	able c	or d	disa	able	in	terr	up	fo	r LA	STT	Хe	eve	nt									
									S	See	EVE	NT.	s	LAS	TT)	(
			Disabled	0					0	Disa	able																					
			Enabled	1					Е	na	able																					

33.8.3 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	numbe	er		31 30	29 28	27 2	26 2	25 24	23	22 21	1 2	0 19	18	3 17	16	5 15	14	13	3 12	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id								J	-1		H	l G	F									D							Α	
Res	et OxC	0000000		0 0	0 0	0	0 (0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value					De	script	ion	1																		
Α	RW	STOPPED							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	ST	OPI	PED	eve	ent								
									Se	e <i>EVEI</i>	NTS	S_ST	ОP	PED																
			Set	1					En	able																				
			Disabled	0					Re	ad: Di	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
D	RW	ERROR							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	ER	RO	R ev	/ent									
									Se	e <i>EVEI</i>	NTS	S_ER	RC)R																
			Set	1					En	able																				
			Disabled	0					Re	ad: Dis	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
F	RW	SUSPENDED							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	SU	SPE	END	ED	eve	nt							
									Se	e <i>EVEI</i>	NTS	s_su	ISP	END	ED)														
			Set	1					En	able																				
			Disabled	0					Re	ad: Di	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
G	RW	RXSTARTED							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	RX	STA	۱RT	ED 6	evei	nt							
									Se	e <i>EVEI</i>	NTS	S_RX	ST.	ART	ED															
			Set	1					En	able																				
			Disabled	0					Re	ad: Dis	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
Н	RW	TXSTARTED							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	TX	STA	\RTI	ED e	ever	١t							
									Se	e <i>EVEI</i>	NTS	S_TX	ST	4RTI	ED															
			Set	1					En	able																				
			Disabled	0					Re	ad: Di	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
1	RW	LASTRX							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	LA	STR	X e	ven	t								
									Se	e <i>EVEI</i>	NTS	5_ <i>LA</i>	ST	RX																
			Set	1					En	able																				
			Disabled	0					Re	ad: Di	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		
J	RW	LASTTX							Wı	rite '1'	' to	Ena	ble	inte	err	upt	for	LA	STT	'X e	ven	t								
									Se	e <i>EVEI</i>	NTS	5_ <i>LA</i>	ST	TX																
			Set	1					En	able																				
			Disabled	0					Re	ad: Dis	sab	oled																		
			Enabled	1					Re	ad: En	nab	led																		

33.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	23	22 2	21 2	0 19	18	17	16	15 1	L4 1	3 12	11	10	9 8	3 7	6	5	4	3	2	1 0
Id										J	-1		H	l G	F								D							A
Res	et 0x0	0000000		0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scrip	tion	1																
Α	RW	STOPPED									W	rite '	1' to	Dis	able	inte	erru	pt f	or S	TOP	PED	evei	nt							
											Se	e <i>EV</i>	ENTS	S_S	ΌΡ	PED														
			Clear	1							Dis	sable	!																	
			Disabled	0							Re	ad: [Disab	led																
			Enabled	1							Re	ad: E	nab	led																
D	RW	ERROR									W	rite '	1' to	Dis	able	inte	erru	pt f	or E	RRO	R ev	ent								
											Se	e <i>EV</i>	ENTS	5_ <i>EI</i>	RRO	R														



Bit	number		31 30 29 28 27 2	26 25 24	23 22 21 20 1	19 18 17	16 15 1	14 13 1	2 11 10	9 8	7	5 5	4 3	2 1	0
Id				J	1 н с	G F				D				А	
Re	set 0x00000000		0 0 0 0 0	0 0 0	0 0 0 0	0 0 0	0 0	0 0 0	0 0	0 0	0	0 0	0 0	0 0	0
Id	RW Field Valu	ue Id	Value		Description										
	Clea	ar	1		Disable										
	Disa	abled	0		Read: Disabled	d									
	Ena	bled	1		Read: Enabled	ł									
F	RW SUSPENDED				Write '1' to Dis	sable inte	errupt f	or SUSF	PENDED	event					
					See EVENTS_S	SUSPENDI	ED								
	Clea	ar	1		Disable										
	Disa	abled	0		Read: Disabled	d									
	Ena	bled	1		Read: Enabled	ł									
G	RW RXSTARTED				Write '1' to Dis	sable inte	errupt f	or RXST	ARTED	event					
					See EVENTS_R	OVCTADTE	-D								
	Clea	ar	1		Disable	MOTANTE	.0								
			0		Read: Disabled	d									
			1		Read: Enabled										
Н	RW TXSTARTED	ibica	•		Write '1' to Dis		errupt f	or TXST	ARTED 6	event					
					See EVENTS_T	TXSTARTE	D								
	Clea		1		Disable										
			0		Read: Disabled										
		bled	1		Read: Enabled										
1	RW LASTRX				Write '1' to Dis	sable inte	errupt f	or LAS I	RX even	t					
					See EVENTS_L	.ASTRX									
	Clea	ar	1		Disable										
	Disa	abled	0		Read: Disabled	d									
	Ena	bled	1		Read: Enabled	ł									
J	RW LASTTX				Write '1' to Dis	sable inte	errupt f	or LAST	TX even	t					
					See EVENTS_L	ASTTX									
	Clea	ar	1		Disable										
	Disa	abled	0		Read: Disabled	d									
	_	bled	1		Read: Enabled	ı									

33.8.5 ERRORSRC

Address offset: 0x4C4

Error source

Bit r	numbe	er		31	30 2	9 2	8 2	7 26	5 25	5 24	23	22 2	21 2	20 1	19 1	.8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0	0	0	0	0 (0 () (0) (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	ue						Des	scrip	otio	n																		
Α	RW	OVERRUN									Ove	erru	n er	ror																		
											A n	new	byte	e wa	as r	ece	ive	d be	for	e pr	evi	ous	byt	e go	ot tr	ans	fer	red				
											into	o RX	(D b	uffe	er. (Pre	vio	ıs d	ata	is l	ost)											
			NotReceived	0							Erro	or d	id n	ot o	occı	ır																
			Received	1							Erro	or o	ccui	rred	t																	
В	RW	ANACK									NA	CK r	ece	ive	d af	ter	sen	din	g th	ne a	ddre	ess (wri	te '	1' to	cle	ear)					
			NotReceived	0							Erro	or d	id n	ot o	occı	ır																
			Received	1							Erro	or o	ccui	rred	t																	
С	RW	DNACK									NA	CK r	ece	ive	d af	ter	sen	din	g a	data	by	te (writ	e '1	l' to	cle	ear)					
			NotReceived	0							Erro	or d	id n	ot o	occı	ır																
			Received	1							Erro	or o	ccui	rrec	b																	

33.8.6 ENABLE

Address offset: 0x500



Enable TWIM

Bit n	umbe	er		31 3	30 2	29 2	28 2	7 2	26 2	25 2	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11 1	.0 !	9	8 7	7 6	5 5	5 4	. 3	2	1	0
Id																															Α	Α	Α	Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 () () (0 0	0	0	0	0
ld	RW	Field	Value Id	Valu	ıe							Des	crip	otic	n																			
A	RW	ENABLE										Ena	ble	or	disa	abl	e T\	ΝIN	Λ															
			Disabled	0								Disa	able	e TV	VIN	1																		
			Enabled	6								Ena	ble	TW	/IM	ı																		

33.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit	numbe	er		31 30 29 28 27 26 2	24 23	3 22 2	1 20	19	18 1	17 16	5 15	14 1	3 12	11 1	.0 9	8	7	6	5	4	3 2	1	0
Id				С																Α	Д А	Α	Α
Res	et 0xF	FFFFFF		1 1 1 1 1 1	1 1	. 1	1 1	1	1	1 1	1	1	1 1	1	1 1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value	De	escrip	tion																
Α	RW	PIN		[031]	Pi	in nun	nber																
С	RW	CONNECT			Co	onnec	tion																
			Disconnected	1	Di	isconr	nect																
			Connected	0	Co	onnec	t																

33.8.8 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	er		31	30 2	9 28	8 27	7 26	5 25	5 24	1 23	3 22	21	20	19 1	18 1	7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				С																								Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1 1	L 1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1 1	۱ 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Val	ue						De	escri	ptic	n																	
Α	RW	PIN		[0	31]						Piı	n nu	mb	er																	
С	RW	CONNECT									Co	nne	ctic	n																	
			Disconnected	1							Di	scor	nec	t																	
			Connected	0							Co	nne	ct																		

33.8.9 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

Bit	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	0 9	9 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	Α Α	Δ Α	A	Α	Α	Α	Α	Α	А А
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	FREQUENCY										TW	/I m	aste	er c	loc	k fr	equ	end	су													
			K100	0x	019	800	000					100) kb	ps																			
			K250	0x	040	0000	000					250) kb	ps																			
			K400	0x	:064	1000	000					400) kb	ps																			

33.8.10 RXD.PTR

Address offset: 0x534

Data pointer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

33.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Е	Bit n	um	ber			31	30 2	9 2	28 27	7 26	25	24	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14	13	12	11 1	.0 9	9 8	3 7	6	5	4	3	2	1	O
1	d																										Α	Α	A	Α	Α	Α	Α	Д
F	Rese	t O	x00	000000		0	0 ()	0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0
1	d	R۱	N	Field	Value Id	Val	lue						Des	crip	tior	n																		
4	4	R۱	Ν	MAXCNT		[1.	255]						Max	kimı	ım i	nun	nbe	r of	byt	es ir	n re	ceiv	e b	uffe	r									_

33.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	umb	er		31	1 30	29	28	27	26	25	24	23	22	21 :	20 1	9 1	8 17	7 16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	A	Α,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Vá	alue							De	scri	ptio	n																	
Α	R	AMOUNT										Nu	mbe	er o	f byt	tes	tran	sfei	red	in 1	he	ast	trar	sac	ion	. In	case	e of				
												NA	CK 6	erro	r, in	clu	des	the	NA	CK'e	d b	yte.										

33.8.13 RXD.LIST

Address offset: 0x540 EasyDMA list type

E	Bit num	nbei	r		31	L 30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
1	d																														A	Α Α	A
F	Reset 0)0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
1	d R\	W	Field	Value Id	Va	alue							Des	crip	tio	n																	
1	A R	W	LIST										List	typ	e																		
				Disabled	0								Disa	ble	Eas	syD	MA	list															
				ArrayList	1								Use	arr	ay I	ist																	

33.8.14 TXD.PTR

Address offset: 0x544

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW PTR		Data pointer

33.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer



Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
A DIM MANYCHIT		[4 255]	
A RW MAXCNT		[1255]	Maximum number of bytes in transmit buffer

33.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit r	umbe	er		3	1 30	29	28	27 26	5 25	5 24	23	22	21 2	20 19	9 18	3 17	16	15	14 1	3 1	2 11	10	9	8	7	6	5 4	4	3 2	1	0
Id																									Α	Α	A	A ,	4 A	Α	. A
Res	et OxC	0000000		0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	V	alue	•					De	scri	ptio	n																	
Α	R	AMOUNT									Νu	ımbe	er of	byt	es t	rans	feri	ed	in th	e la	st tr	ans	acti	on.	In c	ase	of				
											NA	ACK 6	erro	r, ind	clud	es t	he f	NAC	K'ed	byt	e.										

33.8.17 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit	numb	er		31	30	29	28	27	26	25	24	23 2	22 2	1 2	0 1	9 1	.8 1	7 1	6 15	5 14	1 13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																Α ,	А А
Res	et Ox0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	LIST										List	typ	е																			
			Disabled	0								Disa	ble	Eas	syD	MΑ	list																
			ArrayList	1								Use	arr	ay l	ist																		

33.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit r	numbe	er		31	30	29	28 2	7 20	5 25	5 24	23	22	21	20	19 1	18 1	17 1	16	15 1	L4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id																											Α	Α	Α	A	Δ ,	А А
Res	et OxO	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																		
Α	RW	ADDRESS									Ad	dre	ss u	sed	in t	he	TW	'l tr	ans	fer												

33.9 Electrical specification

33.9.1 TWIM interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM,SCL}	Bit rates for TWIM ²⁹	100		400	kbps
I _{TWIM,100kbps}	Run current for TWIM, 100 kbps		50		μΑ
I _{TWIM,400kbps}	Run current for TWIM, 400 kbps		50		μΑ
t _{TWIM,START}	Time from STARTRX/STARTTX task to transmission started				μs

33.9.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns

High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIM,HD_STA,100kbps}	TWIM master hold time for START and repeated START	10000			ns
	condition, 100 kbps				
t _{TWIM,HD_STA,250kbps}	TWIM master hold time for START and repeated START	4000			ns
	condition, 250kbps				
$t_{TWIM,HD_STA,400kbps}$	TWIM master hold time for START and repeated START	2500			ns
	condition, 400 kbps				
$t_{TWIM,SU_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
$t_{TWIM,SU_STO,250kbps}$	TWIM master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
$t_{TWIM,SU_STO,400kbps}$	TWIM master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWIM,BUF,100kbps}	TWIM master bus free time between STOP and START	5800			ns
	conditions, 100 kbps				
t _{TWIM,BUF,250kbps}	TWIM master bus free time between STOP and START	2700			ns
	conditions, 250 kbps				
$t_{\text{TWIM},\text{BUF},\text{400kbps}}$	TWIM master bus free time between STOP and START	2100			ns
	conditions, 400 kbps				

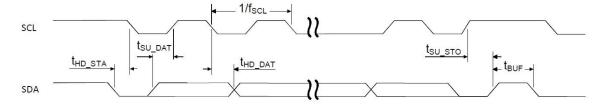


Figure 83: TWIM timing diagram, 1 byte transaction

33.10 Pullup resistor

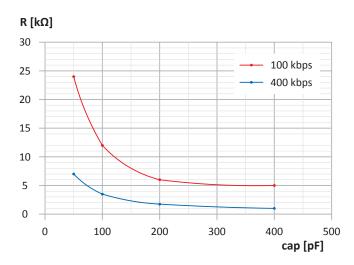


Figure 84: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The value of internal pullup resistor (R_{PU}) for nRF52810 can be found in the GPIO General purpose input/output on page 96 section.



34 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

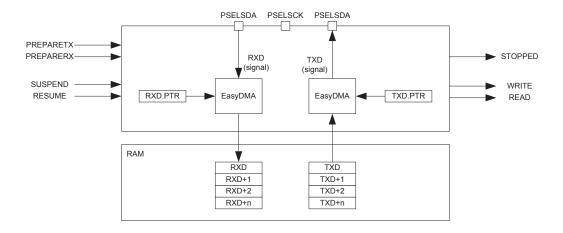


Figure 85: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 86: A typical TWI setup comprising one master and three slaves* on page 305. TWIS is only able to operate with a single master on the TWI bus.



Figure 86: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 87: TWI slave state machine* on page 306 and *Table 73: TWI slave state machine symbols* on page 306 is explaining the different symbols used in the state machine.



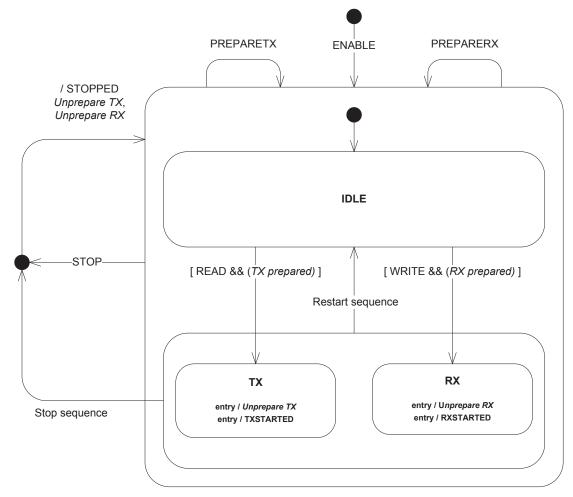


Figure 87: TWI slave state machine

Table 73: TWI slave state machine symbols

Symbol	Туре	Description
ENABLE	Register	The TWI slave has been enabled via the ENABLE register
PREPARETX	Task	The TASKS_PREPARETX task has been triggered
STOP	Task	The TASKS_STOP task has been triggered
PREPARERX	Task	The TASKS_PREPARERX task has been triggered
STOPPED	Event	The EVENTS_STOPPED event was generated
RXSTARTED	Event	The EVENTS_RXSTARTED event was generated
TXSTARTED	Event	The EVENTS_TXSTARTED event was generated
TX prepared	Internal	Internal flag indicating that a TASKS_PREPARETX task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a TASKS_PREPARERX task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next TASKS_PREPARETX task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next TASKS_PREPARERX task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.



34.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the TWI slave.

34.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

34.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master



forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 310.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 88: The TWI slave responding to a read command* on page 308. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

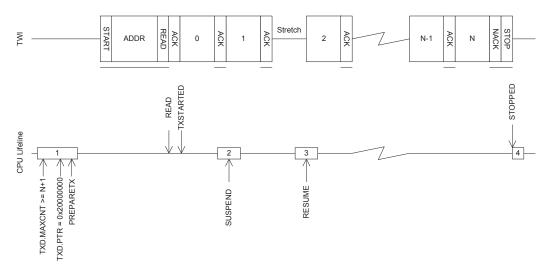


Figure 88: The TWI slave responding to a read command

34.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.



The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 310.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 89: The TWI slave responding to a write command* on page 309. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

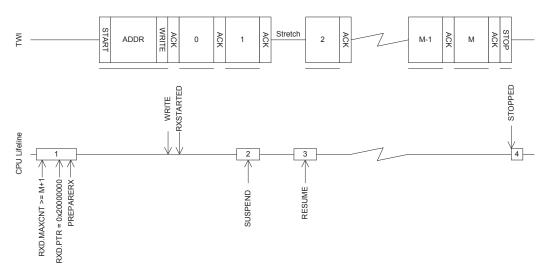


Figure 89: The TWI slave responding to a write command

34.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in Figure 90: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave on page 310.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.



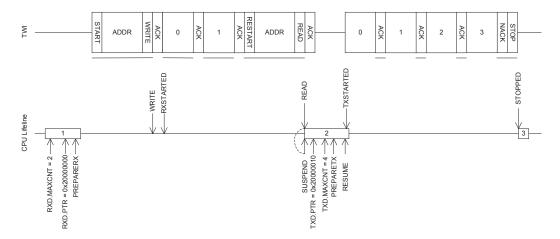


Figure 90: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

34.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

34.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

34.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 74: GPIO configuration before enabling peripheral* on page 310.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 74: GPIO configuration before enabling peripheral

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	S0D1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1



34.9 Registers

Table 75: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave	

Table 76: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

34.9.1 SHORTS

Address offset: 0x200 Shortcut register

Bit	numbe	er		3	1 30	29	28	3 27	7 26	5 25	5 24	4 23	3 2	2 2	1 2	0 1	9 1	8 1	7 16	5 15	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					В	Α													
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	(0 (0) (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	9						D	esc	crip	tion	1																			
Α	RW	WRITE_SUSPEND										Sł	nor	tcu	t be	tw	een	W	RITE	ev	ent	an	d Sl	JSP	END) ta	sk								
												Se	ee l	EVE	NTS	5_ <i>V</i>	VRI	TE a	nd	TAS	KS_	SU	SPE	ND											
			Disabled	0								D	isal	ble	sho	rtc	ut																		
			Enabled	1								Er	nab	ole s	shor	rtcı	ut																		
В	RW	READ_SUSPEND										Sł	nor	tcu	t be	tw	een	RE	AD	eve	nt	and	SU	SPE	ND	tasl	k								
												Se	ee l	EVE	NTS	S_R	EAL	ar	nd 7	ASK	(S_	sus	PEN	ID											
			Disabled	0								D	isal	ble	sho	rtc	ut																		



Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ВА
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
Enabled	1	Enable shortcut

34.9.2 INTEN

Address offset: 0x300

Enable or disable interrupt

D:+				21	20	20	20.2	J 2/	2 2 5	- 2/			21.		10 1	10.1	17 1		Г ′		12.1	12 1	11.	10	2	0 -	7	c [- ,		2	1	0
	numbe	er		31	. 30	29	28 2				1 23	3 22				18 .	1/]	16.	.5 .	L4 .	13 1	12 1	LI.			8 .	/	6 5) ²	1 3	2		
Id									G					F											В							Α	
Res		0000000				0	0 (0 0	0	0					0	0	0	0	0	0	0	0	0	0 (0	0 (0	0 () (0	0	0	0
Id		Field	Value Id	Va	llue							escri																					
Α	RW	STOPPED									En	able	or	disa	able	int	err	upt	for	ST	OPF	PED	ev	ent									
											Se	e <i>EV</i>	EN7	S	STO	PPE	ED																
			Disabled	0							Dis	sable	9																				
			Enabled	1							En	nable																					
В	RW	ERROR									En	nable	or	disa	able	int	err	upt	for	ER	RO	R ev	/en	it									
											Se	e <i>EV</i>	EN7	5 1	ERR	OR																	
			Disabled	0								sable		_																			
			Enabled	1							En	nable																					
Е	RW	RXSTARTED									En	nable	or	disa	able	int	err	upt	for	RX	STA	RTI	ED	eve	nt								
											۵۷	e <i>EV</i>	'FNI7	· C	RYS	ΤΔΕ	?TFI	ח															
			Disabled	0								sable		J_'	III	IAI	112																
			Enabled	1								nable																					
F	RW	TXSTARTED										nable		disa	able	int	erri	upt	for	ТХ	STA	RTI	ED	eve	nt								
			6: 11 1	•								e EV		5_	IXS	IAH	RIEL)															
			Disabled	0								sable																					
_	DIA	WRITE	Enabled	1								able		.1:	- 1- 1 -				£		DITI												
G	KVV	WRITE									En	able	or	JISa	abie	int	erri	upt	TOF	VV	KIII	ev.	en	τ									
											Se	e <i>EV</i>	EN7	S_1	WRI	TE																	
			Disabled	0							Dis	sable	9																				
			Enabled	1							En	nable																					
Н	RW	READ									En	able	or	disa	able	int	err	upt	for	RE	AD	eve	ent										
											Se	e <i>EV</i>	EN7	<u></u>	REA	D																	
			Disabled	0								sable																					
			Enabled	1							En	nable																					

34.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		3	1 30	29	28	27	26	25	24 2	23 2	2 2	1 20) 19	9 18	17	16	15 1	4 1	3 12	2 11	10	9	8 7	7 6	5 5	5 4	3	2	1 0
Id							Н	G				F	Е									В							Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0 () () (0	0	0	0 0
Id RW Field	Value Id	V	alue						0	Desc	ript	tion	ı																
A RW STOPPED									٧	Vrit	e '1	' to	Ena	able	inte	rru	ot fo	or ST	OPI	PED	ever	nt							
									S	See E	EVE	NTS	_5	ГОР	PED														
	Set	1							Е	nab	le																		
	Disabled	0							F	Read	l: Di	isab	led																
	Enabled	1							F	Read	l: Er	nabl	led																
B RW ERROR									٧	Vrit	e '1	' to	Ena	able	inte	rru	ot fo	r Ef	RRO	R ev	ent								
									S	See <i>E</i>	EVE	NTS	_EI	RRO	R														



Bit number	31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		H G F E B A
Reset 0x00000000	0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
E RW RXSTARTED		Write '1' to Enable interrupt for RXSTARTED event
		See EVENTS_RXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
F RW TXSTARTED		Write '1' to Enable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE	-	Write '1' to Enable interrupt for WRITE event
		See EVENTS_WRITE
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ		Write '1' to Enable interrupt for READ event
		See EVENTS_READ
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

34.9.4 INTENCLR

Address offset: 0x308 Disable interrupt

Bit	numbe	er		31 30 29	9 28 27	7 26 2	5 24	23	22 21	20	19 :	18 1	17 1	6 15	5 14	13	12 :	11 1	10 9	8	7	6 5	4	3	2	1 0
Id						Н	à			F	Е								В							Α
	et 0x0	0000000		0 0 0	0 0	0 (0 (0	0 0			0	0 (0 0	0	0	0	0 (0 0	0	0	0 (0	0		0 0
Id	RW	Field	Value Id	Value				Des	scripti	on																
Α	RW	STOPPED						Wr	ite '1'	to [Disab	ole i	nter	rup	t for	STO	PPE	ED e	event							
								See	e <i>EVEN</i>	ITS_	_STO	PPE	ED													
			Clear	1				Dis	able																	
			Disabled	0				Rea	ad: Dis	sabl	led															
			Enabled	1				Rea	ad: Ena	able	ed															
В	RW	ERROR						Wr	rite '1'	to [Disab	ole i	nter	rup	t for	r ERI	ROR	eve	ent							
								See	e <i>EVEN</i>	ITS_	_ERR	OR														
			Clear	1				Dis	able																	
			Disabled	0				Rea	ad: Dis	sabl	led															
			Enabled	1				Rea	ad: Ena	able	ed															
Е	RW	RXSTARTED						Wr	ite '1'	to [Disab	ole i	nter	rup	t for	r RXS	STAF	RTE	D eve	nt						
								See	e <i>EVEN</i>	ITS_	_RXS	TAF	RTEL)												
			Clear	1				Dis	able																	
			Disabled	0				Rea	ad: Dis	sabl	led															
			Enabled	1				Rea	ad: Ena	able	ed															
F	RW	TXSTARTED						Wr	ite '1'	to [Disak	ole i	nter	rup	t for	r TXS	TAF	RTE) eve	nt						
								See	e <i>EVEN</i>	ITS_	_TXS	TAF	RTED)												
			Clear	1				Dis	able																	
			Disabled	0				Rea	ad: Dis	abl	led															



Bit r	umbe	er		31	30 2	9 2	28 27	7 26	5 25	24	23 2	2 2	1 20	19	18	17	16	15 :	L4 1	L3 1	2 1:	1 10	9	8	7	6	5 -	4 3	2	1 0
Id								Н	I G				F	Ε									В							Α
Rese	t OxO	0000000		0	0 (0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	ript	tion																	
			Enabled	1							Read	l: Er	nable	ed																
G	RW	WRITE									Write	e '1	' to I	Disa	able	inte	erru	ıpt f	or \	N RI	TE e	ven	t							
											See L	EVE	NTS	_w	RITE	Ε														
			Clear	1							Disal	ble																		
			Disabled	0							Read	l: Di	isabl	led																
			Enabled	1							Read	l: Er	nable	ed																
Н	RW	READ									Write	e '1	' to I	Disa	able	inte	erru	ıpt f	or F	REAI) ev	ent								
											See L	EVE	NTS	_RE	AD															
			Clear	1							Disal	ble																		
			Disabled	0							Read	l: Di	isabl	led																
			Enabled	1							Read	l: Er	nable	ed																

34.9.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B A
Reset 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW OVERFLOW		RX buffer overflow detected, and prevented
	NotDetected	0 Error did not occur
	Detected	1 Error occurred
B RW DNACK		NACK sent after receiving a data byte
	NotReceived	0 Error did not occur
	Received	1 Error occurred
C RW OVERREAD		TX buffer over-read detected, and prevented
	NotDetected	0 Error did not occur
	Detected	1 Error occurred

34.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bit	numb	er		31	. 30	29	28 2	27 2	6 2	5 2	4 2	23 2	2 2	1 2	0 19	9 18	3 17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2 1	1 0
Id																																Α
Res	et 0x(0000000		0	0	0	0	0 0) (0)	0 (0 (0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						0	Desc	crip	tior	1																	
Α	R	MATCH		[0	1]						١	Nhi	ch d	of th	ne a	ddr	esse	s in	(Al	DDR	ESS	} m	atch	ed t	he i	nco	mir	ıg				
											a	ıddı	ress	;																		

34.9.7 ENABLE

Address offset: 0x500

Enable TWIS

17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
АААА
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
VIS



34.9.8 PSEL.SCL

Address offset: 0x508 Pin select for SCL signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.9 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	11111111111111111111111111111
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.10 RXD.PTR

Address offset: 0x534 **RXD** Data pointer

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	LO	9	8 7	7 (5 5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A ,	Δ Α	Δ /	Δ Δ	A	Α	Α	Α	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	o
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	PTR											D D	ata	ро	inte	r																	

34.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit	numbe	er		31	. 30	29	28	27 :	26	25 :	24	23 2	22 2	21 2	20 1	.9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																											Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	MAXCNT										Max	kim	um	nur	nbe	r of	byt	es i	n R	XD	buff	er										

34.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

Id	RW	Field	Value Id	Value	Description	
Re	set 0x	00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id						A A A A A A A
Bit	numb	er		31 30 29 28 27 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0

A R AMOUNT Number of bytes transferred in the last RXD transaction



34.9.13 TXD.PTR

Address offset: 0x544
TXD Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		TXD Data pointer

34.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 11 10	9 8 7 6	5 4	3 2	1 0
Id					АА	АА	АА	А А
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0	0 0	0 0	0 0
Id RW Field	Value Id	Value	Description					
A RW MAXCN	Т		Maximum number o	of bytes in TXD buffer				

34.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bit	numbe	r		31	. 30	29	28	3 27	26	25	24	23	22 2	21 2	20 1	19 1	.8 1	7 1	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 2	1 0
Id																										Α	Α	Α	Α	A	A A	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue	9						Des	scrip	otio	n																	
Α	R	AMOUNT										Nui	mbe	r of	f by	tes	trar	nsfe	rred	in t	he I	ast .	XD	tran	sac	tior	1					

34.9.16 ADDRESS[0]

Address offset: 0x588 TWI slave address 0

Bit number		31 30 29 28 27 26 25 24 23 2	22 21 20 19 18 17	16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id					$A \ A \ A \ A \ A \ A \ A \ A$
Reset 0x00000000		0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Des	scription		
A RW ADDRESS		TWI	I slave address		

34.9.17 ADDRESS[1]

Address offset: 0x58C TWI slave address 1

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	17 16 15 14 13 12 11 10 9 8 7	7 6 5 4 3 2 1 0
ld					A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
A RW ADDRESS			TWI slave address		

34.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

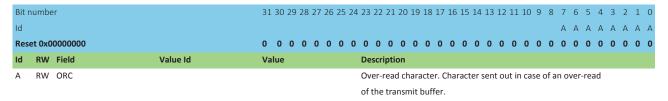


Bit r	numbe	er		31	L 30	29	28	3 27	26	25	24	1 23	3 22	2 21	. 20	19	18	17	7 16	15	14	13	12	11	10	9	8	7	6 !	5	4	3 2	2 2	0 1
Id																																	E	ВА
Res	et OxO	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 () () 1
Id	RW	Field	Value Id	Va	alue							D	escr	ipti	ion																			
Α	RW	ADDRESS0										Er	nabl	e o	r dis	sab	le a	ıdd	res	m	atch	ing	on.	ADI	ORE	SS[0]							
			Disabled	0								Di	sab	led																				
			Enabled	1								Er	nabl	ed																				
В	RW	ADDRESS1										Er	nabl	e o	r dis	sab	le a	dd	res	m	atch	ing	on .	ADI	ORE	SS[1]							
			Disabled	0								Di	sab	led																				
			Enabled	1								Er	nabl	ed																				

34.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.



34.10 Electrical specification

34.10.1 TWIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS,SCL}	Bit rates for TWIS ³⁰				kbps
I _{TWIS,100kbps}	Run current for TWIS (Average current to receive and transfer a				μΑ
	byte to RAM), 100 kbps				
I _{TWIS,400kbps}	Run current for TWIS (Average current to receive and transfer a				μΑ
	byte to RAM), 400 kbps				
I _{TWIS,IDLE}	Idle current for TWIS				μΑ
t _{TWIS,START}	Time from PREPARERX/PREPARETX task to ready to receive/				μs
	transmit				

34.10.2 TWIS slave timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes				ns
t _{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes				ns
$t_{TWIS,HD_STA,100kbps}$	TWI slave hold time from for START condition (SDA low to SCL				ns
	low), 100 kbps				
t _{TWIS,HD_STA,400kbps}	TWI slave hold time from for START condition (SDA low to SCL				ns
	low), 400 kbps				
t _{TWIS,SU_STO,100kbps}	TWI slave setup time from SCL high to STOP condition, 100 kbps				ns
t _{TWIS,SU_STO,400kbps}	TWI slave setup time from SCL high to STOP condition, 400 kbps				ns
t _{TWIS,BUF,100kbps}	TWI slave bus free time between STOP and START conditions,				ns
	100 kbps				
t _{TWIS,BUF,400kbps}	TWI slave bus free time between STOP and START conditions,				ns
	400 kbps				

High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



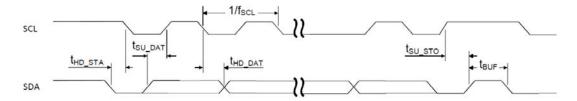


Figure 91: TWIS timing diagram, 1 byte transaction



35 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- · Full-duplex operation
- · Automatic hardware flow control
- Optional even parity bit checking and generation
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- · One or two stop bit
- Least significant bit (LSB) first

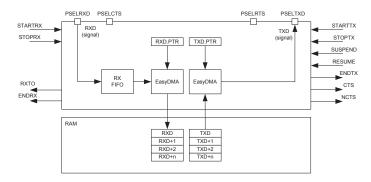


Figure 92: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

35.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

35.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.



The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

35.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled through the HWFC field in the CONFIG register, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 93: UARTE transmission* on page 320. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

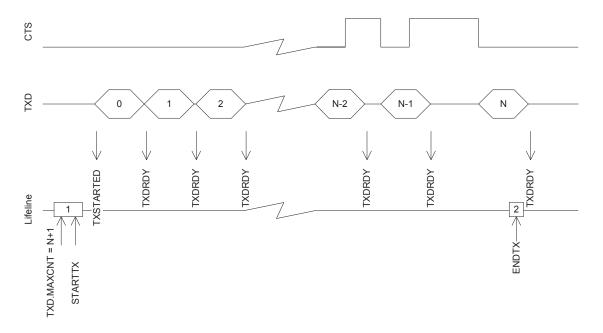


Figure 93: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER* — *Power supply* on page 67 for more information about power modes.

35.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.



The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 94: UARTE reception* on page 321.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

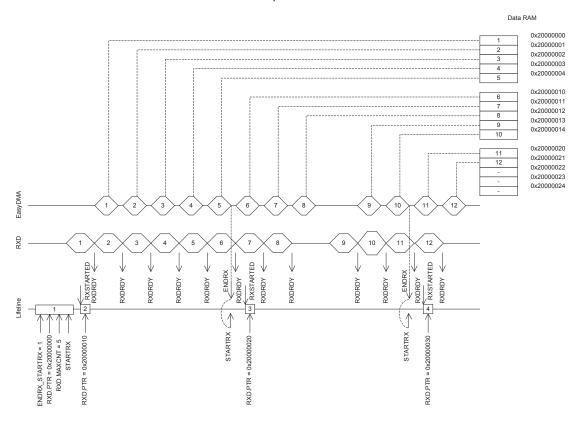


Figure 94: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

Important: If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered.



To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 95: UARTE reception with forced stop via STOPRX* on page 322. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

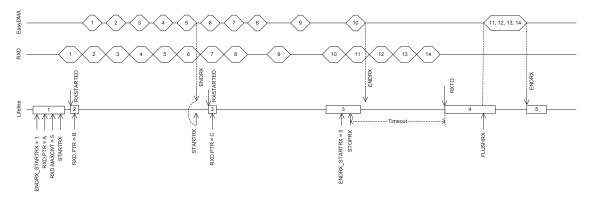


Figure 95: UARTE reception with forced stop via STOPRX

If HW flow control is enabled through the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER* — *Power supply* on page 67 for more information about power modes.

35.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

35.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

35.7 Parity and stop bit configuration

When parity is enabled through the PARITY field in the CONFIG register, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

The amount of stop bits can be configured through the STOP field in the CONFIG register.



35.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

35.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 77: GPIO configuration before enabling peripheral* on page 323.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 77: GPIO configuration before enabling peripheral

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

35.10 Registers

Table 78: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal asynchronous receiver/	
			transmitter with FasyDMA	

Table 79: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD (but potentially not yet transferred to Data RAM)
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started



Register	Offset	Description
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
		Note : this register is read / write one to clear.
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

35.10.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	er		31	30	29	28	27	26 2	25 2	4 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												D	С					
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	esci	ripti	ion																				
С	RW	ENDRX_STARTRX									Sł	hort	cut	bet	we	en E	ND	RX	eve	ent	and	rs b	ΓAR	TR	(ta	sk								_
										See EVENTS_ENDRX and TASKS_STARTRX																								
			Disabled	0					Disable shortcut																									
			Enabled	1							Enable shortcut																							
D	RW	ENDRX_STOPRX									Sł	hort	cut	bet	we	en l	END	RX	eve	ent	and	rs t	ГОР	RX	tasl	<								
											Se	ee <i>E</i>	VEN	VTS_	_EN	DR.	K ar	id 7	'AS	KS_	STO	OPF	RX											
			Disabled	0							D	isab	le s	hor	tcut																			
			Enabled	1							Er	nabl	le sł	hort	cut																			

35.10.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31	30	29	28	27 2	26 2	25 2	4 23	3 22	21 2	20	19 1	18 1	17 1	16 1	5 1	4 13	3 1:	2 11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id												L		J	1	- 1	Н							G	F	Ε			D	(C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						D	escri	ptio	n																		
Α	RW	CTS									Er	nable	or	disa	able	int	err	upt	for	CTS	ev	ent										
											Se	e EV	/EN1	TS_	CTS																	
			Disabled	0							Di	sabl	е																			
			Enabled	1							Er	nable	ė																			
В	RW	NCTS									Er	nable	or	disa	able	int	err	upt	for	NCT	S e	ven	t									
											_																					
											Se	e EV	/EN1	TS_	NCT	S																
			Disabled	0							Di	sabl	e																			
			Enabled	1							Er	nable	9																			



Bit	numb	er		31 30 2	9 28 2	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								L J I H G F E D C B A
Res	et 0x0	0000000		0 0 0	0 0 (0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
С	RW	RXDRDY						Enable or disable interrupt for RXDRDY event
								See EVENTS_RXDRDY
			Disabled	0				Disable
			Enabled	1				Enable
D	RW	ENDRX						Enable or disable interrupt for ENDRX event
								See EVENTS_ENDRX
			Disabled	0				Disable
			Enabled	1				Enable
Е	RW	TXDRDY						Enable or disable interrupt for TXDRDY event
								See EVENTS_TXDRDY
			Disabled	0				Disable
			Enabled	1				Enable
F	RW	ENDTX						Enable or disable interrupt for ENDTX event
								See EVENTS_ENDTX
			Disabled	0				Disable
			Enabled	1				Enable
G	RW	ERROR						Enable or disable interrupt for ERROR event
								See EVENTS_ERROR
			Disabled	0				Disable
			Enabled	1				Enable
Н	RW	RXTO						Enable or disable interrupt for RXTO event
								See EVENTS_RXTO
			Disabled	0				Disable
			Enabled	1				Enable
I	RW	RXSTARTED						Enable or disable interrupt for RXSTARTED event
								See EVENTS_RXSTARTED
			Disabled	0				Disable
			Enabled	1				Enable
J	RW	TXSTARTED						Enable or disable interrupt for TXSTARTED event
								See EVENTS_TXSTARTED
			Disabled	0				Disable
			Enabled	1				Enable
L	RW	TXSTOPPED						Enable or disable interrupt for TXSTOPPED event
								See EVENTS_TXSTOPPED
			Disabled	0				Disable
			Enabled	1				Enable

35.10.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	L 30	29	28	8 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id													L		J	-1		Н							G	F	Ε			D		С	ВА
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																		
Α	RW	CTS										W	ite	'1'	to I	Ena	ble	inte	erru	ıpt i	for	CTS	eve	ent									
												Se	e <i>E</i>	VEN	ITS_	_СТ	S																
			Set	1								En	abl	e																			
			Disabled	0								Re	ad:	Dis	abl	ed																	
			Enabled	1								Re	ad:	En	able	ed																	



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L JIH GFE D CBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
В	RW	NCTS			Write '1' to Enable interrupt for NCTS event
					See EVENTS_NCTS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	RXDRDY			Write '1' to Enable interrupt for RXDRDY event
					See EVENTS_RXDRDY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	ENDRX			Write '1' to Enable interrupt for ENDRX event
					See EVENTS_ENDRX
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	TXDRDY			Write '1' to Enable interrupt for TXDRDY event
					See EVENTS_TXDRDY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	ENDTX			Write '1' to Enable interrupt for ENDTX event
					See EVENTS_ENDTX
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	ERROR			Write '1' to Enable interrupt for ERROR event
					See EVENTS_ERROR
			Set	1	Enable Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	RXTO			Write '1' to Enable interrupt for RXTO event
					. See EMENTS DATO
			Set	1	See EVENTS_RXTO Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
1	RW	RXSTARTED	Litablea	-	Write '1' to Enable interrupt for RXSTARTED event
					·
			C-+	1	See EVENTS_RXSTARTED
			Set Disabled	1	Enable Pead: Disabled
			Disabled Enabled	0	Read: Disabled Read: Enabled
J	R\M/	TXSTARTED	Lilabicu	1	Write '1' to Enable interrupt for TXSTARTED event
J	IVV	MUNICIPALITY			·
			_		See EVENTS_TXSTARTED
			Set	1	Enable
			Disabled	0	Read: Disabled
	DIA	TYCTODDED	Enabled	1	Read: Enabled Write 11 to Enable interrupt for TYSTORRED event
L	KVV	TXSTOPPED			Write '1' to Enable interrupt for TXSTOPPED event
					See EVENTS_TXSTOPPED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



35.10.4 INTENCLR

Address offset: 0x308

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id		-		01 00 23 20 27 20 20 2	L J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	CTS			Write '1' to Disable interrupt for CTS event
					See EVENTS_CTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	NCTS			Write '1' to Disable interrupt for NCTS event
					See EVENTS_NCTS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	RXDRDY			Write '1' to Disable interrupt for RXDRDY event
					See EVENTS_RXDRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	ENDRX			Write '1' to Disable interrupt for ENDRX event
					Son EVENTS ENDRY
			Clear	1	See EVENTS_ENDRX Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	TXDRDY			Write '1' to Disable interrupt for TXDRDY event
			Clear	1	See EVENTS_TXDRDY Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	ENDTX	2.100.100	-	Write '1' to Disable interrupt for ENDTX event
					See EVENTS_ENDTX
			Clear	1	Disable Read: Disabled
			Disabled	1	Read: Enabled
G	RW/	ERROR	Enabled	1	Write '1' to Disable interrupt for ERROR event
•	11.00	EIIIIOII			
					See EVENTS_ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
Н	D\A/	RXTO	Enabled	1	Read: Enabled
П	IV.V.	KATO			Write '1' to Disable interrupt for RXTO event
					See EVENTS_RXTO
			Clear	1	Disable
			Disabled	0	Read: Disabled
	DIA	DVCTARTER	Enabled	1	Read: Enabled
1	ĸW	RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
					See EVENTS_RXSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
		TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event



Bit r	umbe	er		31	30 2	9 2	28 27	7 26	25	24 :	23 2	2 2	1 20	19	18	17 :	16	15 1	4 1	3 12	11	10 9	Э	8 7	6	5	4	3	2 1	1 0
Id											ı	L	J	1		Н						(3	F E			D		C E	3 A
Res	et OxO	0000000		0	0 0) (0 0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0 ()	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Val	ue					- 1	Desc	cript	ion																	
											See	EVE	NTS_	TXS	STAI	RTE	D													
			Clear	1						-	Disal	ble																		
			Disabled	0						-	Reac	d: Di	isabl	ed																
			Enabled	1						-	Reac	d: Er	nable	ed																
L	RW	TXSTOPPED								١	Writ	e '1'	' to I	Disa	ble	inte	rru	pt f	or T	XST	OPPE	D ev	/en	t						
											See	EVE	NTS_	TXS	STO	PPE	D													
			Clear	1						1	Disal	ble																		
			Disabled	0						-	Reac	d: Di	isabl	ed																
			Enabled	1						- 1	Read	d: Er	nable	ed																

35.10.5 ERRORSRC

Address offset: 0x480

Error source

Note: this register is read / write one to clear.

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	OVERRUN			Overrun error
					A start bit is received while the previous data still lies in RXD.
					(Previous data is lost.)
			NotPresent	0	Read: error not present
			Present	1	Read: error present
В	RW	PARITY			Parity error
					A character with bad parity is received, if HW parity check is
					enabled.
			NotPresent	0	Read: error not present
			Present	1	Read: error present
С	RW	FRAMING			Framing error occurred
					A valid stop bit is not detected on the serial data input after all
					bits in a character have been received.
			NotPresent	0	Read: error not present
			Present	1	Read: error present
D	RW	BREAK			Break condition
					The serial data input is '0' for longer than the length of a data
					frame. (The data frame length is 10 bits without parity bit, and
					11 bits with parity bit.).
			NotPresent	0	Read: error not present
			Present	1	Read: error present

35.10.6 ENABLE

Address offset: 0x500

Enable UART

Bit n	umbe	er		31 30	29	28 :	27 2	26 2	25 2	24 :	23 2	22 2	21 2	0 1	9 1	8 17	7 1	5 15	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																														A A	A	Α
Rese	t OxC	0000000		0 0	0	0	0	0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						- 1	Des	crip	tio	1																		
Α	RW	ENABLE								- 1	Ena	ble	or c	lisal	ole	UAF	RTE															
			Disabled	0						1	Disa	ble	UA	RTE																		



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12	11 10 9 8 7 6	5 4 3 2 1 0
Id						AAAA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
	Enabled		Enable UARTE			

35.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.8 PSEL.TXD

Address offset: 0x50C Pin select for TXD signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit	numbe	er		31 30 29 28 27 26	5 25 2	4 23	22 2	1 20	0 19	18 1	17 16	5 15	14 3	13 12	11 1	9	8	7	6	5 4	3	2	1	0
Id				В																Α	A	Α	Α	Α
Res	et 0xF	FFFFFF		1 1 1 1 1 1	1 1	1 1	1 :	1 1	. 1	1	1 1	1	1	1 1	1 1	. 1	1	1	1	1 1	1	1	1	1
Id	RW	Field	Value Id	Value		De	scrip	tion	ı															
Α	RW	PIN		[031]		Pir	num	nber																Ξ
В	RW	CONNECT				Co	nnec	tion																
			Disconnected	1		Dis	conn	ect																
			Connected	0	Co	nnec	t																	

35.10.10 PSEL.RXD

Address offset: 0x514
Pin select for RXD signal

Bit r	numbe	er		3	1 30	29	28	27	26	25	5 24	23	22	21	20	19	18 1	17 1	6 15	5 14	13	12	11	10 9	9 8	7	6	5	4	3	2	1 0
Id				В																									Α	Α	Α.	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	. 1	1	1	1	1	1	1	1 1	۱ 1	. 1	1	1	1	1 :	L 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	2						De	escri	ptio	on																	
Α	RW	PIN		[0	031	.]						Piı	n nu	mb	er																	
В	RW	CONNECT										Co	nne	ctic	n																	
			Disconnected	1								Di	scon	ne	ct																	



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 1	5 14 13 12 11 10 9	8 7 6 5	4 3 2 1 0
Id		В				A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1	1 1 1 1 1
Id RW Field	Value Id	Value	Description			
	Connected	0	Connect			

35.10.11 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

Bit number		31	. 30	29	28 :	27 .	26 2	25 2	24 2	23 2	2 21	1 20	19	18	17	16	15	14	13 1	.2 1	1 10) 9	8	7	6	5	4 3	2	1	0
Id		Α	Α	Α	Α	Α	Α /	A	A	A A	A A	Α.	Α	Α	Α	Α	Α	Α	Α /	A A	A	Α	Α	Α	Α	Α	A A	A	Α	Α
Reset 0x04000000		0	0	0	0	0	1 (0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0
Id RW Field	Value Id	Va	lue						- 1	Desc	ript	ion																		
A RW BAUDRATE									E	Baud	l rat	e																		
	Baud1200	0x	000	4F0	00				1	1200) baı	ud (a	actu	ıal r	ate	: 12	205))												
	Baud2400	0x	000	9D0	000				2	2400) bai	ud (a	actu	ıal r	ate	: 23	396)													
	Baud4800	0x	001	3B0	000				4	1800) bai	ud (a	actu	ıal r	ate	: 48	308))												
	Baud9600	0x	002	750	00				ç	9600) bai	ud (a	actu	ıal r	ate	: 95	98))												
	Baud14400	0x	003	AF0	00				1	1440	00 ba	aud	(act	ual	rat	e: 1	440	01)												
	Baud19200	0x	004	EA0	000				1	1920	00 ba	aud	(act	ual	rat	e: 1	920	08)												
	Baud28800	0x	007	5C0	00				2	2880	00 ba	aud	(act	ual	rat	e: 2	287	77)												
	Baud31250	0x	800	000	00				3	3125	0 b	aud																		
	Baud38400	0x	009	D00	000				3	3840	00 ba	aud	(act	ual	rat	e: 3	883	69)												
	Baud56000	0x	00E	500	00				į	600	00 ba	aud	(act	ual	rat	e: 5	5594	14)												
	Baud57600	0x	00E	B00	00				į	5760	00 ba	aud	(act	ual	rat	e: 5	75	54)												
	Baud76800	0x	013	A90	000				7	7680	00 ba	aud	(act	ual	rat	e: 7	692	23)												
	Baud115200	0x	01D	600	000				1	1152	00 l	baud	d (a	ctua	al ra	ite:	115	510	8)											
	Baud230400	0x	03B	000	000				2	2304	100 l	baud	d (a	ctua	al ra	ite:	23:	188	4)											
	Baud250000	0x	040	000	00				2	2500	000 I	baud	d																	
	Baud460800	0x	074	000	00				4	1608	800 I	baud	d (a	ctua	al ra	ite:	45	714	3)											
	Baud921600	0x	0F0	000	00				ç	9216	00 I	baud	d (a	ctua	al ra	ite:	94:	117	6)											
	Baud1M	0x	100	000	00				2	lMe	ga b	aud	ı																	

35.10.12 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

35.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3	2 1 0
Id				А	A A A A A	A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum number of	hytes in receive huffer		

35.10.14 RXD.AMOUNT

Address offset: 0x53C



Number of bytes transferred in the last transaction

В	it n	umbe	er		31	30	29	28 2	7 2	6 2	5 2	4 2	3 2	2 2:	1 2	0 19	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
lc																										Α	Α	Α	Α	Α	A A	4 Δ	A	Α
R	ese	t 0x0	0000000		0	0	0	0	0 0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Ic	ı	RW	Field	Value Id	Va	lue						D	esc	ript	ion	1																		
Α		R	AMOUNT									N	lum	her	of	hvt	es t	ran	sfer	red	in t	he	last	tra	nsa	ctic	n							

35.10.15 TXD.PTR

Address offset: 0x544

Data pointer

Е	Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20 1	19 1	.8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
10	d				А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	ДД	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α ,	А А
F	Rese	t Ox(000000	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
1	d	RW	Field	Value Id	Va	lue							Des	scri	otic	n																		
A	4	RW	PTR										Dat	ар	oint	ter																		

35.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10	9 8 7 6	5 4 3 2 1 0
Id					AAAA	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum number o	f bytes in transmit buffer		

35.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit	numb	er		31	30 2	29	28 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14 :	L3 1	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																								А	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x(00000000		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue						De	scri	ptic	on																		
Α	R	AMOUNT									Nu	mb	er c	of b	vtes	tra	nsf	err	ed i	n th	ne la	ast :	ran	sact	ion							

35.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit r	umber		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВВВА
Res	et 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW HWFC			Hardware flow control
		Disabled	0	Disabled
		Enabled	1	Enabled
В	RW PARITY			Parity
		Excluded	0x0	Exclude parity bit
		Included	0x7	Include even parity bit
С	RW STOP			Stop bits
		One	0	One stop bit
		Two	1	Two stop bits



35.11 Electrical specification

35.11.1 UARTE electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UARTE}	Baud rate for UARTE ³¹ .			1000	kbps
I _{UARTE1M}	Run current at max baud rate.		55		μΑ
I _{UARTE115k}	Run current at 115200 bps.		55		μΑ
I _{UARTE1k2}	Run current at 1200 bps.		55		μΑ
I _{UARTE,IDLE}	Idle current for UARTE (STARTed, no XXX activity)		1		μΑ
t _{UARTE,CTSH}	CTS high time	1			μs
t _{UARTE,START}	Time from STARTRX/STARTTX task to transmission started				μs

High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



36 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- · Optional LED output signal for optical encoders.

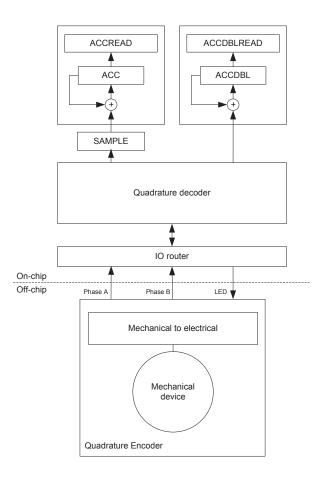


Figure 96: Quadrature decoder configuration

36.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.



The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 80: Sampled value encoding

- 1)	e pair(n	·	les pair(n)	SAMPLE register	ACC operation	ACCDBL operation	Description
Α	В	Α	В				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

36.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

36.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.



Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

36.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

36.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

36.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in



ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 81: GPIO configuration before enabling peripheral* on page 336 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 81: GPIO configuration before enabling peripheral

QDEC signal	QDEC pin	Direction	Output value	Comment	
Phase A	As specified in PSEL.A	Input	Not applicable		
Phase B	As specified in PSEL.B	Input	Not applicable		
LED	As specified in PSEL.LED	Input	Not applicable		

36.7 Registers

Table 82: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 83: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

36.7.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	numbe	er		31 30	29 2	8 27 :	26 2	5 24	23	3 22 2	21 20	0 19	18	17 1	6 15	14	13	12 1	.1 10) 9	8	7	6 5	5 4	1 3	2	1	0
Id																							G F	= E	E D	С	В	Α
Res	et 0x0	0000000		0 0	0 0	0	0 0	0 0	0	0 0	0 0	0	0	0 (0 0	0	0	0 (0 0	0	0	0	0 0) (0	0	0	0
Id	RW	Field	Value Id	Value					De	escrip	tion	1																
Α	RW	REPORTRDY_READCLRAC	С						Sh	nortcu	ut be	twee	en R	EPO	RTRI	DΥ e	ven	t and	d RE	ADC	LRA	CC 1	ask					
									See	ee <i>EVE</i>	ENTS	S_RE	POR	TRD	Y an	d <i>T</i> /	SKS	_RE	ADCI	LRA	CC							
			Disabled	0					Dis	isable	sho	rtcut	t															
			Enabled	1					En	nable s	shor	rtcut																
В	RW	SAMPLERDY_STOP							Sh	nortcu	ut be	twee	en S	AMF	PLERI	DY 6	ven	t an	d ST	OP t	ask							
									See	ee <i>EVE</i>	ENTS	5_ <i>SA</i>	MPL	.ERD	<i>Y</i> an	d TA	ISKS	ST	OP									
			Disabled	0						isable																		
			Enabled	1					En	nable s	shor	rtcut																
С	RW	REPORTRDY_RDCLRACC							Sh	nortcu	ut be	twe	en R	EPO	RTRI	DΥ e	ven	t an	d RD	CLR	ACC	tas	k					
									See	ee <i>EVE</i>	ENTS	S REI	POR	TRD	<i>Y</i> and	d <i>TA</i>	SKS	RD	CLR/	4 <i>CC</i>								
			Disabled	0						isable																		
			Enabled	1					En	nable s	shor	rtcut																
D	RW	REPORTRDY_STOP							Sh	nortcu	ut be	twe	en R	EPO	RTRI	DΥ e	vent	t an	d ST	OP t	ask							
									See	ee <i>EVE</i>	ENTS	S REI	POR	TRD	<i>Y</i> and	d <i>T/</i>	SKS	STI	OP .									
			Disabled	0						isable																		
			Enabled	1					En	nable s	shor	rtcut																
Е	RW	DBLRDY_RDCLRDBL							Sh	nortcu	ut be	twe	en D	BLR	DY e	ven	t and	d RD	CLRI	DBL	task	:						
									See	ee <i>EVE</i>	ENTS	S DB	LRD	<i>Y</i> an	d <i>TA</i>	SKS	RD	CLR	DBL									
			Disabled	0						isable		_				-												
			Enabled	1					En	nable s	shor	rtcut																
F	RW	DBLRDY_STOP							Sh	nortcu	ut be	twee	en D	BLR	DY e	ven	t and	d ST	OP to	ask								
									See	ee <i>EVE</i>	ENTS	S DB	LRD	Y an	d <i>TA</i>	SKS	STO)P										
			Disabled	0						isable					-													
			Enabled	1					En	nable s	shor	rtcut																
G	RW	SAMPLERDY_READCLRAC	С						Sh	nortcu	ıt be	twee	en S	AMF	PLERI	DY 6	ven	t an	d RE	ADO	LRA	CC	task					
									Sei	ee <i>EVE</i>	FNT	5 54	МРІ	FRD	Y an	d T	ısks	RF	ADC	IRΔ	CC							
			Disabled	0						isable		_		,,,	. ull	~ <i>17</i>	رد،دد			27171								
			Enabled	1						nable s																		
				-							251																	

36.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW SAMPLERDY			Write '1' to Enable interrupt for SAMPLERDY event
				See EVENTS_SAMPLERDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REPORTRDY			Write '1' to Enable interrupt for REPORTRDY event
				See EVENTS_REPORTRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACCOF			Write '1' to Enable interrupt for ACCOF event
				See EVENTS_ACCOF
		Set	1	Enable



Bit r	umbe	er		31	30 2	29 2	28 27	7 26	25	24	23 2	22 2	21 20	0 19	18	17	16	15	14 1	13 1	2 11	10	9	8	7 6	5	4	3	2	1 0
Id																											Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	crip	tion	1																
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: E	nabl	led																
D	RW	DBLRDY									Writ	te '1	1' to	Ena	ble	inte	rru	pt f	or D	BLR	DY 6	even	t							
											See	EVE	ENTS	_DE	BLRL	DY														
			Set	1							Enak	ble																		
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: E	nabl	led																
Е	RW	STOPPED									Writ	te '1	1' to	Ena	ble	inte	rru	pt f	or S	TOP	PED	eve	nt							
											See	EVE	ENTS	S_ST	OPI	PED														
			Set	1							Enab	ble																		
			Disabled	0							Read	d: D	isab	led																
			Enabled	1							Read	d: E	nabl	led																

36.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	umbe	r		31 3	30 2	29	28 2	7 2	26 2	5 2	24 2	3 2	2 2	21 2	20	19	18	17	7 1	6 1	.5	14	13	12	2 1	1 1	0 !	9	8	7	6	5	4	3	2	1	0
Id																																	Ε	D	С	В	Α
Rese	t 0x0	0000000		0	0 (0	0 (0	0 0)	0 0) (0	0	0	0	0	0	C) (0	0	0	0	C) () (0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Valu	ıe						D	esc	crip	tio	n																						
Α	RW	SAMPLERDY									W	∕rit	e '1	1' to	o D	isa	ble	in	ter	ru	ot f	or	SA	MF	PLE	RD	Y e	ve	nt								
											Se	ee l	EVE	ENT	<u></u>	SA	MF	LEI	RD	Υ																	
			Clear	1							D	isa	ble																								
			Disabled	0							R	eac	d: D	isa	ble	ed																					
			Enabled	1							R	eac	d: E	nak	ole	d																					
В	RW	REPORTRDY									W	∕rit	e '1	1' to	o D	isa	ble	in	ter	ru	ot 1	or	RE	РО	RT	'RD'	Y e	ver	nt								
											Se	ee l	EVE	ENT	<u>-</u> S_	RE	PO	RTI	RD'	1																	
			Clear	1							D	isa	ble																								
			Disabled	0							R	eac	d: D	isa	ble	ed																					
			Enabled	1							R	eac	d: E	nak	ole	d																					
С	RW	ACCOF									W	√rit	e '1	1' to	o D	isa	ble	in	ter	ru	ot f	or	AC	CC)F e	eve	nt										
											Se	ee i	EVE	ENT	<u>s_</u>	AC	со	F																			
			Clear	1							D	isa	ble																								
			Disabled	0							R	eac	d: D	isa	ble	ed																					
			Enabled	1							R	eac	d: E	nak	ole	d																					
D	RW	DBLRDY									W	√rit	e '1	1' to	o D	isa	ble	in	ter	ru	ot 1	or	DB	LR	DY	ev	ent	t									
											Se	ee l	EVE	ENT	<u>-</u> S_	DB	LR	DΥ																			
			Clear	1							D	isa	ble																								
			Disabled	0							R	eac	d: D	isa	ble	ed																					
			Enabled	1							R	eac	d: E	nak	ole	d																					
E	RW	STOPPED									W	/rit	e '1	1' to	o D	isa	ble	in	ter	ru	ot 1	or	ST	OP	PE	D e	ver	nt									
											Se	ee i	EVE	ENT	<u></u>	ST	OPI	PEL)																		
			Clear	1							D	isa	ble																								
			Disabled	0							R	eac	d: D	isa	ble	ed																					
			Enabled	1							R	eac	d: E	nak	ole	d																					

36.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder



Bit	numbe	er		31	1 30	29	28	8 27	7 2	26 2!	5 2	24 2	3 2	2 2	1 20) 19	9 1	8 1	.7 1	6 1	5 1	.4 1	.3 :	12 1	11 1	.0 9	9 (3 7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	(0 0) (0 0	0	0	0	0	0) (0 () ()	0 (0	0	0	0 () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	ript	tion																				
Α	RW	ENABLE		Value										le c	or di	isal	ole	the	qu	adr	atı	ire	de	code	er										
														n e	nab	led	the	e de	eco	der	pir	ns v	vill	be i	acti	ve.	Wh	en c	lisa	ble	d				
												tł	ne c	qua	drat	ure	e de	co	der	pir	ıs a	re i	not	act	ive	and	ca	n be	us	ed a	as				
													PIC).																					
			Disabled	led 0									isal	ble																					
			Enabled	1								Е	nab	le																					

36.7.5 LEDPOL

Address offset: 0x504 LED output pin polarity

Bit	num	ber			31 3	0 29	28	27	26	25 :	24	23 2	22 2	21 2	0 19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																																Α
Res	et 0	x00	000000										0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	R۱	N	Field	Value Id	Valu	ie						Des	crip	otion	1																	
Α	R۱	Ν	LEDPOL									LED	ou	tput	pin	pol	arity	/														
				ActiveLow	0							Led	act	ive	on o	utp	ut p	in lo	ow													
				ActiveHigh	0 1							Led	act	ive	on o	utp	ut p	in h	igh													

36.7.6 SAMPLEPER

Address offset: 0x508

Sample period

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW SAMPLEPER			Sample period. The SAMPLE register will be updated for every
			new sample
	128us	0	128 us
	256us	1	256 us
	512us	2	512 us
	1024us	3	1024 us
	2048us	4	2048 us
	4096us	5	4096 us
	8192us	6	8192 us
	16384us	7	16384 us
	32ms	8	32768 us
	65ms	9	65536 us
	131ms	10	131072 us

36.7.7 SAMPLE

Address offset: 0x50C Motion sample value

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	12 1	11 1	0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	R	SAMPLE		Value [-12]								Las	t m	oti	on s	sam	ple																



Id A A A A A A A A A A A A A A A A A A A
St 30 25 26 27 20 25 24 25 22 21 20 15 16 17 10 15 14 15 12 11 10 5 6 7 0 5 4 5 2 1 1
8it number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 1

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition

36.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit r	umbe	er		31	1 30	29	28	27	26 2	25 2	4 23	22	21 2	20 1	9 18	8 1	7 16	15	14	13 1	.2 1	1 10	9	8	7	6	5 4	4 3	2	1	0
Id																												Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	alue	9					De	escri	ptio	n																	
Α	RW	REPORTPER									Spe	ecifi	es t	he r	ıum	ber	of s	amı	oles	to b	e ac	cum	nula	ted	in t	he A	ACC				
											reg	giste	r be	for	e the	e RE	EPOF	RTR	DY a	ınd I	DBLI	RDY	eve	nts	can	be					
											gei	nera	ited																		
											The	e re	port	: pe	riod	in [us] i	s gi	ven	as: I	RPU	S = S	SP *	RP '	Wh	ere					
											RP	US i	s the	e re	port	pe	riod	in [us/r	epo	rt],	SP is	the	sar	npl	e pe	erio	ł			
																						and F									
																						EPOF									
			10Smpl	0							10	san	nple	s/r	epo	rt															
			40Smpl	1							40	san	nple	s/r	еро	rt															
			80Smpl	2							80	san	nple	s/r	еро	rt															
			120Smpl	3							12	0 sa	mpl	es /	rep	ort															
			160Smpl	4							16	0 sa	mpl	es /	rep	ort															
			200Smpl	5							20	0 sa	mpl	es /	rep	ort															
			240Smpl	6							24	0 sa	mpl	es /	rep	ort															
			280Smpl	7							28	0 sa	mpl	es /	rep	ort															
			1Smpl	8							1 s	samp	ole /	rep	ort																

36.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Dit months an		21	20.1	0 2	0.0-	7 20	25	24	22.5	22.2	1 20	10	10	17 1	1.0 1	г 1	1 12	12	11 1	2 0	0	7	_	_	4		1	0
Bit number		31	30 2	29 2	8 27	/ 26	25	24	23 2	22 2.	I 20) 19	18	1/ 1	16 1	.5 1	4 13	12	11 1	0 9	8	/	6	5	4 :	5 2	1	U
Id		Α	Α	A A	A Α	Α	Α	Α	Α .	ΑА	A	Α	Α	Α .	A A	Α Α	A A	Α	A A	A	Α	Α	Α	Α	A A	A A	Α	Α
Reset 0x000000	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0 (0 0	0 0	0	0 (0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	Va	lue						Des	cript	ion																	
A R ACC		[-1	.024.	.102	23]				Reg	ister	acc	umu	ılati	ing a	all va	alid	sam	ples	(not	dοι	ıble	trar	nsiti	on)				
									read	d fro	m tl	he SA	AMI	PLE	regi	ster	-											
									Dou	ıble t	tran	sitio	ns (SAN	MPL	E =	2) w	/ill n	ot be	aco	cum	ulat	ed i	in				
									this	regi	ster	. The	e va	lue	is a	32 k	bit 2'	s co	mple	mei	nt va	lue	. If a	a				
									sam	iple t	that	wou	uld (caus	e th	nis r	egist	er t	o ove	rflo	w oi	un	der	flow	V			
									is re	eceiv	ed,	the	sam	ple	will	be	igno	red :	and a	ın o	verfl	ow	eve	ent				
									(AC	COF) w	ill be	e ge	nera	ated	l. Th	ne AC	C re	giste	r is	clea	red	by					
									trigg	gerin	ng th	ne RE	EAD	CLR	ACC	or	the F	RDCI	LRAC	C ta	sk.							

36.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task



Bi	t nu	mbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α ,	Α	Α	Α	Α	Α	Α	A	Δ,	А А
Re	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id		RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Δ		R	ACCREAD		ſ ₋ 1	02/	10	123	1				Sn	ancl	hot	of t	ho	۸۲	۰ r۵	aict	٥r														

The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

36.7.11 PSEL.LED

Address offset: 0x51C Pin select for LED signal

Bit	umbe	er		31 30 29	28 2	7 26	25 2	24 2	3 22	21 2	20 1	9 18	3 17	16 1	5 14	13 1	2 11	l 10	9	8 7	6	5	4	3 2	2 1	0
Id				С																			Α	A A	Δ Δ	Α
Res	et OxF	FFFFFF		1 1 1	1 1	1	1	1 :	1 1	1	1 1	1	1	1 1	. 1	1	1 1	1	1	1 1	1	1	1	1 1	l 1	. 1
Id	RW	Field	Value Id	Value				D	escri	ptio	n															
Α	RW	PIN		[031]				Р	in nu	mbe	er															
С	RW	CONNECT						C	Conne	ctio	n															
			Disconnected	1				D	iscor	nec	t															
			Connected	0				C	Conne	ct																

36.7.12 PSEL.A

Address offset: 0x520 Pin select for A signal

Bit	numbe	er		31	30	29	28 2	27 2	6 2	5 24	4 23	3 22	21	20	19 1	18 1	7 16	15	14 1	L3 12	2 11	10	9	8	7 6	5	4	3	2	1 0
Id				С																							Α	Α	Α	А А
Re	et 0xF	FFFFFF		1	1	1	1	1	1 1	. 1	. 1	. 1	1	1	1	1 1	1	1	1	1 1	1	1	1	1 :	L 1	. 1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																
Α	RW	PIN		[0.	.31]						Pi	in nu	ımb	er																
С	RW	CONNECT									Co	onne	ectio	n																
			Disconnected	1							Di	iscoı	nnec	t																
			Connected	0							Co	onne	ect																	

36.7.13 PSEL.B

Address offset: 0x524 Pin select for B signal

Bit r	umbe	er		31	1 30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	18 1	7 16	15	14	L3 1:	2 11	10	9	8	7 (6 5	5 4	- 3	2	1 0
Id				С																								Α	A	Α	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1 1	. 1	1	1	1	1	1 1	L 1	. 1	1	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	n																
Α	RW	PIN		[0)31	.]						Pin	nu	mbe	er																
С	RW	CONNECT										Co	nne	ctio	n																
			Disconnected	1								Dis	con	nec	t																
			Connected	0								Co	nne	ct																	

36.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters



Bit	numbe	r		31 3	30 29	9 28	3 27	26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	15	14	13	12 :	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						Des	scri	ptio	n																	
Α	RW	DBFEN									Ena	ble	inp	ut d	lebo	unc	e fi	lter	S												
			Disabled	0							Del	bou	nce	inp	ut fi	lter	s dis	sabl	ed												
			Enabled	1							Del	bou	nce	inp	ut fi	lter	s en	abl	ed												

36.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit	numbe	er		31	30 2	29 2	28 2	7 26	25	24	23 :	22 2	1 2	0 19	18	17	16	15 1	L4 1	3 12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id																								Α.	Д	Α.	A	ДД	А	Α	Α
Res	et 0x0	0000010		0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	1 0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tior	1																	
Α	RW	LEDPRE		[1.	.511]					Per	iod i	n us	s the	e LEI	D is	swit	che	d oı	n pri	or to	sar	npl	ing							

36.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit num	nber			31	. 30	29	28 2	27 :	26 2	5 2	24 2	:3 22	21 2	20 :	19 1	.8 1	17 1	6 1	5 1	4 13	12	11 1	10 9	3 (3 7	6	5	4	3 : A /	2	1 (A A)
Reset 0)x00	000000		0	0	0	0	0	0 () (0 (0 0	0	0	0	0 (0 (0	0	0	0	0	0 () (0	0	0	0	0	0	0 ()
Id R	W	Field	Value Id	Va	lue						D	escr	iptio	n																		
A R		ACCDBL		[0]	15]						ti V a o il	ransi Vher ccun verfi legal	tions this nulat ow e tran ed. T	region siti	SAM giste of c nt (, ons field	1PLE dou ACC are	as roble	2). eacl / illo) wi tect	hed ega ill b ted	l its i il tra ie ge afte	maxi nsiti nera r the	mui ons ited i ma	m va will if a	sto ny o um	e the p. A doul val	n ole (or vas					

36.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit r	umbe	er		33	1 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3 2	. 1	0
Id																														A A	Α Α	АА
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue							Des	scri	ptio	n																	
Α	R	ACCDBLREAD		[0	15]						Sna	psh	ot o	of th	e A	CCD	BL	regi	ster	. Th	is fi	eld i	s up	dat	ed v	vhe	n th	ne			
												REA	ADC	LRA	CC (or R	DCL	RDE	3L ta	ask i	is tr	igge	red.									

36.8 Electrical specification

36.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{QDEC}	Run current		5		μΑ
t _{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	μs
t _{LED}	Time from LED is turned on to signals are sampled	0		511	μs



37 SAADC — Successive approximation analog-todigital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
 - One channel per single-ended input and two channels per differential input
 - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of t_{ack}.
- · Support for direct sample transfer to RAM using EasyDMA
- · Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- · Internal resistor string
- · Limit checking on the fly

37.1 Shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

37.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AIN0 to AIN7 pins, or the VDD pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.



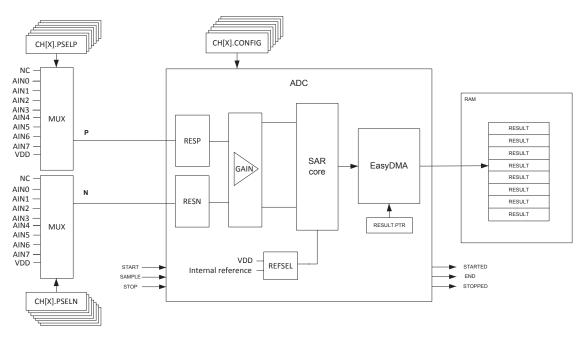


Figure 97: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

37.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

```
RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2 (RESOLUTION - m)
```

where

V(P)

is the voltage at input P

V(N)

is the voltage at input N

GAIN

is the selected gain setting

REFERENCE

is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.



The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ±0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete

37.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See Shared resources on page 343 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

Important: Channels selected for COMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

Table 84: Legal connectivity CH[n] vs. analog input

Channel input	Source	Connectivity
CH[n].PSELP	AINOAIN7	Yes(any)
CH[n].PSELP	VDD	Yes
CH[n].PSELN	AINOAIN7	Yes(any)
CH[n].PSELN	VDD	Yes

37.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

37.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 347.

37.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

fsample < 1/[tacq + tconv]



The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set 2^{OVERSAMPLE} number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE 2^{OVERSAMPLE} times from software
- · Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{\text{OVERSAMPLE}}$ times. With BURST = 1 the ADC will sample the input $2^{\text{OVERSAMPLE}}$ times as fast as it can (actual timing: $<(t_{\text{ACQ}}+t_{\text{CONV}})\times2^{\text{OVERSAMPLE}}$). Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

```
Total time < Sum(CH[x].t<sub>ACO</sub>+t<sub>CONV</sub>), x=0..enabled channels
```

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

Figure 98: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 347 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.



	31 16	15 0
RESULT.PTR	CH[2] 1 st result	CH[1] 1 st result
RESULT.PTR + 4	CH[1] 2 nd result	CH[5] 1 st result
RESULT.PTR + 8	CH[5] 2 nd result	CH[2] 2 nd result
	(.)
RESULT.PTR + 2*(RESULT.MAXCNT – 2)	CH[5] last result	CH[2] last result

Figure 98: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

Figure 99: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 347 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

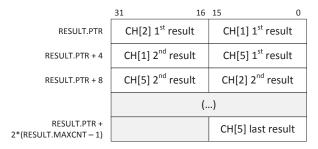


Figure 99: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled

37.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 100: ADC* on page 348. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.



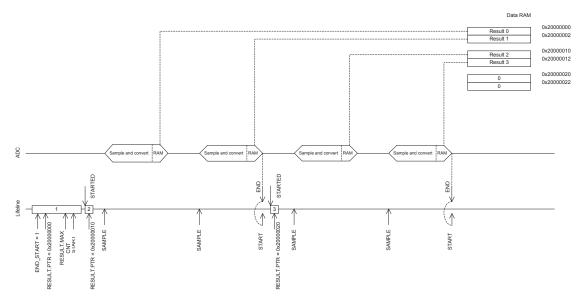


Figure 100: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 346 for more information about Scan mode.

37.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See Figure 101: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP) on page 349. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.



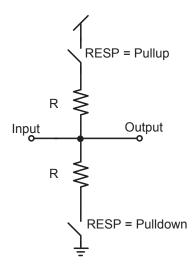


Figure 101: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

37.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- · Internal reference
- · VDD as reference

The internal reference results in an input range of ± 0.6 V on the ADC core. VDD as reference results in an input range of $\pm VDD/4$ on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 \text{ V or } +-\text{VDD}/4)/\text{Gain}
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 \text{ V})/(1/6) = 3.6 \text{ V}
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

37.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 102: Simplified ADC sample network* on page 350. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 85: Acquisition time* on page 350.



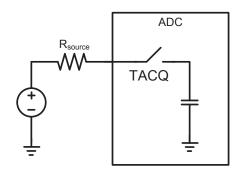


Figure 102: Simplified ADC sample network

Table 85: Acquisition time

TACQ [μs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

37.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

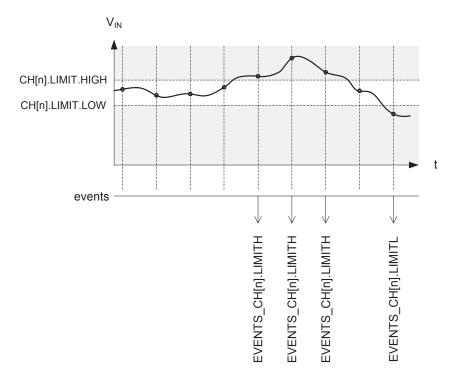


Figure 103: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled



outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

37.11 Registers

Table 86: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40007000	SAADC	SAADC	Analog-to-digital converter	

Table 87: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFSE	0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be
		needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM.
EVENTS_CALIBRATEDON	0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]



Register	Offset	Description
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is
		applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

37.11.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31 30	29	28 2	27 2	6 25	5 24	23 2	22 2	21 20	0 19	9 18	3 17	16	15	14 :	13 1	.2 1	1 10	9	8	7	6	5 4	3	2	1 0
Id											,	Vι	ΙT	S	R	Q	Р	О	N N	M I	. K	J	1	Н	G	F E	D	С	ВА
Res	et 0x0	0000000		0 0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Value	9					Des	crip	otion	1																
Α	RW	STARTED								Enal	ble	or d	isab	ole ir	nter	rup	t fo	r ST	ART	ED	ever	it							
										See	EVE	ENTS	5_57	TART	TED														
			Disabled	0						Disa	ble																		
			Enabled	1						Ena	ble																		
В	RW	END								Enal	ble	or d	isab	ole ir	nter	rup	t fo	r EN	ID e	ven	t								
										See	EVE	ENTS	_ <i>EI</i>	VD															
			Disabled	0						Disa	ble																		
			Enabled	1						Enal	ble																		
С	RW	DONE								Enal	ble	or d	isab	ole ir	ntei	rup	t fo	r DC	ONE	eve	nt								
										See	EVE	ENTS	_D	ONE	Ē														
			Disabled	0						Disa	ble																		
			Enabled	1						Enal	ble																		
D	RW	RESULTDONE								Enal	ble	or d	isab	ole ir	nter	rup	t fo	r RE	SUL	.TD(ONE	eve	nt						
										See	EVE	ENTS	_RE	ESUI	LTD	ONE	Ε												
			Disabled	0						Disa	ble																		
			Enabled	1						Enal	ble																		



Bit r	numbe	er		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res		0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
E	RW	CALIBRATEDONE			Enable or disable interrupt for CALIBRATEDONE event
					See EVENTS_CALIBRATEDONE
			Disabled	0	Disable
-	DVA	CTORRED	Enabled	1	Enable
F	KVV	STOPPED			Enable or disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Disabled	0	Disable
G	D\A/	CHOLIMITH	Enabled	1	Enable Enable or disable interrupt for CH[0].LIMITH event
U	IVV	CHOLIMITH			
			Disabled	0	See EVENTS_CH[0].LIMITH
			Disabled Enabled	0	Disable Enable
Н	RW	CHOLIMITL	Lilabled	1	Enable or disable interrupt for CH[0].LIMITL event
			Disabled	0	See EVENTS_CH[0].LIMITL Disable
			Enabled	1	Enable
ı	RW	CH1LIMITH	Lindbled	-	Enable or disable interrupt for CH[1].LIMITH event
					See EVENTS_CH[1].LIMITH
			Disabled	0	Disable
			Enabled	1	Enable
J	RW	CH1LIMITL			Enable or disable interrupt for CH[1].LIMITL event
					See EVENTS_CH[1].LIMITL
			Disabled	0	Disable
			Enabled	1	Enable
K	RW	CH2LIMITH			Enable or disable interrupt for CH[2].LIMITH event
					See EVENTS_CH[2].LIMITH
			Disabled	0	Disable
			Enabled	1	Enable
L	RW	CH2LIMITL			Enable or disable interrupt for CH[2].LIMITL event
					See EVENTS_CH[2].LIMITL
			Disabled	0	Disable
			Enabled	1	Enable
М	RW	CH3LIMITH			Enable or disable interrupt for CH[3].LIMITH event
					See EVENTS_CH[3].LIMITH
			Disabled	0	Disable
N	R/V/	CH3LIMITL	Enabled	1	Enable Enable or disable interrupt for CH[3].LIMITL event
14	IVVV	CHISCHVIIIE			
			Disabled	0	See EVENTS_CH[3].LIMITL Disable
			Disabled Enabled	0	Enable
0	RW	CH4LIMITH		-	Enable or disable interrupt for CH[4].LIMITH event
					See EVENTS_CH[4].LIMITH
			Disabled	0	Disable
			Enabled	1	Enable
Р	RW	CH4LIMITL			Enable or disable interrupt for CH[4].LIMITL event
					See EVENTS_CH[4].LIMITL
			Disabled	0	Disable
			Enabled	1	Enable
Q	RW	CH5LIMITH			Enable or disable interrupt for CH[5].LIMITH event
					See EVENTS_CH[5].LIMITH



Bit	numbe	er		3	1 30	29	9 28	27	26	25	24	23	22	21	20 1	19 1	18 1	.7 1	6 1	5 1	4 13	3 1:	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id														٧	U	Т	S	R (Q I	P (N	I N	1 L	K	J	1	Н	G	F	Ε	D (В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	٧	alu	е						De	escri	ptio	n																		
			Disabled	0								Dis	sable	e																			
			Enabled	1								Ena	able	è																			
R	RW	CH5LIMITL										Ena	able	or	disa	ble	int	errı	ıpt	for	CH[5].l	IMI	TL e	ven	t							
												See	e <i>EV</i>	/EN	TS (CH[.	51.L	IMI	TL														
			Disabled	0									sable		_	٠	•																
			Enabled	1								Ena	able	9																			
S	RW	CH6LIMITH										Ena	able	or	disa	ble	int	errı	ıpt	for	CH[6].l	IMI	TH 6	ever	nt							
												۲.,	o EV	/E N I	TC /	CLIE	c1 i	18.41	T 11														
			Disabled	0									e <i>EV</i> sable		13_0	СП[oj.L	IIVII	ΙП														
			Enabled	1									able																				
т	D\A/	CH6LIMITL	Eliablea	1									able		dica	hlo	int	orri	ınt	for	CHI	61 1	11/41	TI o	von	+							
	11.00	CHOLINITE																		101	CH	0].1	_11V11	ILC	ven	·							
													e EV		TS_(CH[6].L	IMI	TL														
			Disabled	0									sable																				
			Enabled	1									able																				
U	RW	CH7LIMITH										Ena	able	or	disa	ble	int	erru	ıpt	for	CH[7].[IMI	TH 6	ever	nt							
												See	e <i>EV</i>	/EN	TS_0	CH[7].L	IMI	ТН														
			Disabled	0								Dis	sable	e																			
			Enabled	1								Ena	able	9																			
V	RW	CH7LIMITL										Ena	able	or	disa	ble	int	errı	ıpt	for	CH[7].l	IMI	TL e	ven	t							
												See	e <i>EV</i>	/FN	rs (СНГ	71 I	IМГ	TI														
			Disabled	0									sable			[,		-														
			Enabled	1									able																				
				_																													

37.11.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit nui	mbe	r		31	30	29	28 2	7 2	26 2	5 24	4 23	3 22	21 2	20 19	9 1	8 1	7 16	5 15	14	13	12 :	11 1	0 9	8	7	6	5	4 3	3 2	1 0
Id													V	U T	· S	R	R Q	. P	0	N	М	LI	(J	1	Н	G	F	Ε [) С	ВА
Reset	0x00	0000000		0	0	0	0 0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0 0
Id F	RW	Field	Value Id	Va	lue						D	escri	ptio	n																
A F	RW	STARTED									W	/rite '	1' to	o Ena	able	e int	terr	upt	for	STA	RTE	D ev	/ent							
											Se	ee <i>EV</i>	EN7	rs_st	TAR	TEL	D													
			Set	1							Er	nable																		
			Disabled	0							Re	ead: I	Disa	bled																
			Enabled	1							Re	ead: I	Enal	bled																
B F	RW	END									W	/rite '	1' to	o Ena	able	e int	terr	upt	for	END	ev	ent								
											Se	ee <i>EV</i>	EN7	rs_EI	ND															
			Set	1							Er	nable																		
			Disabled	0							Re	ead: I	Disa	bled																
			Enabled	1							Re	ead: I	Enal	bled																
C F	RW	DONE									W	/rite '	1' to	o Ena	able	e int	terr	upt	for	DOI	NE e	ven	t							
											Se	ee <i>EV</i>	EN7	rs_D	ON	Ε														
			Set	1							Er	nable																		
			Disabled	0							Re	ead: I	Disa	bled																
			Enabled	1							Re	ead: I	Enal	bled																
D F	RW	RESULTDONE									W	/rite '	1' to	o Ena	able	e int	terr	upt	for	RES	ULT	10d	VE e	vent	t					
											Se	ee <i>EV</i>	EN7	rs_Ri	ESL	ILTL	DON	ΙE												
			Set	1							Er	nable																		
			Disabled	0							Re	ead: I	Disa	bled																
			Enabled	1							Re	ead: I	Enal	bled																



Bit r	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Е	RW CALIBRATEDONE			Write '1' to Enable interrupt for CALIBRATEDONE event
				See EVENTS_CALIBRATEDONE
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW CHOLIMITH			Write '1' to Enable interrupt for CH[0].LIMITH event
				See EVENTS CUIOLUMITH
		Cot	1	See EVENTS_CH[0].LIMITH
		Set	1 0	Enable Read: Disabled
		Disabled Enabled	1	Read: Disabled Read: Enabled
Н	RW CHOLIMITL	Ellabled	1	Write '1' to Enable interrupt for CH[0].LIMITL event
"	KW CHOLIWITE			
				See EVENTS_CH[0].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW CH1LIMITH			Write '1' to Enable interrupt for CH[1].LIMITH event
				See EVENTS_CH[1].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW CH1LIMITL			Write '1' to Enable interrupt for CH[1].LIMITL event
				See EVENTS_CH[1].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW CH2LIMITH			Write '1' to Enable interrupt for CH[2].LIMITH event
				See EVENTS_CH[2].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW CH2LIMITL			Write '1' to Enable interrupt for CH[2].LIMITL event
				See EVENTS_CH[2].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
М	RW CH3LIMITH			Write '1' to Enable interrupt for CH[3].LIMITH event
				,
		Cot	1	See EVENTS_CH[3].LIMITH
		Set Disabled	1 0	Enable Read: Disabled
		Enabled	1	Read: Disabled
N	RW CH3LIMITL	LIIGDICU	1	Write '1' to Enable interrupt for CH[3].LIMITL event
14	NVV CHISCHVIIIE			
				See EVENTS_CH[3].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
0	DVA/ CHALINATTI	Enabled	1	Read: Enabled
0	RW CH4LIMITH			Write '1' to Enable interrupt for CH[4].LIMITH event



Bit r	numbe	r		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0(0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
					See EVENTS_CH[4].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Р	RW	CH4LIMITL			Write '1' to Enable interrupt for CH[4].LIMITL event
					See EVENTS_CH[4].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Q	RW	CH5LIMITH			Write '1' to Enable interrupt for CH[5].LIMITH event
					See EVENTS_CH[5].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
R	RW	CH5LIMITL			Write '1' to Enable interrupt for CH[5].LIMITL event
					See EVENTS_CH[5].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
S	RW	CH6LIMITH			Write '1' to Enable interrupt for CH[6].LIMITH event
					See EVENTS_CH[6].LIMITH
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Т	RW	CH6LIMITL			Write '1' to Enable interrupt for CH[6].LIMITL event
					See EVENTS_CH[6].LIMITL
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
U	RW	CH7LIMITH			Write '1' to Enable interrupt for CH[7].LIMITH event
			Set	1	See EVENTS_CH[7].LIMITH Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
V	RW	CH7LIMITL			Write '1' to Enable interrupt for CH[7].LIMITL event
			Sot	1	See EVENTS_CH[7].LIMITL
			Set Disabled	0	Enable Read: Disabled
			Enabled	1	Read: Enabled
			LITABLEU	1	Neau. Liiabieu

37.11.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 :	20	19 1	18 :	17 :	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1 ()
Id														V	U	Т	S	R	Q	Р	О	N	M	L I	(J	- 1	Н	G	F	Ε	D	С	В	Д
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 (o
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																			
Α	RW	STARTED										Wr	ite '	1' t	o D	isab	le i	inte	rru	pt 1	for	STA	RTE	D e	ven	t								_
												See	e EV	ENT	TS_:	STA	RTE	ED																
			Clear	1								Dis	able	2																				



Bit r	umber			31	30	29	28 2	7 26	25 :	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id										V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0000	00000		0	0	0	0 (0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fie	eld	Value Id		lue					Description
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
В	RW EN	ND .								Write '1' to Disable interrupt for END event
										See EVENTS_END
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
С	RW DO	ONE								Write '1' to Disable interrupt for DONE event
										See EVENTS_DONE
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
D	RW RE	ESULTDONE								Write '1' to Disable interrupt for RESULTDONE event
										See EVENTS_RESULTDONE
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Е	RW CA	ALIBRATEDONE								Write '1' to Disable interrupt for CALIBRATEDONE event
										See EVENTS_CALIBRATEDONE
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
F	RW ST	OPPED								Write '1' to Disable interrupt for STOPPED event
										See EVENTS_STOPPED
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
G	RW CH	HOLIMITH								Write '1' to Disable interrupt for CH[0].LIMITH event
										See EVENTS_CH[0].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW CH	HOLIMITL								Write '1' to Disable interrupt for CH[0].LIMITL event
										See EVENTS_CH[0].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
I	RW CF	H1LIMITH								Write '1' to Disable interrupt for CH[1].LIMITH event
										See EVENTS_CH[1].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
J	RW CH	H1LIMITL								Write '1' to Disable interrupt for CH[1].LIMITL event
										See EVENTS_CH[1].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
K	RW CH	H2LIMITH								Write '1' to Disable interrupt for CH[2].LIMITH event
										See EVENTS_CH[2].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			2.0dbicu	J						Ticaa, Sisabica



Bit r	umbe	er		3:	1 30	29	28 2	7 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id										V U T S R Q P O N M L K J I H G F E D C B A
Res	et OxC	0000000		0	0	0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	V	alue					Description
			Enabled	1						Read: Enabled
L	RW	CH2LIMITL								Write '1' to Disable interrupt for CH[2].LIMITL event
										See EVENTS_CH[2].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
М	RW	CH3LIMITH								Write '1' to Disable interrupt for CH[3].LIMITH event
										See EVENTS_CH[3].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
	5111	0.10.11.41.	Enabled	1						Read: Enabled
N	RW	CH3LIMITL								Write '1' to Disable interrupt for CH[3].LIMITL event
										See EVENTS_CH[3].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
	DIA	CHALINATTI	Enabled	1						Read: Enabled
0	KVV	CH4LIMITH								Write '1' to Disable interrupt for CH[4].LIMITH event
										See EVENTS_CH[4].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
Р	D\A/	CH4LIMITL	Enabled	1						Read: Enabled
r	NVV	CH4LIMITE								Write '1' to Disable interrupt for CH[4].LIMITL event
										See EVENTS_CH[4].LIMITL
			Clear	1						Disable
			Disabled Enabled	0						Read: Disabled Read: Enabled
Q	RW	CH5LIMITH	Ellableu	1						Write '1' to Disable interrupt for CH[5].LIMITH event
~		0.132								
			Clear	1						See EVENTS_CH[5].LIMITH Disable
			Clear Disabled	1						Read: Disabled
			Enabled	1						Read: Enabled
R	RW	CH5LIMITL								Write '1' to Disable interrupt for CH[5].LIMITL event
										See EVENTS CHIET LIMITI
			Clear	1						See EVENTS_CH[5].LIMITL Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
S	RW	CH6LIMITH								Write '1' to Disable interrupt for CH[6].LIMITH event
										See EVENTS_CH[6].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Т	RW	CH6LIMITL								Write '1' to Disable interrupt for CH[6].LIMITL event
										See EVENTS_CH[6].LIMITL
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
U	RW	CH7LIMITH								Write '1' to Disable interrupt for CH[7].LIMITH event
										See EVENTS_CH[7].LIMITH
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled



Bit	numbe	er		31	1 30	29	2	8 2	7 :	26 2	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8 7	' (5 5	4	3	2	1 0	ĺ
Id															٧	U	Т	S	R	Q	Р	О	Ν	M	L	K	J	I F	1 (6 F	Е	D	С	ВА	ı
Res	et 0x0	0000000		0	0	0	C	0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	(0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	alue								De	scri	iptio	on																			l
V	RW	CH7LIMITL											Wr	ite	'1' 1	to [Disa	ble	int	errı	upt	for	СН	[7].	LIM	ITL (eve	nt							
													See	e <i>E</i> \	/EN	ITS_	СН	[7].	LIN	IITL															
			Clear	1									Dis	abl	e																				
			Disabled	0									Rea	ad:	Dis	able	ed																		
			Enabled	1									Rea	ad:	Ena	able	d																		

37.11.4 STATUS

Address offset: 0x400

Status

Bit	num	ber			3	1 30	29	28	27	26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																																			Α
Res	et 0	х О О	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	N	Field	Value Id	V	alue	9						D	escr	ipti	on																			
Α	R		STATUS										St	atu	S																				
				Ready	0								ΑI	DC i	s re	ady	. No	on	-go	ing	cor	ive	rsic	n.											
				Busy	1								ΑI	DC i	s bu	sy.	Con	ver	sior	n in	pro	ogr	ess.												

37.11.5 ENABLE

Address offset: 0x500 Enable or disable ADC

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Res	et 0 x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	ENABLE			Enable or disable ADC
			Disabled	0	Disable ADC
			Enabled	1	Enable ADC
					When enabled, the ADC will acquire access to the analog input
					pins specified in the CH[n].PSELP and CH[n].PSELN registers.

37.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELP		Analog positive input channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7
	VDD	9 VDD



37.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit n	umbe	r		31	30	29	28 2	7 2	6 25	5 24	23 22	2 21	1 20	19	18	17 :	16 1	15 1	L4 1	3 12	11	10	9	8	7	6	5 4	, ,	_	1 0 A A
Rese	t 0x00	0000000		0	0	0	0 (0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desci	ript	ion																	
Α	RW	PSELN									Analo	og n	nega	tive	inp	ut,	ena	ble	s dif	fere	ntia	l ch	anr	nel						
			NC	0							Not c	oni	nect	ed																
			AnalogInput0	1							AIN0																			
			AnalogInput1	2							AIN1																			
			AnalogInput2	3							AIN2																			
			AnalogInput3	4							AIN3																			
			AnalogInput4	5							AIN4																			
			AnalogInput5	6							AIN5																			
			AnalogInput6	7							AIN6																			
			AnalogInput7	8							AIN7																			
			VDD	9							VDD																			

37.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

Bit	numb	er		31	. 30 :	29 2	28 2	7 26	5 25	24	23	22 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id										G			F		Е	Ε	E				D		С	С	С			В	В		A	A
Res	et 0x(00020000		0	0	0	0 0	0	0	0	0	0 0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						De	script	ion																			
Α	RW	RESP									Po	sitive	chai	nnel	res	sisto	or c	ont	rol													
			Bypass	0							Ву	pass r	esis	tor I	ado	ler																
			Pulldown	1							Pu	II-dow	n to	GN	ID																	
			Pullup	2							Pu	ll-up t	o VI	DD																		
			VDD1_2	3							Set	t inpu	t at	VDD)/2																	
В	RW	RESN									Ne	gative	cha	anne	el re	esis	tor	cor	itro	I												
			Bypass	0							Ву	pass r	esis	tor I	ado	ler																
			Pulldown	1							Pu	II-dow	n to	GN	ID																	
			Pullup	2							Pu	II-up t	o VI	DD																		
			VDD1_2	3							Set	t inpu	t at	VDD)/2																	
С	RW	GAIN									Ga	in con	trol																			
			Gain1_6	0							1/6	6																				
			Gain1_5	1							1/5	5																				
			Gain1_4	2							1/4	4																				
			Gain1_3	3							1/3	3																				
			Gain1_2	4							1/2	2																				
			Gain1	5							1																					
			Gain2	6							2																					
			Gain4	7							4																					
D	RW	REFSEL									Re	feren	ce co	ontr	ol																	
			Internal	0							Int	ernal	refe	ren	ce (0.6	V)															
			VDD1_4	1							VD	D/4 a	s re	fere	nce	:																
Ε	RW	TACQ									Ac	quisiti	on t	ime	, th	e ti	me	th	e Al	OC t	ıse:	s to	sar	mpl	le th	ne ii	npu	t				
											vol	ltage																				
			3us	0							3 u	ıs																				
			5us	1							5 u	ıs																				
			10us	2							10	us																				
			15us	3							15	us																				
			20us	4							20	us																				



Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23 2	2 2:	1 20	19	18	17	16	15	14 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id											G			F		Ε	Ε	Ε			D		С	С	С		E	3 B			Α	Α
Res	et 0x0	0020000		0	0	0	0	0	0	0	0	0 (0	0	0	0	1	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	alue						- 1	Desc	ript	ion																		
			40us	5							4	40 u	S																			
F	RW	MODE									ı	Enab	ole d	liffe	ren	tial	mo	de														
			SE	0								Sing	e ei	nde	d, P	SEL	N w	ill b	e ig	nore	d, n	egat	ive	inp	ut t	οА	DC					
												shor	ted	to 0	SND)																
			Diff	1							-	Diffe	ren	tial																		
G	RW	BURST									-	Enab	le b	urs	t m	ode																
			Disabled	0							ı	Burs	t m	ode	is d	lisal	oled	(nc	rm	al op	erat	ion)										
			Enabled	1							ı	Burs	t m	ode	is e	nab	led	. SA	ADO	C tak	es 2	^OV	ERS	ΑN	1PLE	nu	mbe	er of				
												sam	nles	asi	ast	as i	t ca	n a	nd	send	s th	av.	eras	e t	o Da	ata	RAN	1.				

37.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit	num	ber			31	. 30	29	28	27	26	25	24	23	22 :	21 :	20 1	.9 1	18 1	17 1	16 1	15 1	14 :	13 :	12 :	11 1	10	9	8	7	6	5	4	3 2	1	. 0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	A	Α .	Α	Α.	Α	Α	Α	Α	A A	Δ	А
Res	et 0	x7F	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RV	N	Field	Value Id	Va	lue							De	scrip	otio	n																			
Α	RV	Ν	LOW		[-3	3276	8 t	0 +3	327	'67]			Lov	v le	vel I	limi	t																		
В	RV	Ν	HIGH		[-3	3276	8 t	0 +3	327	67]			Hig	h le	vel	limi	t																		

37.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

Bit r	umbe	r		31	L 30 2	9 2	28 2	7 26	25	24	23 2	22 2	21 20	1	9 18	3 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	2 1	0
Id																												A	Α Δ	A	Α
Res	et OxO	0000000		0	0)	0 0	0	0	0	0	0	0 0	C	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue						Des	crip	tion																		
Α	RW	PSELP									Ana	log	posit	tive	e inp	out	cha	nne	1												
			NC	0							Not	cor	nnect	ted																	
			AnalogInput0	1							AIN	0																			
			AnalogInput1	2							AIN	1																			
			AnalogInput2	3							AIN	2																			
			AnalogInput3	4							AIN	3																			
			AnalogInput4	5							AIN	4																			
			AnalogInput5	6							AIN	5																			
			AnalogInput6	7							AIN	6																			
			AnalogInput7	8							AIN	7																			
			VDD	9							VDD)																			

37.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bit	numbe	er		3	1 30	29	28	27	26	25	24	23 2	22 2	1 2	0 19	9 1	8 17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																													Α	A A	A /	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	٧	alue	9						Des	crip	tion	1																	
Α	RW	PSELN										Ana	log ı	neg	ativ	e ir	nput	, en	able	es d	iffe	ent	ial cl	nanı	nel							
			NC	0								Not	con	nec	ted																	
			AnalogInput0	1								AIN	0																			



Bit number		31	. 30	29 :	28 2	27 :	26 2	5 2	4 2	3 22	21	20	19	18	17 :	L6 1	L5 1	4 1	3 12	11	10	9	8	7	6 5	4	3	2	1 ()
Id																										Α	Α	Α	A A	4
Reset 0x00000000		0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 ()	0 0	0	0	0	0 ()
Id RW Field	Value Id	Va	alue						D	escr	iptic	n																		
	AnalogInput1	2							Α	IN1																				
	AnalogInput2	3							Α	IN2																				
	AnalogInput3	4							Α	IN3																				
	AnalogInput4	5							Α	IN4																				
	AnalogInput5	6							Α	IN5																				
	AnalogInput6	7							Α	IN6																				
	AnalogInput7	8							Α	IN7																				
	VDD	9							٧	DD																				

37.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

nput configuration for CH[1			
iit number	31		24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			G F E E E D C C C B B A A
leset 0x00020000			0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	ie Id Va	lue	Description
RW RESP			Positive channel resistor control
Вура			Bypass resistor ladder
	down 1		Pull-down to GND
Pulli	•		Pull-up to VDD
VDD	1_2 3		Set input at VDD/2
RW RESN			Negative channel resistor control
Вура			Bypass resistor ladder
	down 1		Pull-down to GND
Pulli			Pull-up to VDD
VDD	1_2 3		Set input at VDD/2
RW GAIN			Gain control
Gair	1_6 0		1/6
Gair	1_5 1		1/5
Gair	_		1/4
Gair	1_3 3		1/3
Gair	1_2 4		1/2
Gair			1
Gair			2
Gair	14 7		4
RW REFSEL			Reference control
Inte	rnal 0		Internal reference (0.6 V)
VDD	1_4 1		VDD/4 as reference
RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
3us	0		3 us
5us	1		5 us
10us	2		10 us
15us	3		15 us
20us	5 4		20 us
40u:	5		40 us
RW MODE			Enable differential mode
SE	0		Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
Diff	1		Differential
Diff G RW BURST	1		Differential Enable burst mode



Bit number		31 30 29 28 27	7 26 25 24 23 2	21 20 19	9 18 17	16 15	14 13	12 11	10	9	8 7	6	5	4	3 2	1	0
Id			G	F	E E	Е		D	С	С	С		В	В		Α	Α
Reset 0x00020000		0 0 0 0 0	0 0 0 0 0	0 0 0	0 1	0 0	0 0	0 0	0	0	0 0	0	0	0	0 0	0	0
Id RW Field	Value Id	Value	Desc	ription													
	Enabled	1	Burst	mode is	enabled	l. SAA[OC take	s 2^O\	/ERS	AM	PLE r	num	ber	of			
			samp	les as fast	as it c	an, and	l sends	the av	erag	ge to	Dat	a RA	M.				

37.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bit	num	nbe	r		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	19 1	l8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	ВЕ	3 B	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α Α	A	Α	Α
Res	et 0)x7F	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	R	w	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	R۱	W	LOW		[-3	3276	8 t	0 +3	327	67]			Lov	v le	vel l	imi	t																	
В	R۱	W	HIGH		[-3	3276	8 t	0 +3	327	67]			Hig	h le	vel	limi	it																	

37.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit number		31 3	30 29	28	27	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14 :	L3 1	.2 1	1 10	9	8	7	6	5 4	1 3	2	1 0
Id																									A	Δ Δ	Α	A A
Reset 0x00000000		0	0 0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0 0
Id RW Field	Value Id	Valu	ue					D	escr	iptic	n																	
A RW PSELP								Α	nalo	g po	siti	ve i	npı	ut c	han	ne												
	NC	0						N	lot c	onne	cte	ed																
	AnalogInput0	1						Α	IN0																			
	AnalogInput1	2						Α	IN1																			
	AnalogInput2	3						Α	IN2																			
	AnalogInput3	4						Α	IN3																			
	AnalogInput4	5						Α	IN4																			
	AnalogInput5	6						Α	IN5																			
	AnalogInput6	7						Α	IN6																			
	AnalogInput7	8						Α	IN7																			
	VDD	9						V	DD																			

37.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELN		Analog negative input, enables differential channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7
	AnalogInput0 AnalogInput1 AnalogInput2 AnalogInput3 AnalogInput4 AnalogInput5 AnalogInput6	1 AIN0 2 AIN1 3 AIN2 4 AIN3 5 AIN4 6 AIN5 7 AIN6



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	VDD	9	VDD

37.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

t number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		(G FEEE D CCC BB AA
eset 0x00020000		0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
RW Field	Value Id	Value	Description
RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
			samples as fast as it can, and sends the average to Data RAM.

37.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel



Bit	numbe	er		33	1 30	29	28	27	26	25	24	23	22 2	1 2	20 19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				В	В	В	В	В	В	В	В	В	В	В	ВВ	В	В	В	Α	Α	Α.	Δ	A	Α	Α	Α	Α	Α	Α	A A	Α	Α
Res	et 0 x7	FFF8000		0	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Α	RW	LOW		[-]	327	68 t	0 +	327	67]			Lov	v lev	el li	imit																	
D	RW	HIGH		г.	277	co +		227	671			۵ia	h lev	ر ا ا	limi+																	

37.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit r	numbe	er		31	30 2	9 28	3 27	26 2	5 24	23 2	2 21	20	19 1	.8 1	7 16	15	14 1	13 12	11	10 !	9	8 7	6	5		3 2 A A	_	0 A
Res	et 0x0	0000000		0	0 (0 0	0	0 (0	0 0	0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue					Desc	riptic	n																
Α	RW	PSELP								Anal	og po	siti	ve ir	put	chai	nnel												
			NC	0						Not	conne	ecte	ed															
			AnalogInput0	1						AIN0)																	
			AnalogInput1	2						AIN1																		
			AnalogInput2	3						AIN2	2																	
			AnalogInput3	4						AIN3	3																	
			AnalogInput4	5						AIN4	ļ																	
			AnalogInput5	6						AIN5	;																	
			AnalogInput6	7						AIN6	5																	
			AnalogInput7	8						AIN7	,																	
			VDD	9						VDD																		

37.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
A RW PSELN			Analog negative input, enables differential channel
	NC	0	Not connected
	AnalogInput0	1	AINO
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 1	19 18 17 16	5 15 14 13 12 11	. 10 9 8 7 6	5 5 4 3 2 1 0
Id		G	F	E E E	D	ССС	B B A A
Reset 0x00020000		0 0 0 0 0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
Id RW Field	Value Id	Value	Description				
A RW RESP			Positive chann	nel resistor	control		



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		(G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0 0	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
			samples as fast as it can, and sends the average to Data RAM.

37.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit r	numbe	er		31	L 30	29	28	27	26	25	24 2	23 2	22 2	1 20	0 19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id				В	В	В	В	В	В	В	В	В	ВЕ	3 B	В	В	В	В	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	A	A /	A A
Res	et 0x7	'FFF8000		0	1	1	1	1	1	1	1	1	1 1	1	. 1	1	1	1	1	0	0	0 (0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	alue						ı	Des	crip	tion	1																	
Id A		Field LOW	Value Id				to +	327	'67]				crip																			

37.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]



Bit	numbe	er		31	30 2	9 2	28 2	7 2	6 25	5 24	23 2	2 2	1 20	19	18	17	16	15	14 1	.3 12	2 11	10	9	8	7	6 !	5 4	3	2	1 0
Id																											Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0 0) (0 0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	crip	tion																	
Α	RW	PSELP									Anal	log	posit	ive	inp	ut c	han	nel												
			NC	0							Not	con	nect	ed																
			AnalogInput0	1							AIN)																		
			AnalogInput1	2							AIN1	1																		
			AnalogInput2	3							AIN	2																		
			AnalogInput3	4							AIN3	3																		
			AnalogInput4	5							AIN	4																		
			AnalogInput5	6							AINS	5																		
			AnalogInput6	7							AIN	ŝ																		
			AnalogInput7	8							AIN	7																		
			VDD	9							VDD)																		

37.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit r	numbe	er		31	30 2	29 2	28 2	7 2	26 25	5 24	1 23	22 2	21 20) 1	9 18	17	16	15	14	13 1	L2 1	1 10	9	8	7	6	5 4	4 3	3 2	1	0
Id																											,	Α Α	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0 ()	0 0	0	0	0	0 0	(0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	scrip	otion																		
Α	RW	PSELN									Ana	alog	nega	ativ	e in	put	, en	able	es d	iffer	enti	al cl	nanr	nel							
			NC	0							Not	t cor	nnect	tec	I																
			AnalogInput0	1							AIN	10																			
			AnalogInput1	2							AIN	11																			
			AnalogInput2	3							AIN	12																			
			AnalogInput3	4							AIN	13																			
			AnalogInput4	5							AIN	14																			
			AnalogInput5	6							AIN	15																			
			AnalogInput6	7							AIN	16																			
			AnalogInput7	8							AIN	17																			
			VDD	9							VDI	D																			

37.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit r	numbe	er		31	30 29	9 2	8 27	26	25	24	23.2	2 21	20	19	18	17	16	15	14	13 1	12 1	1 10	9	8	7	6 5	. 4	3	2	1 0
Id										G			F			E					D -		С	- C		F	В			 А А
	et 0x0	0020000		0	0 0	C	0 (0	0	0	0	0 0	0	0	0	1	0	0	0	0	0 (0 (0	0	0	0 0	0	0		0 0
Id	RW	Field	Value Id	Va	lue						Des	cripti	ion																	
Α	RW	RESP									Posi	tive	char	nnel	res	sist	or c	onti	rol											
			Bypass	0							Вур	ass re	esist	or I	ado	ler														
			Pulldown	1							Pull	-dow	n to	GN	ID															
			Pullup	2							Pull	up to	o VE	D																
			VDD1_2	3							Set	input	at \	VDD)/2															
В	RW	RESN									Neg	ative	cha	nne	el re	esis	tor	con	tro											
			Bypass	0							Вур	ass re	esist	or I	ado	ler														
			Pulldown	1							Pull	-dow	n to	GN	ID															
			Pullup	2							Pull	up t	o VE	D																
			VDD1_2	3							Set	input	at \	VDD)/2															
С	RW	GAIN									Gair	n con	trol																	
			Gain1_6	0							1/6																			
			Gain1_5	1							1/5																			



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G F E E E D C C C B B A A
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Gain1_4	2 1/4
	Gain1_3	3 1/3
	Gain1_2	4 1/2
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	O Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

37.11.25 CH[4].LIMIT

Address offset: 0x55C

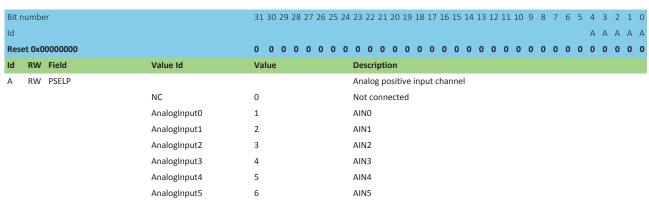
High/low limits for event monitoring a channel

Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B B B B B B B	3
Reset 0x7FFF8000	0 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW LOW	[-32768 to +32767]	Low level limit
B RW HIGH	[-32768 to +32767]	High level limit

37.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]





Bit number		31 30 29 28	27 26 25 24 23 22	21 20 19	18 17 1	16 15	14 13	12 11	10 9	8	7	6	5	4	3 2	1 0
Id														Α	A A	АА
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0	0 0 0	0 0	0 0	0 0	0 0	0 (0	0	0	0	0	0 0	0 0
Id RW Field	Value Id	Value	Descr	iption												
	AnalogInput6	7	AIN6													
	AnalogInput7	8	AIN7													
	Analoginput	O	Ally													

37.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit	numb	er		31	30 2	9 2	28 2	7 2	26 2	5 2	24 23	22	21 2	0 2	19 1	.8 1	17 1	6 1	L5 1	4 1	3 1	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																												,	4 <i>A</i>	A A	Α	Α
Res	et 0x	0000000		0	0 ()	0 0)	0 0) (0 0	0	0	0	0 (0	0 ()	0 (0 (0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	n																		
Α	RW	PSELN									Aı	nalo	g neg	gati	ve i	npı	ut, e	na	bles	dit	fere	entia	ıl ch	ann	ıel							
			NC	0							N	ot co	onne	cte	d																	
			AnalogInput0	1							ΑI	N0																				
			AnalogInput1	2							Al	N1																				
			AnalogInput2	3							Al	N2																				
			AnalogInput3	4							Al	N3																				
			AnalogInput4	5							Al	N4																				
			AnalogInput5	6							Al	N5																				
			AnalogInput6	7							Al	N6																				
			AnalogInput7	8							Al	N7																				
			VDD	9							VI	DD																				
			• .																													

37.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

Bit	numbe	er		3	1 30	29	28	27	26 2	25 2	24 2	23	22 21	L 20	0 19	18	3 17	7 16	5 1	5 1	4 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id											G			F		Е	Е	E				D		С	С	С		E	ВВ			Α	Α
Res	et 0x0	0020000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	1	. 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	Field	Value Id	٧	alue	•						Des	script	ion	1																		
Α	RW	RESP									F	Pos	sitive	cha	anne	el r	esis	tor	CO	ntro	ol												
			Bypass	0							E	Вур	pass r	esi	stor	lac	dde	r															
			Pulldown	1							F	Pul	ll-dow	n t	o G	ND																	
			Pullup	2							F	Pul	ll-up t	o V	/DD																		
			VDD1_2	3							S	Set	inpu	t at	t VD	D/2	2																
В	RW	RESN									١	Ne	gative	ch	nanr	iel	resi	sto	r co	onti	ol												
			Bypass	0							E	Вур	pass r	esi	stor	lac	dde	r															
			Pulldown	1							F	Pul	ll-dow	n t	o G	ND																	
			Pullup	2							F	Pul	ll-up t	o V	/DD																		
			VDD1_2	3							S	Set	inpu	t at	t VD	D/2	2																
С	RW	GAIN									(Gai	in con	tro	ol																		
			Gain1_6	0							1	1/6	5																				
			Gain1_5	1							1	1/5	5																				
			Gain1_4	2							1	1/4	1																				
			Gain1_3	3							1	1/3	3																				
			Gain1_2	4							1	1/2	2																				
			Gain1	5							1	1																					
			Gain2	6							2	2																					
			Gain4	7							4	4																					
D	RW	REFSEL									F	Ref	ferend	ce c	cont	rol																	
			Internal	0							- 1	nte	ernal	ref	ere	nce	(0.	6 V)														



Bit r	numbe	er		31	30	29 2	28 2	27 2	26 2	5 2	4 23	22	21	20 1	19 :	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	C
Id										G	à			F		Е	Ε	Ε			- 1	D	C	С	С			В	В		Α	
Res	et 0x0	0020000		0	0	0	0	0	0 0	0	0	0	0	0	0	0	1	0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																		
			VDD1_4	1							VD	D/4	as	refe	erer	nce																
Е	RW	TACQ									Ac	quis	itio	n tir	ne,	the	e ti	me	the	ΑD	C us	ses	to sa	amp	le t	ne i	npu	it				
											vo	ltag	e																			
			3us	0							3 ι	ıs																				
			5us	1							5 ι	ıs																				
			10us	2							10	us																				
			15us	3							15	us																				
			20us	4							20	us																				
			40us	5							40	us																				
F	RW	MODE									En	able	dif	fere	enti	al n	noc	le														
			SE	0							Sir	ngle	end	ed,	PSI	ELN	l wi	II b	e ig	nor	ed,	neg	ativ	e in	out	to A	ADC					
											sh	orte	d to	GN	۱D																	
			Diff	1							Dif	ffere	entia	al																		
G	RW	BURST									En	able	bu	rst r	mo	de																
			Disabled	0							Bu	rst i	mod	e is	dis	abl	led	(no	rm	al o	oera	atio	n)									
			Enabled	1							Bu	rst i	mod	e is	en	abl	ed.	SA	ADO	tal	es	2^C	VEF	RSAN	ИPL	E n	umb	oer	of			
											saı	mpl	es a	s fas	st a	s it	ca	ո, a	nd:	send	ls tl	he a	ver	age	to D	ata	RA	Μ.				

37.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B B B B B B	B	3
Res	et 0x7FFF8000		0 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description	
Id A	RW Field RW LOW	Value Id	Value [-32768 to +32767]	Description Low level limit	

37.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit number Id		31 30	29	28 2	27 2	26 25	5 24	23	22 2	21 20) 19	18	17	16	15	14 1	3 12	2 11	10	9	8	7	6 5		3 A	2 1 A <i>A</i>	1 0 A A
Reset 0x00000000		0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0 0	0 0
Id RW Field	Value Id	Value						Des	scrip	tion																	
A RW PSELP								Ana	alog	posi	tive	inp	ut c	han	nel												
	NC	0						Not	t cor	nec	ted																
	AnalogInput0	1						AIN	10																		
	AnalogInput1	2						AIN	11																		
	AnalogInput2	3						AIN	12																		
	AnalogInput3	4						AIN	13																		
	AnalogInput4	5						AIN	14																		
	AnalogInput5	6						AIN	15																		
	AnalogInput6	7						AIN	16																		
	AnalogInput7	8						AIN	17																		
	VDD	9						VDI	D																		

37.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]



Bit	numbe	er		31	30 2	9 2	28 2	7 2	6 25	24	23 2	2 21 :	20	19 1	8 1	7 1	6 1	5 1	1 13	3 12	11	10	9	8	7	6 !	5 4	. 3	2	1	0
Id																											Δ	A	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0 0) (0	0	0 0	0	0	0 () (0 0) (0	0	0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	riptio	n																		
Α	RW	PSELN									Anal	og ne	gat	ive i	npı	ıt, e	nak	les	diff	erei	ntia	l cha	ann	el							
			NC	0							Not o	conne	cte	d																	
			AnalogInput0	1							AIN0																				
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

input configuration ic		
Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		G F E E E D C C C B B A
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW RESP		Positive channel resistor control
	Bypass	0 Bypass resistor ladder
	Pulldown	1 Pull-down to GND
	Pullup	2 Pull-up to VDD
	VDD1_2	3 Set input at VDD/2
B RW RESN		Negative channel resistor control
	Bypass	0 Bypass resistor ladder
	Pulldown	1 Pull-down to GND
	Pullup	2 Pull-up to VDD
	VDD1_2	3 Set input at VDD/2
C RW GAIN		Gain control
	Gain1_6	0 1/6
	Gain1_5	1 1/5
	Gain1_4	2 1/4
	Gain1_3	3 1/3
	Gain1_2	4 1/2
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	O Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential



Bit	numl	per		3	1 30	29	9 28	3 27	7 26	5 25	5 24	1 2	3 22	2 2 1	20	19	18	17	16	15	14	13	12 1	.1 1	0 9	9 8	7	6	5	4	3	2	1	0
Id											G	i			F		Ε	Ε	Ε				D	(0				В	В			Α	Α
Res	et Ox	00020000		0	0	0	0	0	0	0	0	C	0	0	0	0	0	1	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0
Id	RW	/ Field	Value Id	V	alue	9						D	esci	ipti	on																			
G	RW	/ BURST										Е	nab	e b	urs	t mo	ode																	_
			Disabled	0								В	urst	mo	de	is d	isak	olec	d (no	orm	al o	per	atio	n)										
			Enabled	1								В	urst	mo	de	is e	nab	led	. SA	AD	C ta	kes	2^0	OVE	RSA	MP	LE i	num	be	r of				
												Sã	amp	les	as f	ast	as i	t ca	ın, a	and	sen	ds 1	he a	avei	age	to	Dat	a R	ΑM	١.				

37.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit r	umb	ber			3:	1 3	30	29	28	27	7 26	5 2!	5 2	4 2	3 2	2 2	21 2	20 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id					В		В	В	В	В	В	В	3 E	ВЕ	3 E	ВІ	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	١,	A A
Res	et Ox	۲F	FF8000		0		1	1	1	1	1	1	1 1	1 1	L :	1 :	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	V	Field	Value Id	V	alı	ue							D	esc	crip	tio	n																			
Α	RW	V	LOW		[-	32	76	8 t	0 +	32	767]		L	ow	lev	el l	imi	t																		
В	RW	V	HIGH		[-	32	76	8 t	0 +	32	767	1		Н	ligh	ı lev	vel	limi	it																		

37.11.34 CH[7].PSELP

Address offset: 0x580

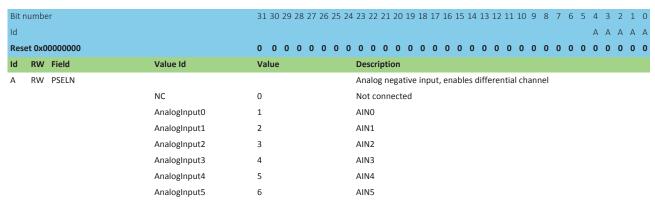
Input positive pin selection for CH[7]

Bit r	numbe	r		31	30 2	29 2	28 2	7 2	6 25	24	23	22	21 2	20 1	19 1	18 1	7 1	6 1	15 1	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																													Α	A A	A A	Α.
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 (0 (0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																		
Α	RW	PSELP									An	alog	gpos	sitiv	/e ir	าрน	t ch	anı	nel													
			NC	0							No	t co	nne	cte	d																	
			AnalogInput0	1							ΑI	NO																				
			AnalogInput1	2							ΑI	V1																				
			AnalogInput2	3							ΑI	V2																				
			AnalogInput3	4							ΑI	N3																				
			AnalogInput4	5							ΑI	٧4																				
			AnalogInput5	6							ΑI	N 5																				
			AnalogInput6	7							ΑI	٧6																				
			AnalogInput7	8							ΑI	٧7																				
			VDD	9							VD	D																				

37.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]





Bit number		31 30 29	28 27	26	25 24	4 23	3 22 :	21 2	0 19	18	17	16 1	.5 1	4 13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id																						Α	4 А	Α	Α
Reset 0x00000000		0 0 0	0 0	0	0 0	0	0	0 (0	0	0	0 (0 (0	0	0 (0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Value				D	escrip	ptior	1																
	AnalogInput6	7				ΑI	N6																		
	AnalogInput7	8				ΑI	N7																		
	VDD	9				VI	DD																		

37.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

Bit r	umbe	er		31 30	0 29	28	27 2	6 25	5 24	23	22 2	1 20	19	18	17	16	15	14	13	12	11 :	10	9 8	8 7	7 (5 5	4	3	2	1
Id									G			F		Ε	Ε	E				D		С	C (С		В	В			A
Res	et 0x0	0020000		0 0	0	0	0 (0 0	0	0	0 0	0	0	0	1	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0
Id	RW	Field	Value Id	Value	е					De	script	ion																		
Α	RW	RESP								Pos	sitive	cha	nnel	re	sist	or (cont	rol												
			Bypass	0						Вур	pass r	esis	tor I	ado	der															
			Pulldown	1						Pul	II-dov	n to	GN	ID																
			Pullup	2						Pul	ll-up t	o VI	DD																	
			VDD1_2	3						Set	t inpu	t at	VDD)/2																
В	RW	RESN								Ne	gative	e ch	anne	el r	esis	tor	cor	itro	I											
			Bypass	0						Вур	pass r	esis	tor I	ado	der															
			Pulldown	1						Pul	II-dov	n to	GN	ID																
			Pullup	2						Pul	ll-up t	o VI	DD																	
			VDD1_2	3						Set	t inpu	t at	VDD)/2																
С	RW	GAIN								Gai	in cor	ntro	l																	
			Gain1_6	0						1/6	5																			
			Gain1_5	1						1/5	5																			
			Gain1_4	2						1/4	4																			
			Gain1_3	3						1/3	3																			
			Gain1_2	4						1/2	2																			
			Gain1	5						1																				
			Gain2	6						2																				
			Gain4	7						4																				
D	RW	REFSEL								Ref	feren	ce c	ontr	ol																
			Internal	0						Inte	ernal	refe	eren	ce l	(0.6	V)														
			VDD1_4	1						VD	D/4 a	s re	fere	nce	ē															
E	RW	TACQ								Acc	quisit	ion 1	time	, th	ne ti	me	e the) A	Cι	ıses	to	san	ıple	the	in	put				
										vol	ltage																			
			3us	0						3 u	IS																			
			5us	1						5 u	IS																			
			10us	2						10	us																			
			15us	3						15	us																			
			20us	4						20	us																			
			40us	5						40	us																			
F	RW	MODE								Ena	able d	liffe	rent	ial	mo	de														
			SE	0						Sin	ıgle eı	nded	d, PS	ELI	N w	ill b	oe ig	gnoi	ed,	ne	gati	ive i	npu	it to	Αſ	C				
										sho	orted	to G	SND																	
			Diff	1						Dif	feren	tial																		
G	RW	BURST								Ena	able b	urs	t mo	de																
			Disabled	0						Bui	rst m	ode	is di	sak	led	(n	orm	al c	pei	atio	on)									
			Enabled	1						Bui	rst m	ode	is er	nab	led	. SA	AAD	C ta	kes	2^	OVE	ERS	٩MF	PLE	nuı	nbe	r of	:		
											nples									-h-a				_						

37.11.37 CH[7].LIMIT

Address offset: 0x58C



High/low limits for event monitoring a channel

Bit r	านท	nbei	r		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	8 1	7 16	15	14	13	12	11	10	9	8	7 6	5 5	5 4	3	2	1)
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	3 B	В	Α	Α	Α	Α	Α	Α	Α	A	A A	A /	\ <i>A</i>	A	Α	Α .	Ą
Res	et 0	x7F	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	L 1	. 1	1	0	0	0	0	0	0	0) (0) (0	0	0)
Id	R	w	Field	Value Id	Va	lue							Des	scri	otio	n																		
Α	R	W	LOW		[-3	3276	8 t	0 +3	327	67]			Lov	v le	vel l	imi	t																	
В	R'	W	HIGH		[-3	3276	8 t	0 +3	327	67]			Hig	h le	vel	limi	it																	

37.11.38 RESOLUTION

Address offset: 0x5F0
Resolution configuration

Bit	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				ААА
Res	et 0x00000001		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW Field	Value Id	Value	Description
Α	RW VAL			Set the resolution
		8bit	0	8 bit
		10bit	1	10 bit
		12bit	2	12 bit
		14bit	3	14 bit

37.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Bit r	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	23	22 2	21 20	19	9 18	17	16	15	14 1	3 12	11	10	9	8	7 (5 5	4	3	2 2	1 0
Id																												Α	A A	A A
Res	et 0x0	0000000		0	0	0	0 (0 0	0 0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 () (0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						Des	scrip	tion																	
Α	RW	OVERSAMPLE									Ove	ersa	mple	co	ntro	ol														
			Bypass	0							Вур	oass	over	san	npli	ng														
			Over2x	1							Ove	ersa	mple	2x																
			Over4x	2							Ove	ersa	mple	4x																
			Over8x	3							Ove	ersa	mple	8x																
			Over16x	4							Ove	ersa	mple	16	X															
			Over32x	5							Ove	ersa	mple	32	X															
			Over64x	6							Ove	ersa	mple	64	X															
			Over128x	7							Ove	ersa	mple	12	8x															
			Over256x	8							Ove	ersa	mple	25	6х															

37.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bit	umbe	er		31	30 2	9 28	3 27	26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																						В		Α	Α	Α	A	Α	A A	Α Α	Α	Α	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	ue						De	scri	ptic	n																			
Α	RW	CC		[80.	.204	7]					Ca	ptur	e a	nd (com	ηра	ire	valı	ле.	San	nple	rat	te is	16	MI	Hz/0	СС						
В	RW	MODE									Sel	ect	mo	de 1	for :	sar	npl	e ra	ite	con	trol												
			Task	0							Rat	te is	coı	ntro	olle	d fr	om	s SA	MF	LE 1	task	<											
			Timers	1							Rat	te is	col	ntro	olle	d fr	om	ı lo	cal	time	er (ı	use	CC	to c	ont	trol	the	rat	e)				



37.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit n	umb	er		33	1 30	29	28	27	26	25	24	23	22	21	20 :	19	18 :	17 :	16 1	L5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Α	Α Α	Α Α	A	Α	Α	Α	Α	Α	Α	A	A A	А А
Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	V	alue							De	scri	ptic	on																		
Α	RW	PTR										Da	ta n	oin	ter																		

37.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19	18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3	3 2 1 0
Id				AAAA	A A A A A A A	A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum numh	per of buffer words to tran	nsfer	

37.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A	Α	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				
Α	R	AMOUNT										Nu	mb	er c	f b	uffe	er w	oro	ls t	ran	sfe	rre	d si	nce	last	t ST	AR	Т. Т	his						-

register can be read after an END or STOPPED event.

37.12 Electrical specification

37.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution				LSB
INL	Integral non-linearity, 10-bit resolution				LSB
V _{OS}	Differential offset error (calibrated), 10-bit resolution ^a				LSB
C _{EG}	Gain error temperature coefficient				%/°C
f _{SAMPLE}	Maximum sampling rate				kHz
t _{ACQ,10k}	Acquisition time (configurable), source Resistance <= 10kOhm				μs
t _{ACQ,40k}	Acquisition time (configurable), source Resistance <= 40kOhm				μs
t _{ACQ,100k}	Acquisition time (configurable), source Resistance <= 100kOhm				μs
t _{ACQ,200k}	Acquisition time (configurable), source Resistance <= 200kOhm				μs
t _{ACQ,400k}	Acquisition time (configurable), source Resistance <= 400kOhm				μs
t _{ACQ,800k}	Acquisition time (configurable), source Resistance <= 800kOhm				μs
t _{CONV}	Conversion time				μs
I _{ADC,CONV}	ADC current during ACQuisition and CONVersion				μΑ
I _{ADC,IDLE}	Idle current, when not sampling, excluding clock sources and				μΑ
	regulator base currents ³²				

^a Digital output code at zero volt differential input.

When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active,



Symbol	Description	Min.	Тур.	Max.	Units
E _{G1/6}	Error ^b for Gain = 1/6				%
E _{G1/4}	Error ^b for Gain = 1/4			••	%
E _{G1/2}	Error ^b for Gain = 1/2				%
E _{G1}	Error ^b for Gain = 1			••	%
C _{SAMPLE}	Sample and hold capacitance at maximum gain ³³				pF
R _{INPUT}	Input resistance			••	ΜΩ
E _{NOB}	Effective number of bits, differential mode, 12-bit resolution,				Bit
	$1/1$ gain, 3 μs acquisition time, crystal HFCLK, 200 ksps				
S _{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-			••	dB
	bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
S _{FDR}	Spurious free dynamic range, differential mode, 12-bit				dBc
	resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
R _{LADDER}	Ladder resistance				kΩ

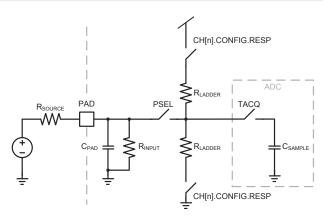


Figure 104: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($t_{ADC,CONV}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

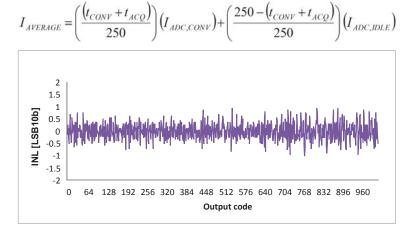


Figure 105: ADC INL vs Output Code

refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACQ} and other resources' needs, the appropriate base current needs to be taken into account.

Does not include temperature drift

Maximum gain corresponds to highest capacitance.



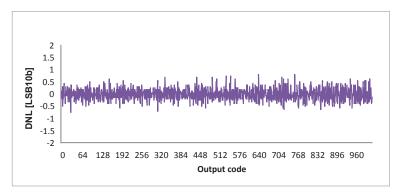


Figure 106: ADC DNL vs Output Code

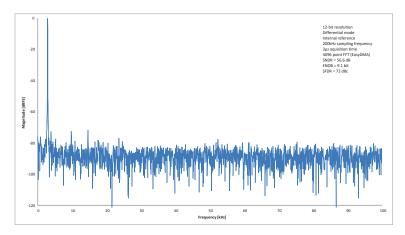


Figure 107: FFT of a 2.8 kHz sine at 200 ksps ()

37.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.



38 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived either from an analog input pin (AIN0-AIN6) or VDD/2. VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
 - · Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
 - Configurable 50 mV hysteresis
- Reference inputs (VREF):
 - VDD
 - External reference from AIN0 to AIN7 (between 0 V and VDD)
 - Internal references 1.2 V, 1.8 V and 2.4 V
- · Three speed/power consumption modes: low-power, normal and high-speed
- Single-pin capacitive sensor support
- Event generation on output changes
 - UP event on VIN- > VIN+
 - DOWN event on VIN- < VIN+
 - · CROSS event on VIN+ and VIN- crossing
 - · READY event on core and internal reference (if used) ready

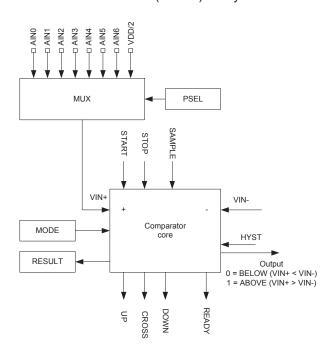


Figure 108: Comparator overview

Once enabled (using the *ENABLE* register), the comparator is started by triggering the START task and stopped by triggering the STOP task. After a start-up time of $t_{COMP,START}$, the comparator will generate a READY event to indicate that it is ready for use and that its output is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.



38 Operation modes

The comparator can be configured to operate in two main operation modes, differential mode and single-ended mode. See the *MODE* register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the *PSEL* register to select any of the AIN0-AIN6 pins (or VDD/2) as VIN+ input, irregardless of the operation mode selected for the comparator. The source of VIN- depends on which operation mode is used:

- · Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the *HYST* register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see *Figure 111: Comparator in single-ended mode* on page 381). This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 112: Hysteresis example where VIN+ starts below VUP* on page 381 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to *RESULT* register by triggering the SAMPLE task.

38.1 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the differential mode:

- PSEL
- MODE
- EXTREFSEL

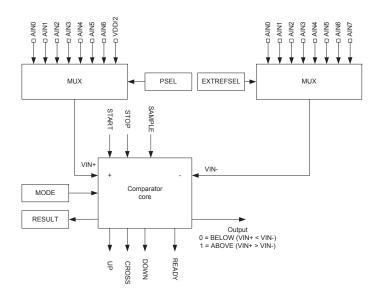


Figure 109: Comparator in differential mode



Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When *HYST* register is turned on while in this mode, the output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes lower than VIN- - (V_{DIFFHYST} / 2). It will also change from BELOW to ABOVE whenever VIN+ becomes higher than VIN- + (V_{DIFFHYST} / 2). This behavior is illustrated in *Figure 110: Hysteresis enabled in differential mode* on page 380.

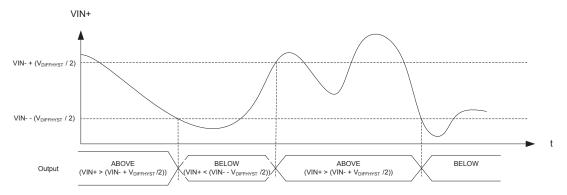


Figure 110: Hysteresis enabled in differential mode

38.2 Single-ended mode

In single-ended mode, VIN- is derived from the reference ladder.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the single-ended mode:

- PSEL
- MODE
- REFSEL
- EXTREFSEL
- TH

The reference ladder uses the reference voltage (VREF) to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured using THUP and THDOWN respectively in the *TH* register. VREF can be derived from any of the available reference sources, configured using the *EXTREFSEL* and *REFSEL* registers as illustrated in *Figure 111: Comparator in single-ended mode* on page 381. When AREF is selected in the *REFSEL* register, the *EXTREFSEL* register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.



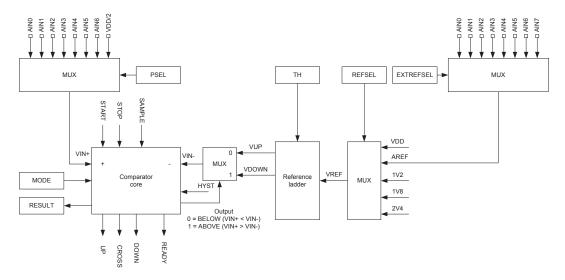


Figure 111: Comparator in single-ended mode

Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the *RESULT* register, VIN- will switch to VDOWN. When VIN+ falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis can be generated as illustrated in *Figure 112: Hysteresis example where VIN+ starts below VUP* on page 381 and *Figure 113: Hysteresis example where VIN+ starts above VUP* on page 382.

Writing to *HYST* has no effect in single-ended mode, and the content of this register is ignored.

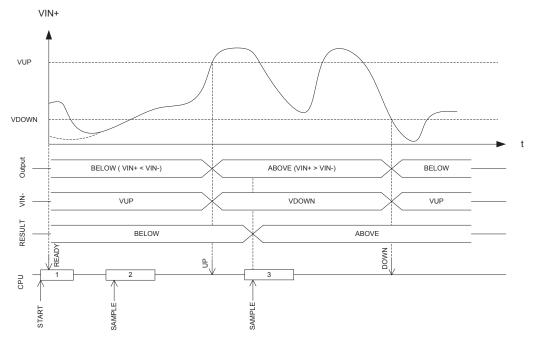


Figure 112: Hysteresis example where VIN+ starts below VUP



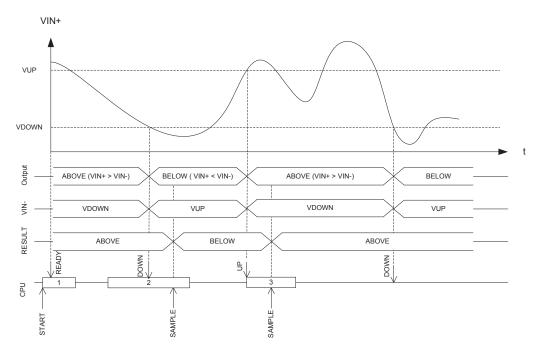


Figure 113: Hysteresis example where VIN+ starts above VUP

38.3 Registers

Table 88: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40013000	COMP	COMP	General purpose comparator		

Table 89: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select for single-ended mode
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable

38.3.1 SHORTS

Address offset: 0x200



Shortcut register

Bit	numbe	er		3	31 3	0 2	9 2	8 27	7 2	6 25	5 2	4 2	3 2	22 2	21 2	0 1	.9 1	.8	17 1	L6	15	14	13	12	11 :	LO S	9 ;	8 7	7 (6 5	, 4	4 3	2	1	. 0
Id																															E	Ξ C) C	В	ВА
Res	et 0x0	0000000		C	0 (0 (0 0	0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0) (0 0	(0	0	0	0
Id	RW	Field	Value Id	١	Valu	ie						D	es	crip	otio	n																			
Α	RW	READY_SAMPLE										SI	hoi	rtcı	ut b	etw	eeı	n R	EAC	Υ	eve	nt a	nd	SAI	MPL	.E ta	sk		Т						
												Se	ee	EV	ENT	S_F	REA	DΥ	and	<i>T</i> ,	4 <i>Sk</i>	'S_S	āΑ٨	1PL	E										
			Disabled	(0							D	isa	able	sho	orto	ut																		
			Enabled	1	1							Ei	nal	ble	sho	rtc	ut																		
В	RW	READY_STOP										SI	hoi	rtcı	ut b	etw	eeı	n R	EAC	Υ	eve	nt a	nd	STO	OP t	ask									
												Se	ee	EV	ENT	S_F	REA	DY	and	t T	4 <i>Sk</i>	'S_S	то	P											
			Disabled	C	0							D	isa	able	sho	orto	ut																		
			Enabled	1	1							E	nal	ble	sho	rtc	ut																		
С	RW	DOWN_STOP										SI	hoi	rtcı	ut b	etw	eeı	n D	OW	/N	eve	nt a	and	ST	OP t	ask									
												Se	ee	EV	ENT	S_E	001	VN	and	<i>T</i>	ASI	(S	STC	P											
			Disabled	(0							D	isa	able	sho	orto	ut																		
			Enabled	1	1							E	nal	ble	sho	rtc	ut																		
D	RW	UP_STOP										SI	hoi	rtcı	ut b	etw	eeı	n U	P e	ver	nt a	nd	STC)P t	ask										
												Se	ee	EV	ENT	s_L	JP a	nd	TA	SK.	s_s	ΤΟΙ)												
			Disabled	(0							D	isa	able	sho	orto	ut																		
			Enabled	1	1							Ei	nal	ble	sho	rtc	ut																		
Е	RW	CROSS_STOP										SI	hoi	rtcı	ut b	etw	eei	n C	ROS	SS 6	eve	nt a	nd	STC	OP t	ask									
												Se	ee	EV	ENT	s_c	CRO	SS	and	T	4 <i>SK</i>	s_s	то	Р											
			Disabled	C	0							D	isa	able	sho	orto	ut																		
			Enabled	1	1							Ei	nal	ble	sho	rtc	ut																		

38.3.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Enable or disable interrupt for READY event
					See EVENTS_READY
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	DOWN			Enable or disable interrupt for DOWN event
					See EVENTS_DOWN
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	UP			Enable or disable interrupt for UP event
					See EVENTS_UP
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	CROSS			Enable or disable interrupt for CROSS event
					See EVENTS_CROSS
			Disabled	0	Disable
			Enabled	1	Enable

38.3.3 INTENSET

Address offset: 0x304



Enable interrupt

Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

38.3.4 INTENCLR

Address offset: 0x308

Disable interrupt

																45.							_				_	
	number		31	30 2	29 2	28 27	26	25 .	24 2.	3 22	21.	20 19) 18	3 1/	16	15	14 :	13 1	21	1 10	9	8	/	6 5) 4		2	1 0
Id																										D		ВА
Res	et 0x00000000		0	0	0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0 0
Id	RW Field	Value Id	Va	lue					D	escri	ptio	n																
Α	RW READY								W	/rite	'1' t	o Dis	able	e int	err	upt f	or I	REA	DY 6	even	t							
									Se	ee <i>EV</i>	'EN	TS_RE	EAD	Υ														
		Clear	1						D	isabl	е																	
		Disabled	0						R	ead:	Disa	bled																
		Enabled	1						R	ead:	Ena	bled																
В	RW DOWN								W	/rite	'1' t	o Dis	able	e int	err	upt f	or I	OOV	VN (even	t							
									Se	ee <i>EV</i>	'EN	TS_D	ow	N														
		Clear	1						D	isabl	е																	
		Disabled	0						R	ead:	Disa	bled																
		Enabled	1						R	ead:	Ena	bled																
С	RW UP								W	/rite	'1' t	o Dis	able	e int	err	upt f	or I	JP 6	ver	it								
									Se	ee <i>EV</i>	EN1	TS_UI	P															
		Clear	1						D	isabl	е																	
		Disabled	0						R	ead:	Disa	bled																
		Enabled	1						R	ead:	Ena	bled																
D	RW CROSS								W	/rite	'1' t	o Dis	able	e int	err	upt f	or (CRO	SS e	ven	t							
									Se	ee <i>EV</i>	EN1	TS_CF	ROS	S														
		Clear	1						D	isabl	е																	
		Disabled	0						R	ead:	Disa	bled																
		Enabled	1						R	ead:	Ena	bled																



38.3.5 RESULT

Address offset: 0x400

Compare result

Bit	numbe	er		3	1 30	29	28	3 27	26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alue	9						De	escr	ipti	on																			
Α	R	RESULT										Re	esul	t of	last	со	mp	are.	De	cisi	on	poi	nt S	AN	PLE	E ta	sk.							
			Below	0								In	put	vol	tage	e is	bel	ow	the	thr	esh	old	(V	IN+	< V	IN-)							
			Above	1								In	put	vol	tage	e is	abo	ve	the	thr	esh	old	(V	N+	> V	IN-)							

38.3.6 ENABLE

Address offset: 0x500

COMP enable

Bit	numb	ber			3	1 30	29	9 28	3 2	7 2	6 2	5 2	24 2	23 2	22 2	21 2	20 :	19	18	17	16	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1 0	ı
Id																																				A A	ı
Re	et 0x	x00	000000		0	0	0	0	0) (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	N	Field	Value Id	V	alue	е							Des	crip	tio	n																				ı
Α	RW	N	ENABLE										E	Ena	ble	or	disa	ble	CC	DM	Р																
				Disabled	0								[Disa	ble																						
				Enabled	2								Е	Ena	ble																						

38.3.7 PSEL

Address offset: 0x504

Pin select

Bit number	31 30 29 28 27	27 26 25 24 2	3 22 21 20	19 18	8 17	16 1	L5 1	4 13	12 1	1 10	9	8	7	6	5 4	1 3	2	1 0 A A
Reset 0x00000000	0 0 0 0 0	0 0 0 0	0 0 0	0 0	0	0 (0 (0 0	0 (0	0	0	0	0	0 0	0	0	0 0
Id RW Field Value Id	Value	ı	escription															
A RW PSEL		,	nalog pin s	elect														
AnalogInpu	ut0 0	,	INO selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut1 1	,	IN1 selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut2 2	,	IN2 selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut3 3	,	IN3 selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut4 4	,	IN4 selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut5 5	,	IN5 selecte	ed as a	nalo	g inp	out											
AnalogInpu	ut6 6	,	IN6 selecte	ed as a	nalo	g inp	out											
VddDiv2	7	\	DD/2 selec	ted as	ana	log i	npu	t										

38.3.8 REFSEL

Address offset: 0x508

Reference source select for single-ended mode

Bit r	umbe	er		31 30	29	28	3 27	26	25	24 2	23 2	22 2	1 20) 19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																														A ,	А А
Res	et 0x0	000004		0 0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	1	0 0
Id	RW	Field	Value Id	Valu	9					ı	Desc	crip	tion																		
Α	RW	REFSEL								F	Refe	eren	ice s	elec	t																
			Int1V2	0						١	/RE	F = i	inte	rnal	1.2	V re	efer	enc	e (\	/DD	>=	1.7 \	/)								
			Int1V8	1						١	/RE	F = i	inte	rnal	1.8	V re	efer	enc	e (\	/DD	>=	VRE	+ ().2 \	/)						
			Int2V4	2						١	/RE	F = i	inte	rnal	2.4	V re	efer	enc	e (\	'DD	>=	VRE	+ ().2 \	/)						
			VDD	4						١	/RE	F = \	VDD	1																	
			ARef	5						١	/RE	F = /	AREI	F (V	DD:	>= \	REF	=>=	AR	EFIV	IIN)										



38.3.9 EXTREFSEL

Address offset: 0x50C External reference select

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EXTREFSEL		External analog reference select
	AnalogReference0	0 Use AINO as external analog reference
	AnalogReference1	1 Use AIN1 as external analog reference
	AnalogReference2	2 Use AIN2 as external analog reference
	AnalogReference3	3 Use AIN3 as external analog reference
	AnalogReference4	4 Use AIN4 as external analog reference
	AnalogReference5	5 Use AIN5 as external analog reference
	AnalogReference6	6 Use AIN6 as external analog reference
	AnalogReference7	7 Use AIN7 as external analog reference

38.3.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit r	umbe	er		31	. 30	29	28 2	27 26	5 2	5 24	23	22	21 2	20 1	9 1	8 1	7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																				В	В	ВЕ	В	В			Α	Α	Α	Α.	А А
Rese	t OxO	00000000		0	0	0	0	0 0	0	0	0	0	0	0 () (0) (0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																	
Id A	RW RW	Field THDOWN	Value Id		ilue 3:0]							scri _l OW	•		DO	WN	+1)	/64'	*VR	EF											

38.3.11 MODE

Address offset: 0x534 Mode configuration

Bit	numb	er		31	30	29 2	28 :	27 2	26 2	5 2	24 2	23 2	22	21 2	20	19	18	17	16	15	14 :	13 :	L2 1	.1 1	0 9	8	7	6	5	4	3 2	2 1	0 1
Id																										В						A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
Α	RW	SP									9	Spe	ed	and	рс	owe	r m	ode	es														
			Low	0							L	.ow	-pc	owe	r m	nod	е																
			Normal	1							1	Vor	ma	l mo	ode	е																	
			High	2							H	High	n-sp	pee	d m	nod	е																
В	RW	MAIN									1	Иai	n o	per	ati	on r	no	des															
			SE	0							9	Sing	gle-	end	ed	mo	de																
			Diff	1							[Diffe	ere	ntia	l m	nod	е																

38.3.12 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		А
Reset 0x00000000	0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field Value Id	Value	Description
A RW HYST		Comparator hysteresis
NoHyst	0	Comparator hysteresis disabled
Hyst50mV	1	Comparator hysteresis enabled



38.4 Electrical specification

38.4.1 COMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{COMP,LP}	Core run current in low power mode		2		μΑ
I _{COMP,N}	Core run current in normal mode		5		μΑ
I _{COMP,HS}	Core run current in high-speed mode		10		μΑ
t _{PROPDLY,LP}	Propagation delay, low-power mode ^a		0.6		μS
t _{PROPDLY,N}	Propagation delay, normal mode ^a		0.2		μS
t _{PROPDLY,HS}	Propagation delay, high-speed mode ^a		0.1		μS
V _{DIFFHYST}	Optional hysteresis applied to differential input		30		mV
V _{VDD-VREF}	Required difference between VDD and a selected VREF, VDD >	0.3			V
	VREF				
I _{INT_REF}	Current used by the internal bandgap reference when selected		13		μΑ
	as source for VREF				
I _{VDD_DIV2}	Current in internal resistor ladder when VDD/2 is selected as				μΑ
	analog input				
t _{INT_REF,START}	Startup time for the internal bandgap reference		50	80	μS
E _{INT_REF}	Internal bandgap reference error	-3		3	%
R _{LADDER}	Reference ladder resistance, I _{LADDER} = VREF / R _{LADDER}		550		kΩ
V _{INPUTOFFSET}	Input offset	-10		10	mV
D _{NLLADDER}	Differential non-linearity of reference ladder				LSB
t _{COMP,START}	Startup time for the comparator core		3		μS

Total comparator run current must be calculated from the I_{COMP} , I_{INT_REF} , and I_{LADDER} values for a given reference voltage.

^a Propagation delay is with 10 mV overdrive.



39 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK* — *Clock control* on page 87.

39.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

39.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

39.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 70 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 71.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.



39.4 Registers

Table 90: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog timer	

Table 91: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

39.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	L 30	29	28	8 27	7 2	26 2	5 2	24 2	23 2	22	21	20	19	18	1	7 1	6 1	.5	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Rese	t 0x0	0000000		0	0	0	0	0) (0 ()	0	0	0	0	0	0	0	C) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								es	cri	ptic	on																					
Α	RW	TIMEOUT										١	Vri	te '	1' t	о Е	na	ble	in	ter	rup	t f	or -	ПΝ	1EC	TU	ev	ent									
												9	iee	EV	ΈN	TS_	TII	ME	οι	IT																	
			Set	1								Е	na	ble																							
			Disabled	0								F	Rea	d: I	Disa	able	ed																				
			Enabled	1								F	Rea	d: l	Ena	ble	d																				

39.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	umbe	er		33	1 30	29	2	8 2	7 2	6 2	5 2	4 2	23 2	22	21	20	19	18	1	7 1	5 1	5 1	4 1	3 1	.2 1	1 1	.0 !	Э	8 7	7	6 !	5	4	3 2	2 :	1 0
Id																																				Α
Res	et 0x0	0000000		0	0	0	C	0) (0 () (0	0	0	0	0	0	0	0	0	())	0	0	0	0 (0	0 ()	0 (0	0	0 (0 (0 0
Id	RW	Field	Value Id	V	alue	•							Des	cri	ptic	on																				
Α	RW	TIMEOUT										١	۷ri	te '	'1' t	:о С)isa	ble	ir	ter	rup	ot f	or 1	IM	ΕOI	JT (eve	nt								
												9	See	ΕV	ΈN	TS_	TII	ИE	οu	Т																
			Clear	1								[Disa	ble	Э																					
			Disabled	0								F	Rea	d: I	Disa	able	ed																			
			Enabled	1								F	Rea	d: I	Ena	ble	d																			



39.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bit	numbe	er		3	1 3	0 2	9 2	8 2	7 2	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0x0	0000000		0	C	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	'alu	e							Des	cri	ptic	on																				
Α	R	RUNSTATUS											Ind	icat	tes	wh	eth	er c	or n	ot 1	he	wa	tch	dog	is r	unr	ning	3								_
			NotRunning	0									Wa	tch	dog	gno	ot ru	unn	ing																	
			Running	1									Wa	tch	dog	g is	run	nin	g																	

39.4.4 REQSTATUS

Address offset: 0x404

Request status

D.:										0.5																_		_				
	umbe	er		31	. 30	29	28	2/	26	25	24	23	22 2	21 2	0 19	9 18	3 1/	16	15 1	.4 1	3 12	11	10	9			6	5	4 3		. 1	0
Id																													E [
Rese		0000001		0	0	0	0	0	0	0	•	•	0	_		0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Va	llue								escrip																			
Α	R	RR0											ques					-	•													
			DisabledOrRequested	0								RR	R[0] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[0] r	egis	ter i	s en	able	ed,	and	are	not y	/et i	equ	est	ing	relo	oad					
В	R	RR1										Re	eques	st st	atus	for	RR[1] r	egist	er												
			DisabledOrRequested	0								RR	R[1] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			${\sf EnabledAndUnrequested}$	1								RR	R[1] r	egis	ter i	s en	able	ed,	and	are	not y	et ı	equ	est	ing	relo	oad					
С	R	RR2										Re	ques	st st	atus	for	RR[2] r	egist	er												
			DisabledOrRequested	0								RR	R[2] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[2] r	egis	ter i	s en	able	ed,	and	are	not y	et ı	equ	est	ing	relo	oad					
D	R	RR3										Re	eques	st st	atus	for	RR[3] r	egist	er												
			DisabledOrRequested	0								RR	R[3] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[3] r	egis	ter i	s en	able	ed,	and	are	not y	et ı	equ	est	ing	relo	oad					
Е	R	RR4										Re	ques	st st	atus	for	RR[4] r	egist	er												
			DisabledOrRequested	0								RR	R[4] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[4] r	egis	ter i	s en	able	ed,	and a	are	not y	/et i	equ	est	ing	relo	oad					
F	R	RR5										Re	eques	st st	atus	for	RR[5] r	egist	er												
			DisabledOrRequested	0								RR	R[5] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[5] r	egis	ter i	s en	able	ed,	and :	are	not y	et ı	equ	est	ing	relo	oad					
G	R	RR6										Re	ques	st st	atus	for	RR[6] r	egist	er												
			DisabledOrRequested	0								RR	R[6] r	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1								RR	R[6] r	egis	ter i	s en	able	ed,	and :	are	not y	/et i	equ	est	ing	relo	oad					
Н	R	RR7										Re	eques	st st	atus	for	RR[7] r	egist	er												
			DisabledOrRequested	0								RR	R[7] n	egis	ter i	s no	t er	abl	ed, d	or a	e alı	eac	ly re	que	esti	ng r	relo	ad				
			EnabledAndUnrequested	1									 R[7] r	-												_						
														0 -				,							0							

39.4.5 CRV

Address offset: 0x504 Counter reload value

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW CRV	[0x0000000F0xFFFFFFF Counter reload value in number of cycles of the 32.768 kHz

-1--1

clocl



39.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit r	numbe	er		31	30	29	28 2	7 26	5 25	5 24	4 23	3 22	2 21	20	19	18	17	16	15	14	13 :	12 1	11 1	.0 9	8	7	6	5	4	3 2	2 1	. 0
Id																										Н	G	F	ΕI) (В	A
Res	et 0x0	0000001		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	1
Id	RW	Field	Value Id	Va	lue						De	esci	ripti	on																		
Α	RW	RRO									En	nabl	le or	r dis	sabl	e R	R[0]	re	gist	er												
			Disabled	0							Di	isab	le R	R[C] re	gist	er															
			Enabled	1							En	nabl	le RI	R[0]] reg	giste	er															
В	RW	RR1									En	nabl	le or	r dis	sabl	e R	R[1]	re	gist	er												
			Disabled	0							Di	isab	le R	R[1	.] re	gist	er															
			Enabled	1							En	nabl	le RI	R[1]] reg	giste	er															
С	RW	RR2									En	nabl	le or	r dis	sabl	e R	R[2]	re	gist	er												
			Disabled	0							Di	isab	le R	R[2	l] re	gist	er															
			Enabled	1							En	nabl	le RI	R[2]] reg	giste	er															
D	RW	RR3									En	nabl	le or	r dis	sabl	e R	R[3]	re	gist	er												
			Disabled	0							Di	isab	le R	R[3] re	gist	er															
			Enabled	1							En	nabl	le RI	R[3]] reg	gist	er															
Е	RW	RR4									En	nabl	le or	r dis	sabl	e R	R[4]	re	gist	er												
			Disabled	0							Di	isab	le R	R[4] re	gist	er															
			Enabled	1							En	nabl	le RI	R[4]] reg	gist	er															
F	RW	RR5									En	nabl	le or	r dis	sabl	e R	R[5]	re	gist	er												
			Disabled	0							Di	isab	le R	R[5] re	gist	er															
			Enabled	1							Er	nabl	le RI	R[5]] reg	giste	er															
G	RW	RR6									En	nabl	le or	r dis	sabl	e R	R[6]	re	gist	er												
			Disabled	0							Di	isab	le R	R[6	i] re	gist	er															
			Enabled	1							En	nabl	le RI	R[6]] reg	giste	er															
Н	RW	RR7									En	nabl	le or	r dis	sabl	e R	R[7]	re	gist	er												
			Disabled	0							Di	isab	le R	R[7] re	gist	er															
			Enabled	1							Er	nabl	le RI	R[7]] reg	giste	er															

39.4.7 CONFIG

Address offset: 0x50C Configuration register

Bit number		31	30 29	9 28	27	26 2	25 24	1 23	22 :	21 2	0 19	9 18	3 17	16	15 3	L4 1:	3 12	11	10	9	8	7	6 5	5 4	3	2	1 0
Id																									С		Α
Reset 0x00000001		0	0 0	0	0	0	0 0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0 1
Id RW Field	Value Id	Val	ue					De	scrip	otion	1																
A RW SLEEP								Co	nfigu	ure t	he v	wat	chdo	og to	eit	her l	be p	aus	ed,	or k	ept	run	nin	g,			
								wh	ile t	he C	PU	is sl	eepi	ng													
	Pause	0						Pai	use v	wato	hdc	og w	hile	the	CPI	J is s	lee	oing									
	Run	1						Kee	ep tl	he w	atcl	hdo	g ru	nnir	ng w	hile	the	CPL	l is s	lee	ping						
C RW HALT								Co	nfigu	ure t	he v	wat	chdo	og to	eit	her l	be p	aus	ed,	or k	ept	run	nin	g,			
								wh	ile t	he C	PU	is h	alted	d by	the	deb	ugg	er									
	Pause	0						Pai	use v	wato	hdc	og w	hile	the	CPI	J is ł	nalte	ed b	y th	e de	ebug	ge	r				
	Run	1						Kee	ep tl	he w	atcl	hdo	g ru	nnir	ng w	hile	the	CPL	l is h	alte	ed b	y th	ne				
								del	bugg	ger																	

39.4.8 RR[0]

Address offset: 0x600 Reload request 0



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A	Α	Α	Α	Α	A	4 Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																	
Α	W	RR										Rel	oad	rec	lues	t re	giste	er														
			Reload	0x	6E5	246	35					Val	ue t	o re	eque	est a	rel	oad	of t	the	wat	chd	og ti	mer	,							

39.4.9 RR[1]

Address offset: 0x604 Reload request 1

Bit r	umbe	er		31	. 30	29	28	3 2	7 26	25	24	23	22	21	20	19	18 1	17 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	0
Id				Α	Α	Α	Α	Δ	A A	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	\ <i>A</i>	λ Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A /	АА
Res	et OxC	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue	2						De	scri	ptic	n																		
Α	W	RR										Re	load	l re	que	st r	egis	ter															
			Reload	0х	6E5	524	635	5				Va	lue	to r	equ	est	a re	eloa	d of	f th	e w	atch	dog	tin	ner								

39.4.10 RR[2]

Address offset: 0x608 Reload request 2

Bit r	nun	nbe	r		31	. 30	29	28	3 2	7 26	5 25	5 24	23	22	21	20 1	19 1	18 1	7 16	5 15	14	13	12	11 1	.0 !	9 8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α		A A	Α	Α	Α	Α	Α	A	A ,	А А	. A	Α	Α	Α	Α	Α	Δ,	\ <i>A</i>	A	Α	Α	Α	Α	Α	А А
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	W	٧	RR										Re	loac	l red	ques	st re	egist	er														
				Reload	0x	6E5	524	635	5				Va	lue 1	to r	equ	est	a rel	oad	d of	the	wat	cho	log 1	ime	r							

39.4.11 RR[3]

Address offset: 0x60C Reload request 3

				Reload	Λv	6F5	2/16	525					\/al	۵۱۱	to r	וחם	ıest	- 2 1	مام	he	of t	-ha	W/2	cho	امم	tim	ωr									
	A ۱	N	RR										Rel	oa	d re	que	est r	regi	iste	r																
1	ld F	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
1	Reset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 0	
	Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	A A	
	Bit nuı	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0	

39.4.12 RR[4]

Address offset: 0x610 Reload request 4

Bit r	nur	mbe	r		31	L 30	29	28	3 27	7 2	6 25	24	23	22	21	20 1	19 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id					Α	Α	Α	Α	A	. 4	A	Α	Α	Α	Α	Α.	A	Δ /	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A
Res	et	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	R	RW	Field	Value Id	Va	alue							De	scri	ptio	n																		
Α	٧	N	RR										Re	loac	l red	que	st re	egist	ter															
				Reload	0х	6E5	246	635	5				Va	lue :	to re	equ	est	a re	loa	d of	the	wa	tcho	gob	tim	er								

39.4.13 RR[5]

Address offset: 0x614 Reload request 5



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A A	Α	Α	Α	Α	A	4 Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A
Res	t OxC	00000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																	
Α	W	RR										Rel	oad	rec	lues	t re	giste	er														
			Reload	0x	6E5	246	35					Val	ue t	o re	eque	est a	rel	oad	of t	the	wat	chd	og ti	mer	,							

39.4.14 RR[6]

Address offset: 0x618 Reload request 6

Bit r	umbe	er		31	. 30	29	28	3 2	7 26	25	24	23	22	21	20	19	18 1	.7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Д	А	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	A A	Α Α	λ Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A
Res	et OxC	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue	:						De	scri	ptic	n																		
Α	W	RR										Re	load	l re	que	st r	egis	ter															
			Reload	0х	6E5	524	635	;				Va	lue	to r	equ	est	a re	eloa	d of	f th	e w	atch	dog	tin	ner								

39.4.15 RR[7]

Address offset: 0x61C Reload request 7

Bit r	nun	nbe	r		31	. 30	29	28	3 2	7 26	5 25	5 24	23	22	21	20 1	19 1	18 1	7 16	5 15	14	13	12	11 1	.0 !	9 8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α		A A	Α	Α	Α	Α	Α	A	A ,	А А	. A	Α	Α	Α	Α	Α	Δ,	\ <i>A</i>	A	Α	Α	Α	Α	Α	А А
Res	et (0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	W	٧	RR										Re	loac	l red	ques	st re	egist	er														
				Reload	0x	6E5	524	635	5				Va	lue 1	to r	equ	est	a rel	oad	d of	the	wat	cho	log 1	ime	r							

39.5 Electrical specification

39.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{WDT}	Run current for watchdog timer		0.3	2	μΑ
t _{WDT}	Time out interval	458 μs		36 h	



40 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

40.1 Registers

Table 92: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	SWI	SWI0	Software interrupt 0		
0x40015000	SWI	SWI1	Software interrupt 1		
0x40016000	SWI	SWI2	Software interrupt 2		
0x40017000	SWI	SWI3	Software interrupt 3		
0x40018000	SWI	SWI4	Software interrupt 4		
0x40019000	SWI	SWI5	Software interrupt 5		



41 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- · Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- · EasyDMA support for sample buffering
- · HW decimation filters

The PDM module illustrated in *Figure 114: PDM module* on page 395 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

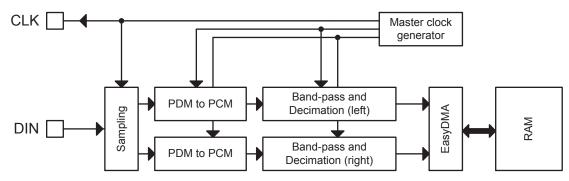


Figure 114: PDM module

41.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

41.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.



The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

41.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low), its output is 2×16 -bit PCM samples at a sample rate 64 times lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain ($G_{PDM,default}$) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to - $G_{PDM,default}$ dB to achieve the requirement.

With $G_{PDM,default}$ =3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

41.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

Table 93: DMA sample storage

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]; L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.



For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

41.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.



Figure 115: Example of a single PDM microphone, wired as left



Figure 116: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

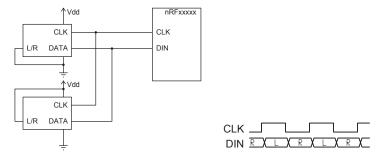


Figure 117: Example of two PDM microphones

41.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.



The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER* — *Power supply* on page 67 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 94: GPIO configuration before enabling peripheral* on page 398 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

Table 94: GPIO configuration before enabling peripheral

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

41.7 Registers

Table 95: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse-density modulation (digital	
			microphone interface)	

Table 96: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP
		task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

41.7.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	numbe	r		31	30 2	9 28	27	26 2	5 24	23 2	22 21	L 20	19	18 1	17 16	5 15	14	13 3	12 1	1 10	9	8	7	6 5	4	3	2	1 0
Id																											С	ВА
Res	et 0x0	0000000		0	0 (0 0	0	0 0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Val	lue					Des	cripti	ion																
Α	RW	STARTED								Ena	ble o	r dis	able	int	erru	pt fo	or S	ΓAR	ΓED	even	t							
										See	EVEN	VTS_	STA	RTE	D													
			Disabled	0						Disa	able																	
			Enabled	1						Ena	ble																	
В	RW	STOPPED								Ena	ble o	r dis	able	int	erru	pt fo	or S	ГОРІ	PED	even	t							
										See	EVEN	VTS_	STC	PPE	D													
			Disabled	0						Disa	able																	
			Enabled	1						Ena	ble																	
С	RW	END								Ena	ble o	r dis	able	int	erru	pt fo	or El	ND e	ven	t								
										See	EVEN	VTS_	ENL)														
			Disabled	0						Disa	able																	
			Enabled	1						Ena	ble																	

41.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	er		31	. 30	29	28	27 2	26 2	5 24	4 23 :	22 2	21 2	0 1	9 18	3 1	7 16	5 1	5 1	4 1	3 1	2 1:	10	9	8	7	6	5	4 3	3 2	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0 0	0	0 0	0	0	() () (0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tior	1																		
Α	RW	STARTED									Wri	ite ':	1' to	En	able	e in	terr	up	t fo	r S	TAR	TED	eve	nt								
											See	EVI	ENTS	s_s	TAR	TEI	D															
			Set	1							Ena	ble																				
			Disabled	0							Rea	ıd: E	Disab	oled	ł																	
			Enabled	1							Rea	nd: E	nab	led																		
В	RW	STOPPED									Wri	ite ':	1' to	En	able	e in	terr	up	t fo	r S	ГОР	PEC	eve	nt								
											See	EVI	ENTS	s_s	TOP	PE	D															
			Set	1							Ena	ble																				
			Disabled	0							Rea	ıd: E	Disab	oled	ł																	
			Enabled	1							Rea	ıd: E	nab	led																		
С	RW	END									Wri	ite '	1' to	En	able	e in	terr	up	t fo	r E	ND (evei	nt									
											See	EVI	ENTS	S_E	ND																	
			Set	1							Ena	ble																				
			Disabled	0							Rea	nd: [Disab	oled	ł																	
			Enabled	1							Rea	ıd: E	nab	led																		

41.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit nur	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	L 0
Id																																C	: E	3 A
Reset	0x0(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0 0
Id R	RW	Field	Value Id	Va	lue							De	escr	ipti	on																			
A R	RW	STARTED										W	rite	'1'	to [Disa	ble	in	err	upt	fo	ST	ART	ED	eve	nt								
												Se	e <i>E</i>	VΕN	ITS_	ST	4R	ΓED																
			Clear	1								Di	sab	le																				
			Disabled	0								Re	ad:	Dis	abl	ed																		
			Enabled	1								Re	ad:	Ena	able	ed																		
B R	RW	STOPPED										W	rite	'1'	to [Disa	ble	in	terr	upt	fo	ST	OPF	ED	eve	nt								



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Disable interrupt for END event
			See EVENTS_END
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

41.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bit	num	ber			3	1 30	29	9 28	3 27	7 26	6 25	5 24	1 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0	x00	000000		0	0	0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RV	W	Field	Value Id	٧	alue	9						D	esc	ript	ion																			
Α	RV	N	ENABLE										Е	nab	le o	r di	sab	le F	DIV	1 m	odı	ıle													
				Disabled	0								D	isab	le																				
				Enabled	1								Е	nab	le																				

41.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit n	umbe	er		31	30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Rese	t 0x0	8400000		0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				
A	RW	FREQ										PD	M_(CLK	fre	que	ency	У																	
			1000K	0x	080	000	000					PD	M_(CLK	= 3	2 N	1Hz	/ 3	2 =	1.0	000	M	Ηz												
			Default	0x	084	100	000					PD	M_(CLK	= 3	2 N	1Hz	/ 3	1 =	1.0	32	M	Ηz												
			1067K	0x	088	300	000					PD	M_(CLK	= 3	2 N	1Hz	/ 3	0 =	1.0	67	M	Ηz												

41.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit	numbe	er		31	. 30	29	28	27	26	25 :	24	23 :	22 :	21 2	20 2	19 1	18 1	17 1	16 1	15 1	14 1	3 1	12 1	11 1	.0	9	8	7	6	5	4	3	2	1	0
Id																																		В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																				
Α	RW	OPERATION										Mo	no (or s	tere	eo (pe	rati	on																_
			Stereo	0								San	nple	e an	d st	ore	on	e p	air	(Le	ft +	Rig	ht)	of :	16t	it s	am	ple	s pe	er					
												RAN	M w	ord	R=	[31	:16]; L:	=[1	5:0]															
			Mono	1								San	nple	e an	d st	ore	tw	o s	ucc	ess	ive	Lef	t sa	mp	les	(16	bit	ea	ich)	ре	r				
												RAN	M w	ord	L1	=[3	1:1	6]; I	-0=	[15	:0]														
В	RW	EDGE										Def	fine	s on	wł	nich	PD	M_	CLI	(ec	lge	Lef	t (o	r m	on	o) i	s sa	mp	led						
			LeftFalling	0								Left	t (oı	r mo	no) is	san	nple	ed c	on f	allir	ng e	edg	e of	PE	DM.	_CL	K							
			LeftRising	1								Left	t (oı	r mo	no) is	san	nple	ed c	on r	isin	g e	dge	of	PD	M_	CLK								



41.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

Bit n	umbe	er					31	. 30	29 2	28 2	7 2	6 25	24	23 2	2 21	20	19 1	.8 1	17 16	5 15	5 14	13	12 1	1 10	9	8	7 6	5 5	4	3	2	1 0
Id																											A	A A	Α	Α	Α .	А А
Rese	et OxC	0000	0028				0	0	0	0 (0 0	0	0	0 0	0	0	0 (0 (0 0	0	0	0	0 0	0 0	0	0	0 () 1	0	1	0	0 0
Id	RW	Fie	ld		Value Id		Va	lue						Desc	riptio	on																
Α	RW	GA	INL											Left	outpu	ut g	ain a	adju	ıstm	ent	i, in (0.5	IB st	eps, a	arou	ınd	the	defa	ult			
														mod	ule ga	ain	(see	ele	ctric	al p	para	met	ers)									
														0x00	-20 (dB g	ain a	adjı	ust													
														0x01	-19.5	5 dE	gai	n a	djust	t												
														()																		
														0x27	-0.5	dB :	gain	adj	just													
														0x28	0 dB	gai	n ad	lius	t													
																_																
														0x29	+0.5	αB	gaın	ı ad	ljust													
														()																		
														0x4F	+19.	5 dl	3 gai	in a	djus	t												
														0x50	+20	dB į	gain	adj	just													
					MinGain		0х	00						-20dl	B gaiı	n ac	ljust	me	nt (n	nin	imuı	m)										
					DefaultGai	n	0х	28						OdB 8	gain a	adju	ıstm	ent	('25	00	RMS	S' re	quire	emen	t)							
					MaxGain		0x	50						+20d	B gai	in a	djust	tme	ent (ı	max	ximu	um)										

41.7.8 **GAINR**

Address offset: 0x51C

Right output gain adjustment

Bit	umbe	r		33	1 30	29	28	3 27	7 26	6 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																												Α	Α	Α	Α	Α.	Α	А А
Res	et 0x0	0000028		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	escr	ipti	on																			
Α	RW	GAINR										Rig	ght	out	put	ga	in a	dju	stn	en	t, ir	0.5	dE	ste	ps,	arc	ounc	d th	ie					
												de	fau	lt m	nod	ule	gai	n (s	ee	ele	ctri	cal	oara	ame	eter	s)								
			MinGain	0>	x00							-20	OdE	gai	in a	dju	stm	en	t (m	ini	mui	m)												
			DefaultGain	0>	x28							0d	Вg	ain	adj	ust	mei	nt (250	00 F	RMS	s' re	qui	ren	nen	t)								
			MaxGain	0>	x50							+2	0dl	B ga	in a	dju	stn	nen	t (n	nax	imι	ım)												

41.7.9 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit n	umbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	A A A A
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

41.7.10 PSEL.DIN

Address offset: 0x544



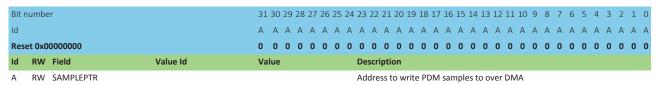
Pin number configuration for PDM DIN signal

Bit	numbe	er		31 30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	7 16	15	14 :	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				В																								A A	A A	Α	Α
Res	et OxF	FFFFFF		1 1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	۱ 1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	۱ 1	1	1
Id	RW	Field	Value Id	Value	2						Des	crip	tio	n																	
Α	RW	PIN		[031	.]						Pin	nun	nbe	r																	
В	RW	CONNECT									Con	nec	tior	ı																	
			Disconnected	1							Disc	onr	nect																		
			Connected	0							Con	nec	t																		

41.7.11 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA



41.7.12 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW BUFFSIZE		[032767] Length of DMA RAM allocation in number of samples

41.8 Electrical specification

41.8.1 PDM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PDM,stereo}	PDM module active current, stereo operation ³⁴				μΑ
f _{PDM,CLK}	PDM clock speed				MHz
t _{PDM,JITTER}	Jitter in PDM clock output				ns
T _{dPDM,CLK}	PDM clock duty cycle				%
t _{PDM,DATA}	Decimation filter delay				ms
t _{PDM,cv}	Allowed clock edge to data valid				ns
t _{PDM,ci}	Allowed (other) clock edge to data invalid				ns
t _{PDM,s}	Data setup time at f _{PDM,CLK} =1.024 MHz				ns
t _{PDM,h}	Data hold time at f _{PDM,CLK} =1.024 MHz				ns
G _{PDM,default}	Default (reset) absolute gain of the PDM module				dB

Average current including PDM and DMA transfers, excluding clock and power supply base currents



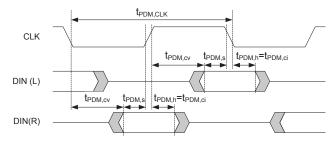


Figure 118: PDM timing diagram



42 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- · Enables SW triggering of interrupts
- · Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Refer to Table 97: Instances on page 404 for a list of the various EGU instances

42.1 Registers

Table 97: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	EGU	EGU0	Event generator unit 0		
0x40015000	EGU	EGU1	Event generator unit 1		

Table 98: Register Overview

Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task
EVENTS_TRIGGERED[5]	0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED[6]	0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERED[7]	0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED[8]	0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED[9]	0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED[10]	0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task



Register	Offset	Description
EVENTS_TRIGGERED[2	1] 0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED[2	.2] 0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED[2	3] 0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED[2	.4] 0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED[2	.5] 0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

42.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

		or disable int	19-7		
	numbe	er		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld		Field	Value Id	Value	Description
Α	RW	TRIGGERED0			Enable or disable interrupt for TRIGGERED[0] event
					See EVENTS_TRIGGERED[0]
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	TRIGGERED1			Enable or disable interrupt for TRIGGERED[1] event
					See EVENTS_TRIGGERED[1]
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	TRIGGERED2			Enable or disable interrupt for TRIGGERED[2] event
					See EVENTS_TRIGGERED[2]
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	TRIGGERED3			Enable or disable interrupt for TRIGGERED[3] event
					See EVENTS TRIGGERED[3]
			Disabled	0	Disable
			Enabled	1	Enable
Е	RW	TRIGGERED4			Enable or disable interrupt for TRIGGERED[4] event
					See EVENTS_TRIGGERED[4]
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	TRIGGERED5			Enable or disable interrupt for TRIGGERED[5] event
					See EVENTS_TRIGGERED[5]
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	TRIGGERED6			Enable or disable interrupt for TRIGGERED[6] event
					See EVENTS_TRIGGERED[6]
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	TRIGGERED7			Enable or disable interrupt for TRIGGERED[7] event
					Son EVENTS TRICCEREDITI
			Disabled	0	See EVENTS_TRIGGERED[7] Disable
			Enabled	1	Enable
I	RW	TRIGGERED8			Enable or disable interrupt for TRIGGERED[8] event
			Disabled	0	See EVENTS_TRIGGERED[8] Disable
			Enabled	1	Enable
J	RW/	TRIGGERED9	LIIUDICU	•	Enable or disable interrupt for TRIGGERED[9] event
•					



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_TRIGGERED[9]
		Disabled	0	Disable
		Enabled	1	Enable
K	RW TRIGGERED10			Enable or disable interrupt for TRIGGERED[10] event
				See EVENTS TRIGGERED[10]
		Disabled	0	Disable
		Enabled	1	Enable
L	RW TRIGGERED11			Enable or disable interrupt for TRIGGERED[11] event
				See EVENTS_TRIGGERED[11]
		Disabled	0	Disable
		Enabled	1	Enable
М	RW TRIGGERED12	Enablea	-	Enable or disable interrupt for TRIGGERED[12] event
				See EVENTS_TRIGGERED[12]
		Disabled	0	Disable
	DW TRICCEDEDAS	Enabled	1	Enable Tolographic
N	RW TRIGGERED13			Enable or disable interrupt for TRIGGERED[13] event
				See EVENTS_TRIGGERED[13]
		Disabled	0	Disable
		Enabled	1	Enable
0	RW TRIGGERED14			Enable or disable interrupt for TRIGGERED[14] event
				See EVENTS_TRIGGERED[14]
		Disabled	0	Disable
		Enabled	1	Enable
Р	RW TRIGGERED15			Enable or disable interrupt for TRIGGERED[15] event
				See EVENTS_TRIGGERED[15]
		Disabled	0	Disable
		Enabled	1	Enable

42.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	L 30	29	28	27	26 2	5 2	4 23	22 2	1 20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																		Р	0	N N	ΛL	. K	J	1	Н	G	F	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue						Des	scrip	tion																		
Α	RW	TRIGGERED0									Wri	ite '1	' to I	Ena	ble	inte	erru	pt f	or T	RIG	GEF	ED[0] e	vent	t						
											See	e EVE	NTS	_TR	IGG	SERI	D[C	0]													
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: D	isabl	led																	
			Enabled	1							Rea	ad: E	nable	ed																	
В	RW	TRIGGERED1									Wri	ite '1	' to I	Ena	ble	inte	erru	pt f	or T	RIG	GEF	ED[1] e	vent	t						
											See	e <i>EVE</i>	NTS	_TR	IGG	SERI	D[1	1]													
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: D	isabl	led																	
			Enabled	1							Rea	ad: E	nable	ed																	
С	RW	TRIGGERED2									Wri	ite '1	' to I	Ena	ble	inte	erru	pt f	or T	RIG	GEF	ED[2] e	ven	t						
											See	e EVE	NTS	_TR	IGG	SERI	D[2	2]													
			Set	1							Ena	able																			
			Disabled	0							Rea	ad: D	isabl	led																	
			Enabled	1							Rea	ad: E	nable	ed																	



Bit r	number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				PONMLKJIHGFEDCBA
	set 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description Write 14 to English intervent for TRICCERED[3] quant
D	RW TRIGGERED3			Write '1' to Enable interrupt for TRIGGERED[3] event
				See EVENTS_TRIGGERED[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
E	RW TRIGGERED4	Enabled	1	Read: Enabled Write '1' to Enable interrupt for TRIGGERED[4] event
-	NW INIGGERED4			
				See EVENTS_TRIGGERED[4]
		Set	1	Enable
		Disabled Enabled	0 1	Read: Disabled Read: Enabled
F	RW TRIGGERED5	Ellabled	1	Write '1' to Enable interrupt for TRIGGERED[5] event
	NW INIGGENEDS			
				See EVENTS_TRIGGERED[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
G	RW TRIGGERED6	Enabled	1	Read: Enabled Write '1' to Enable interrupt for TRIGGERED[6] event
d	NV INIGGEREDO			
				See EVENTS_TRIGGERED[6]
		Set	1	Enable
		Disabled	0	Read: Disabled
Н	RW TRIGGERED7	Enabled	1	Read: Enabled Write '1' to Enable interrupt for TRIGGERED[7] event
"	NW INIGOLILED?			
				See EVENTS_TRIGGERED[7]
		Set	1	Enable
		Disabled Enabled	0	Read: Disabled Read: Enabled
	RW TRIGGERED8	Eliableu	1	Write '1' to Enable interrupt for TRIGGERED[8] event
	NW INIGGENEDO			
				See EVENTS_TRIGGERED[8]
		Set Disabled	1 0	Enable Read: Disabled
		Enabled	1	Read: Enabled
J	RW TRIGGERED9	Enablea	1	Write '1' to Enable interrupt for TRIGGERED[9] event
		C-+	4	See EVENTS_TRIGGERED[9]
		Set Disabled	1	Enable Read: Disabled
		Enabled	1	Read: Enabled
K	RW TRIGGERED10	Enabled	-	Write '1' to Enable interrupt for TRIGGERED[10] event
		Set	1	See EVENTS_TRIGGERED[10] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TRIGGERED11			Write '1' to Enable interrupt for TRIGGERED[11] event
		Set	1	See EVENTS_TRIGGERED[11] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
М	RW TRIGGERED12			Write '1' to Enable interrupt for TRIGGERED[12] event
		Set	1	See EVENTS_TRIGGERED[12] Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
N	RW TRIGGERED13			Write '1' to Enable interrupt for TRIGGERED[13] event
				, , , , , , , , , , , , , , , , , , , ,



Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
Re	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
					See EVENTS_TRIGGERED[13]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
0	RW	TRIGGERED14			Write '1' to Enable interrupt for TRIGGERED[14] event
					See EVENTS_TRIGGERED[14]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Р	RW	TRIGGERED15			Write '1' to Enable interrupt for TRIGGERED[15] event
					See EVENTS_TRIGGERED[15]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

42.1.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit number			21	30.2	9 20	2 27	26.5	25.27	1 2:	2 1	22 21	20	10 1	2 1	7 1	6 10	11	12	12	11 10) 0	Q	7	6	5	1	3 2	1	0
Id			21	30 2	.9 20	5 27	20 2	23 22	+ 23	3	22 21	20	15 1	.0]	./ 1					L K									
Reset 0x000	00000		0	0 (0	0	0 0			0 0	^	0	_															
Id RW F		Value Id		lue	0 0	U	U	0 0			criptic		U	0		, 0	U	U	U	0 0	U	U	U	U	U	U	0 0	U	U
	RIGGEREDO	value lu	Va	iue							ite '1' t)icah	lo i	ntor	run	for	TDI	IGGI	EDED	[0]	01/01	·+						
A IVV	MOGENEDO								v	VIII	ite I t	.0 0	/isau	ic i	iiiei	rup	. 101	1111	1001	LINED	[O]	evei	10						
									Se	ee	EVEN	TS_	TRIC	GE	RED	[0]													
		Clear	1						D	isa	able																		
		Disabled	0						Re	ea	d: Disa	able	ed																
		Enabled	1						Re	ea	id: Ena	ble	d																
B RW T	RIGGERED1								W	Vrit	ite '1' t	to D	isab	le i	nter	rup	for	rTRI	IGGI	ERED	[1]	ever	nt						
									Se	ee	EVEN	TS_	TRIC	GE	RED	[1]													
		Clear	1						D	isa	able																		
		Disabled	0						Re	ea	d: Disa	able	ed																
		Enabled	1						Re	ea	d: Ena	ble	d																
C RW T	RIGGERED2								W	Vrit	ite '1' t	o D	isab	le i	nter	rup	for	r TRI	IGGI	ERED	[2]	ever	nt						
									Se	ee ee	EVEN	TS	TRIC	GE	RFF	121													
		Clear	1								able		,,,,,			L—J													
		Disabled	0								nd: Disa	able	ed																
		Enabled	1						Re	ea	id: Ena	ble	d																
D RW T	RIGGERED3								W	Vrit	ite '1' t	to D	isab	le i	nter	rup	for	r TRI	IGGI	ERED	[3]	ever	nt						
									Se	PР	EVEN	TS	TRIC	GGF	RFF	131													
		Clear	1								able	,	,,,,,,	,02		رحا													
		Disabled	0								nd: Disa	able	-d																
		Enabled	1						Re	ea	id: Ena	ble	d																
E RW T	RIGGERED4								W	Vrit	ite '1' t	to D	isab	le i	nter	rup	for	r TRI	IGGI	ERED	[4]	ever	nt						
		CI.									EVEN	15_	IRIC	GE	KEL	[4]													
		Clear	1								able																		
		Disabled	0								id: Disa																		
E D)4/ T	TNICCEDEDE	Enabled	1								id: Ena			1				. TD	100		[-]								
F RW T	RIGGERED5								VV	vrit	ite '1' t	נס ט	ısab	ıe I	nter	rup	101	TKI	IGGI	EKED	[5]	ever	ΙŢ						
									Se	ee	EVEN	TS_	TRIC	GE	RED	[5]													
		Clear	1						D	isa	able																		



	umbe	er		31 30) 29	9 28	27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id										PONMLKJIHGFEDCBA
Rese		0000000				0	0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	3					Description
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
G	RW	TRIGGERED6								Write '1' to Disable interrupt for TRIGGERED[6] event
										See EVENTS_TRIGGERED[6]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW	TRIGGERED7								Write '1' to Disable interrupt for TRIGGERED[7] event
										See EVENTS_TRIGGERED[7]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
1	R\M	TRIGGERED8	Litabica	1						Write '1' to Disable interrupt for TRIGGERED[8] event
'	11.44	TRIGGEREDS								write 1 to bisable interrupt for introduction of event
										See EVENTS_TRIGGERED[8]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
J	RW	TRIGGERED9								Write '1' to Disable interrupt for TRIGGERED[9] event
										See EVENTS_TRIGGERED[9]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
K	RW	TRIGGERED10								Write '1' to Disable interrupt for TRIGGERED[10] event
										See EVENTS TRICCEPED[40]
			Clear	1						See EVENTS_TRIGGERED[10] Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
L	R\M	TRIGGERED11	Lilabled							Write '1' to Disable interrupt for TRIGGERED[11] event
-	11.44	INIOGENEDII								White I to bisable interrupt for introduced[11] event
										See EVENTS_TRIGGERED[11]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
M	RW	TRIGGERED12								Write '1' to Disable interrupt for TRIGGERED[12] event
										See EVENTS_TRIGGERED[12]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
N	RW	TRIGGERED13								Write '1' to Disable interrupt for TRIGGERED[13] event
										See EVENTS_TRIGGERED[13]
			Clear	1						Disable
			Disabled	0						Read: Disabled
0	B/V/	TRIGGERED14	Enabled	1						Read: Enabled Write '1' to Disable interrupt for TRIGGERED[14] event
J	IVVV	INIOULNED14								write 1 to pisable lifterrupt for Eniggeneral 141 exelle
										See EVENTS_TRIGGERED[14]
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
P	RW	TRIGGERED15								Write '1' to Disable interrupt for TRIGGERED[15] event
										See EVENTS_TRIGGERED[15]
			Clear	1						Disable
			Disabled	0						Read: Disabled



Bit number	31 30 29	9 28 27 26 25 24 23 22 2	1 20 19 18 17 16 15 :	14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id			Р	ONMLKJ	I H G F E D C B A
Reset 0x00000000	0 0 0	00000000	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	d Value	Descrip	tion		
Enable	d 1	Read: E	nabled		

42.2 Electrical specification

42.2.1 EGU Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{EGU,EVT}	Latency between setting an EGU event flag and the system		1		cycles
	setting an interrupt				



43 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- · Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- · Multiple duty-cycle arrays (sequences) defined in Data RAM
- · Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- · Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

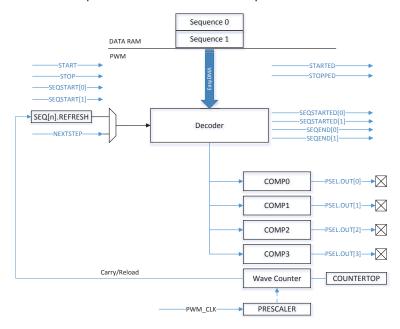


Figure 119: PWM Module

43.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 122: Decoder memory access modes* on page 414), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,



and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 414 below).

Figure 120: PWM up counter example - FallingEdge polarity on page 412 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16 t pwm seq[4] = {PWM CH0 DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY);
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE
                     = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
NRF PWM0->MODE
                     = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                 PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
NRF PWM0->LOOP
                = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF PWM0->DECODER
                  = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                     (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16 t)) <<
                                                 PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

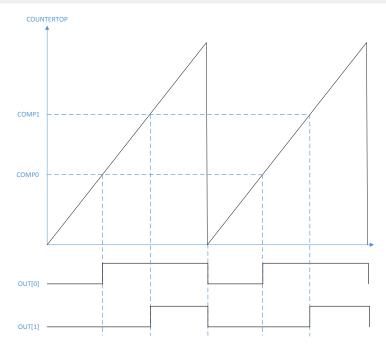


Figure 120: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

```
PWM period: TPWM(Up) = TPWM_CLK * COUNTERTOP
```

Step width/Resolution: $T_{steps} = T_{PWM_CLK}$



Figure 121: PWM up-and-down counter example on page 413 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16 t pwm seq[4] = {PWM CHO DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY };
NRF PWMO->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                      = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                      = (PWM MODE UPDOWN UpAndDown << PWM_MODE_UPDOWN_Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                 PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
                     = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF
   PWM0->LOOP
NRF PWM0->DECODER
                    = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos) |
                      (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t) (pwm seq) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16 t)) <<
                                                 PWM SEQ CNT CNT Pos);
NRF_PWM0 -> SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

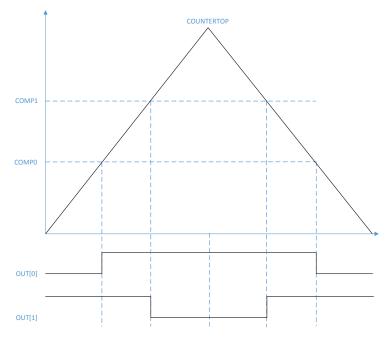


Figure 121: PWM up-and-down counter example

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

```
T_{PWM} (Up And Down) = T_{PWM} CLK * 2 * COUNTERTOP
```

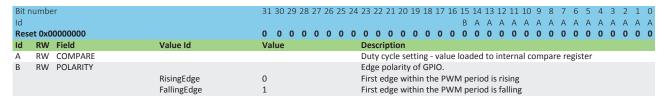
Step width/Resolution: $T_{steps} = T_{PWM} CLK * 2$



43.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.



The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 122: Decoder memory access modes* on page 414 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)th PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

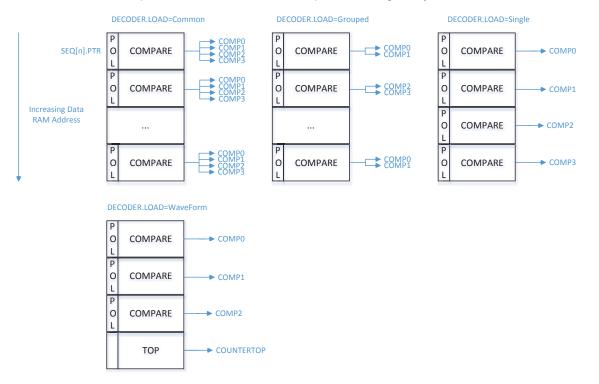


Figure 122: Decoder memory access modes



SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 123: Simple sequence example* on page 416 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 99: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
	PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired) $$
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)
	PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored.	Before starting PWM generation through a SEQSTART[n] task
	In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Important: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).



Figure 123: Simple sequence example on page 416 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos) |
                           (PWM PSEL OUT CONNECT Connected <<
                                                       PWM PSEL OUT CONNECT Pos);
NRF_PWM0->ENABLE
                        = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                        = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                       PWM PRESCALER PRESCALER Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF PWM0->DECODER
                      = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos)
                        (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(uint16 t))) < < (sizeof(seq0 ram) / sizeof(uint16 t))
                                                       PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0->SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

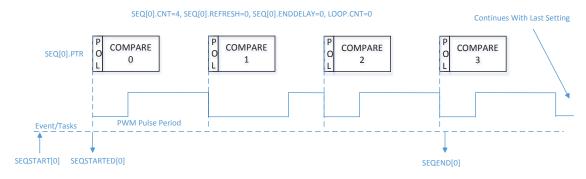


Figure 123: Simple sequence example

A more complex example is shown in *Figure 124: Example using two sequences* on page 417, where LOOP.CNT>0. In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).



```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_
                      = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
   PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                 PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
                    = (1 \ll PWM LOOP CNT Pos);
NRF PWM0->LOOP
NRF PWM0->DECODER = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos) |
                     (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(uint16 t)) <<
                                                 PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 1;
NRF PWM0->SEQ[0].ENDDELAY = 1;
NRF PWM0->SEQ[1].PTR = ((uint32 t)(seq1 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[1].CNT = ((sizeof(seq1_ram) / sizeof(uint16_t)) < < 
                                                 PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[1].REFRESH = 0;
NRF PWM0->SEQ[1].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

SEQ[0].CNT=2, SEQ[1].CNT=3, SEQ[0].REFRESH=1, SEQ[1].REFRESH=0, SEQ[0].ENDDELAY=1, SEQ[1].ENDDELAY=0, LOOP.CNT=1

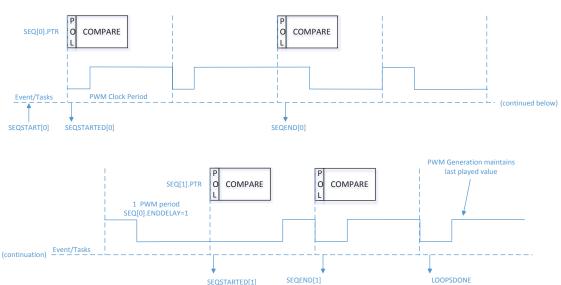


Figure 124: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- Influence of registers on the sequence
- Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.



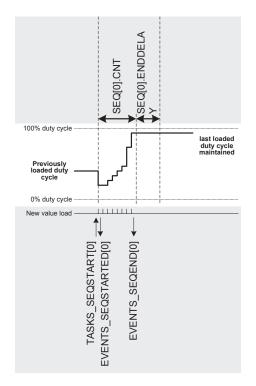


Figure 125: Single shot (LOOP.CNT=0)

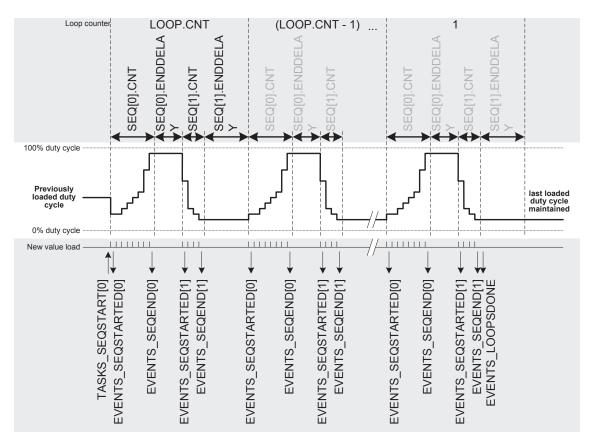


Figure 126: Complex sequence (LOOP.CNT>0) starting with SEQ[0]



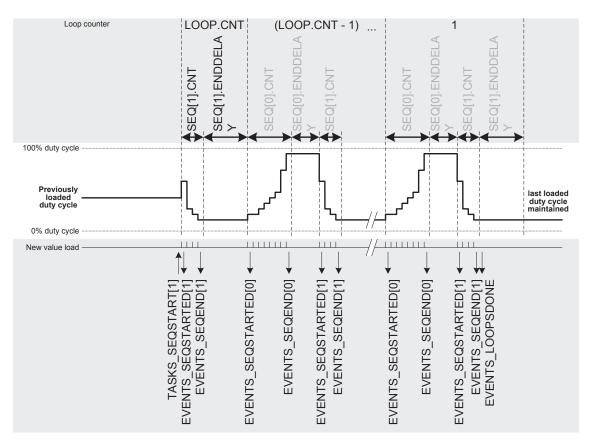


Figure 127: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

43.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

43.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 100: Recommended GPIO configuration before starting PWM generation* on page 420 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.



Table 100: Recommended GPIO configuration before starting PWM generation

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n]	Output	0	Idle state defined in GPIO->OUT
	(n=0, 3)			

43.5 Registers

Table 101: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001C000	PWM	PWM0	Pulse-width modulation unit 0		

Table 102: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence
		playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that
		sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that
		sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep.
		Does not cause PWM generation to start it was not running.
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0	0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1] 0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODE	N 0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of this sequence
SEQ[0].CNT	0x524	Amount of values (duty cycles) in this sequence
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded into compare register
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of this sequence
SEQ[1].CNT	0x544	Amount of values (duty cycles) in this sequence
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded into compare register
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3

43.5.1 SHORTS

Address offset: 0x200



Shortcut register

Bit	numbe	er		3	31 3	0 2	9 28	3 27	7 26	6 25	5 2	4 2	3 2	22 2	21 2	0 1	9 1	8 :	17 1	L6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																E	D	С	В	Α
Res	et 0x0	0000000		0) (0	0	0	0	0	C	0)	0	0	0 (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	/alu	e						D	es	crip	otio	า																				
Α	RW	SEQENDO_STOP										SI	hoi	rtcı	ut b	etw	eer	ı SI	EQE	NΓ	0][0]	ev	en	t an	d S	то	P ta	ısk								Τ
												Se	ee	EV	ENT	s_s	EQI	ΕN	D[0]] aı	nd	TAS	KS	_ST	ОР											
			Disabled	0)							D	isa	able	sho	orto	ut																			
			Enabled	1	L							Ei	nal	ble	sho	rtcı	ut																			
В	RW	SEQEND1_STOP										SI	hoi	rtcı	ut b	etw	eer	ı SI	EQE	NE	0[1]	ev	en	t an	d S	ТО	P ta	sk								
												Se	ee	EV	ENT	s_s	EQI	ΕN	D[1]] aı	nd	TAS	KS	_ST	ОР											
			Disabled	0)							D	isa	able	sho	orto	ut																			
			Enabled	1	L							Ei	nal	ble	sho	rtcı	ut																			
С	RW	LOOPSDONE_SEQSTARTO										SI	hoi	rtcı	ut b	etw	eer	ı L(OOF	PSE	100	IE €	eve	nt a	and	SE	QST	AR	Γ[0]	tas	k					
												Se	ee	EV	ENT	S_L	00	PSI	DOI	٧E	and	d TA	4 <i>SK</i>	(S_S	EQ	STA	ART,	[0]								
			Disabled	0)							D	isa	able	sho	orto	ut																			
			Enabled	1	L							Ei	nal	ble	sho	rtcı	ut																			
D	RW	LOOPSDONE_SEQSTART1										SI	hoı	rtcı	ut b	etw	eer	ı L(OOF	PSE	100	IE 6	eve	nt a	and	SE	QST	AR	Γ[1]	tas	k					
												Se	ee	EV	ENT	S_L	00	PSI	DOI	٧E	and	t TA	4SK	s_s	EQ	STA	\RT	[1]								
			Disabled	0)							D	isa	able	sho	orto	ut																			
			Enabled	1	L							Ei	nal	ble	sho	rtcı	ut																			
Ε	RW	LOOPSDONE_STOP										SI	hoi	rtcı	ut b	etw	eer	ı L0	OOF	PSE	100	IE e	eve	nt a	and	ST	OP 1	task	:							
												Se	ee	EV	ENT	S_L	00	PSI	DOI	٧E	and	d TA	4 <i>SK</i>	(S_S	то	Р										
			Disabled	0)							D	isa	able	sho	orto	ut																			
			Enabled	1	L							Eı	nal	ble	sho	rtcı	ut																			

43.5.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit	numbe	er		31 30	29	28 2	7 26	25	24 2	23	22 2	1 2	0 19	18	17	16	15 1	4 13	12	11 :	10 9	8	7	6	5	4	3 2	1	0
Id																							Н	G	F	Ε () C	В	
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0	0 0	0 0	0	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value	9					Des	script	tior	1																
В	RW	STOPPED							E	Ena	able o	or d	lisab	le ii	nterr	upt	for	STO	PPEC	ev ev	ent								
									S	See	e EVE	NTS	S_ST	ОР	PED														
			Disabled	0						Disa	able																		
			Enabled	1					E	Ena	able																		
С	RW	SEQSTARTED0							E	Ena	able o	or d	lisab	le ii	nterr	upt	for	SEQ:	STAF	RTE	0[0]	evei	nt						
									S	See	e EVE	NTS	S_SE	QS	TART	ED	[0]												
			Disabled	0					[Disa	able																		
			Enabled	1					E	Ena	able																		
D	RW	SEQSTARTED1							E	Ena	able o	or d	lisab	le ii	nterr	upt	for	SEQ:	STAF	RTE	0[1]	evei	nt						
									S	See	e EVE	NTS	S_SE	QS	TART	ED	1]												
			Disabled	0						Disa	able																		
			Enabled	1					E	Ena	able																		
Ε	RW	SEQEND0							E	Ena	able o	or d	lisab	le ii	nterr	upt	for	SEQ	END	[0] 6	even	t							
									S	See	e EVE	NTS	S_SE	QE	ND[0]													
			Disabled	0					[Disa	able																		
			Enabled	1					E	Ena	able																		
F	RW	SEQEND1							E	Ena	able o	or d	lisab	le ii	nterr	upt	for	SEQ	END	[1] 6	even	t							
									S	See	e EVE	NTS	S_SE	QE	ND[1]													
			Disabled	0					[Disa	able																		
			Enabled	1					E	Ena	able																		



Bit r	numbe	er		31	1 30 2	29	28 2	27	26 2	5 2	4 23	3 22	21 2	0 1	19 1	8 1	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																									Н	G	F	E C	С	В	
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0 (0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue						D	escri	iptio	n																	
G	RW	PWMPERIODEND									Er	nable	e or c	lisa	ble	inte	erru	ot fo	or P\	ΝM	PERI	ODE	ND	eve	nt						
											Se	ee <i>E</i> V	/ENT	S_F	PWN	ΛРΕ	RIO	DEN	ID												
			Disabled	0							Di	sabl	e																		
			Enabled	1							Er	nable	е																		
Н	RW	LOOPSDONE									Er	nable	e or c	disa	ble	inte	erru	ot fo	or LO	OOP	SDO	NE e	ven	t							
											Se	ee <i>E</i> V	/ENT	S_L	.001	PSD	ONI	Ε													
			Disabled	0							Di	sabl	е																		
			Enabled	1							Er	nable	9																		

43.5.3 INTENSET

Address offset: 0x304

Enable interrupt

⊢n	able	e interrupt			
Bit	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					HGFEDCB
Res	et 0x(0000000		0 0 0 0 0 0 0	000000000000000000000000000000000000000
Id	RW	Field	Value Id	Value	Description
В	RW	STOPPED			Write '1' to Enable interrupt for STOPPED event
					See EVENTS_STOPPED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	SEQSTARTED0			Write '1' to Enable interrupt for SEQSTARTED[0] event
					See EVENTS_SEQSTARTED[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	SEQSTARTED1			Write '1' to Enable interrupt for SEQSTARTED[1] event
					See EVENTS_SEQSTARTED[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	SEQEND0			Write '1' to Enable interrupt for SEQEND[0] event
					See EVENTS_SEQEND[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	SEQEND1			Write '1' to Enable interrupt for SEQEND[1] event
					See EVENTS_SEQEND[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	PWMPERIODEND			Write '1' to Enable interrupt for PWMPERIODEND event
					See EVENTS_PWMPERIODEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	LOOPSDONE			Write '1' to Enable interrupt for LOOPSDONE event
					See EVENTS_LOOPSDONE
			Set	1	Enable
			Disabled	0	Read: Disabled
			Disabled	U	nead. Disabled



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					HGFEDCB
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	00000000	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Read: Enabled		

43.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d				HGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value	Description
В	RW STOPPED			Write '1' to Disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
0	RW SEQSTARTEDO			Write '1' to Disable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW SEQSTARTED1			Write '1' to Disable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Ξ	RW SEQENDO			Write '1' to Disable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SEQEND1			Write '1' to Disable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW PWMPERIODEND			Write '1' to Disable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW LOOPSDONE			Write '1' to Disable interrupt for LOOPSDONE event
				See EVENTS_LOOPSDONE
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

43.5.5 ENABLE

Address offset: 0x500

PWM module enable register



Bit r	numbe	r		31 3	80 29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	3 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						Des	scrip	otio	n																	
Α	RW	ENABLE									Ena	ble	or (disal	ble	lWP	M m	nodi	ule												
			Disabled	0							Dis	able	ed																		
			Enabled	1							Ena	ble																			

43.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit r	umbe	r		31 3	30 29	28	27	26	25	24	23 2	22 2	21 2	20 1	9 18	3 17	16	15	14	13 1	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						Des	crip	otio	n																	
Α	RW	UPDOWN									Sele	ects	up	or u	ір аі	nd d	ıwo	ı as	wa	ve c	our	iter	mo	de							
			Up	0							Up	cou	nte	r - e	dge	alig	ned	PW	/M (duty	у-су	cle									
			UpAndDown	1							Up a	and	do	wn (nuo	nter	- ce	nte	r ali	gne	d P	WM	dut	у су	/cle						

43.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

Bit	numbe	er		31 30	29	28	27	26 2	25 2	24 2	23 2	2 2	1 20	19	18	17 :	L6 1	5 14	13	12	11 1) 9	8	7	6	5	4	3	2	1 0
Id																		Α	Α	Α	A A	A	. A	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	00003FF		0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0 0	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Value	2						Desc	cript	ion																	
Α	RW	COUNTERTOP		[332	767	7]				١	/alu	ie up	to	whi	ch tl	ne p	ulse	ger	erat	or o	oun	ter	cou	nts.	Thi	s				
										r	egis	ster	is ig	nore	ed w	hei	n DE	COD	ER.N	JOL	E=V	/av	eFo	rm a	and	onl	ly			
										\	/alu	es fr	om	RAN	Λwi	ll b	e use	ed.												

43.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААА
Reset 0x00000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
A RW PRESCALER			Pre-scaler of PWM_CLK
	DIV_1	0	Divide by 1 (16MHz)
	DIV_2	1	Divide by 2 (8MHz)
	DIV_4	2	Divide by 4 (4MHz)
	DIV_8	3	Divide by 8 (2MHz)
	DIV_16	4	Divide by 16 (1MHz)
	DIV_32	5	Divide by 32 (500kHz)
	DIV_64	6	Divide by 64 (250kHz)
	DIV_128	7	Divide by 128 (125kHz)

43.5.9 DECODER

Address offset: 0x510

Configuration of the decoder



Bit r	numbe	er		31	30 2	9 28	27	26 25	5 24	23	22 2	1 20	19	18 1	17 1	6 15	5 14	13 1	.2 1	1 10	9	8	7 6	5 5	4	3	2	1 0
Id																						В					1	А А
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0 (0	0	0	0 (0	0	0	0 0	0	0	0 (0 (0	0	0	0 (0 0
Id	RW	Field	Value Id	Val	lue					Des	scrip	tion																
Α	RW	LOAD								Нον	w a s	eque	ence	is r	ead	fror	n RA	M a	nd sį	orea	d to	the	con	npar	e			
										reg	gister																	
			Common	0						1st	half	wor	d (16	5-bit	t) us	ed i	n all	PWN	∕l ch	anne	els O	3						
			Grouped	1						1st	half	wor	d (16	5-bit	t) us	ed i	n ch	anne	I 0:	1; 2n	d w	ord	in cl	nanr	nel			
										23	3																	
			Individual	2						1st	half	wor	d (16	5-bit	t) in	ch.C); 2n	d in	ch.1	;; 4	4th	in ch	.3					
			WaveForm	3						1st	half	wor	d (16	5-bit	t) in	ch.C); 2n	d in	ch.1	;; 4	4th	in						
										COI	UNTI	ERTC	P															
В	RW	MODE								Sele	ects	sour	ce fo	r ac	dvan	cing	g the	acti	ve se	eque	nce							
			RefreshCount	0						SEC	Q[n].l	REFR	RESH	is u	sed	to d	lete	mine	e loa	ding	int	erna	l co	mpa	re			
										reg	gister	S																
			NextStep	1						NEX	XTST	EP ta	ask c	aus	es a	nev	v val	ue to	be	load	ed t	o int	ern	al				
										con	mpar	e reg	gistei	rs														

43.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit	numb	er		31	. 30	29	28	3 2	7 2	6 2	25 2	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x	00000000		0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue								De	scri	ipti	on																				
Α	RW	CNT											Am	nou	nt d	of p	lay	bac	k o	ра	tte	rn (ycl	es												-
			Disabled	_										: .			L. I.	.ı /.	stor	-+	+6.0			ــــــــــــــــــــــــــــــــــــــ				٠,١								

43.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

43.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in this sequence

Bit r	umbe	r		31	. 30	29	28	27 2	26 2	25 2	24 2	23 2	2 2	1 2	0 19	18	3 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2	1 0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	١,	A А
Rese	et 0x0	0000000		0	0	0	0	0	0	0 (0	0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	lue							Desc	cript	tior	1																		
Α	RW	CNT									P	١mc	unt	of	valu	ıes	(dut	у с	/cle	s) ir	th	is se	qu	enc	e								
			Disabled	0							S	equ	uend	e is	s dis	abl	ed, i	and	sha	all n	ot k	oe s	tart	ed	as	it is	en	pty	,				

43.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded into compare register



Bit	numb	er		31	L 30	29	28	3 27	7 26	5 25	24	23	22	21	20	19 :	18 :	17 :	16	15	14	13 :	l2 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 <i>A</i>	A	Α	Α	Α	Α	Α	Α	Α .	А А
Res	et Ox0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																		
Α	RW	CNT										An	nour	nt o	fac	dditi	iona	al P	W١	Λр	eric	ds	oetv	vee	ı sa	mpl	es l	oad	ed				
												int	о со	mp	are	reg	giste	er (I	loa	d ev	very	RE	FRE	SH.	CNT	+1 F	WN	Λ					
												pe	riod	s)																			
			Continuous	0								Up	date	e ev	ery	/ PW	۷M	per	rioc	ł													

43.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	А А
Rese	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Δ	R\M	CNT										Tir	ne :	hhe	ed	afte	r th	ne s	eai	ıen	ce i	n P	M/Ν.	1 ne	rio	ds								

43.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

43.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in this sequence

	Bit n	umbe	er		31	30	29	28 2	27 2	6 2	25 2	24 2	23 2	22 2	1 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 :	12 :	11:	LO	9	8	7	6	5	4	3	2	1	0
	Id																				1	Δ,	4	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
	Rese	t 0x0	0000000		0	0	0	0	0 (0 (0	0	0	0 (0	0 () (0) (0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Id	RW	Field	Value Id	Va	lue)es	crip	tio	า																				
Ī	Α	RW	CNT									A	١mc	oun	t of	val	ues	(dı	ıty	cycl	les)	in	thi	s se	qu	enc	e									_
	Disabled			Disabled	0							9	equ	uen	ce i	s di	sab	led.	, an	d sl	hall	l nc	t b	e s	art	ed :	as i	it is	em	pty	,					

43.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded into compare register

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000001	0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
A RW CNT		Amount of additional PWM periods between samples loaded
		into compare register (load every REFRESH.CNT+1 PWM
		periods)
Continuous	0	Update every PWM period

43.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C



Time added after the sequence

Bit n	umbe	er		31	30	29 :	28	27	26	25 2	24	23	22	21 :	20	19 :	18 :	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0	
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ /	А А	Ĺ
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	
Id	RW	Field	Value Id	Va	lue							Des	cri	ptio	n																				ı
Α	RW	CNT										Tim	ie a	dde	ed a	fter	th.	e se	eau	enc	e ir	۱ P۱	ΝN	1 pe	rioc	ds									

43.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit	numbe	er		31 30 2	9 2	8 27	⁷ 26	25	24	23 2	22 2	1 20	19	18	17 1	.6 15	5 14	13 1	.2 11	10	9	8	7 6	5	4	3	2	1 0
Id				С																					Α	Α	A	А А
Res	et 0xF	FFFFFF		1 1 :	1 :	1 1	1	1	1	1	1 :	l 1	1	1	1	1 1	1	1	1 1	1	1	1 :	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Value						Des	crip	tion																
Α	RW	PIN		[031]						Pin	nun	ber																
С	RW	CONNECT								Con	nec	tion																
			Disconnected	1						Disc	conn	ect																
			Connected	0						Con	nec	t																

43.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	L6 1	5 1	4 13	12	11 1	.0 9	8	7	6	5	4	3	2 :	0
Id				С																									Α	Α.	A A	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	1	1 1	. 1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Va	alue							De	escri	iptic	on																	
Α	RW	PIN		[0	31]							Piı	n nu	ımb	er																	
С	RW	CONNECT										Co	nne	ectic	n																	
			Disconnected	1								Di	scor	nnec	ct																	
			Connected	0								Co	nne	ect																		

43.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

43.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

Bit number		31 30 29 28 27	26 25 24 23 22 21 20	19 18 17 1	.6 15 14 13 1	2 11 10 9	8 7	6 5	4 3	2 1 0
Id		С							АА	A A A
Reset 0xFFFFFFF		1 1 1 1 1	1 1 1 1 1 1 1	1 1 1	1 1 1 1 1	1 1 1	1 1	1 1	1 1	1 1 1
Id RW Field	Value Id	Value	Description							
A RW PIN		[031]	Pin number							



Bit r	numbe	er		31 3	0 29	28	27	26 2	25 2	4 2	3 22	21	20 1	19 1	.8 17	7 16	15	14 1	13 1	2 11	10	9	8	7	6	5	4 3	3 2	1 0
Id				С																							A A	A A	A A
Res	et OxF	FFFFFF		1 1	۱ 1	1	1	1	1 1	1 1	. 1	1	1	1 :	1 1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 1	1	1 1
Id	RW	Field	Value Id	Valu	е					D	escr	iptio	on																
С	RW	CONNECT								С	onne	ectic	n																
			Disconnected	1						D	iscoı	nne	t																
			Connected	0						С	onne	ect																	

43.6 Electrical specification

43.6.1 PWM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PWM,16MHz}	PWM run current, Prescaler set to DIV_1 (16 MHz), excluding				μΑ
	DMA and GPIO				
I _{PWM,8MHz}	PWM run current, Prescaler set to DIV_2 (8 MHz), excluding				μΑ
	DMA and GPIO				
I _{PWM,125kHz}	PWM run current, Prescaler set to DIV_128 (125 kHz), excluding				μΑ
	DMA and GPIO				



44 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

44.1 QFN48 6 x 6 mm package

Dimensions in millimeters for the nRF52810 QFN48 6 x 6 mm package.

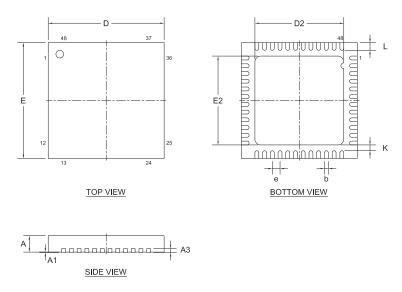


Figure 128: QFN48 6 x 6 mm package

Table 103: QFN48 dimensions in millimeters

Package	Α	A1	А3	b	D, E	D2, E2	е	K	L	
	0.80	0.00		0.15		4.50		0.20	0.35	Min.
QFN48 (6x6)	0.85	0.04	0.20	0.20	6.00	4.60	0.40		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.

44.2 QFN32 5 x 5 mm package

Dimensions in millimeters for the nRF52810 QFN32 5 x 5 mm package.



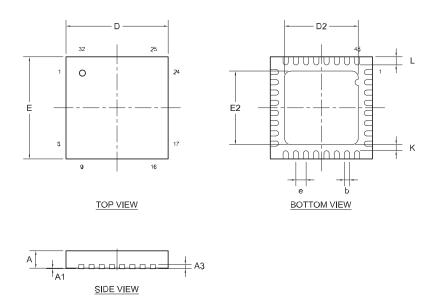


Figure 129: QFN32 5 x 5 mm package

Table 104: QFN32 dimensions in millimeters

Package	Α	A1	A3	b	D, E	D2, E2	е	K	L	
	0.80	0.00		0.20		3.40		0.20	0.35	Min.
QFN32 (5x5)	0.85	0.04	0.20	0.25	5.00	3.50	0.50		0.40	Nom.
	0.90	0.05		0.30		3.60			0.45	Max.



45 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

45.1 IC marking

The IC package is marked like described below.

N	5	2	8	1	0
<p< td=""><td>P></td><td><v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<></td></p<>	P>	<v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<>	V>	<h></h>	<p></p>
<y< td=""><td>Y></td><td><w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<></td></y<>	Y>	<w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<>	W>	<l< td=""><td>L></td></l<>	L>

Figure 130: Package marking

45.2 Box labels

Here are the box labels used for the IC.

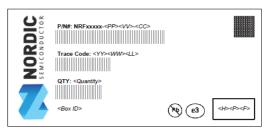


Figure 131: Inner box label



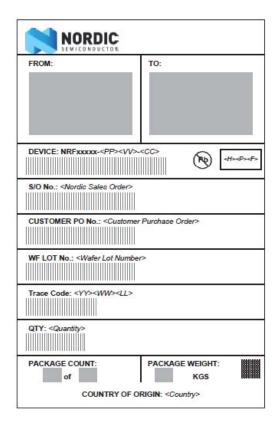


Figure 132: Outer box label

45.3 Order code

Here are the nRF52810 order codes and definitions.

n	R	F	5	2	8	1	0	-	<p< th=""><th>P></th><th><v< th=""><th>V></th><th>-</th><th><c< th=""><th>C></th><th></th></c<></th></v<></th></p<>	P>	<v< th=""><th>V></th><th>-</th><th><c< th=""><th>C></th><th></th></c<></th></v<>	V>	-	<c< th=""><th>C></th><th></th></c<>	C>	
---	---	---	---	---	---	---	---	---	--	----	--	----	---	--	----	--

Figure 133: Order code

Table 105: Abbreviations

Abbrevitation	Definition and implemented codes
N52/nRF52	nRF52 Series product
810	Part code
<pp></pp>	Package variant code
<vv></vv>	Function variant code
<h><p><f></f></p></h>	Build code
	H - Hardware version code
	P - Production configuration code (production site, etc.)
<yy><ww><ll></ll></ww></yy>	F - Firmware version code (only visible on shipping container label) Tracking code
	YY - Year code
	WW - Assembly week number
<cc></cc>	LL - Wafer lot code Container code

45.4 Code ranges and values

Defined here are the nRF52810 code ranges and values.



Table 106: Package variant codes

<pp></pp>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
QF	QFN	5 x 5	32	0.5

Table 107: Function variant codes

<vv></vv>	Flash (kB)	RAM (kB)
AA	192	24

Table 108: Hardware version codes

<h></h>	Description
[A Z]	Hardware version/revision identifier (incremental)

Table 109: Production configuration codes

<p></p>	Description
[09]	Production device identifier (incremental)
[A Z]	Engineering device identifier (incremental)

Table 110: Production version codes

<f></f>	Description	
[A N, P Z]	Version of preprogrammed firmware	
[0]	Delivered without preprogrammed firmware	

Table 111: Year codes

<yy></yy>	Description
[1599]	Production year: 2015 to 2099

Table 112: Week codes

<ww></ww>	Description
[152]	Week of production

Table 113: Lot codes

<ll></ll>	Description
[AA ZZ]	Wafer production lot identifier

Table 114: Container codes

<cc></cc>	Description
R7	7" Reel
R	7" Reel 13" Reel
Т	Tray

45.5 Product options

Defined here are the nRF52810 product options.

Table 115: nRF IC order codes

Order code	MOQ (minimum ordering quantity)	Comment
nRF52810-QFAA-R7	1000	Availability to be announced.
nRF52810-QFAA-R	3000	
nRF52810-QFAA-T	490	

Table 116: Development tools order code

Order code	Description
nRE52-DK	nRE52832 development kit with tools to support nRE52810 development



46 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from *Reference layout nRF52 Series*.

46.1 Schematic QFAA QFN48 with internal LDO setup

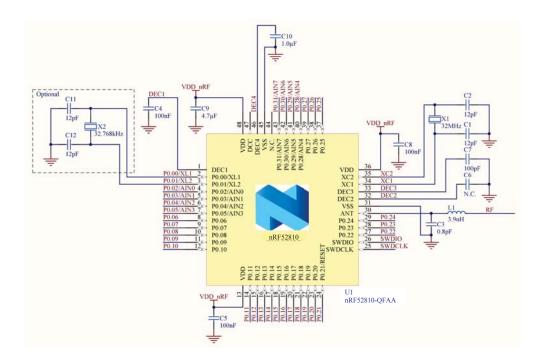


Figure 134: QFAA QFN48 with internal LDO setup

Important: For PCB reference layouts, see *Reference layout nRF52 Series*.

Table 117: Bill of material for QFAA QFN48 with internal LDO setup

Designator	Value	Description	Footprint
•		•	
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
U1	nRF52810-QFAA	Multi-protocol Bluetooth low energy, ANT and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL 3215



46.2 Schematic QFAA QFN48 with DC/DC regulator setup

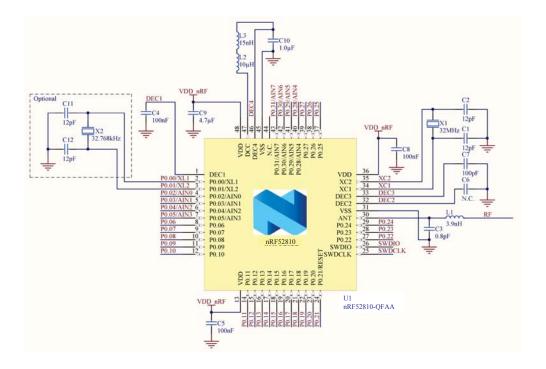


Figure 135: QFAA QFN48 with DC/DC regulator setup

Important: For PCB reference layouts, see *Reference layout nRF52 Series*.

Table 118: Bill of material for QFAA QFN48 with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52810-QFAA	Multi-protocol Bluetooth low energy, ANT and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215

46.3 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *Reference layout nRF52 Series* .

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna



matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended QFN48 package reference circuitry from *Schematic QFAA QFN48 with internal LDO setup* on page 434.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

46.4 PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see Reference layout nRF52 Series.

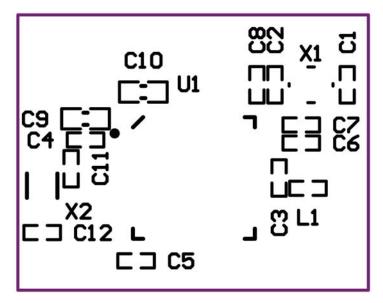


Figure 136: Top silk layer



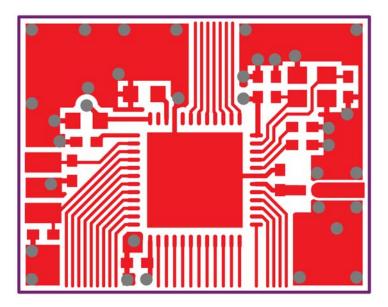


Figure 137: Top layer

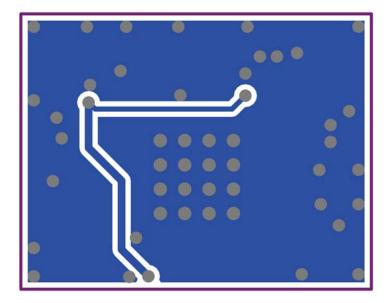


Figure 138: Bottom layer

Important: No components in bottom layer.



47 Liability disclaimer

Liability disclaimer

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