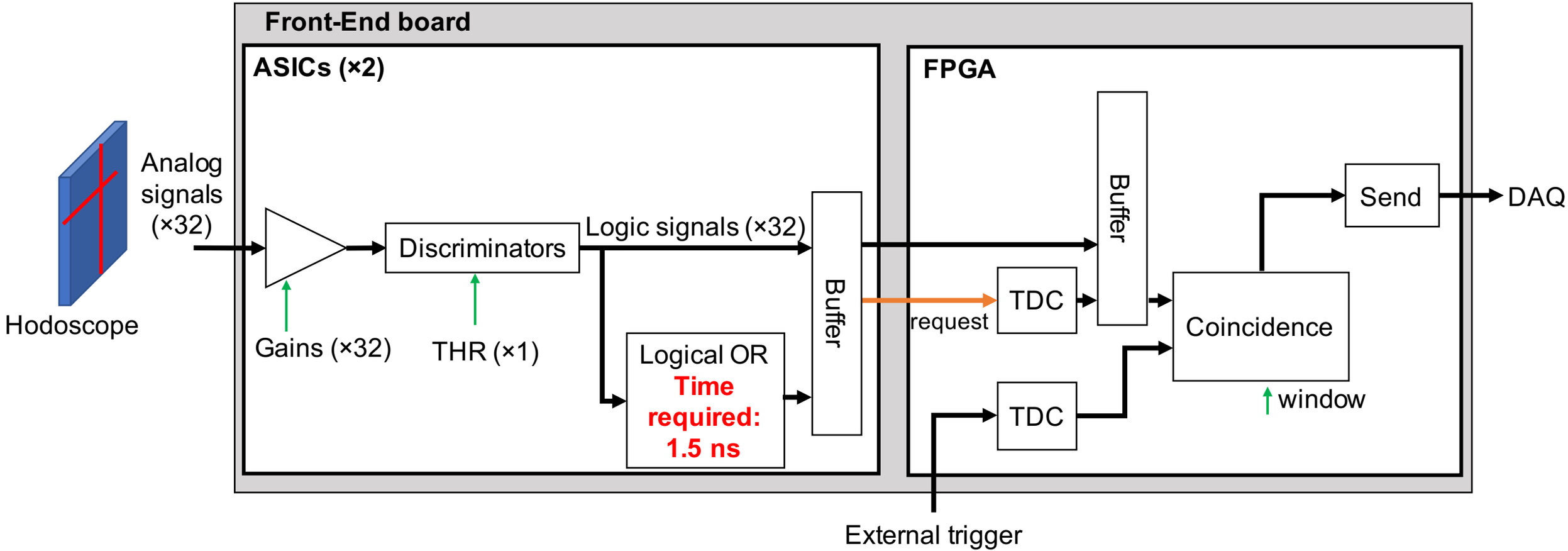
Front-End board
ASICs (×2)
FPGA
Analog signals (×32)
Hodoscope
Discriminators
Logic signals (×32)
Gains (×32)
THR (×1)
Logical OR
Time required: 1.5 ns
Buffer
Buffer
request
TDC
TDC
Coincidence
window
Send
DAQ
External trigger