BeMicro Max 10 FPGA Evaluation Kit

Getting Started User Guide

Version 14.0.2 | 11/24/2014 | User Guide

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1. OVERVIEW

BeMicro Max 10 is a FPGA evaluation kit that is designed to get you started with using an FPGA. BeMicro Max 10 adopts Altera's non-volatile **MAX® 10 FPGA** built on 55-nm flash process.

MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device. The devices also include full-featured FPGA capabilities such as digital signal processing, analog functionality, Nios II embedded processor support and memory controllers.

The BeMicro Max 10 includes a variety of peripherals connected to the FPGA device, such as 8MB SDRAM, accelerometer, digital-to-analog converter (DAC), temperature sensor, thermal resistor, photo resistor, LEDs, pushbuttons and several different options for expansion connectivity.

The kit retains the 80-pin edge connector interface used on previous Arrow BeMicro kits. Users can migrate their designs from BeMicro SDK or BeMicro CV easily and take advantage of the new features Altera offers in the MAX 10 FPGA device, such as an ADC block, temperature sense diode and flash memory.

1.1 Board Features

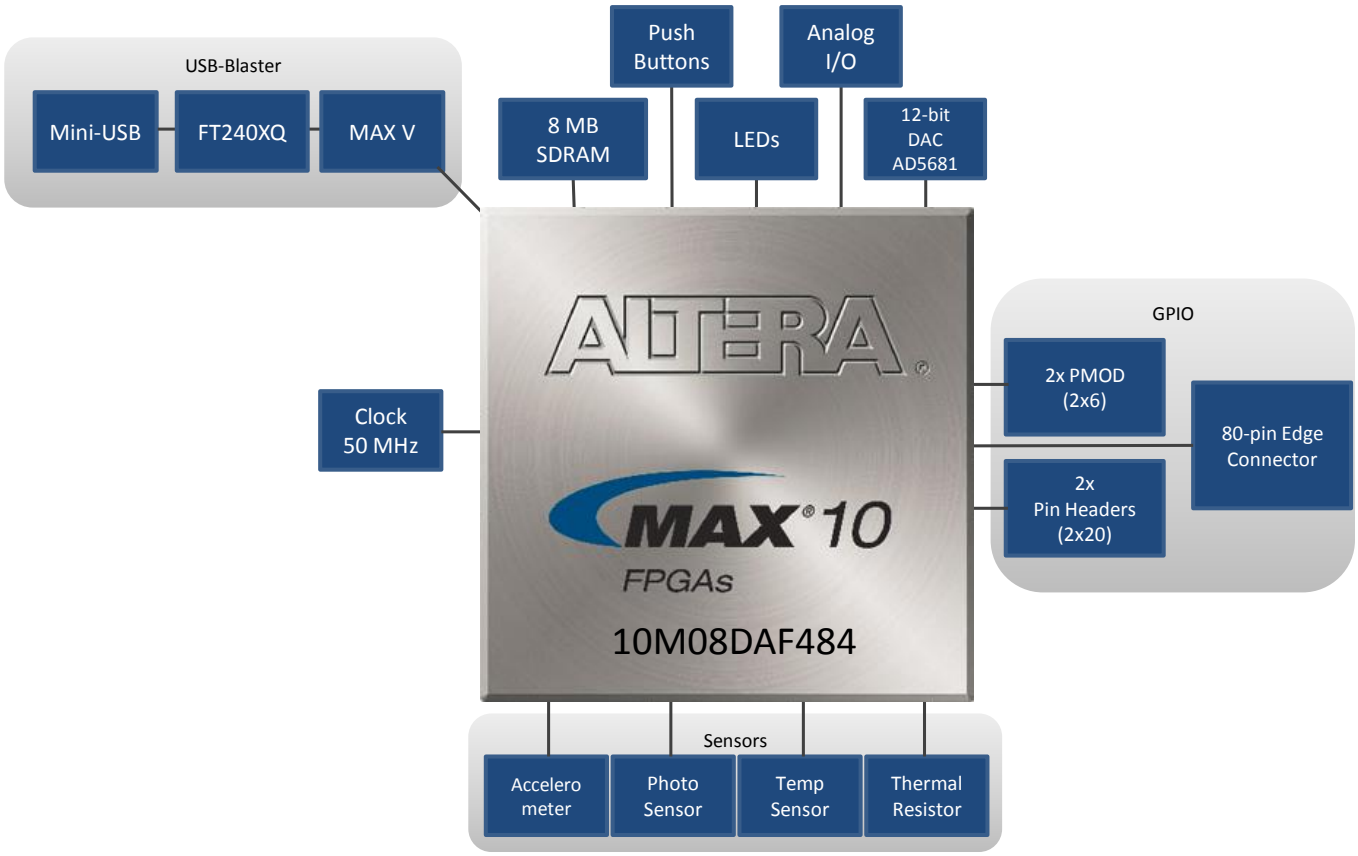
- One MAX® 10 FPGA (10M08DAF484)
  - 8,000 LEs
  - 414 Kbit (Kb) on-chip memory
  - 256 Kbit (Kb) user flash memory
  - 2 phase locked loops (PLLs)
  - 24 18x18-bit multipliers
  - 1 ADC block – 1 MSPS, 12-bit, 18-channels
  - 17 analog inputs
  - 1 temperature sense diode
  - 250 general purpose input/output (GPIO)
  - Non-volatile self-configuration with dual-boot support
- Embedded USB-Blaster™ for use with the Quartus® II Programmer
- Clocking circuitry
  - 50 MHz oscillator
- External peripherals
  - 8MB SDRAM (4Mb x 16) (ISSI IS42S16400)
  - Accelerometer, 3-Axis, SPI interface (Analog Devices ADXL362)
  - DAC, 12-bit, SPI interface (Analog Devices AD5681)
  - Temperature sensor, I2C interface (Analog Devices ADT7420)
  - Thermal resistor
  - Photo resistor
- General user input / output
  - 8 user LEDs
  - 2 user Pushbuttons
- Prototyping
  - Two 6-pin PMOD expansion headers
  - Two 40-pin prototyping headers which provide access to 64 digital I/O
  - One 6-pin analog input header

- One 80-pin BeMicro card edge connector
- Power via USB or via user-provided 5V supply

1.2 Block Diagram

Below is a block diagram of the board.

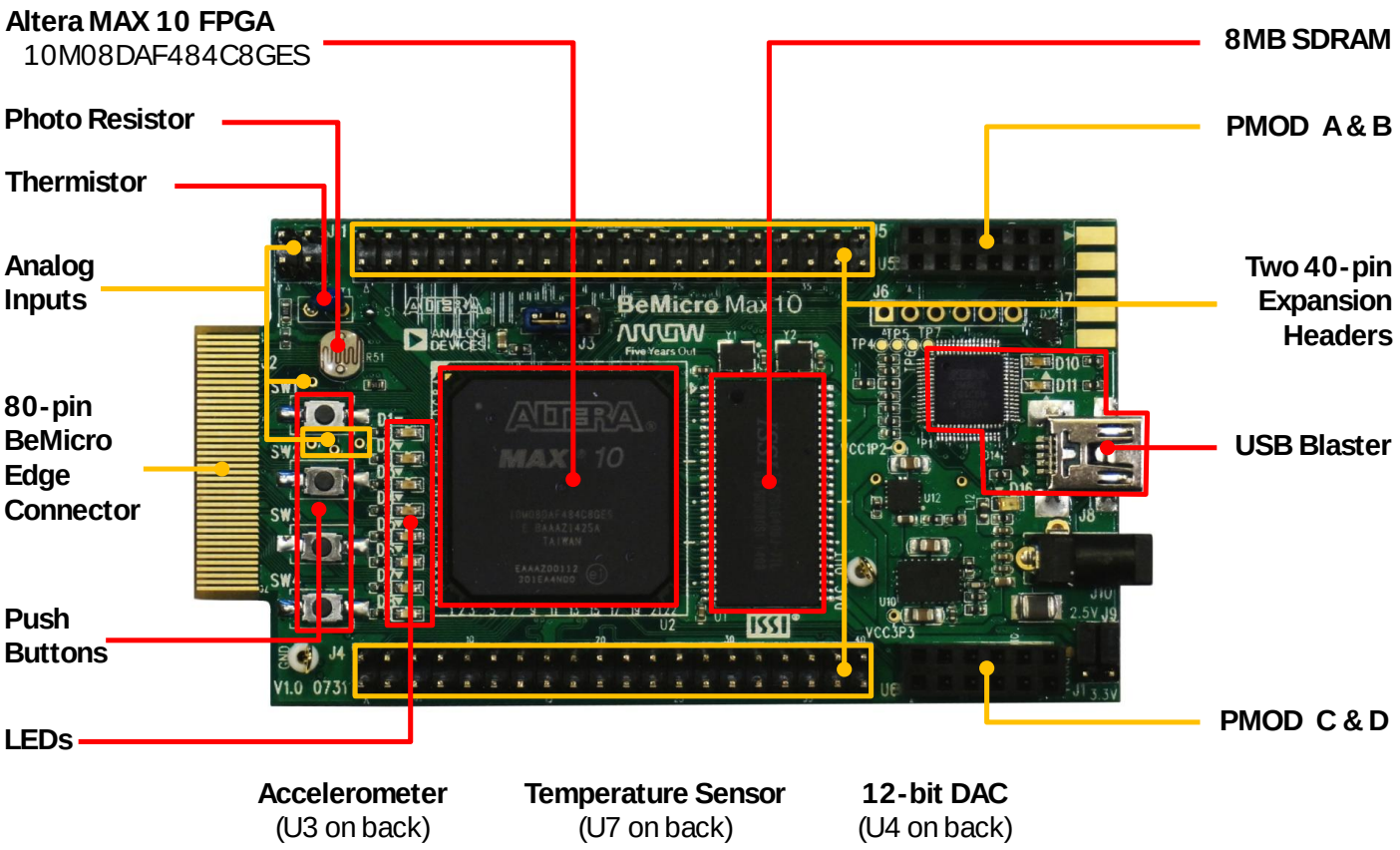
Figure 1-1: BeMicro Max 10 Block Diagram



1.3 Getting To Know Your Kit

Below is an annotated photo of the board to help you get familiar with the kit and locate the various peripherals and expansion connectors.

Figure 1-2: BeMicro Max 10 Development Kit



Your BeMicro Max10 is preloaded with a simple design which can be used to confirm that your kit is operational upon power up.

- Connect your BeMicro Max10 board to any USB power source(PC or USB charger) and watch the LED1 shine.
- Put your finger on the Analog Devices ADT7420 temperature sensor and watch the LEDs change intensity. (Your finger need to be somewhat close to body temperature.) The temperatures sensor device is component U7 on the back of the board.

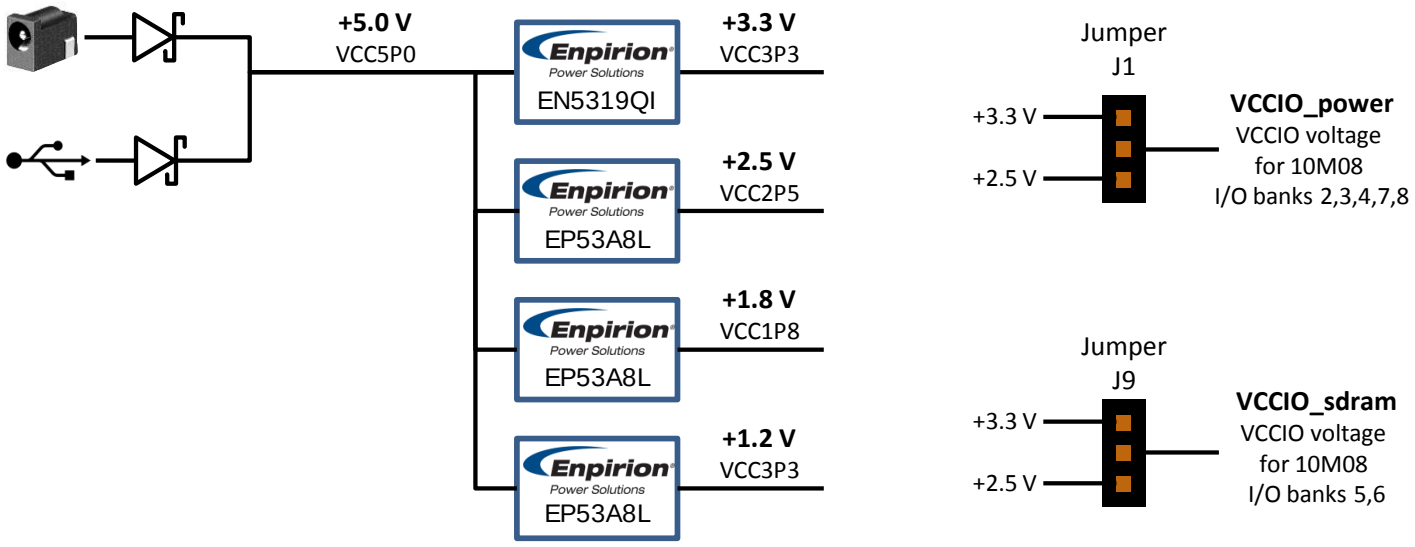
1.3.1 Powering the BeMicro MAX 10

The BeMicro MAX 10 is powered through the USB connection provided for the USB-Blaster functionality. If you wish to run the board stand-alone, you will need to source a 5V power supply with a 2.5mm jack. This optional power supply is not included with the kit.

1.3.2 Enpirion® PowerSoC Power Tree

The 5V input voltage is used to generate four lower voltage power rails needed by the devices on the BeMicro Max 10 board. Altera Enpirion® PowerSoC devices are fully integrated switching regulators and are used to create an efficient and compact power solution. The power tree on the kit is shown below.

Figure 1-3: BeMicro Max 10 Power Tree



Below is a table showing the use of each power rail.

Power Rail	*Voltage*	*Usage*
VCC3P3	+3.3 V	• possible source for VCCIO_power & VCCIO_sdram (see below) • MAX 10 I/O bank 1 • DAC • oscillator • serial flash • USB Blaster
VCC2P5	+2.5 V	• possible source for VCCIO_power & VCCIO_sdram (see below) • MAX 10 analog voltage and ADC V_{REF} • LEDs
VCC1P8	+1.8 V	• 5M80 core voltage (the 5M80 is part of the USB Blaster circuit)
VCC1P2	+1.2 V	• 10M08 core voltage
VCCIO_power	+3.3 V or +2.5 V (jumper J1)	• MAX 10 I/O banks 2,3,4,7,8 • temperature sensor
VCCIO_sdram	+3.3 V or +2.5 V (jumper J9)	• MAX 10 I/O banks 5,6 • SDRAM • Accelerometer

2. SOFTWARE INSTALLATION

This section lists the required software design tools and explains how to install the software needed to create and compile designs for your MAX 10 FPGA.

List of Required Software:

- Altera Quartus II v14.0 with Update 2 (or newer)
- BeMicro Max 10 Evaluation Kit Files
- USB-Blaster™ Driver

2.1 Install the Altera Design Software

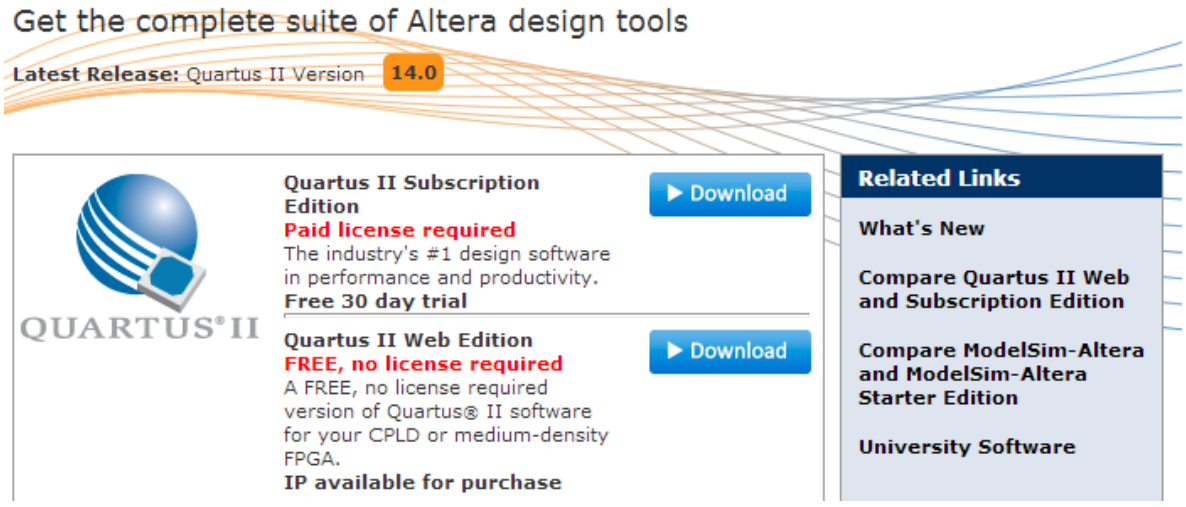
The MAX 10 FPGA device family is supported in Quartus II software versions 14.0.2 and newer. You will need to download and install the following design software package:

- **Quartus II Web Edition design software v14.0** – FPGA synthesis and compilation tool that includes the IP Catalog and QSys integration tools. You will first install the full installation of version 14.0. This installation will not contain support for MAX 10 FPGA so it will need to be updated to 14.0.2 or newer. Web Edition is a free version of the software with no licensing required.
  NOTE: Subscription Edition, which requires a paid license, can be used in place of Web Edition.
- **Quartus II Software v14.0 Update 2** – This is an update to Quartus which will add support for MAX 10 FPGA.

2.1.1 Download and Install Quartus II Web Edition v14.0

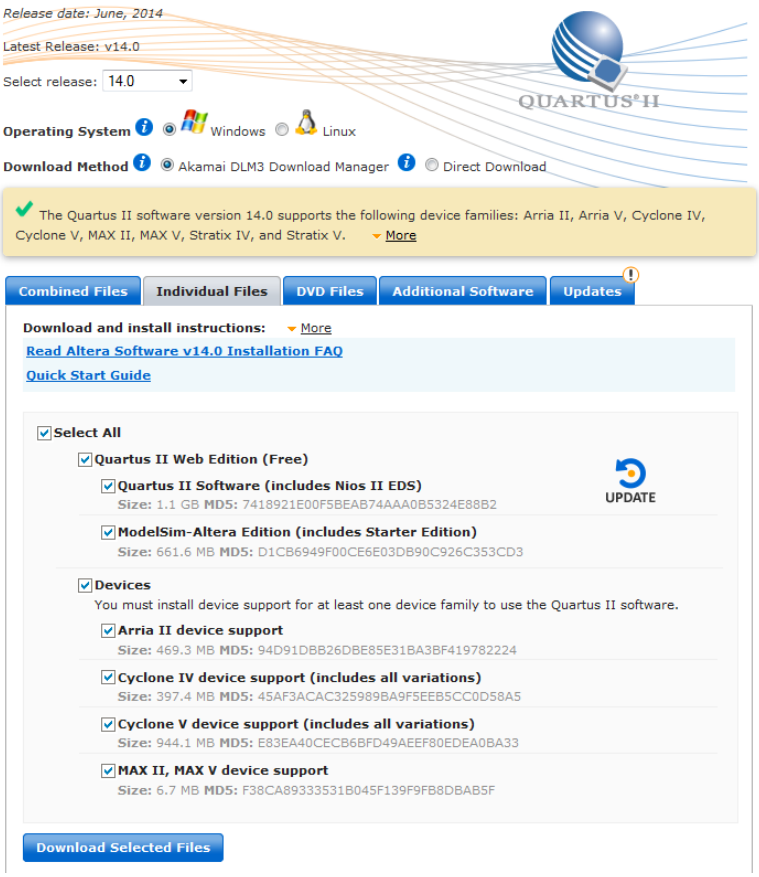
The following steps will guide you through the installation instructions. Quartus II Web Edition can be downloaded from the Altera web site. ***Please carefully follow the steps shown below***.

- Go to the Altera Download web page at **https://www.altera.com/download/dnl-index.jsp**

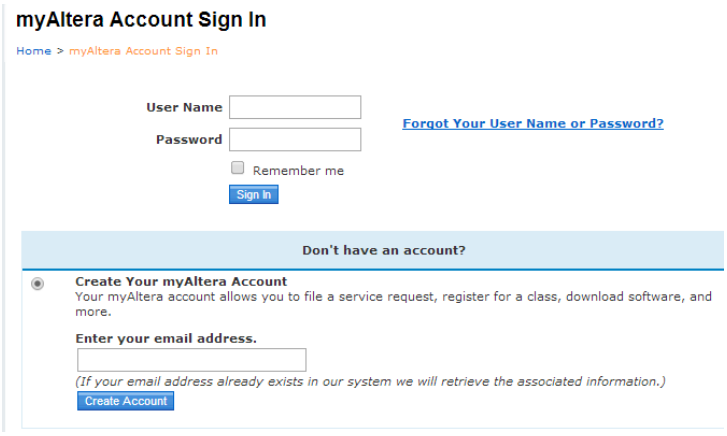


- Click on the "**Download**" button next to "**Quartus II Web Edition**"

- Ensure that the release of **Quartus II Web Edition** is set to **14.0** and select your operating system:
- Select the **"Individual Files"** Tab
- Select the **" Download Selected Files"** Button
- **Download** the Quartus II software files onto your computer.

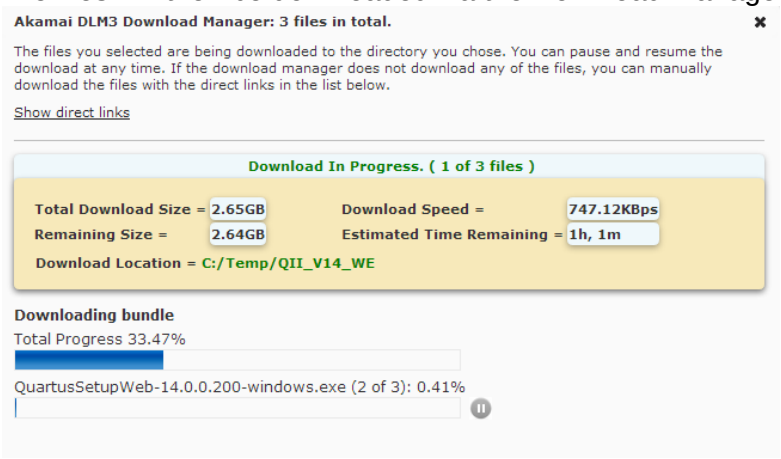


- Login to **myAltera** account. Use your **existing login**, or **Create Your myAltera account.**

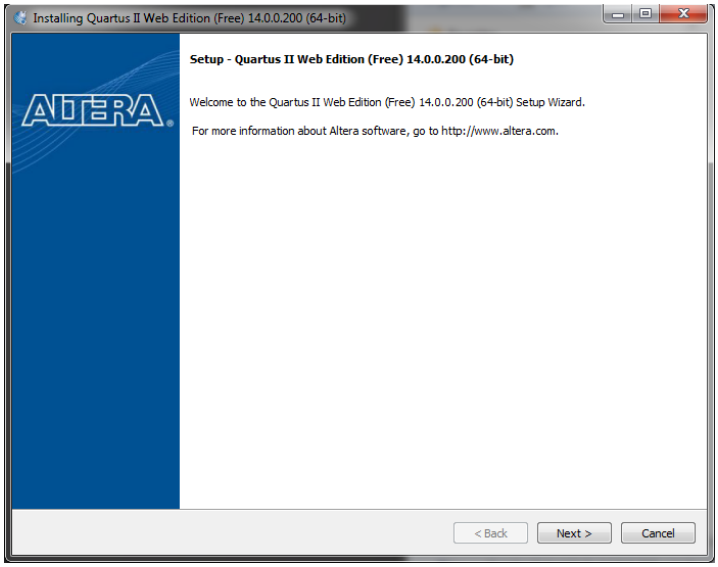


- Select a download folder (may have to Make New Folder)

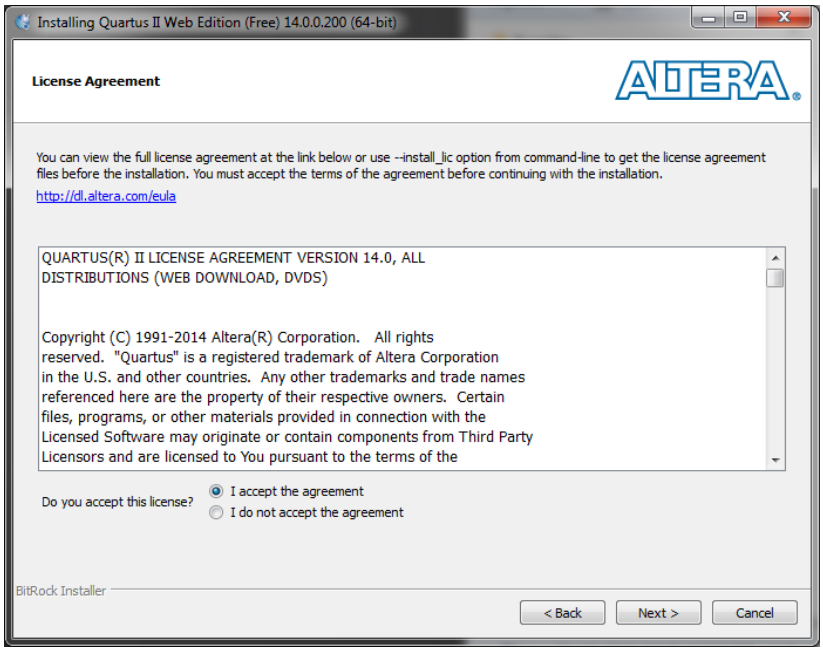
- The files will then be downloaded via the Download Manager



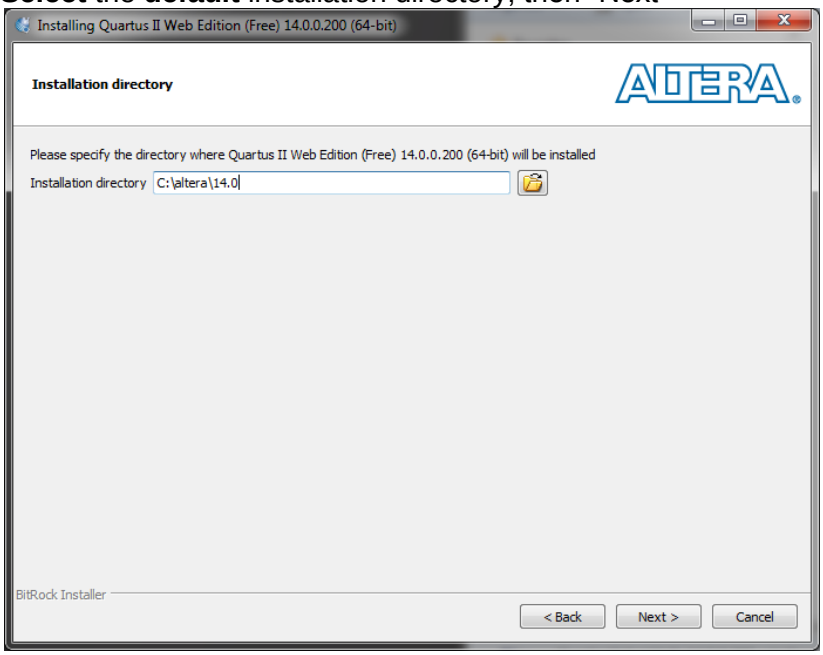
- After the **file** is downloaded on the computer, select the *.exe file, and **install the software**.



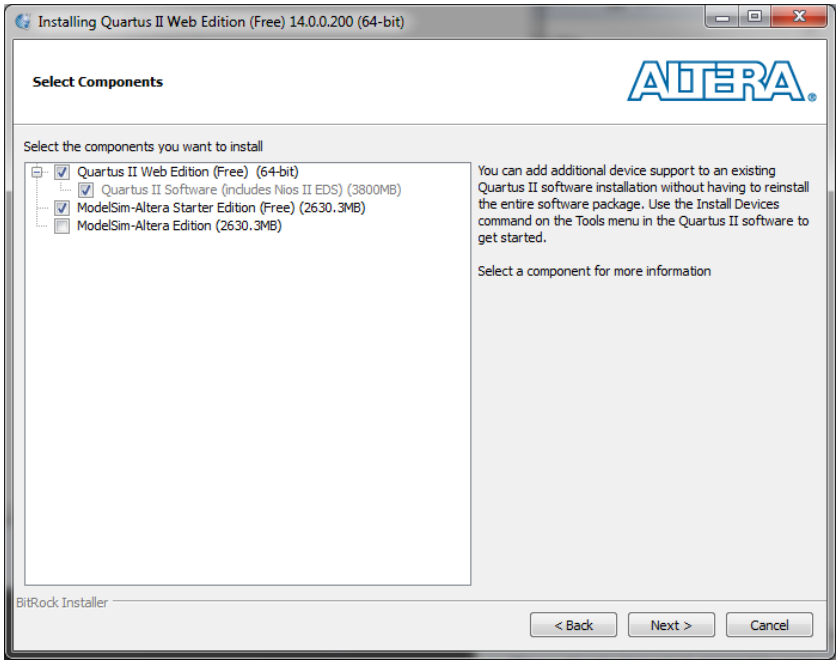
- **Accept the license agreement**, then “Next >”.



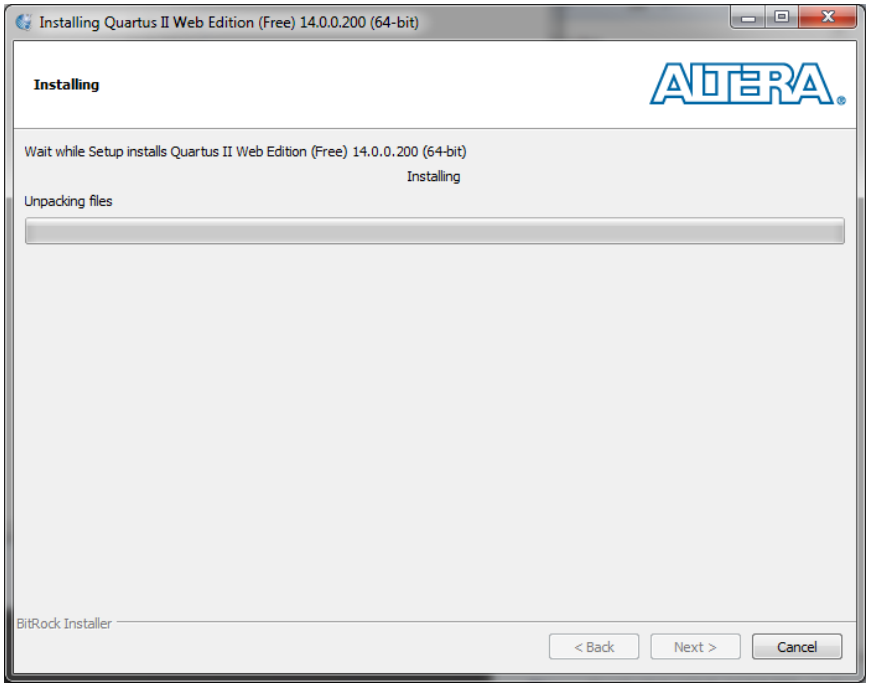
- **Select** the **default** installation directory, then “Next >”



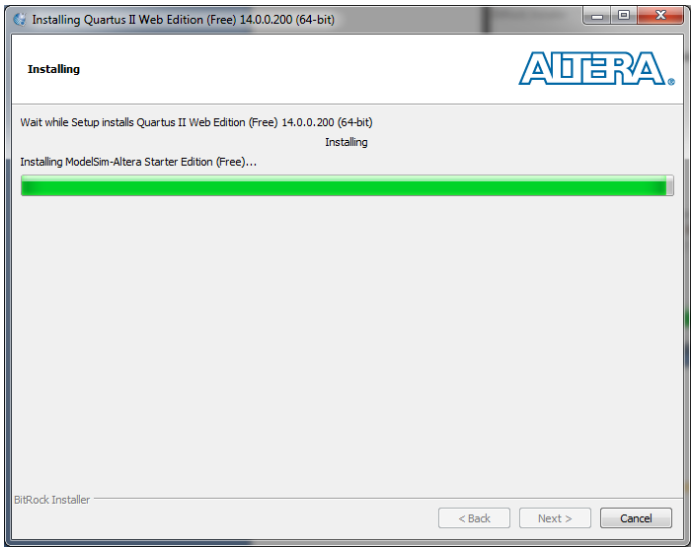
- **Select** all of the **defaults** for the installation, then “Next >”

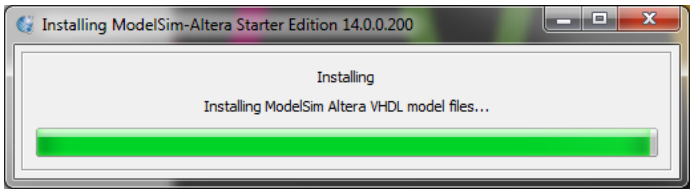


- The installation of QII Web Edition will begin:

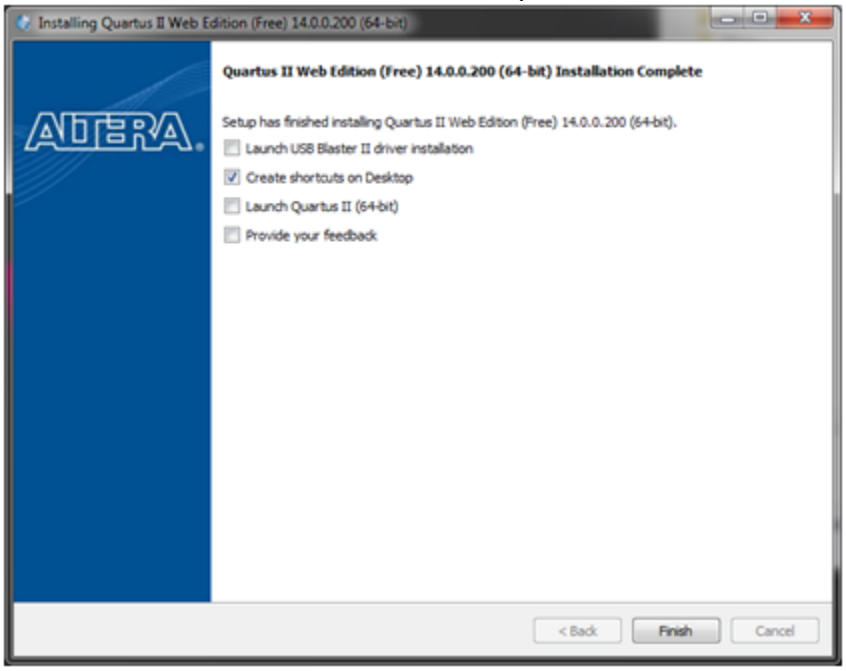


- The installation will continue with ModelSim Starter Edition:





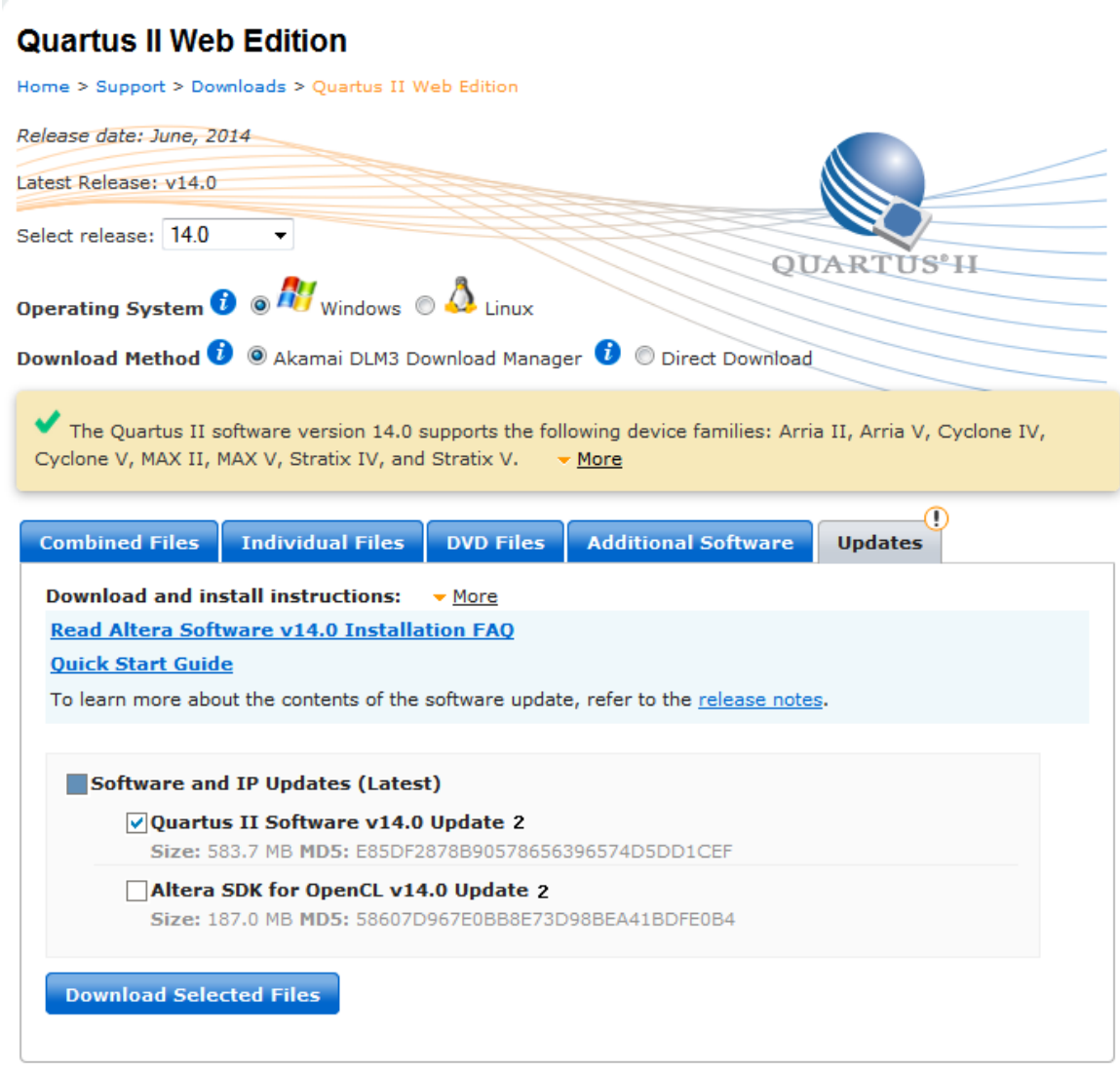
- **<u>Uncheck</u> the "Launch USB Blaster <u>II</u> driver installation"**, select **"Finish"**.
  (The BeMicro Max 10 has an integrated USB Blaster, which is different than the USB Blaster <u>II</u> and has a separate driver. The USB Blaster driver will be installed in a later step when the BeMicro Max 10 is connected to the PC.)



- Select "**Finish**"

2.1.2 Download and Install Update 2 which includes the MAX 10 FPGA device family support

- Return to the **Altera Download web page** at **https://www.altera.com/download/dnl-index.jsp**
- This time, select the "**Updates(!)**" tab.



- Select **"Quartus II Software v14.0 Update 2"**.
- Click on the "**Download Selected Files**" button and the follow the instructions to download and install the update.

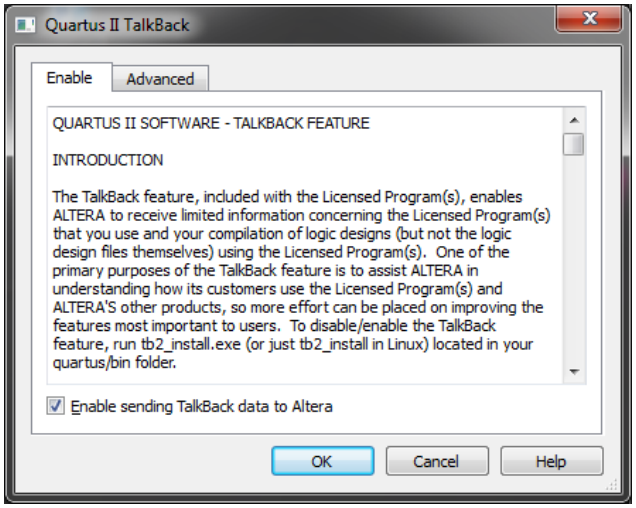
2.2 Enable TalkBack

Several features within the free Quartus Web Edition design software can only be utilized if the TalkBack feature is enabled. TalkBack bundles information (meta-data, not design files) about the current session, which is sent over a Secure Sockets Layer (SSL) connection to Altera.

By enabling TalkBack, this will enable useful features, such as the SignalTap™ II Logic Analyzer, SignalProbe and multiprocessor compilation support.

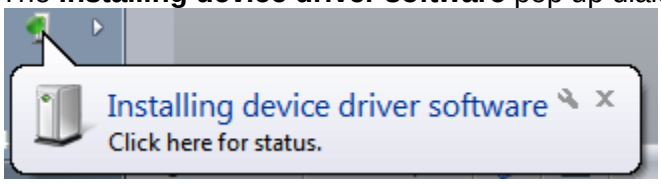
- **Select -> All Programs -> Altera 14.0.0.200 Web Edition -> Quartus II Web Edition 14.0.0.200 (64 bit) -> Quartus II 14.0 (64 bit)**

- **Enable Talkback**

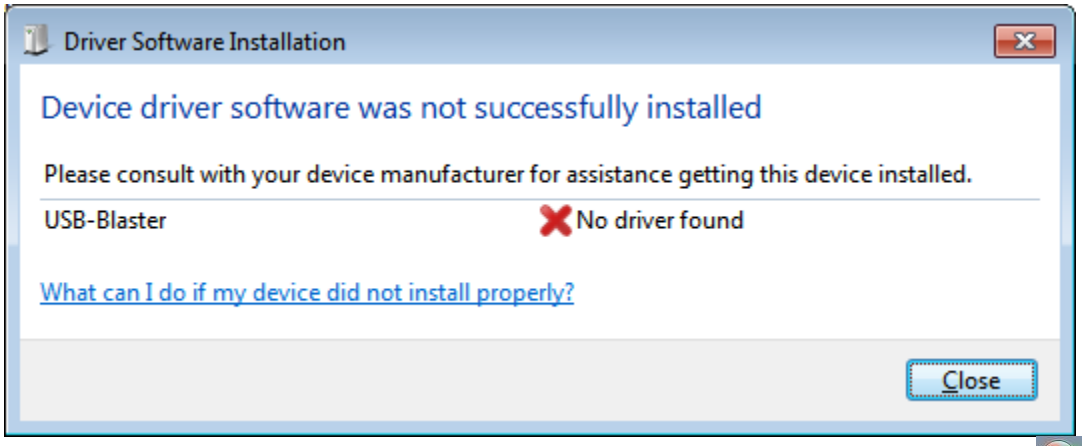


2.3 Install USB Blaster Driver

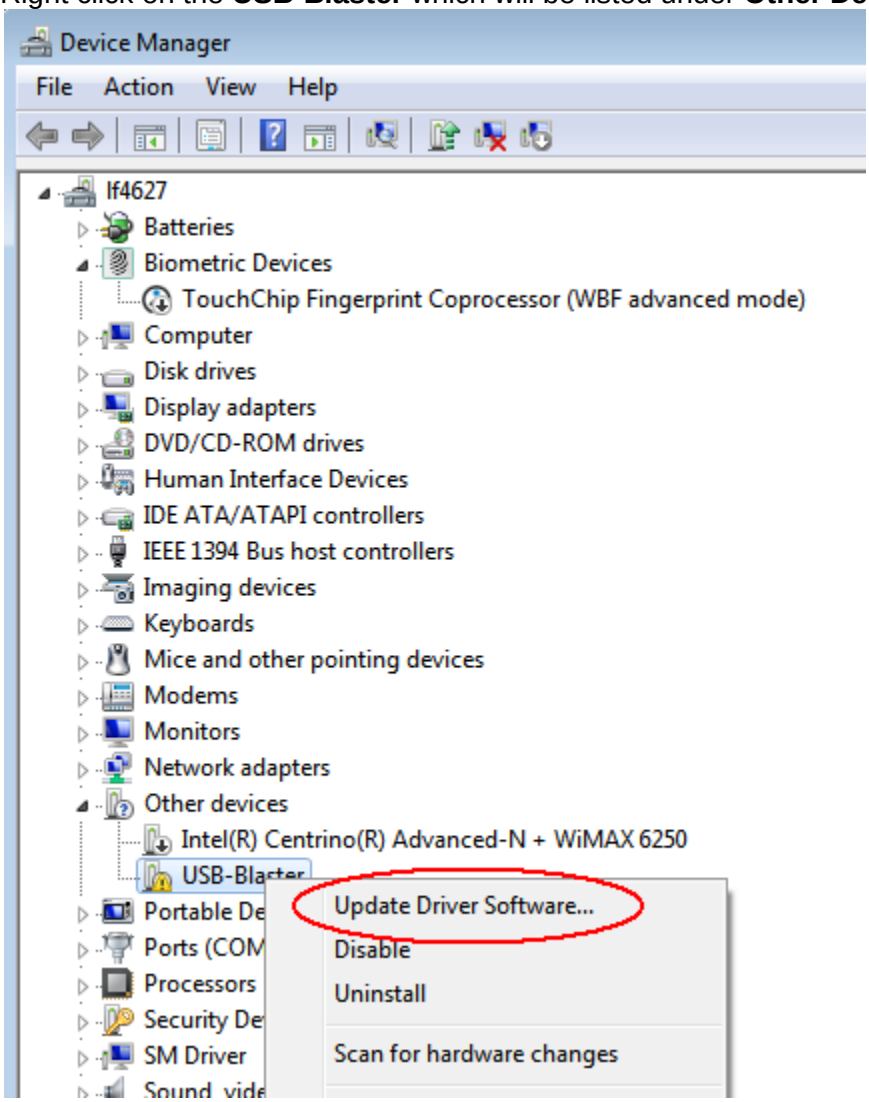
- **Connect your BeMicro Max 10 kit to your PC** using the provided mini-USB cable.
- The **Installing device driver software** pop up dialog box appears.



- The Windows driver installation will ***not*** find a driver. Click **Close**.

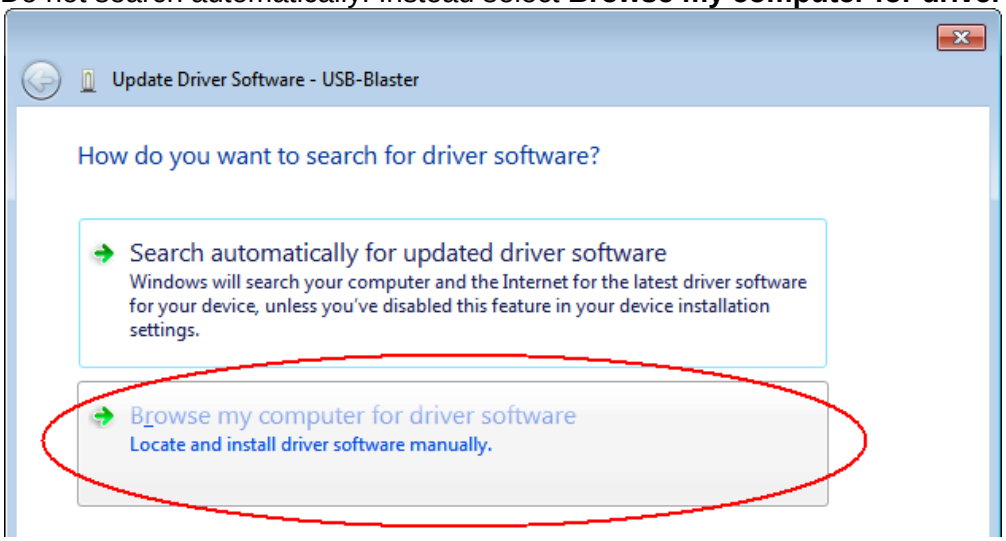


- Launch the Windows **Device Manager** by clicking on the Windows Start button and selecting **Control Panel** then double clicking on the **Device Manager** icon.
- Right click on the **USB-Blaster** which will be listed under **Other Devices**.

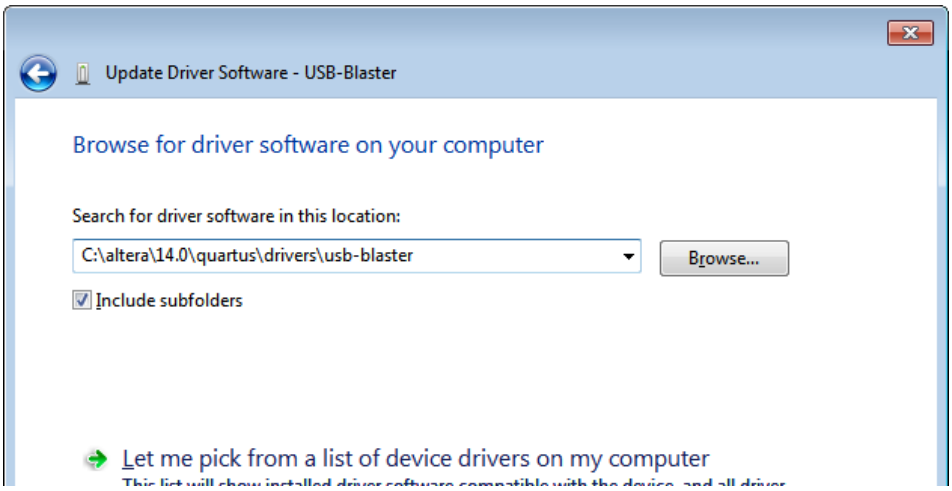


- Select "**Update Driver Software…**".

- Do not search automatically. Instead select **Browse my computer for driver software**.



- When you are prompted to **Insert the disc that came with your USB-Blaster**, select **I don't have the disc. Show me other options**.
- Select **Browse my computer for driver software (advanced)** when you see the **Windows couldn't find driver software for your device** dialog box.
- Click **Browse**, and browse to the ***C:\altera\14.0\quartus\drivers\usb-blaster*** directory.
    - Note: Do not select the x32 or x64 directories.



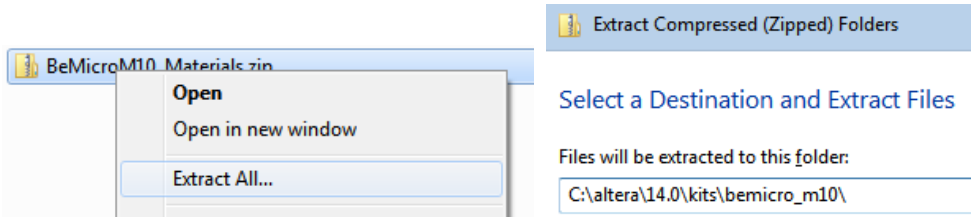
- Click **OK**.
- Select the **Include subfolders** option, and click **Next**.
- If you are prompted **Windows can't verify the publisher of this driver software**, select **Install this driver software anyway** in the **Window Security** dialog box. The installation wizard guides you through the installation process.
- When **The software for this device has been successfully installed** dialog box appears, click **Close**.

2.4 Download and Extract a BeMicro Max 10 Kit Example Project

An example project, as well as several hands-on tutorials, are available to assist you in getting started. The projects can be found online at the AlteraWiki:

http://www.alterawiki.com/wiki/BeMicro_MAX_10

- Create a folder **C:\altera\14.0\kits\bemicro_m10** on your PC.
- Download and extract the files for one of the project examples to the folder you just created.



CONGRATULATIONS!!

You have just completed all the setup and installation requirements and are now ready to begin your FPGA design.

3. PINOUT INFORMATION FOR MAX 10 FPGA I/O

The BeMicro Max 10 contains a variety of external peripheral devices and expansion headers connected to the MAX 10 FPGA's configurable I/O pins. The details of the board circuitry and these connections can be found in the schematic for the kit. (Refer to Section 2.4 for details on locating these files.)

This section presents the information in the schematic organized into pinout tables by peripheral. While the schematic provides a board level view of all the pins for a given connector or peripheral, the tables in this section focus on the FPGA signals needed for FPGA pin assignment and compilation. The "*Signal Name*" column in the tables throughout this section indicates the naming of the signal in the Quartus projects' QSF[1] file provided in the various FPGA projects.

3.1 Analog Devices External Peripherals

3.1.1 Accelerometer, 3-Axis, SPI interface (ADXL362)

Signal Name	*MAX 10 Pin*
ADXL362_CS	L14
ADXL362_INT1	M15
ADXL362_INT2	M14
ADXL362_MISO	L18
ADXL362_MOSI	L19
ADXL362_SCLK	M18

3.1.2 DAC, 12-bit, SPI interface (AD5681)

Signal Name	*MAX 10 Pin*
AD5681R_LDACn	N18
AD5681R_RSTn	L15
AD5681R_SCL	G17
AD5681R_SDA	H17
AD5681R_SYNCn	N19

3.1.3 Temperature sensor, I2C interface (ADT7420)

Signal Name	*MAX 10 Pin*
ADT7420_CT	P13
ADT7420_INT	AB14
ADT7420_SCL	W13
ADT7420_SDA	R13

[1] A "QSF file" is a Quartus Settings File, a file with extension of *.qsf, in which Quartus stores all project settings including pin assignments.

3.2 External Memory Devices

3.2.1 8MB SDRAM

The BeMicro Max 10 contains an ISSI IS42S16400J-7TL SDRAM device , which is connected to the MAX 10 FPGA and provides 8MB of memory which can be accessed by an FPGA design.

Signal Name	*MAX 10 Pin*
SDRAM_A[0]	T20
SDRAM_A[1]	T19
SDRAM_A[2]	T18
SDRAM_A[3]	AA21
SDRAM_A[4]	AA22
SDRAM_A[5]	U22
SDRAM_A[6]	T22
SDRAM_A[7]	R22
SDRAM_A[8]	P20
SDRAM_A[9]	P22
SDRAM_A[10]	U21
SDRAM_A[11]	P19
SDRAM_A[12]	N20
SDRAM_BA[0]	R20
SDRAM_BA[1]	T21
SDRAM_CASn	N21
SDRAM_CKE	N22
SDRAM_CLK	M22
SDRAM_CSn	P21
SDRAM_DQ[0]	C22
SDRAM_DQ[1]	D22
SDRAM_DQ[2]	E22
SDRAM_DQ[3]	F22
SDRAM_DQ[4]	G22
SDRAM_DQ[5]	H22
SDRAM_DQ[6]	J22
SDRAM_DQ[7]	K22
SDRAM_DQ[8]	K21
SDRAM_DQ[9]	J21
SDRAM_DQ[10]	H21
SDRAM_DQ[11]	G20
SDRAM_DQ[12]	F21
SDRAM_DQ[13]	E21
SDRAM_DQ[14]	D21
SDRAM_DQ[15]	C21
SDRAM_DQMH	L22
SDRAM_DQML	L20
SDRAM_RASn	M20

Signal Name	MAX 10 Pin
SDRAM_WEn	M21

3.2.2 Serial Flash, 16 Mbit

The BeMicro MAX 10 contains a 16 Mbit SPI-interface serial NOR flash device, Micron M25P16-VMN6, which can be used for off-chip storage in case a design's flash storage needs are larger than the internal MAX 10 FPGA User Flash Memory (UFM).

Signal Name	MAX 10 Pin
SFLASH_ASDI	R11
SFLASH_CSn	R10
SFLASH_DATA	P10
SFLASH_DCLK	P11

3.3 User Interaction

3.3.1 LEDs

Board Label	Signal Name	MAX 10 Pin
D1	USER_LED[1]	M2
D2	USER_LED[2]	N1
D3	USER_LED[3]	R2
D4	USER_LED[4]	T1
D5	USER_LED[5]	V4
D6	USER_LED[6]	T6
D7	USER_LED[7]	AB4
D8	USER_LED[8]	AA5

3.3.2 Push Buttons

Board Label	Signal Name	MAX 10 Pin
SW1	PB[1]	M1
SW2	PB[2]	R1
SW3	PB[3]	V5
SW4	PB[4]	AB5

3.4 MAX 10 FPGA Analog Inputs

3.4.1 Analog Input Header

One of the key features of the MAX 10 FPGA is the analog block. Connector J11 can be used to attach input signals to the MAX 10 FPGA device. The signals coming from the connector pass through a signal conditioning RC circuit and then are fed into the analog input pins of the MAX 10 FPGA device.

Signal Name	*MAX 10 Pin*	*MAX 10 ADC channel number*	*Board Connection Point*
AIN[0]	F5	Ch. 1	2x2 header J11, pin 1
AIN[1]	E4	Ch. 9	2x2 header J11, pin 2
AIN[2]	F4	Ch. 2	testpoint TP12 (silkscreen “AIN3” on back)
AIN[3]	E3	Ch. 16	testpoint TP13 (silkscreen “AIN4” on back)
AIN[4]	J8	Ch. 3	testpoint TP15 (silkscreen “AIN5” on back)
AIN[5]	G4	Ch. 11	testpoint TP14 (silkscreen “AIN6” on back)

3.4.2 Photo Resistor

The BeMicro Max 10 board contains a photo resistor attached to one of the analog input pins of the MAX 10 FPGA.

Signal Name	*MAX 10 Pin*	*MAX 10 ADC channel number*
AIN[6]	J9	Ch. 4

3.4.3 Thermistor (Thermal Resistor)

The BeMicro Max 10 board also contains a thermistor attached to one of the analog input pins of the MAX 10 FPGA.

Signal Name	*MAX 10 Pin*	*MAX 10 ADC channel number*
AIN[7]	F3	Ch. 12

3.4.4 Other MAX 10 ADC inputs

The remaining MAX 10 ADC inputs are connected to various power rails on the BeMicro Max 10 kit.

Signal Name	*MAX 10 Pin*	*MAX 10 ADC channel number*	*Board Connection Point*
VCC3P3	J4	Ch. 5	3.3V power rail
VCC2P5	H4	Ch. 13	2.5V power rail
VCC1P8	H3	Ch. 6	1.8V power rail
VCC1P2	G3	Ch. 14	1.2V power rail
GND	K5, K6, J3,	Ch. 7, 8, 10, 15	ground

	K4		

3.5 Expansion Headers and Connectors

3.5.1 BeMicro Edge Connector

The BeMicro Max 10 contains the same 80-pin edge connector used on previous Arrow BeMicro kits such as the BeMicro CV and the BeMicro SDK. A Samtec connector part number MEC6-140-02-X-D-RA1 can be used to mate to this edge connector.

Signal Name	*MAX 10 Pin*
EG_P1	C1
EG_P2	D2
EG_P3	D1
EG_P4	D3
EG_P5	E1
EG_P6	F2
EG_P7	F1
EG_P8	G1
EG_P9	H1
EG_P10	J1
EG_P11	K2
EG_P12	L2
EG_P13	N2
EG_P14	P3
EG_P15	P1
EG_P16	R3
EG_P17	T2
EG_P18	R4
EG_P19	T5
EG_P20	Y1
EG_P21	Y2
EG_P22	AA1
EG_P23	AA2
EG_P24	Y3
EG_P25	Y4
EG_P26	AB6
EG_P27	AB7
EG_P28	AA8
EG_P29	AB8

Signal Name	*MAX 10 Pin*
EG_P35	E11
EG_P36	E10
EG_P37	D9
EG_P38	E9
EG_P39	E8
EG_P40	D8
EG_P41	E6
EG_P42	D7
EG_P43	C8
EG_P44	C7
EG_P45	D6
EG_P46	C6
EG_P47	D5
EG_P48	C5
EG_P49	C4
EG_P50	H11
EG_P51	J10
EG_P52	M9
EG_P53	M8
EG_P54	N9
EG_P55	N8
EG_P56	N5
EG_P57	N4
EG_P58	N3
EG_P59	P5
EG_P60	P4
EXP_PRESENT	R5
RESET_EXPn	C2

3.5.2 Two 40-pin Expansion Headers

Two 40-pin prototyping headers, J3 and J4, provide access to single ended digital signals, differential LVDS transmit pairs and differential receive pairs. The pinout for these connectors match the pinout of several daughter cards available from third-party vendors such as Terasic.

Signal Name	MAX 10 Pin	J3 Pin
GPIO_01	B2	1
GPIO_02	B1	2
GPIO_03	C3	3
GPIO_04	A2	4
GPIO_05	B3	5
GPIO_06	A3	6
GPIO_07	B4	7
GPIO_08	A4	8
GPIO_09	B5	9
GPIO_10	A5	10
GPIO_11	B7	13
GPIO_12	A6	14
DIFF_RX_P[0]	K14	39
DIFF_RX_P[0](n)	K15	40
DIFF_RX_P[1]	E16	37
DIFF_RX_P[1](n)	E15	38
DIFF_RX_P[2]	D17	35
DIFF_RX_P[2](n)	C17	36
DIFF_RX_P[3]	H14	33
DIFF_RX_P[3](n)	J13	34
DIFF_RX_P[4]	C14	31
DIFF_RX_P[4](n)	C13	32
DIFF_RX_P[5]	A14	27
DIFF_RX_P[5](n)	B14	28
DIFF_RX_P[6]	D14	25
DIFF_RX_P[6](n)	E13	26
DIFF_RX_P[7]	E12	23
DIFF_RX_P[7](n)	D13	24
DIFF_RX_P[8]	H12	21
DIFF_RX_P[8](n)	J11	22
DIFF_RX_P[9]	B10	19
DIFF_RX_P[9](n)	C9	20
DIFF_RX_P[10]	A9	17
DIFF_RX_P[10](n)	B8	18
DIFF_RX_P[11]	A7	15
DIFF_RX_P[11](n)	A8	16

Signal Name	MAX 10 Pin	J4 Pin
I2C_SDA	AA14	3
I2C_SCL	AB15	4
GPIO_A	AA15	5
GPIO_B	Y16	6
LVDS_TX_P[0]	V17	39
LVDS_TX_P[0](n)	W17	40
LVDS_TX_P[1]	V16	37
LVDS_TX_P[1](n)	U15	38
LVDS_TX_P[2]	W15	35
LVDS_TX_P[2](n)	V14	36
LVDS_TX_P[3]	W14	31
LVDS_TX_P[3](n)	V13	32
LVDS_TX_P[4]	Y14	29
LVDS_TX_P[4](n)	Y13	30
LVDS_TX_P[5]	AA10	27
LVDS_TX_P[5](n)	Y10	28
LVDS_TX_P[6]	V10	23
LVDS_TX_P[6](n)	V9	24
LVDS_TX_P[7]	AA7	21
LVDS_TX_P[7](n)	AA6	22
LVDS_TX_P[8]	W8	19
LVDS_TX_P[8](n)	W7	20
LVDS_TX_P[9]	U7	15
LVDS_TX_P[9](n)	U6	16
LVDS_TX_P[10]	W6	13
LVDS_TX_P[10](n)	W5	14
LVDS_TX_P[11]	W3	11
LVDS_TX_P[11](n)	W4	12

3.5.3 PMOD™ Connectors

The BeMicro MAX 10 provides two 2x6 female PMOD™ connectors, labeled as U5 & U6. PMODs are small I/O interface boards that offer an ideal way to extend the capabilities of our FPGA/CPLD and embedded control board. More information and examples can be found online at: www.digilent.com/pmods.

Signal Name	*MAX 10 Pin*
PMOD_A[0]	C20
PMOD_A[1]	D19
PMOD_A[2]	D18
PMOD_A[3]	E18

Signal Name	*MAX 10 Pin*
PMOD_B[0]	E19
PMOD_B[1]	F18
PMOD_B[2]	F20
PMOD_B[3]	G19

Signal Name	*MAX 10 Pin*
PMOD_C[0]	U18
PMOD_C[1]	U17
PMOD_C[2]	R18
PMOD_C[3]	P18

Signal Name	*MAX 10 Pin*
PMOD_D[0]	R14
PMOD_D[1]	R15
PMOD_D[2]	P15
PMOD_D[3]	P14

3.6 Clock Inputs

The clocking on the BeMicro Max 10 is provided by a 50 MHz oscillator, which connects to the one of the MAX 10 FPGA's clock input pins. The 50 MHz clock input is used in many of the example designs as the primary "system" clock. The BeMicro Max 10 PCB also contains an unpopulated oscillator footprint, which is provided as an optional secondary clock source for user designs.

Signal Name	*MAX 10 Pin*	*Description*
SYS_CLK	N14	50 MHz "System" Clock Input
USER_CLK	N15	Unpopulated "User" Clock Input

3.7 Boot Select

Jumper J3 is used to strap the MAX 10 FPGA device's BOOT_SEL pin. The 10M08 device supports holding two FPGA images is its Configuration Flash Memory. The BOOT_SEL pin can be used to allow the user to select which image is loaded by default on power up.

4. HANDS-ON TUTORIALS AND EXAMPLE DESIGNS

Several hands-on tutorials are available to assist you in getting started. These tutorials can be found online at the AlteraWiki:

http://www.alterawiki.com/wiki/BeMicro_MAX_10

Some of the tutorials available, which can be found on the above AlteraWiki site, are:

- **Intro to FPGAs Lab** – designed to get someone familiar with the basics of FPGA design by building a simple design from scratch.
- **Temperature Sensor Lab** – another simple lab to show using the MAX10 ADC and temp sensor.
- **Embedded System Lab** – advanced lab to show building a QSys and Nios II system. This lab will be based around the example Quartus Project that will be included with the kit.