NTR4501N, NSTR4501N

Power MOSFET

20 V, 3.2 A, Single N−Channel, SOT−23

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 2.5 V Rated for Low Voltage Gate Drive
- SOT−23 Surface Mount for Small Footprint
- NSTR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Load/Power Switch for Portables
- Load/Power Switch for Computing
- DC−DC Conversion

MAXIMUM RATINGS (T_J= 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.2	A
		T_A = 85°C		2.4	A
Steady State Power Dissipation (Note 1)	Steady State		P_D	1.25	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	10.0	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150	°C
Continuous Source Current (Body Diode)			I_S	1.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient (Note 1)	$R_{\theta JA}$	100	°C/W
Junction−to−Ambient (Note 2)	$R_{\theta JA}$	300	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size.

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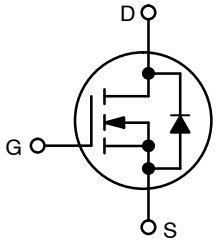
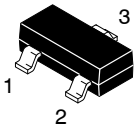
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max (Note 1)
20 V	70 mΩ @ 4.5 V	3.6 A
	88 mΩ @ 2.5 V	3.1 A

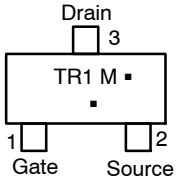
N−Channel





SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM & PIN ASSIGNMENT



TR1 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTR4501NT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
NSTR4501NT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage (Note 3)	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20	24.5		V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				22		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	T_J = 25°C			1.5	μA
		V_{DS} = 16 V	T_J = 85°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V				±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage (Note 3)	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.65		1.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−2.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 3.6 A			70	80	mΩ
		V_{GS} = 2.5 V, I_D = 3.1 A			88	105	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 3.6 A			9		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 10 V			200		pF
Output Capacitance	C_{oss}				80		
Reverse Transfer Capacitance	C_{rss}				50		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.6 A			2.4	6.0	nC
Gate−to−Source Gate Charge	Q_{GS}				0.5		
Gate−to−Drain Charge	Q_{GD}				0.6		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.6 A, R_G = 6.0 Ω			6.5	13	ns
Rise Time	t_r				12	24	
Turn−Off Delay Time	$t_{d(off)}$				12	24	
Fall Time	t_f				3	6	
SOURCE−DRAIN DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 1.6 A			0.8	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 1.6 A			7.1		ns
Charge Time	t_a				5		
Discharge Time	t_b				1.9		
Reverse Recovery Charge	Q_{RR}				3.0		nC

3. Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

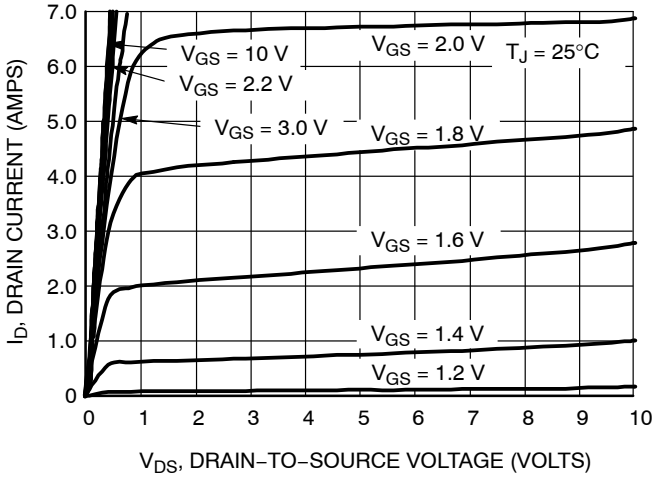


Figure 1. On−Region Characteristics

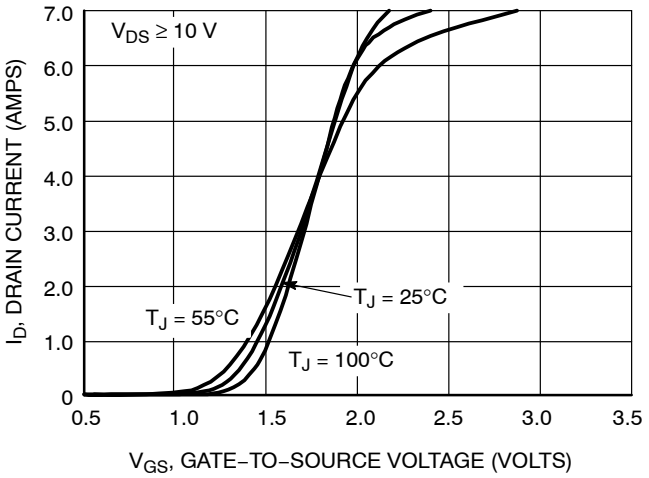


Figure 2. Transfer Characteristics

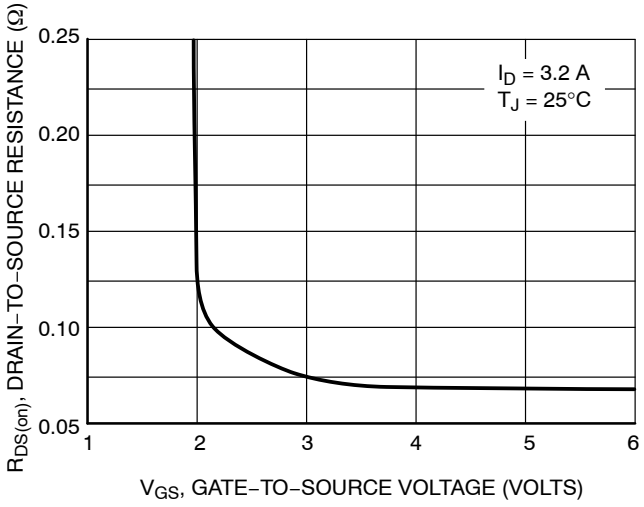


Figure 3. On−Resistance versus Gate−to−Source Voltage

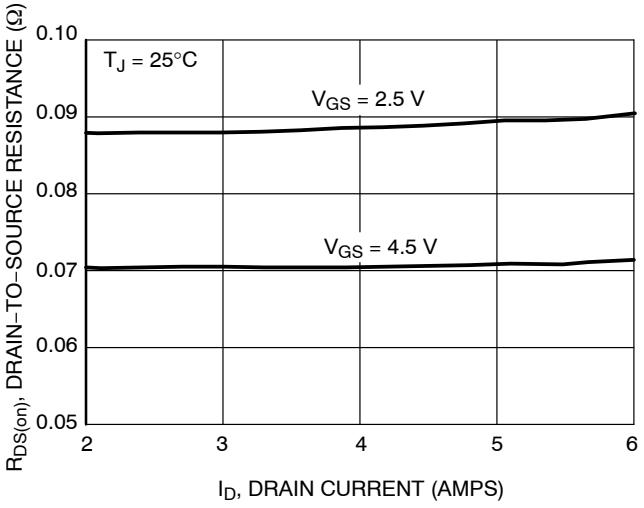


Figure 4. On−Resistance versus Drain Current and Gate Voltage

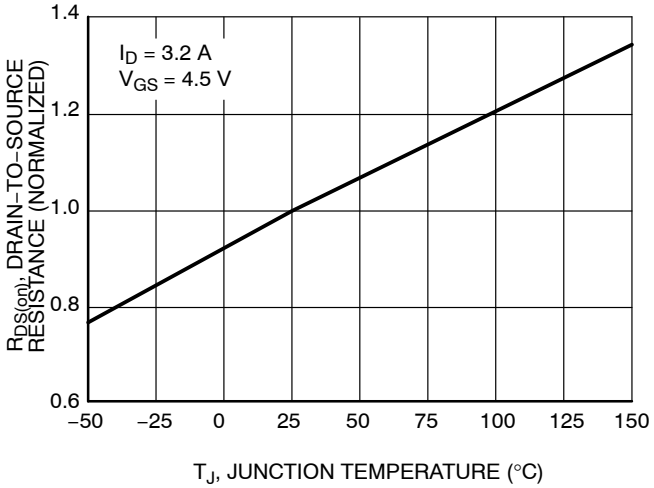


Figure 5. On−Resistance Variation with Temperature

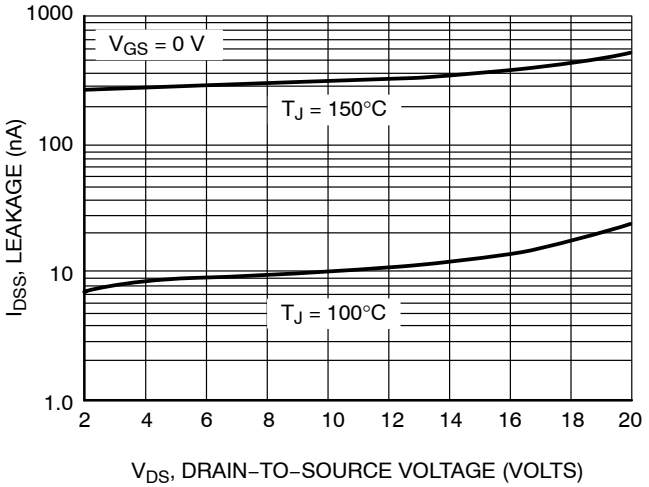


Figure 6. Drain−to−Source Leakage Current versus Voltage

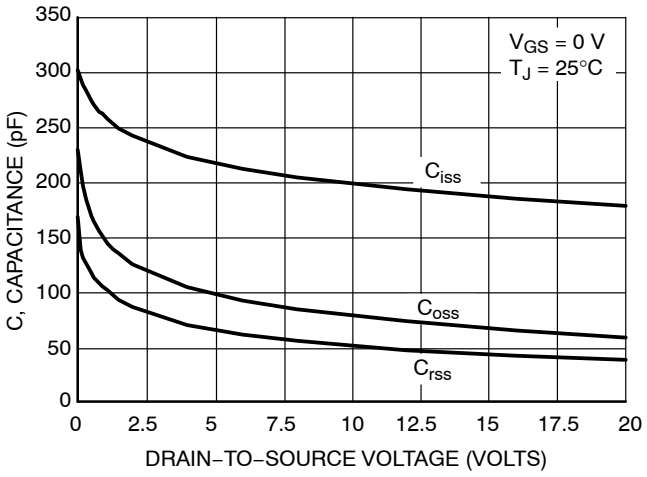


Figure 7. Capacitance Variation

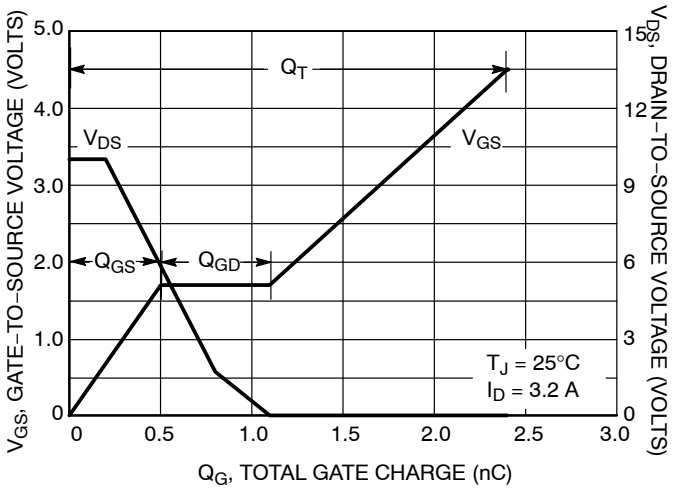


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

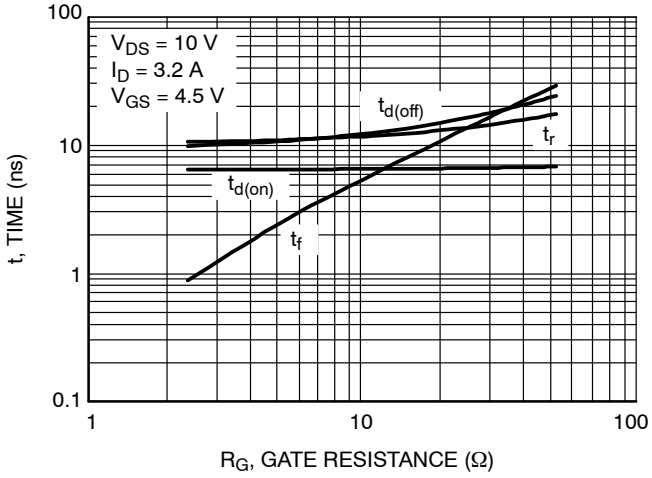


Figure 9. Resistive Switching Time Variation versus Gate Resistance

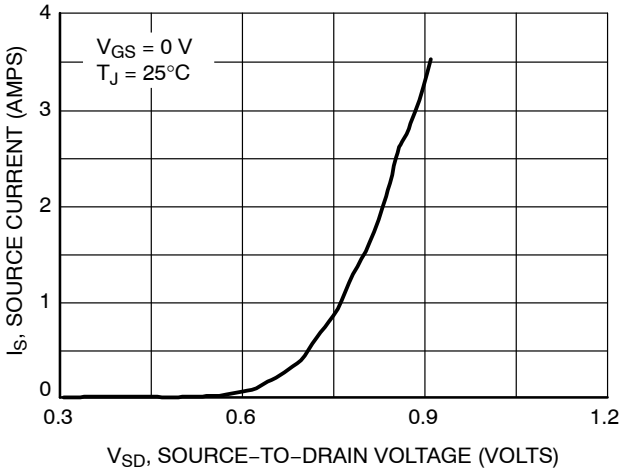
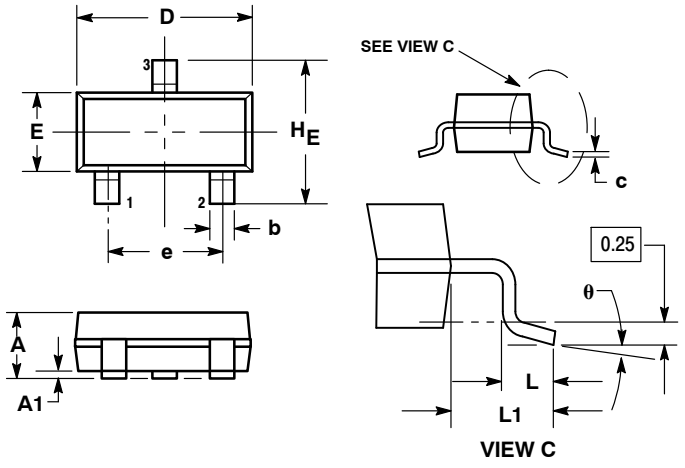


Figure 10. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

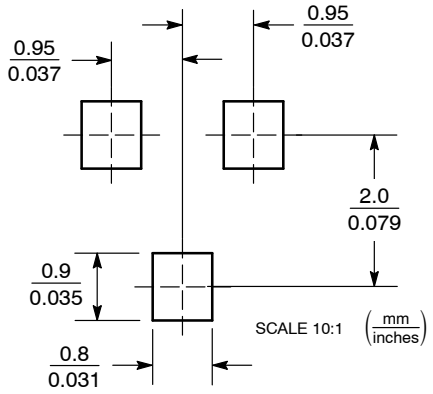


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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