DATE:02.06.2023

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CSE 224 REPORT

VSCPU ASSEMBLY CODE THAT IMPLEMENTS FLOOR DIVISION

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Introduction:

The aim of Project is to make a VSCPU(Very Simple Central Processing Unit) that makes floor division. While running the VSCPU to make floor division, the code ensures that each statement is checked with an interrupt, the code also ensures that the statements are controlled on the positive clock and can perform operations accordingly.

Assembly:

To make a floor division. I used assembly language with the help of the instruction set of cpu.tc website. Thanks to the instruction set. I wrote the assembly code in the screenshot.

Input ASM Code

```
1   0: ADDi 100 101
2   1: ADDi 101 4
3   2: CP 98 101
4   3: NAND 101 101
5   4: ADDi 101 1
6   5: CP 99 100
7   6: LT 99 98
8   7: BZJ 150 99
9   8: BZJi 152 0
10  9: ADD 100 101
11  10: ADDi 102 1
12  11: BZJi 151 0
13  98: 0
14  99: 0
15  100: 0
16  101: 0
17  102: 0
18  150: 9
19  151: 5
20  152: 12
21
```

In the Assembly code, I made floor division with a series for subtraction. First assigned two addresses and two copy addresses for the dividend and divisor, one for the result. Then for a series of subtraction, i made 2's complement method using NAND and ADDi instruction. To check dividend and divisor, i used LT and BZJ instruction to make a subtraction loop.

The loop iterates until the value which is to be diveded is smaller than the divisor, in each iteration value of divident is reduced by the value of divisor and the result is incremented by one.

Output Initial Memory

```
memory[0] = 32'h10190065;
memory[1] = 32'h10194004;
memory[2] = 32'h80188065;
memory[3] = 32'h20194065;
memory[4] = 32'h10194001;
memory[5] = 32'h8018c064;
memory[6] = 32'h6018c062;
memory[7] = 32'hc0258063;
memory[8] = 32'hd0260000;
memory[9] = 32'h190065;
memory[10] = 32'h10198001;
memory[11] = 32'hd025c000;
memory[98] = 32'h0;
memory[99] = 32'h0;
memory[100] = 32'h0;
memory[101] = 32'h0;
memory[102] = 32'h0;
memory[150] = 32'h9;
memory[151] = 32'h5;
memory[152] = 32'hc;
```

This is an example of the assembly code converted to verilog code where dividend is 101 and divisor is 4.

Conclusion:

In this project, how VSCPU works and the use of assembly language were taught. The assembly code that performs floor division with assembly language was written, and the corresponding verilog code was implemented.

EDA Playground link: https://www.edaplayground.com/x/JEeT