EXAMPLE

Exception in a Pipelined Computer

Given this instruction sequence,

```
40hex  sub   $11, $2, $4
44hex  and   $12, $2, $5
48hex  or    $13, $2, $6
4Chex  add    $1, $2, $1
50hex  slt   $15, $6, $7
54hex  lw    $16, 50($7)
...
```

assume the instructions to be invoked on an exception begin like this:

```
80000180hex  sw      $25, 1000($0)
80000184hex  sw      $26, 1004($0)
...
```

Show what happens in the pipeline if an overflow exception occurs in the `add` instruction.

ANSWER

Figure 4.67 shows the events, starting with the `add` instruction in the EX stage. The overflow is detected during that phase, and 8000 0180_{hex} is forced into the PC. Clock cycle 7 shows that the `add` and following instructions are flushed, and the first instruction of the exception code is fetched. Note that the address of the instruction *following* the `add` is saved: $4C_{hex} + 4 = 50_{hex}$.