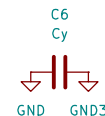
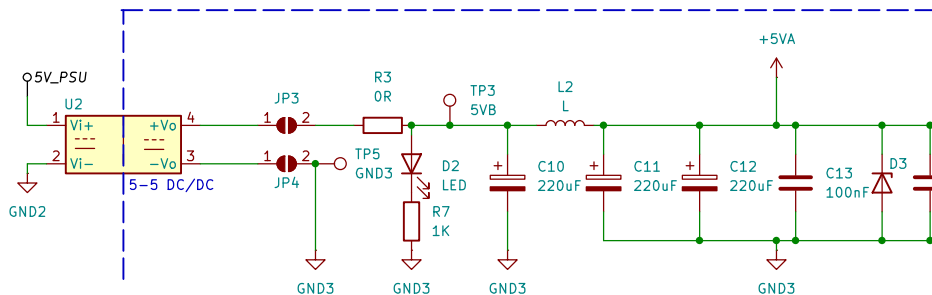
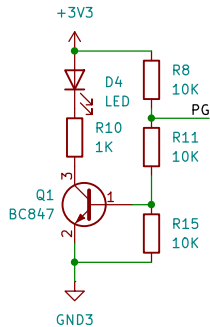
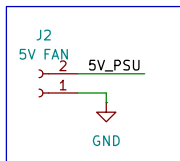
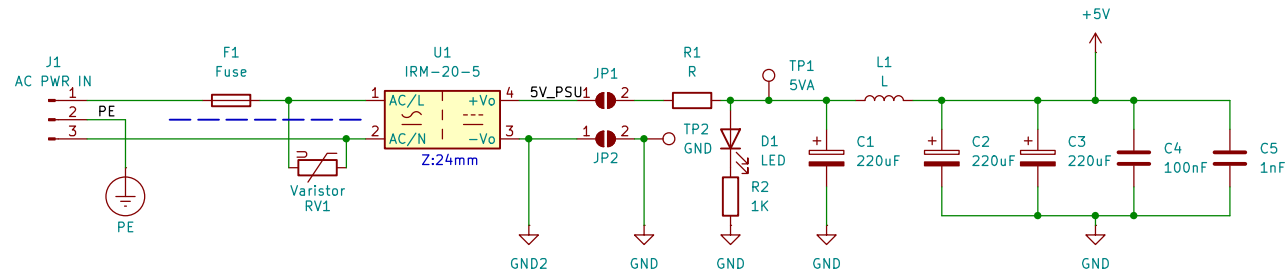
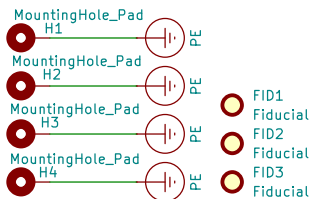
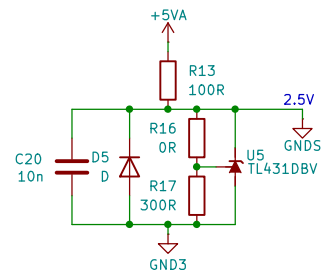
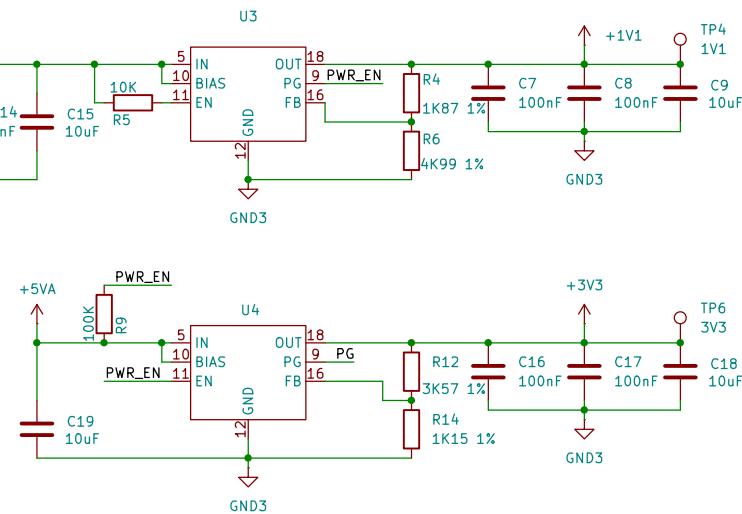




JP1 && JP2 --> MW PSU FOR NON ISOLATED
JP3 && JP4 --> MW PSU FOR ISOLATED



FPGA PWR SEQUENCE:
1: VCC & VCCA_xx (1V1)
2: VCCIO (3V3)



Reinforced Isolation
Functional Isolation



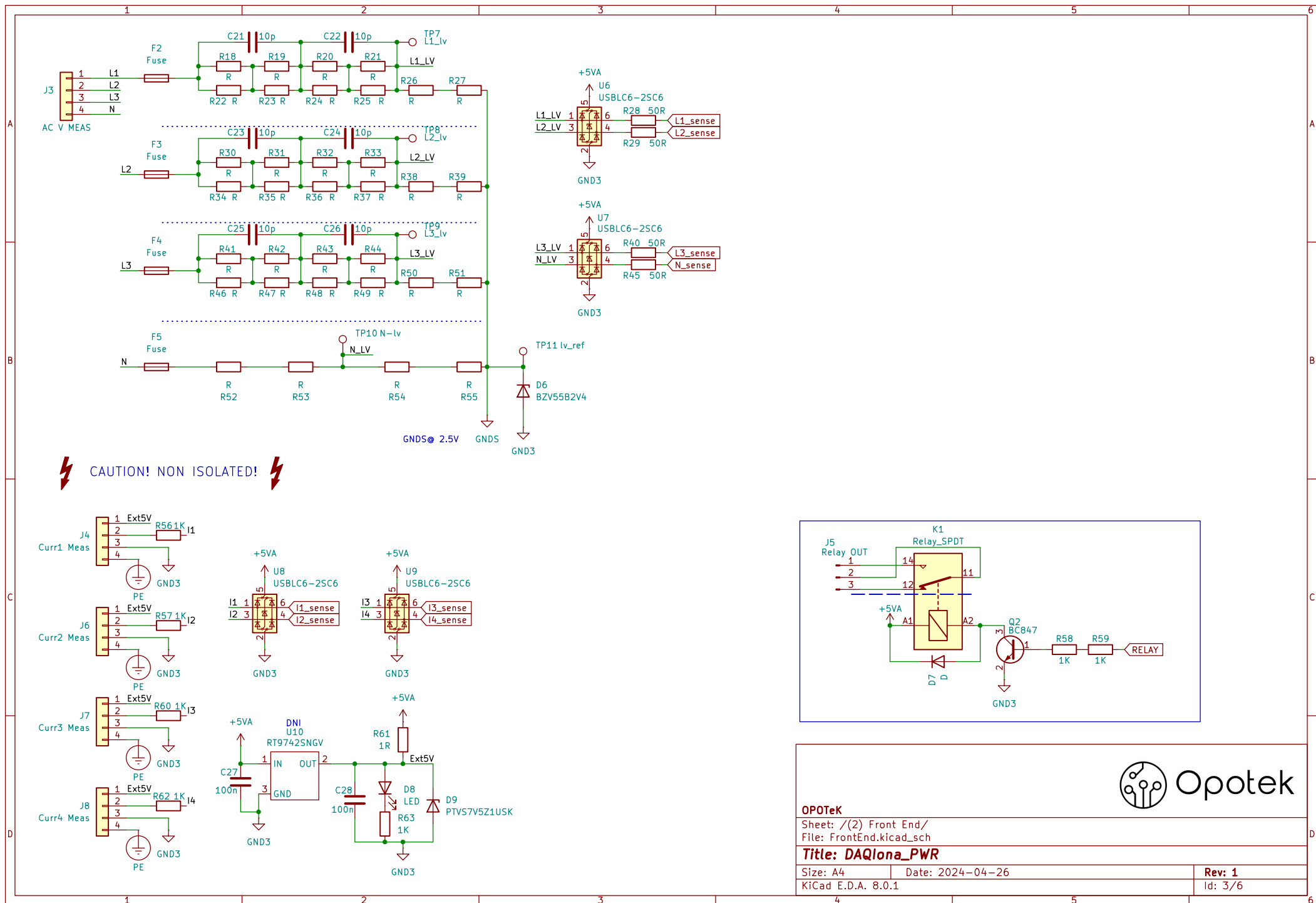
OPOTEK

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Title: DAQlona_PWR

Size: A4 Date: 2024-04-26
KiCad E.D.A. 8.0.1

Rev: 1
Id: 2/6



OPOTek

Sheet: /(2) Front End/
File: FrontEnd.kicad_sch

Title: DAQlona_PWR

Size: A4 Date: 2024-04-26

KiCad E.D.A. 8.0.1

Rev: 1

Id: 3/6

