TECHNISCHE UNIVERSITÄT WIEN
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Institut für Computertechnik
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Midterm Presentation - P4 Accuracy of Approximate Circuits

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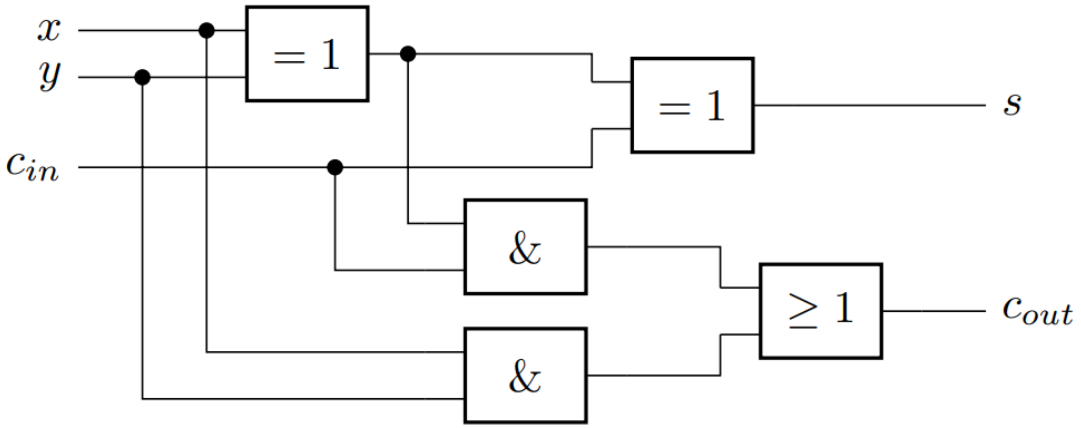
Introduction

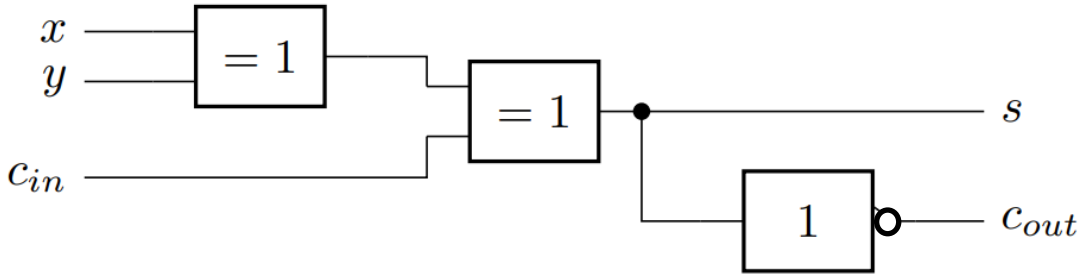
- Advantages of approximate computing
- Energy-efficient
- Less area
- Less computing time

Circuit Designs

Circuit Designs



Conventional Full Adder Circuit Design



Approximate Full Adder Circuit Design as proposed by Priyadharshni et al

Truth Table

Input			Full Adder		INXA1	
x	y	c_{in}	c_{out}	s	c_{out}	s
0	0	0	0	0	0 ✓	0 ✓
0	0	1	0	1	1 ✗	1 ✓
0	1	0	0	1	0 ✓	1 ✓
0	1	1	1	0	1 ✓	0 ✓
1	0	0	0	1	0 ✓	1 ✓
1	0	1	1	0	1 ✓	0 ✓
1	1	0	1	0	0 ✗	0 ✓
1	1	1	1	1	1 ✓	1 ✓

Error Analysis

- For multi bit inputs, the error is not Hamming distance
- Error must be interpreted as number

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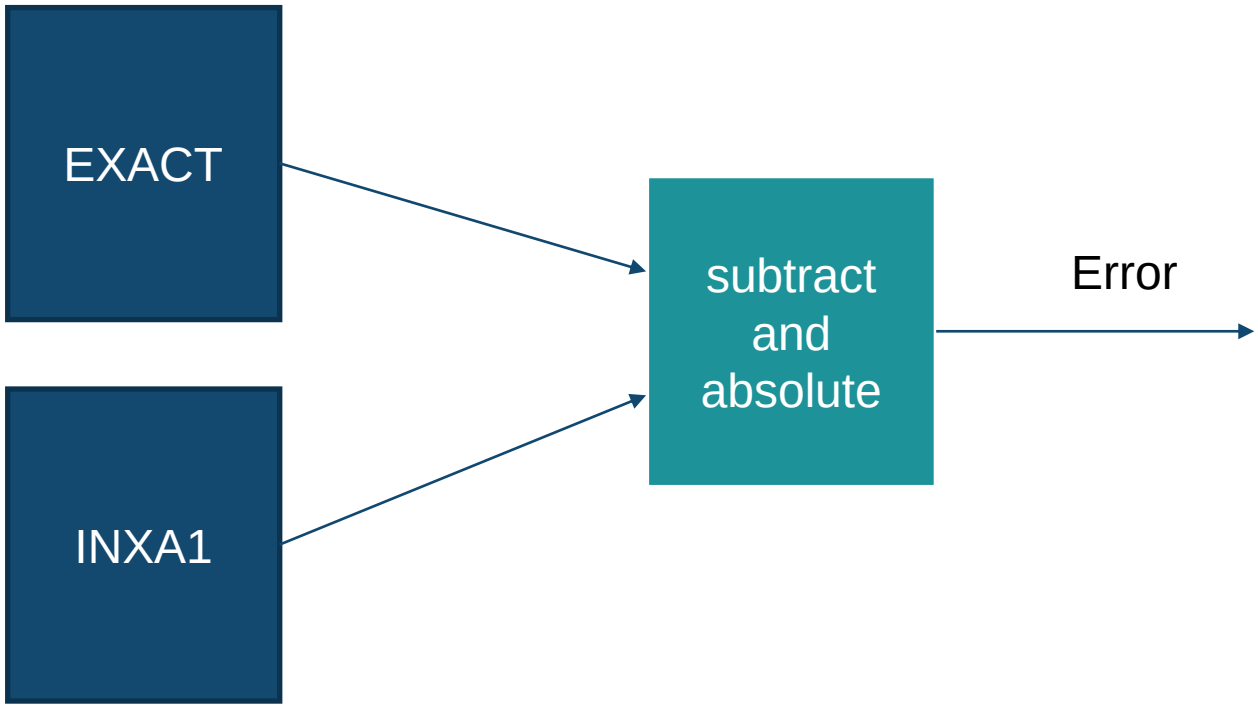
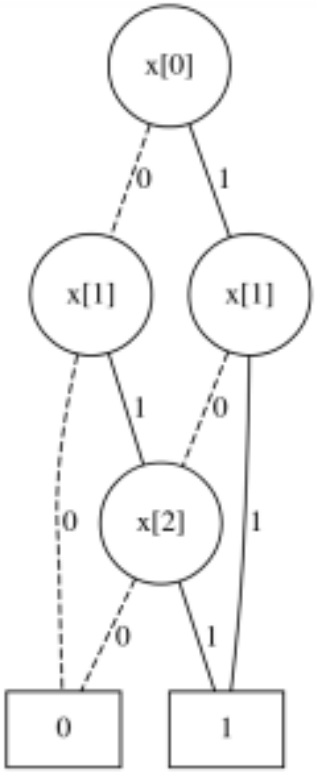


Binary Decision Diagram

Input			Output
X[0]	X[1]	X[2]	out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



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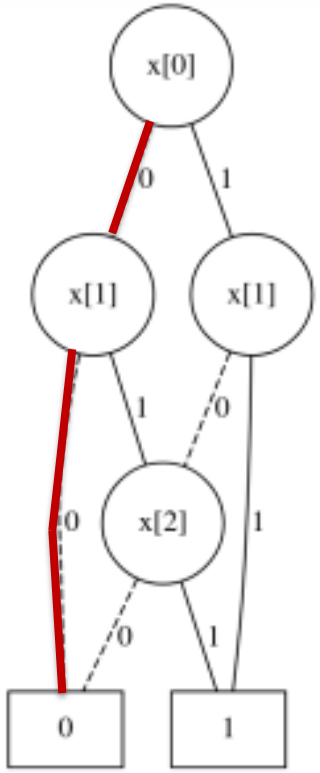

Current Status

- VHDL code for full adder and INXA1 finished
- Python code for Binary Decision Diagram for 1 bit analysis
- First estimation of power consumption

Future Plans

- Time, Area and Power Analysis with VHDL TOOL
- Adding functionality for generic N bit Adders
- Implementation in Open Source Processor
- Worst Case Error Analysis with BDD
- Implementing on Zedboard (Hardware)

Thank you!