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EEE419 Lab 2 Experimental

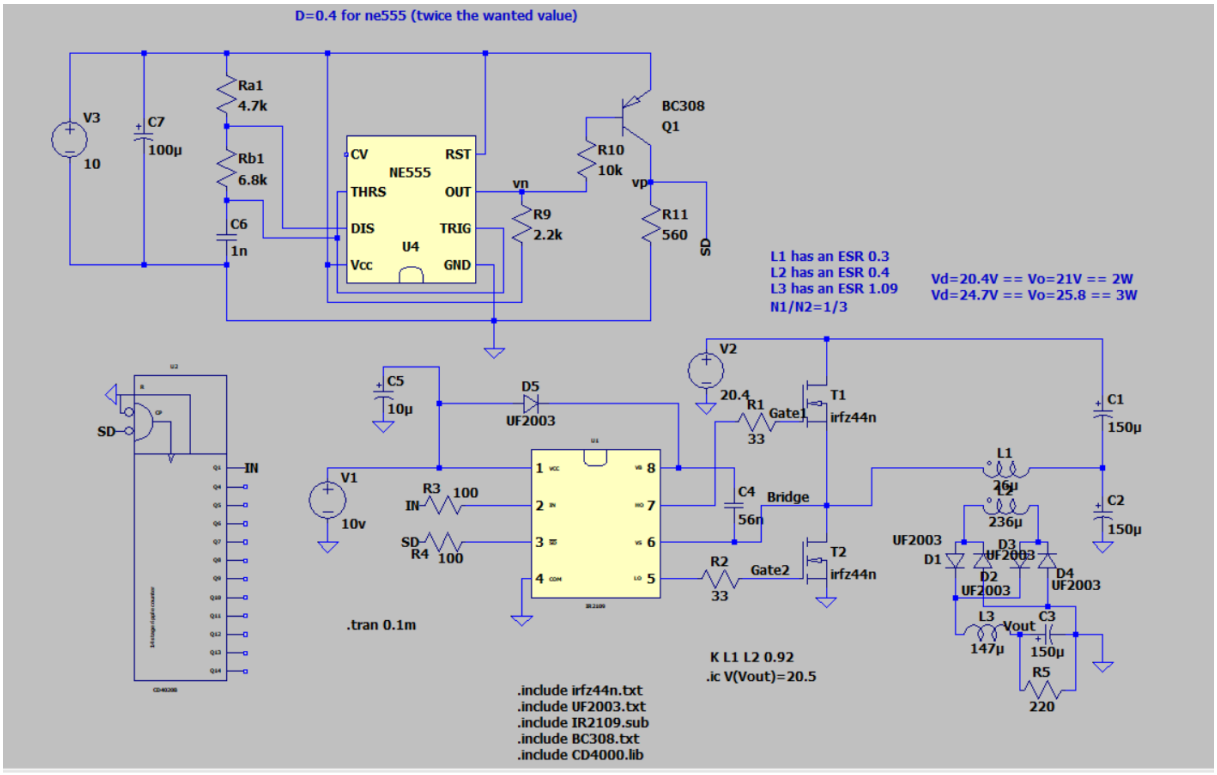

Fig. 1: Circuit Schematic

Analysis:

I installed the NE555 and pnp transistor circuit on the breadboard. The duty cycle in the preliminary was measured as 0.4. In the experiment, t_{ON} time is measured as 9.2µs and T_S time is measured as 21.2µs. The duty cycle is calculated as 0.43. This signal is labeled as $\overline{SD}$ in the schematic. Fig. 2 and Fig. 3 shows the waveforms and corresponding time values respectively.

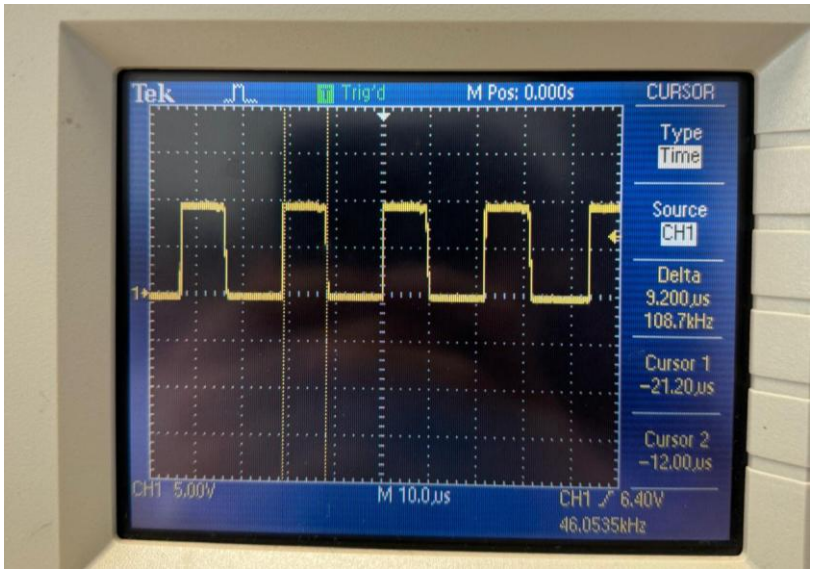

Fig. 2: t_{ON} time of $\overline{SD}$ signal

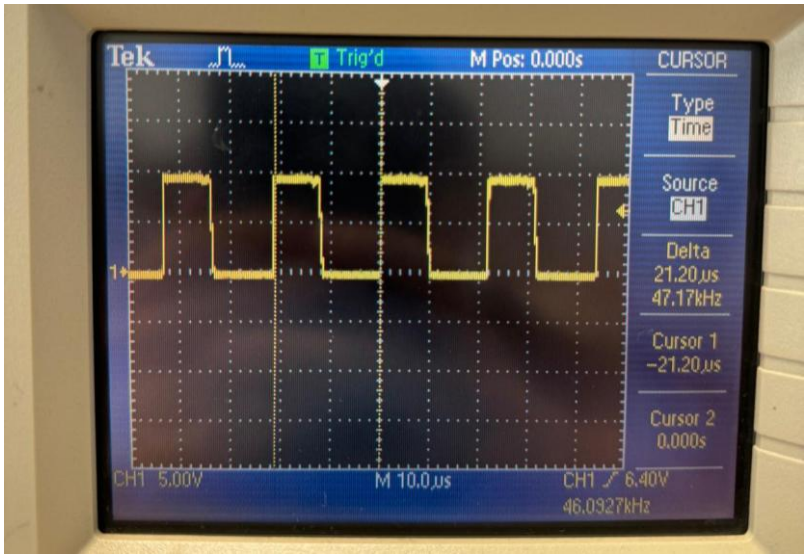

Fig. 3: T_S time of $\overline{SD}$ signal

Using $\overline{SD}$ signal as input to the CD4020 binary counter, IN signal is generated. It simply counts the falling edges of the input signal and every time it counts, complements the signal and gives is at the output signal. As expected, one period of $\overline{SD}$ signal will be t_{ON} time of IN signal, as 21.2µs, and T_s value is measured as 43.6µs. Fig. 4 and Fig. 5 show the results respectively.

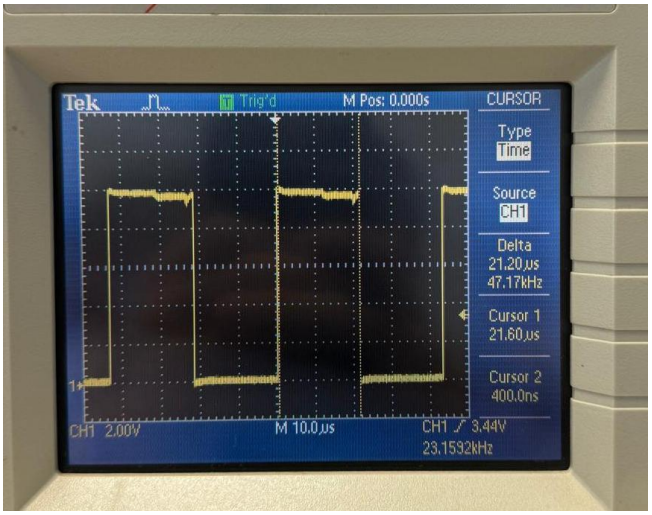

Fig. 4: t_{ON} time for IN signal

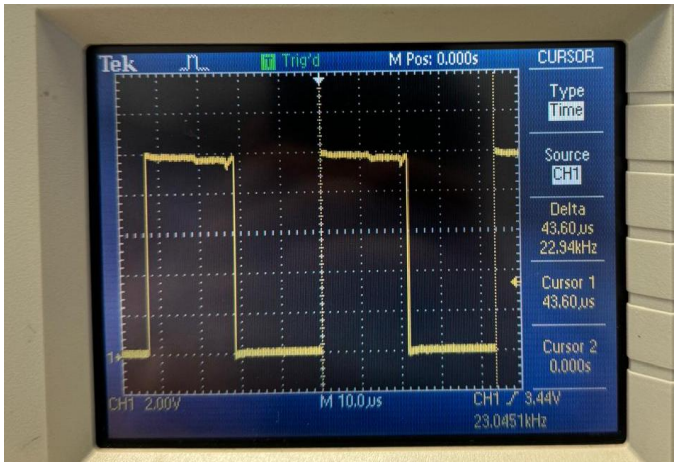

Fig. 5: T_S time for IN signal

Next, I added the IR2109 circuit and switches (transistors) to the circuit. Fig. 6 shows the input current from +10V and Fig. 6 shows the input current from V_d. As expected, from +10V, the current is less than 30mA (21mA) and from V_d (+20.4V), the current is 0A.

Fig. 6: Input current of +10V

Fig. 7: Input current of V_d

At this step, bridge voltage and gate voltages of the transistors are measured and compared to the simulation results. Fig. 8 shows the waveform of the bridge voltage and the following figure shows the LTspice simulation graph.

Fig. 8: Bridge voltage = V_d

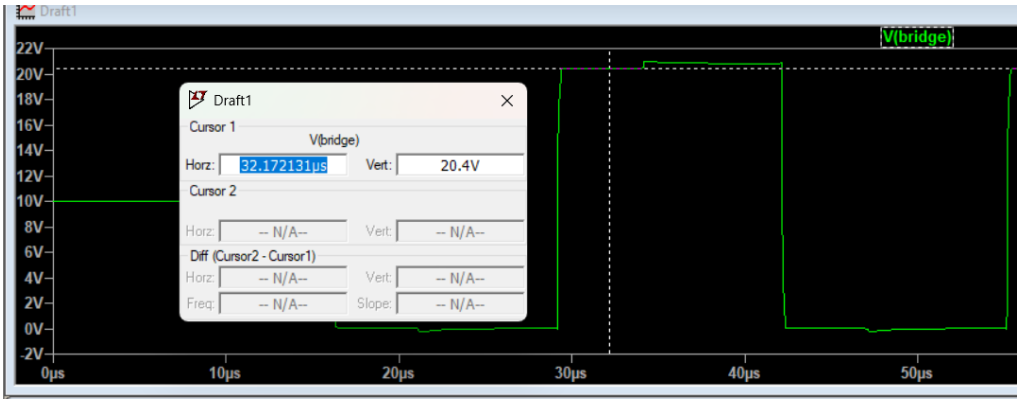

Fig. 9: Bridge voltage

Fig. 10 shows the gate voltage of the floating switch, which is connected to +20.4V (V_d). It is driven by the IN signal. The peak voltage is measured as 28.8V and it reduces to V_d, then zero. In the simulation, the peak voltage 29.3V and then it reduces to 20.8V then zero. The values and waveforms resembles to each other as expected.

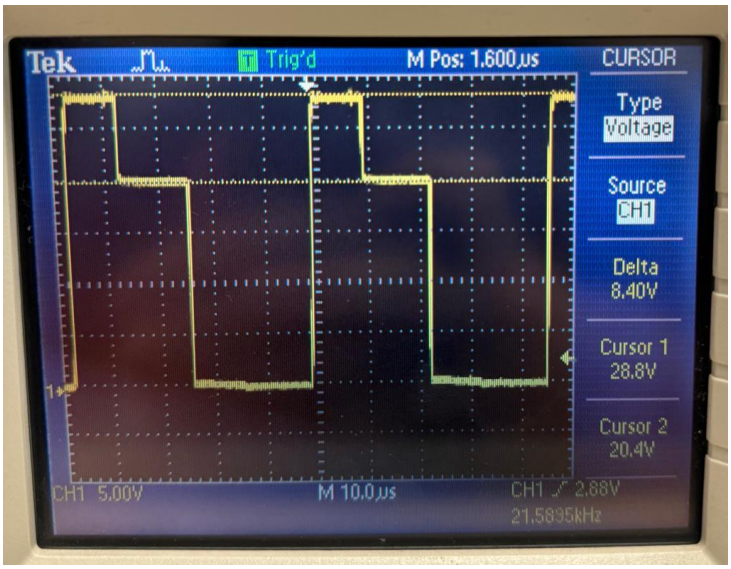

Fig. 10: Gate voltage of floating switch

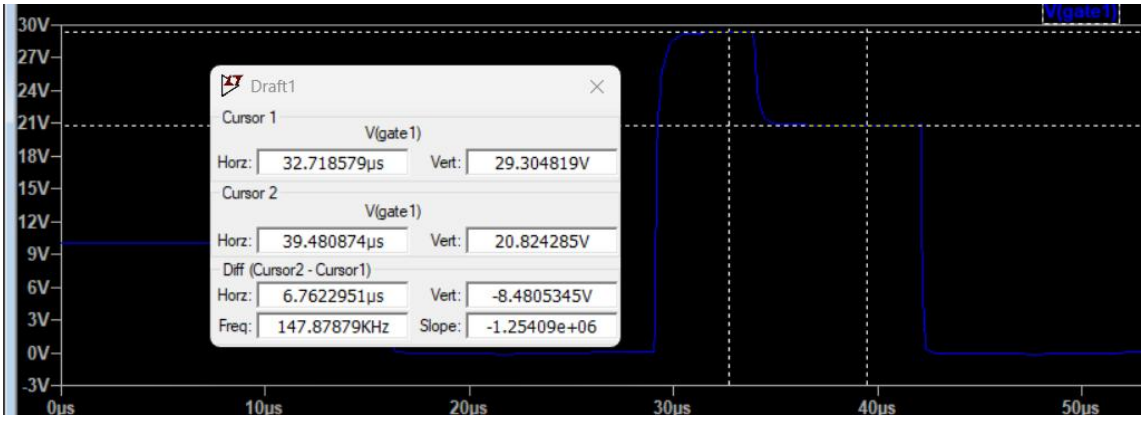

Fig. 11: Gate voltage graph of floating switch from simulation

Fig. 12 shows the gate voltage of the lower switch. It is driven by $\overline{SD}$ signal. The peak voltage value is measured as +10.6V. In the simulation, it is measured as +10V.

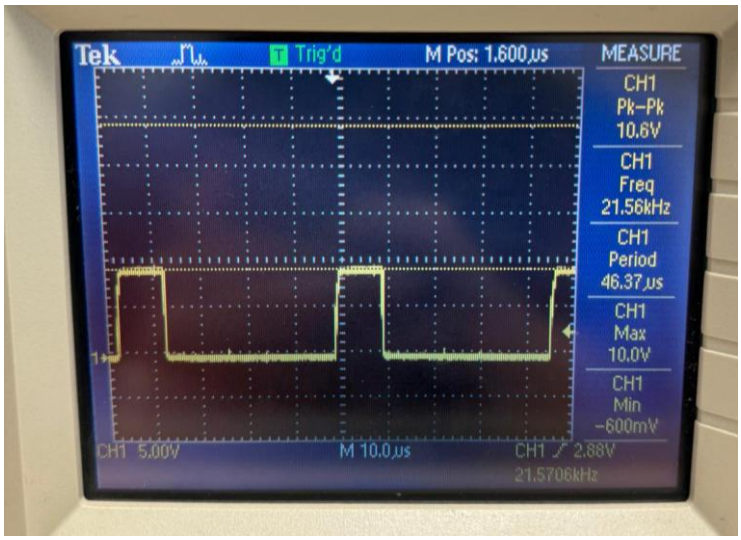

Fig. 12: Gate voltage of lower switch

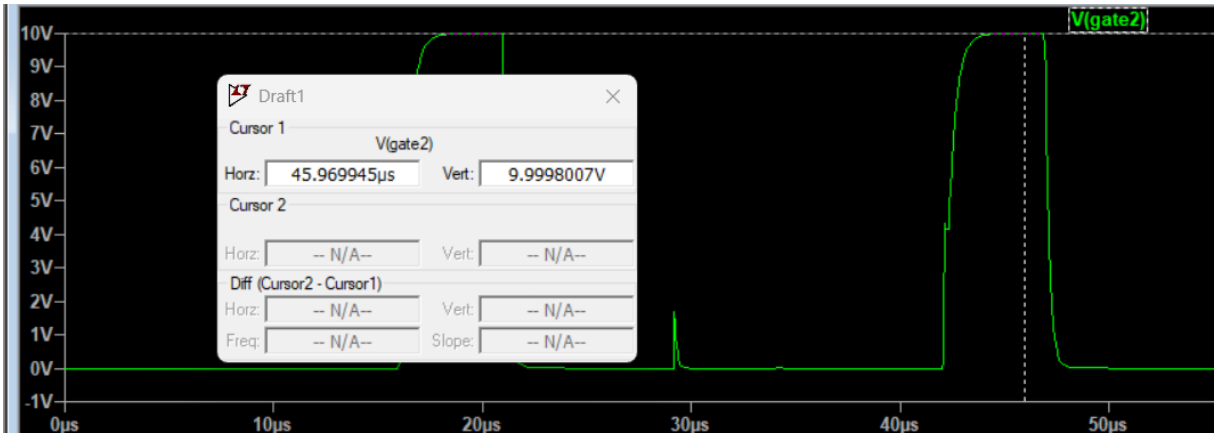

Fig. 13: Gate voltage of lower transistor from the simulation

Then, the capacitors and transformer is added to the circuit, and the voltage at the secondary winding is observed. Fig. 14 shows the waveform.

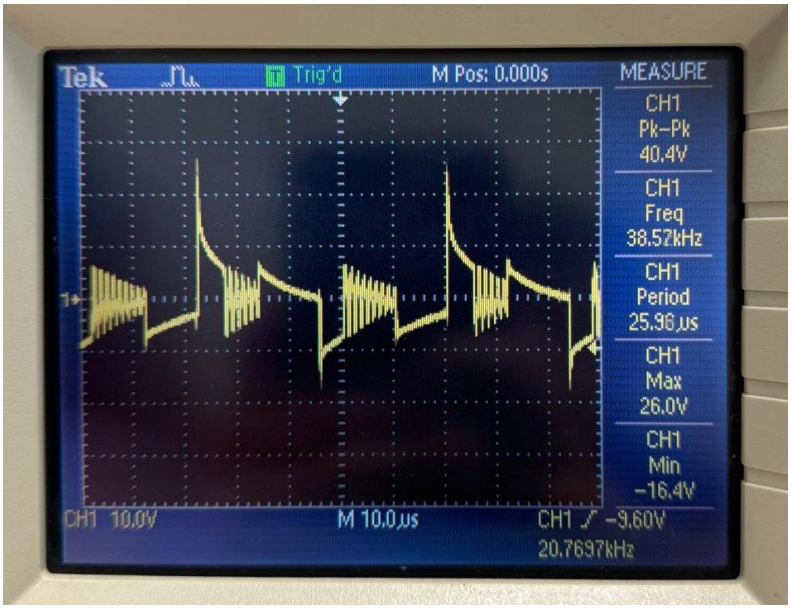

Fig. 14: Voltage at the secondary winding

The voltage at the primary is bridge voltage – $V_d/2$, which is $V_d/2$. It is around +10V. The turns ratio of the transformer is 3. Therefore, as expected, the voltage at the secondary is three times the input voltage. The voltage is measured as 26V, which is a little lower than +30V. It is the error of the circuit elements and handmade transformer.

Finally, the circuit is completed and output voltage is observed. For the first case, when V_d=+20.4V, the output voltage graph can be seen from Fig. 15. The voltage is also measurede with a multimeter because there are more than expected ripple at the output voltage at the oscilloscope.

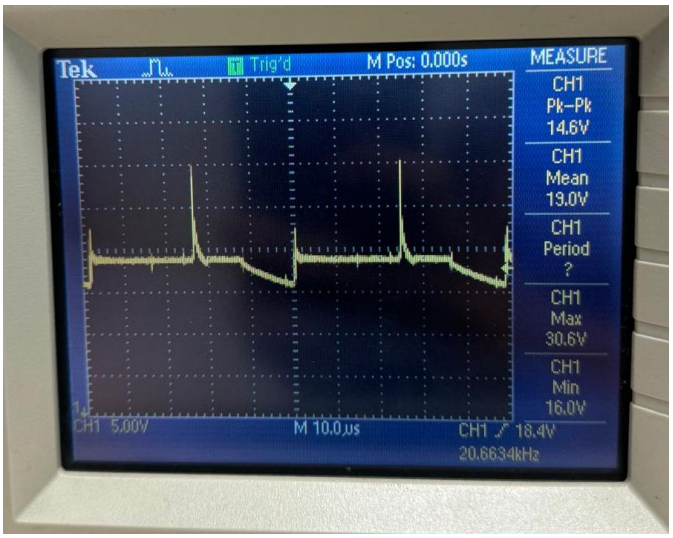

Fig. 15: Output voltage graph

Fig. 16: Output voltage with V_d=+20.4V

As seen from figure above, when V_d=+20.4V, the output voltage is measured as +19.52V.

With the given values, the input power is calculated as 2.87W and output power is calculated as 1.73W. The efficiency is calculated as 60%.

Fig. 17: Input voltage and current

When V_d=+22.1V, the output voltage is at the desired value, which is +21V. Figure below shows the output voltage graph with V_d=+22.1V.

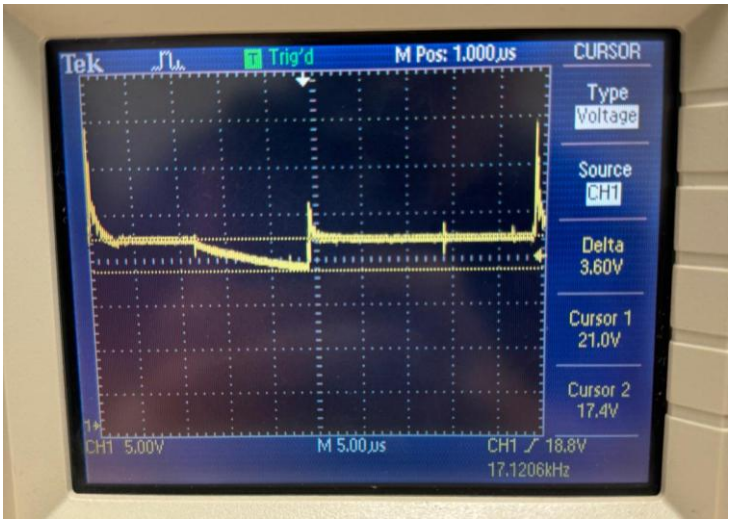

Fig. 18: Output voltage graph with V_d=+22.1V

Fig. 19: Output voltage measured with multimeter

With these values, input power is calculated as 3.42W, and output power is calculated as 2W. The efficiency of the system is calculated as 58%. Whereas, in the simulation, the efficiency is calculated as around 60%. The results are similar with a slight error included.

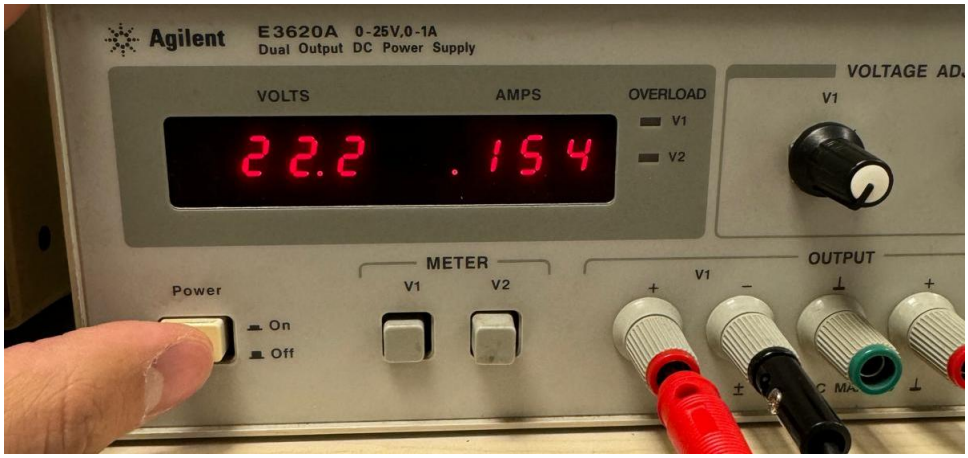

Fig. 20: Input power when V_d=22.2V