# PICO 2

# A computer chip with different colored labels AI-generated content may be incorrect.

# MCP4912

The MCP4912 is a Dual 10-Bit Voltage Output DAC (Digital to Analog Converter) that operates from a 2.7 V to a 5.5V supply and are SPI compatible.

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**Fig 1**: MCP4912 pinouts.

**Pin Function Table**:

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**Pin Descriptions**:

1. **CS**: Tells the peripheral that data is ready to be sent and allows the user to select the peripheral it want to talk to. The Chip select pin is HIGH by default and becomes LOW when data is ready to be sent thereby activating the peripheral. After data has been sent it returns to HIGH.
2. **LDAC**: Transfer input latch registers to their corresponding DAC registers (VOUT).
   1. When LOW both Vouta and Voutb are updated simultaneously with their input register contents..
   2. When tied to VSS, Vout is updated at the rising edge of the CS pin.
   3. Or can be driven by an external control device (MCU I/O pin)
3. **SHDN:** When LOW, both DAC channels are shut down. No DAC output available during the shutdown.
4. **Vouta, Voutb:** output pins each with its own amplifier. The output amplifier of each can drive the output pin with a range of VSS to VDD.
5. **Vrefa, Vrefb:** Determines the reference voltage that will be used by the DAC to determine the output voltage. If the input value is 50%, the output voltage will be 50% of Vref.

**GENERAL OVERVIEW**

**Note**: The MCP4912 takes values strictly in binary form.

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**Fig 2**: Equation for analog output voltage.

**Output range**:

MCP4912 takes an input of 10 bit. Considering a constant gain of 1 for simplicity.

**n=10, G=1, Vref = 3.3v**

**Range** = volts

**Serial Interface:**

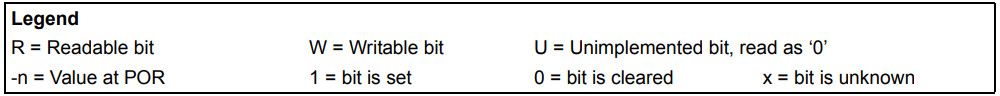
Data is sent to the device via the SDI pin and is clocked in on the rising edge of the SCK (unidirectional communication). CS is LOW during the duration of a write operation. The write command is initiated by driving the CS pin low, followed by clocking the 4 configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. CS the goes HIGH causing data to be latched into the selected DAC’s input registers.

All writes are 16-bit words and anything past 16 bits is ignored.

* 4 MSBs 🡪 Configuration bits
* 12 remaining 🡪 Data bits.

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**Note**:

MOSI (TX)🡪 Master Out Slave Input: transmits data from the master to the slave.

MISO (RX)🡪 Master In Slave Output: transmits data from the slave to the master.

# 23K256 SRAM.

A diagram of a circuit board

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AI-generated content may be incorrect.The 23K256 chip is a memory chip with 256 Kbits accessed via SPI. Requires a SCK (clock) input, data in (SI) and data out (SO). Chip select determines the access mode.

**Operation:**

* Chip contains an 8-bit instruction register accessed via SI.
* SI must be LOW and HOLD must be HIGH while accessing this register
* Instructions are transferred MSB first then LSB last.

**A close-up of a list

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* Addresses are 16 bits

Read sequence

* CS to LOW
* Send 8-bit instruction
* Send 16-bit address (8-bits at a time)
* Read outputs from SO pin

Write sequence:

* CS to LOW
* Send write instruction
* Send 16-bit address
* Write data
* Bring CS to HIGH

Number of addresses =

Address bits = 16 bit in total where the MSB is ignored since only 15 bits are needed to address all 32 000 spots.